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Micropower, 3-Axis, ±2 *g*/±4 *g*/±8 *g* Digital Output MEMS Accelerometer

Data Sheet **ADXL362**

FEATURES

- **Ultralow power**
  - **Power can be derived from coin cell battery**
  - **1.8 µA at 100 Hz ODR, 2.0 V supply**
  - **3.0 µA at 400 Hz ODR, 2.0 V supply**
  - **270 nA motion activated wake-up mode**
  - **10 nA standby current**
- **High resolution: 1 mg/LSB**
- **Built-in features for system-level power savings:**
  - **Adjustable threshold sleep/wake modes for motion activation**
  - **Autonomous interrupt processing, without need for microcontroller intervention, to allow the rest of the system to be turned off completely**
  - **Deep embedded FIFO minimizes host processor load**
  - **Awake state output enables implementation of standalone, motion activated switch**
- **Low noise down to 175 µg/√Hz**
- **Wide supply and I/O voltage ranges: 1.6 V to 3.5 V**
  - **Operates off 1.8 V to 3.3 V rails**
- **Acceleration sample synchronization via external trigger**
- **On-chip temperature sensor**
- **SPI digital interface**
- **Measurement ranges selectable via SPI command**
- **Small and thin 3 mm × 3.25 mm × 1.06 mm package**

APPLICATIONS

- **Hearing aids**
- **Home healthcare devices**
- **Motion enabled power save switches**
- **Wireless sensors**
- **Motion enabled metering devices**

GENERAL DESCRIPTION

The ADXL362 is an ultralow power, 3-axis MEMS accelerometer that consumes less than 2 µA at a 100 Hz output data rate and 270 nA when in motion triggered wake-up mode. Unlike accelerometers that use power duty cycling to achieve low power consumption, the ADXL362 does not alias input signals by undersampling; it samples the full bandwidth of the sensor at all data rates.

The ADXL362 always provides 12-bit output resolution; 8-bit formatted data is also provided for more efficient single-byte transfers when a lower resolution is sufficient. Measurement ranges of ±2 *g*, ±4 *g*, and ±8 *g* are available, with a resolution of 1 mg/LSB on the ±2 *g* range. For applications where a noise level lower than the normal 550 µg/√Hz of the ADXL362 is desired, either of two lower noise modes (down to 175 µg/√Hz typical) can be selected at minimal increase in supply current.

In addition to its ultralow power consumption, the ADXL362 has many features to enable true system level power reduction. It includes a deep multimode output FIFO, a built-in micropower temperature sensor, and several activity detection modes including adjustable threshold sleep and wake-up operation that can run as low as 270 nA at a 6 Hz (approximate) measurement rate. A pin output is provided to directly control an external switch when activity is detected, if desired. In addition, the ADXL362 has provisions for external control of sampling time and/or an external clock.

The ADXL362 operates on a wide 1.6 V to 3.5 V supply range, and can interface, if necessary, to a host operating on a separate, lower supply voltage. The ADXL362 is available in a 3 mm × 3.25 mm × 1.06 mm package.

FUNCTIONAL BLOCK DIAGRAM

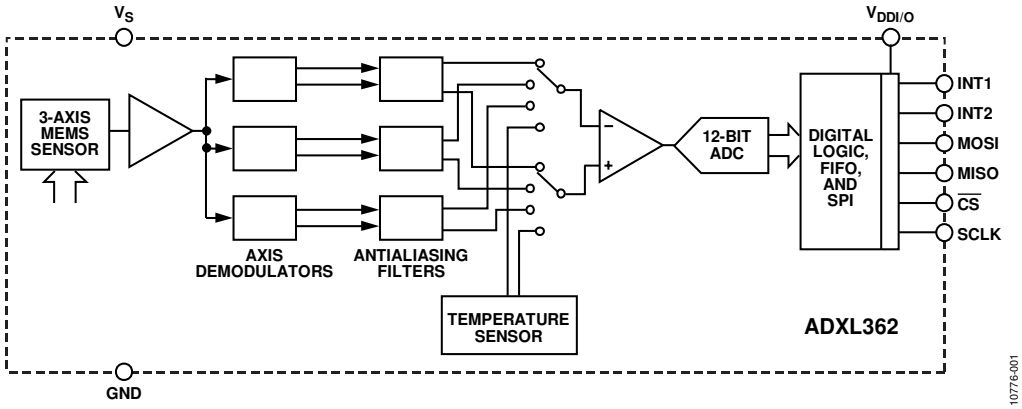

Figure 1.

Rev. E **Document Feedback**

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ADXL362* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADXL362 Breakout Board
- ADXL362 Datalogger / Development Board
- Real Time Eval System for Digital Output Sensor
- Ultra-Low Power Accelerometer with Display Arduino Shield
- Wireless Sensor Network (WSN) Development Kits for Your IoT Solutions

DOCUMENTATION

Data Sheet

- ADXL362: Micropower Three-Axis, ±2g/±4g/±8g Digital-Output MEMS Accelerometer Data Sheet

User Guides

- UG-351: Ultralow Power, ±2 *g*/±4 *g*/±8 *g* Digital Accelerometer Breakout Board

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADXL362 - No-OS Driver for Microchip Microcontroller Platforms
- ADXL362 - No-OS Driver for Renesas Microcontroller Platforms
- ADXL362 Input 3-Axis Digital Accelerometer Linux Driver
- ADXL362 Sample C code and Header Files
- ADXL362 Pmod Xilinx FPGA Reference Design

REFERENCE DESIGNS

- CN0274

REFERENCE MATERIALS

Press

- Analog Devices Introduces Industry's Lowest Power MEMS Accelerometer
- Analog Devices MEMS Technology Enables Withings Pulse Activity Tracker

Solutions Bulletins & Brochures

- Technologies and Applications for the Internet of Things

Technical Articles

- Blackbox Biometrics testing ADI MEMS for Blast Gauge Monitor
- Home is Where the Heart Is
- Industrial IoT Sensing and Measurement: the Edge Node
- Precision Counts in IoT
- Reduced Time to Insight: Industrial IoT Edge Node Processing
- Soldier-worn sensor that measures the destructive power of explosives uses MEMS accelerometer from Analog Devices

DESIGN RESOURCES

- ADXL362 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADXL362 EngineerZone Discussions.

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8/2012—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 2.0 V, $V_{DD\ I/O}$ = 2.0 V, 100 Hz ODR, HALF_BW = 0, ±2 *g* range, acceleration = 0 *g*, default settings for other registers, unless otherwise noted.[1]

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range	User selectable		±2, ±4, ±8		*g*
Nonlinearity	Percentage of full scale		±0.5		%
Sensor Resonant Frequency			3000		Hz
Cross Axis Sensitivity[2]			±1.5		%
OUTPUT RESOLUTION	Each axis				
All *g* Ranges			12		Bits
SENSITIVITY	Each axis				
Sensitivity Calibration Error				±10	%
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	2 *g* range		1		m*g*/LSB
	4 *g* range		2		m*g*/LSB
	8 *g* range		4		m*g*/LSB
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	2 *g* range		1000		LSB/*g*
	4 *g* range		500		LSB/*g*
	8 *g* range		250		LSB/*g*
Sensitivity Change Due to Temperature[3]	−40°C to +85°C		0.05		%/°C
0 *g* OFFSET	Each axis				
0 *g* Output[4]	X_{OUT}, Y_{OUT}	−150	±35	+150	m*g*
	Z_{OUT}	−250	±50	+250	m*g*
0 *g* Offset vs. Temperature[3]					
Normal Operation	X_{OUT}, Y_{OUT}		±0.5		m*g*/°C
	Z_{OUT}		±0.6		m*g*/°C
Low Noise Mode and Ultralow Noise Mode	X_{OUT}, Y_{OUT}, Z_{OUT}		±0.35		m*g*/°C
NOISE PERFORMANCE					
Noise Density					
Normal Operation	X_{OUT}, Y_{OUT}		550		µ*g*/√Hz
	Z_{OUT}		920		µ*g*/√Hz
Low Noise Mode	X_{OUT}, Y_{OUT}		400		µ*g*/√Hz
	Z_{OUT}		550		µ*g*/√Hz
Ultralow Noise Mode	X_{OUT}, Y_{OUT}		250		µ*g*/√Hz
	Z_{OUT}		350		µ*g*/√Hz
	V_S = 3.5 V; X_{OUT}, Y_{OUT}		175		µ*g*/√Hz
	V_S = 3.5 V; Z_{OUT}		250		µ*g*/√Hz
BANDWIDTH					
Low Pass (Antialiasing) Filter, −3 dB Corner	HALF_BW = 0		ODR/2		Hz
	HALF_BW = 1		ODR/4		Hz
Output Data Rate (ODR)	User selectable in 8 steps	12.5		400	Hz
SELF TEST					
Output Change[5]	X_{OUT}	230	550	870	m*g*
	Y_{OUT}	−870	−550	−230	m*g*
	Z_{OUT}	270	535	800	m*g*
POWER SUPPLY					
Operating Voltage Range (V_S)		1.6	2.0	3.5	V
I/O Voltage Range ($V_{DD\ I/O}$)		1.6	2.0	V_S	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Supply Current					
Measurement Mode	100 Hz ODR (50 Hz bandwidth)[6]				
Normal Operation			1.8		μA
Low Noise Mode			3.3		μA
Ultralow Noise Mode			13		μA
Wake-Up Mode			0.27		μA
Standby			0.01		μA
Power Supply Rejection Ratio (PSRR)	C_S = 1.0 μF, R_S = 100 Ω, C_{IO} = 1.1 μF, input is 100 mV sine wave on V_S				
Input Frequency 100 Hz to 1 kHz			−13		dB
Input Frequency 1 kHz to 250 kHz			−20		dB
Turn-On Time	100 Hz ODR (50 Hz bandwidth)				
Power-Up to Standby			5		ms
Measurement Mode Instruction to Valid Data			4/ODR		
TEMPERATURE SENSOR					
Bias Average	@ 25°C		350		LSB
Standard Deviation			290		LSB
Sensitivity Average			0.065		°C/LSB
Standard Deviation			0.0025		°C/LSB
Sensitivity Repeatability			±0.5		°C
Resolution			12		Bits
ENVIRONMENTAL					
Operating Temperature Range		−40		+85	°C

[1] All minimum and maximum specifications are guaranteed. Typical specifications may not be guaranteed.
[2] Cross axis sensitivity is defined as coupling between any two axes.
[3] −40°C to +25°C or +25°C to +85°C.
[4] Different supplies and measurement range cause different offset.
[5] Self test change is defined as the output change in *g* when self test is asserted. Different supplies cause different self test changes. These limits apply to the specific test conditions stated in Table 1. For variations over the full V_s supply range, see Table 22.
[6] Refer to Figure 30 for current consumption at other bandwidth settings.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Acceleration (Any Axis, Unpowered)	5000 *g*
Acceleration (Any Axis, Powered)	5000 *g*
V_S	−0.3 V to +3.6 V
$V_{DD\ I/O}$	−0.3 V to +3.6 V
All Other Pins	−0.3 V to V_S
Output Short-Circuit Duration (Any Pin to Ground)	Indefinite
ESD	2000 V (HBM)
Short Term Maximum Temperature	
Four Hours	150°C
One Minute	260°C
Temperature Range (Powered)	−50°C to +150°C
Temperature Range (Storage)	−50°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
16-Terminal LGA	150°C/W	85°C/W	18 mg

PACKAGE INFORMATION

Figure 2 and Table 4 provide details about the package branding for the ADXL362. For a complete listing of product availability, see the Ordering Guide section.

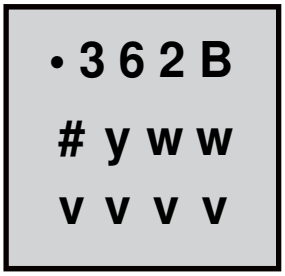

Figure 2. Product Information on Package (Top View)

Table 4. Package Branding Information

Branding Key	Field Description
•362B	Pin 1 indicator and device identifier
#yww	Pb-free designator (#) and date code
vvvv	Factory lot code

RECOMMENDED SOLDERING PROFILE

Figure 3 and Table 5 provide details about the recommended soldering profile.

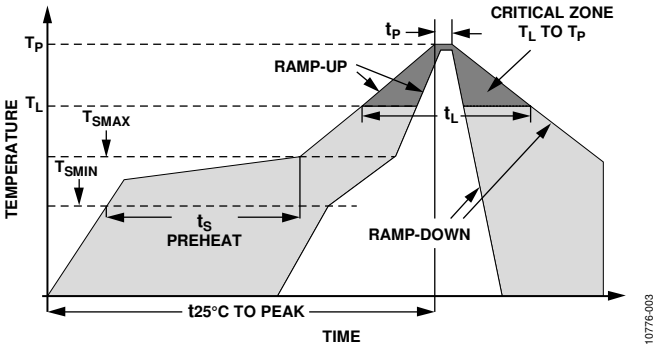

Figure 3. Recommended Soldering Profile

Table 5. Recommended Soldering Profile

	Condition	
Profile Feature	**Sn63/Pb37**	**Pb-Free**
Average Ramp Rate (T_L to T_P)	3°C/sec max	3°C/sec max
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time (T_{SMIN} to T_{SMAX})(t_S)	60 sec to 120 sec	60 sec to 180 sec
T_{SMAX} to T_L Ramp-Up Rate	3°C/sec max	3°C/sec max
Time Maintained Above Liquidous (T_L)		
Liquidous Temperature (T_L)	183°C	217°C
Time (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_P)	240 + 0/−5°C	260 + 0/−5°C
Time Within 5°C of Actual Peak Temperature (t_P)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 minutes max	8 minutes max

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

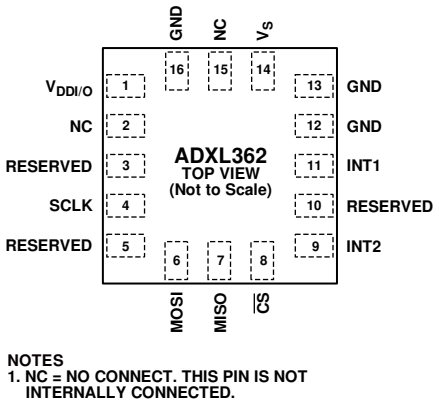

Figure 4. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{DD\ I/O}$	Supply Voltage for Digital I/O.
2	NC	No Connect. Not internally connected.
3	Reserved	Reserved. Can be left unconnected or connected to GND.
4	SCLK	SPI Communications Clock.
5	Reserved	Reserved. Can be left unconnected or connected to GND.
6	MOSI	Master Output, Slave Input. SPI serial data input.
7	MISO	Master Input, Slave Output. SPI serial data output.
8	$\overline{CS}$	SPI Chip Select, Active Low. Must be low during SPI communications.
9	INT2	Interrupt 2 Output. INT2 also serves as an input for synchronized sampling.
10	Reserved	Reserved. Can be left unconnected, or connected to GND.
11	INT1	Interrupt 1 Output. INT1 also serves as an input for external clocking.
12	GND	Ground. This pin must be grounded.
13	GND	Ground. This pin must be grounded.
14	V_S	Supply Voltage.
15	NC	No Connect. Not internally connected.
16	GND	Ground. This pin must be grounded.

TYPICAL PERFORMANCE CHARACTERISTICS

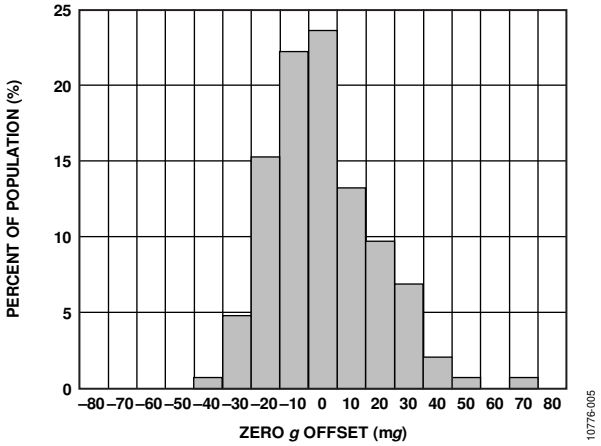

Figure 5. X-Axis Zero g *Offset at 25°C, V_S = 2 V*

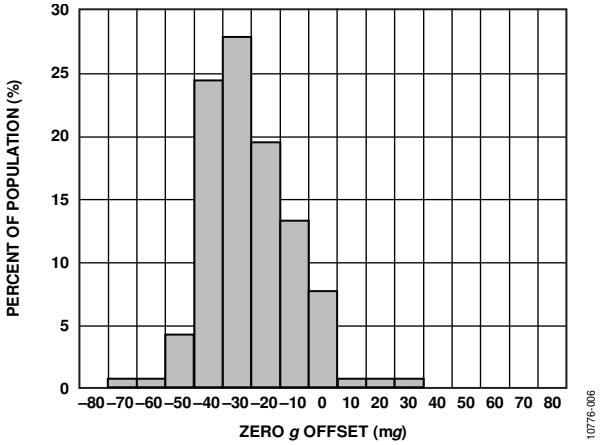

Figure 6. Y-Axis Zero g *Offset at 25°C, V_S = 2 V*

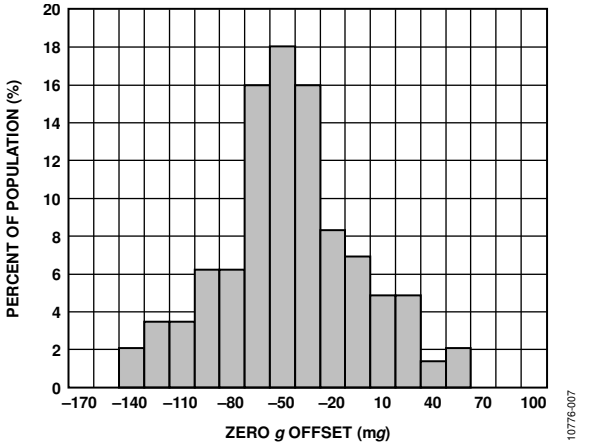

Figure 7. Z-Axis Zero g *Offset at 25°C, V_S = 2 V*

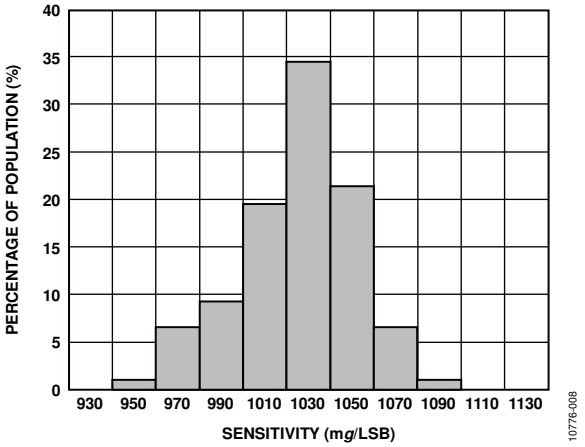

Figure 8. X-Axis Sensitivity at 25°C, V_S = 2 V, ±2 g *Range*

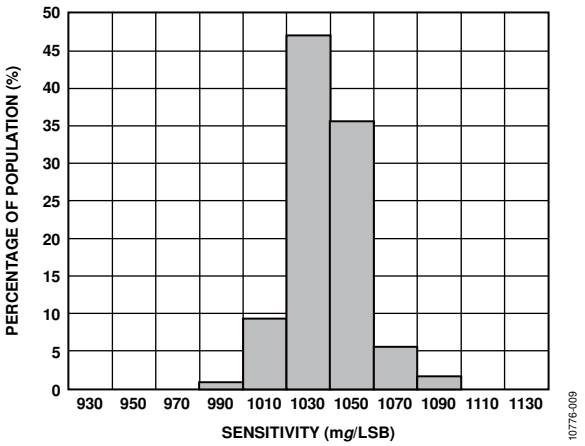

Figure 9. Y-Axis Sensitivity at 25°C, V_S = 2 V, ±2 g *Range*

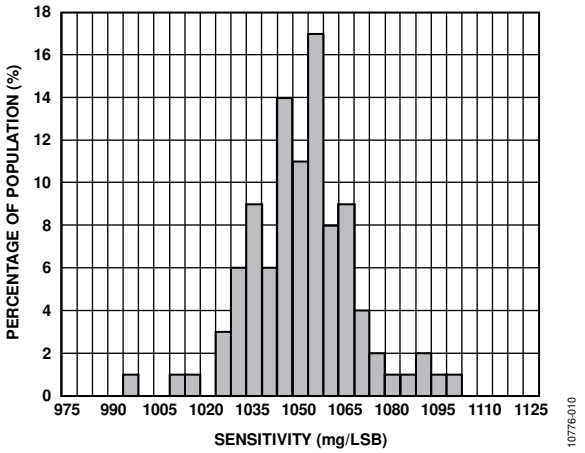

Figure 10. Z-Axis Sensitivity at 25°C, V_S = 2 V, ±2 g *Range*

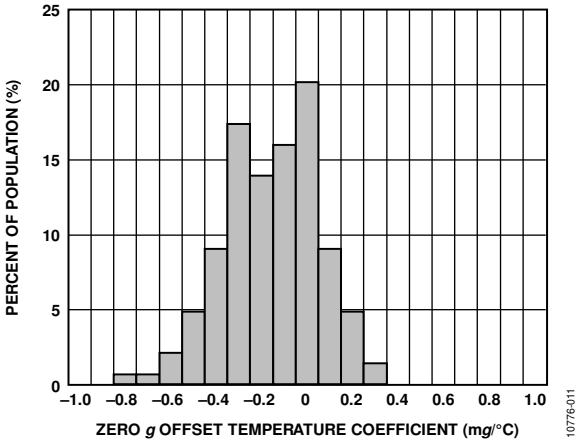

Figure 11. X-Axis Zero g Offset Temperature Coefficient, V_S = 2 V

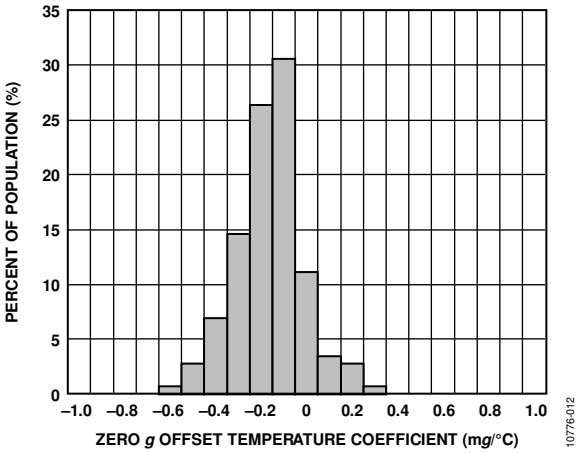

Figure 12. Y-Axis Zero g Offset Temperature Coefficient, V_S = 2 V

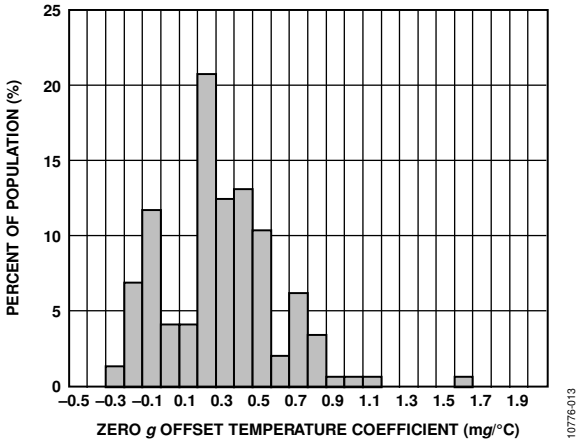

Figure 13. Z-Axis Zero g Offset Temperature Coefficient, V_S = 2 V

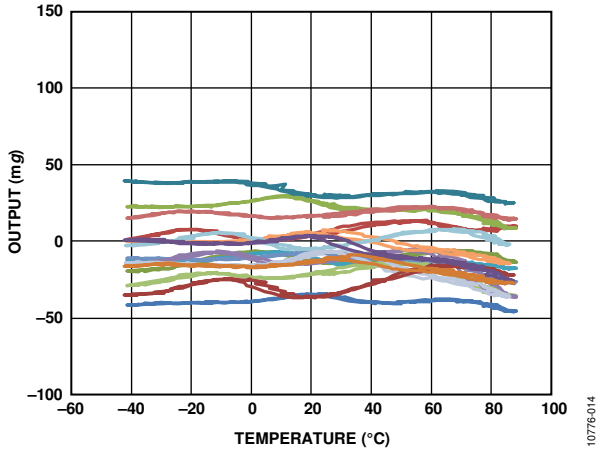

Figure 14. X-Axis Zero g Offset vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, V_S = 2 V

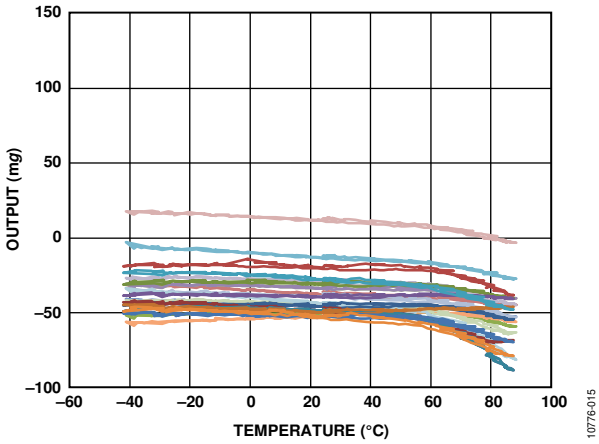

Figure 15. Y-Axis Zero g Offset vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, V_S = 2 V

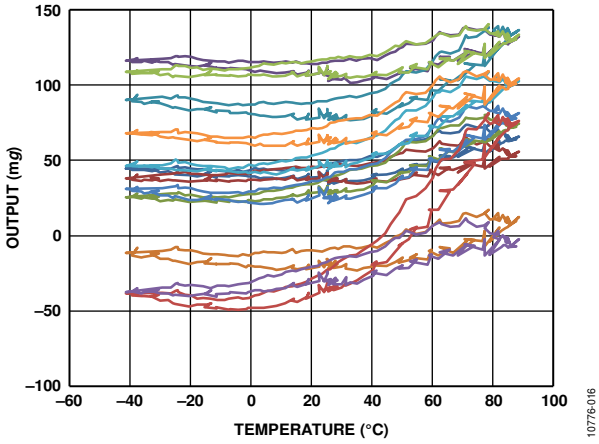

Figure 16. Z-Axis Zero g Offset vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, V_S = 2 V

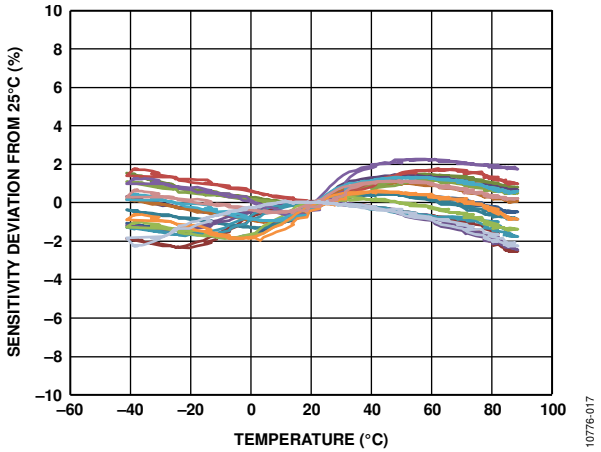

Figure 17. X-Axis Sensitivity Deviation from 25°C vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, V_S = 2 V

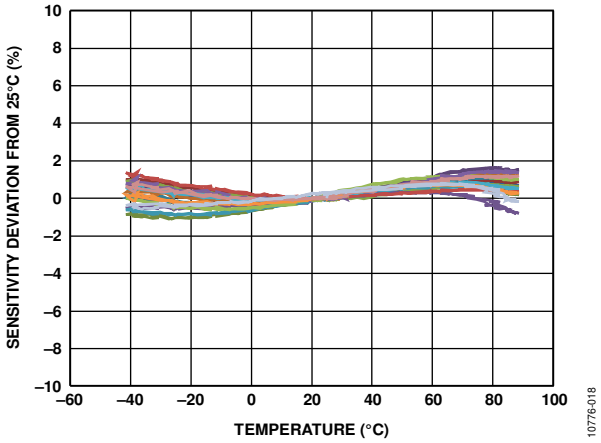

Figure 18. Y-Axis Sensitivity Deviation from 25°C vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, V_S = 2 V

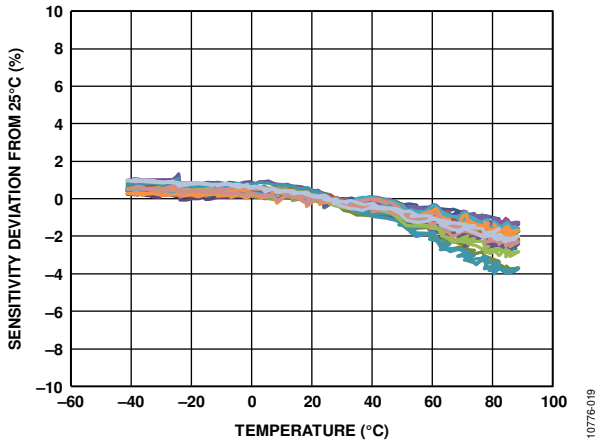

Figure 19. Z-Axis Sensitivity Deviation from 25°C vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, V_S = 2 V

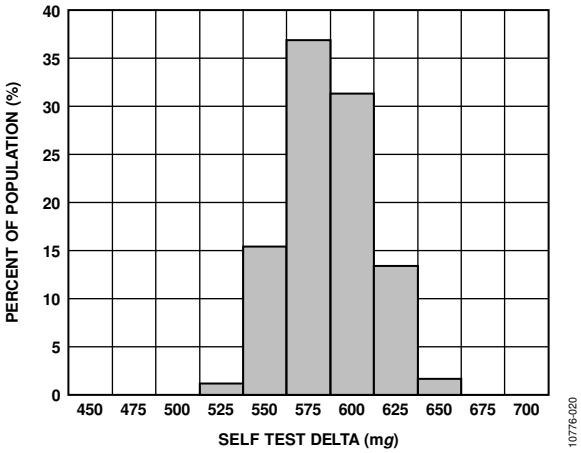

Figure 20. X-Axis Self Test Response at 25°C, V_S = 2 V

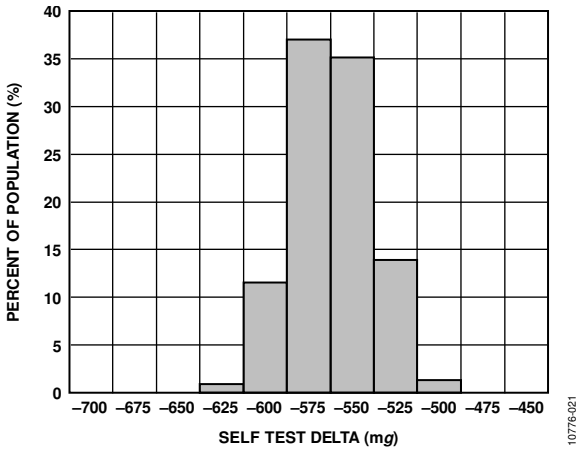

Figure 21. Y-Axis Self Test Response at 25°C, V_S = 2 V

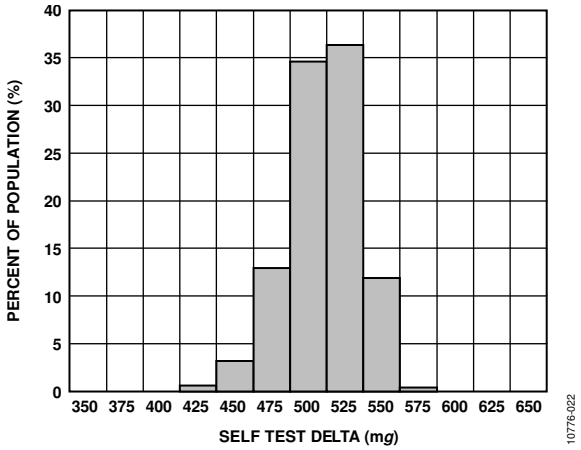

Figure 22. Z-Axis Self Test Response at 25°C, V_S = 2 V

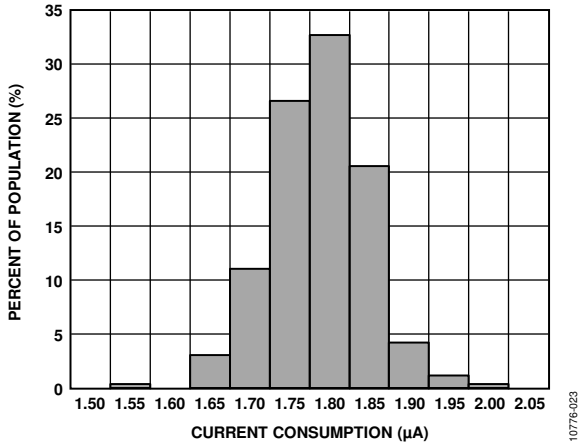

Figure 23. Current Consumption at 25°C, Normal Mode, ODR = 100 Hz, V_S = 2 V

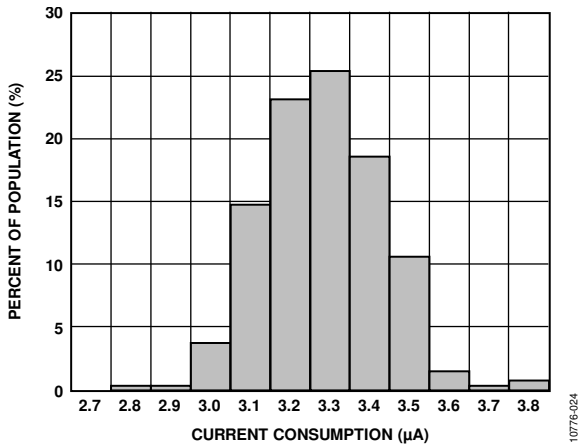

Figure 24. Current Consumption at 25°C, Low Noise Mode, ODR = 100 Hz, V_S = 2 V

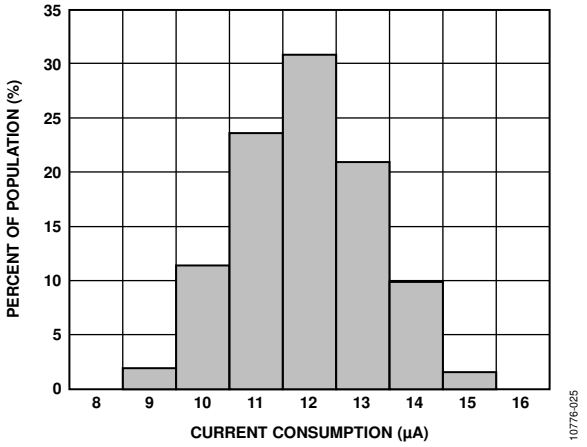

Figure 25. Current Consumption at 25°C, Ultralow Noise Mode, ODR = 100 Hz, V_S = 2 V

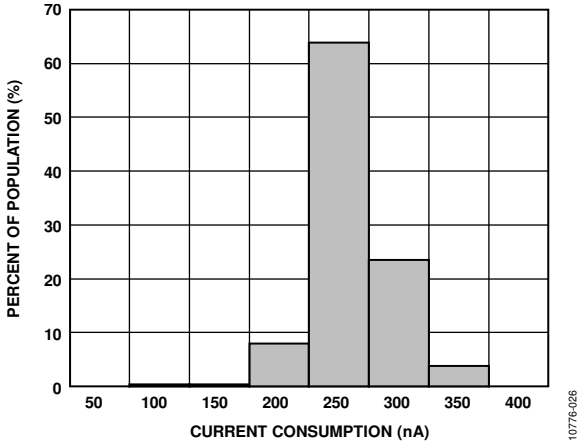

Figure 26. Current Consumption at 25°C, Wake-Up Mode, V_S = 2 V

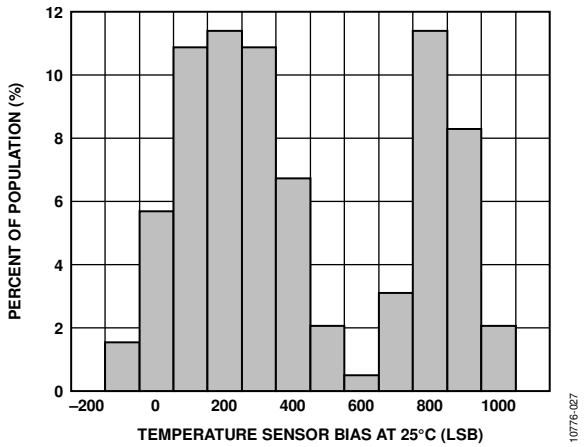

Figure 27. Temperature Sensor Response at 25°C, V_S = 2 V

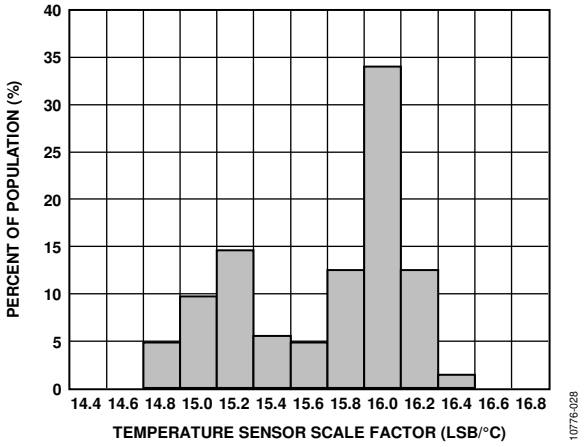

Figure 28. Temperature Sensor Scale Factor, V_S = 2 V

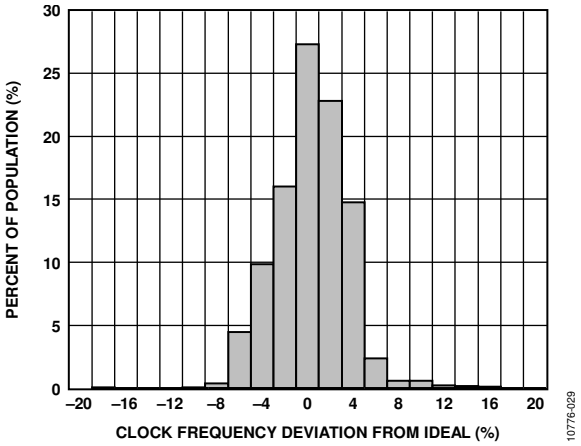

Figure 29. Clock Frequency Deviation from Ideal at 25°C, V_S = 2 V

THEORY OF OPERATION

The ADXL362 is a complete 3-axis acceleration measurement system that operates at extremely low power consumption levels. It measures both dynamic acceleration, resulting from motion or shock, and static acceleration, such as tilt. Acceleration is reported digitally and the device communicates via the SPI protocol. Built-in digital logic enables autonomous operation and implements functionality that enhances system level power savings.

MECHANICAL DEVICE OPERATION

The moving component of the sensor is a polysilicon surface-micromachined structure that is built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against acceleration forces.

Deflection of the structure is measured using differential capacitors that consist of independent fixed plates and plates attached to the moving mass. Acceleration deflects the structure and unbalances the differential capacitor, resulting in a sensor output whose amplitude is proportional to acceleration. Phase sensitive demodulation determines the magnitude and polarity of the acceleration.

OPERATING MODES

The ADXL362 has two operating modes: measurement mode for continuous, wide bandwidth sensing; and wake-up mode for limited bandwidth activity detection. In addition, measurement can be suspended altogether by placing the device in standby.

Measurement Mode

Measurement mode is the normal operating mode of the ADXL362. In this mode, acceleration data is read continuously and the accelerometer consumes less than 3 μA (typical) across its entire range of output data rates of up to 400 Hz using a 2.0 V supply. All features described in this datasheet are available when operating the ADXL362 in this mode.

The ability to continuously output data from the minimum 12.5 Hz to the maximum 400 Hz data rate while still delivering less than 3 μA (typical) of current consumption is what defines the ADXL362 as an ultralow power accelerometer. Other accelerometers derive low current by using a specific low power mode that power cycles acceleration sensing. The result is a small effective bandwidth in the low power modes and undersampling of input data; therefore, unwanted aliasing can occur. Undersampling and aliasing do not occur with the ADXL362 because it continuously samples the full bandwidth of its sensor at all data rates.

Wake-Up Mode

Wake-up mode is ideal for simple detection of the presence or absence of motion at extremely low power consumption (270 nA at a 2.0 V supply voltage). Wake-up mode is useful particularly for implementation of a motion activated on/off switch, allowing the rest of the system to be powered down until activity is detected.

Wake-up mode reduces current consumption to a very low level by measuring acceleration only about six times per second to determine whether motion is present. If motion is detected, the accelerometer can respond autonomously in the following ways:

- Switch into full bandwidth measurement mode
- Signal an interrupt to a microcontroller
- Wake up downstream circuitry, depending on the configuration
- In wake-up mode, all accelerometer features are available with the exception of the activity timer. All registers can be accessed, and real-time data can be read and/or stored in the FIFO.

Standby

Placing the ADXL362 in standby suspends measurement and reduces current consumption to 10 nA (typical). Pending interrupts and data are preserved and no new interrupts are generated.

The ADXL362 powers up in standby with all sensor functions turned off.

SELECTABLE MEASUREMENT RANGES

The ADXL362 has selectable measurement ranges of ±2 *g*, ±4 *g*, and ±8 g. Acceleration samples are always converted by a 12-bit ADC; therefore, sensitivity scales with g range. Ranges and corresponding sensitivity values are listed in Table 1. Data can temporarily not represent maximum gees while overranging but no damage is caused to the accelerometer when acceleration exceeds the corresponding range maximum. Table 2 lists the absolute maximum ratings for acceleration, indicating the acceleration level that can cause permanent damage to the device.

SELECTABLE OUTPUT DATA RATES

The ADXL362 can report acceleration data at various data rates ranging from 12.5 Hz to 400 Hz. The internal low-pass filter pole is automatically set to ¼ or ½ the selected ODR (based on the HALF_BW setting) to ensure the Nyquist sampling criterion is met and no aliasing occurs.

Current consumption varies somewhat with output data rate as shown in Figure 30, remaining below 5.0 µA over the entire range of data rates and operating voltages.

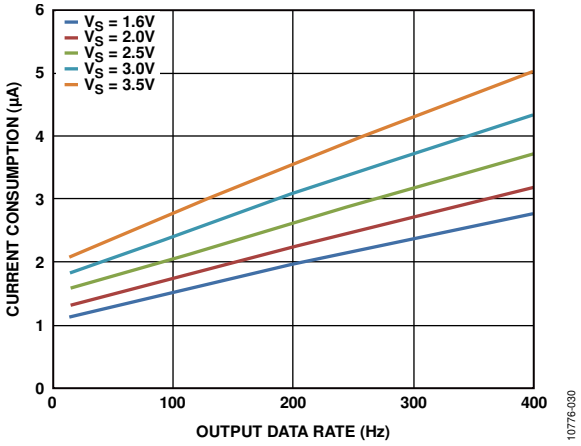

Figure 30. Current Consumption vs. Output Data Rate at Several Supply Voltages

Antialiasing

The analog-to-digital converter (ADC) of the ADXL362 samples at the (user selected) output data rate. In the absence of antialiasing filtering, it aliases any input signals whose frequency is more than half the data rate. To mitigate this, a two-pole low-pass filter is provided at the input of the ADC.

The user can set this antialiasing filter to a bandwidth that is at ½ the data rate or ¼ the data rate. Setting the antialiasing filter pole to ½ of the output data rate provides less aggressive antialiasing filtering, but maximizes bandwidth and is adequate for most applications. Setting the pole to ¼ of the data rate reduces bandwidth for a given data rate, but provides more aggressive antialiasing.

The antialiasing filter of the ADXL362 defaults to the more conservative setting, where bandwidth is set to one-fourth the output data rate.

POWER/NOISE TRADEOFF

The ADXL362 offers a few options for decreasing noise at the expense of only a small increase in current consumption.

The noise performance of the ADXL362 in normal operation, typically 7 LSB rms at 100 Hz bandwidth, is adequate for most applications, depending upon bandwidth and the desired resolution. For cases where lower noise is needed, the ADXL362 provides two lower noise operating modes that trade reduced noise for a somewhat higher current consumption.

Table 7 lists the current consumption and noise densities obtained for normal operation and the two lower noise modes at a typical 2.0 V supply.

Table 7. Noise and Current Consumption: Normal Operation, Low Noise Mode, and Ultralow Noise Mode at V_S = 2.0 V, ODR = 100 Hz

Mode	Noise (µg/√Hz) Typical	Current Consumption (µA) Typical
Normal Operation	550	1.8
Low Noise	400	3.3
Ultralow Noise	250	13

Operating the ADXL362 at a higher supply voltage also decreases noise. Table 8 lists the current consumption and noise densities obtained for normal operation and the two lower noise modes at the highest recommended supply, 3.3 V.

Table 8. Noise and Current Consumption: Normal Operation, Low Noise Mode, and Ultralow Noise Mode at V_S = 3.3 V, ODR = 100 Hz

Mode	Noise (µg/√Hz) Typical	Current Consumption (µA) Typical
Normal Operation	380	2.7
Low Noise	280	4.5
Ultralow Noise	175	15

POWER SAVINGS FEATURES

Designed for the most power conscious applications, the ADXL362 includes several features (as described in this section) for enabling power savings at the system level, as well as at the device level.

ULTRALOW POWER CONSUMPTION IN ALL MODES

At the device level, the most obvious power saving feature of the ADXL362 is its ultralow current consumption in all configurations. The ADXL362 consumes between 1.1 µA (typical) and 5 µA (typical) across all data rates up to 400 Hz and all supply voltages up to 3.5 V (see Figure 30). An even lower power, 270 nA (typical) motion triggered wake-up mode is provided for simple motion detection applications that require a power consumption lower than 1 µA.

At these current levels, the accelerometer consumes less power in full operation than the standby currents of many other system components, and is, therefore, optimal for applications that require continuous acceleration monitoring and very long battery life. Because the accelerometer is always on, it can act as a motion activation switch. The accelerometer signals to the rest of the system when to turn on, thereby managing power at the system level.

As important as its low operating current, the 10 nA (typical) standby current of the ADXL362 contributes to a much longer battery life in applications that spend most of their time in a sleep state and wake up via an external trigger.

MOTION DETECTION

The ADXL362 features built-in logic that detects activity (presence of acceleration above a threshold) and inactivity (lack of acceleration above a threshold). Activity and inactivity events can be used as triggers to manage the accelerometer mode of operation, trigger an interrupt to a host processor, and/or autonomously drive a motion switch.

Detection of an activity or inactivity event is indicated in the status register and can be configured to generate an interrupt. In addition, the activity status of the device, that is, whether it is moving or stationary, is indicated by the AWAKE bit, described in the Using the AWAKE Bit section.

Activity and inactivity detection can be used when the accelerometer is in either measurement mode or wake-up mode.

Activity Detection

An activity event is detected when acceleration remains above a specified threshold for a specified time period.

Referenced and Absolute Configurations

Activity detection can be configured as referenced or absolute.

When using absolute activity detection, acceleration samples are compared to a user set threshold to determine whether motion is present. For example, if a threshold of 0.5 *g* is set and the acceleration on the z-axis is 1 *g* for longer than the user defined activity time, the activity status asserts.

In many applications, it is advantageous for activity detection to be based not on an absolute threshold, but on a deviation from a reference point or orientation. This is particularly useful because it removes the effect on activity detection of the static 1 *g* imposed by gravity. When an accelerometer is stationary, its output can reach 1 *g*, even when it is not moving. In absolute activity, when the threshold is set to less than 1 *g*, activity is immediately detected in this case.

In the referenced configuration, activity is detected when acceleration samples are at least a user set amount above an internally defined reference for the user defined amount of time, as described in Equation 1.

$$ABS(Acceleration - Reference) > Threshold \quad (1)$$

Consequently, activity is detected only when the acceleration has deviated sufficiently from the initial orientation. The reference for activity detection is calculated when activity detection is engaged in the following scenarios:

- When the activity function is turned on and measurement mode is engaged;
- If link mode is enabled: when inactivity is detected and activity detection begins; or
- If link mode is not enabled: when activity is detected and activity detection repeats.

The referenced configuration results in a very sensitive activity detection that detects even the most subtle motion events.

Fewer False Positives

Ideally, the intent of activity detection is to wake up a system only when motion is intentional, ignoring noise or small, unintentional movements. In addition to being sensitive to subtle motion events, the ADXL362 activity detection algorithm is designed to be robust in filtering out undesired triggers.

The ADXL362 activity detection functionality includes a timer to filter out unwanted motion and ensure that only sustained motion is recognized as activity. The duration of this timer, as well as the acceleration threshold, are user adjustable from one sample (that is, no timer) to up to 20 seconds of motion.

Note that the activity timer is operational in measurement mode only. In wake-up mode, one-sample activity detection is used.

Inactivity Detection

An inactivity event is detected when acceleration remains below a specified threshold for a specified time. Inactivity detection is also configurable as referenced or absolute.

When using absolute inactivity detection, acceleration samples are compared to a user set threshold for the user set time to determine the absence of motion. Inactivity is detected when enough consecutive samples are all below the threshold. The absolute configuration of inactivity must be used for implementing free fall detection.

When using referenced inactivity detection, inactivity is detected when acceleration samples are within a user specified amount of an internally defined reference (as described by Equation 2) for a user defined amount of time.

$$ABS(Acceleration - Reference) < Threshold \quad (2)$$

Referenced inactivity, like referenced activity, is particularly useful for eliminating the effects of the static acceleration due to gravity. With absolute inactivity, if the inactivity threshold is set lower than 1 *g*, a device resting motionless may never detect inactivity. With referenced inactivity, the same device under the same configuration detects inactivity.

The inactivity timer can be set to anywhere from 2.5 ms (a single sample at 400 Hz ODR) to almost 90 minutes (65,535 samples at 12.5 Hz ODR) of inactivity. A requirement for inactivity detection is that for whatever period of time the inactivity timer has been configured, the accelerometer detects inactivity only when it has been stationary for that amount of time.

For example, if the accelerometer has been configured for 90 minutes, the accelerometer detects inactivity when it has been stationary for 90 minutes. The wide range of timer settings means that in applications where power conservation is critical, the system can be put to sleep after very short periods of inactivity. In applications where continuous operation is critical, the system stays on for as long as any motion is present.

Linking Activity and Inactivity Detection

The activity and inactivity detection functions can be used concurrently and processed manually by a host processor, or they can be configured to interact in several other ways, as follows.

Default Mode

The user must enable the activity and inactivity functions because these functions are not automatically enabled by default. After the user enables the activity and inactivity functions, the ADXL362 exhibits the following behavior when it enters default mode: Both activity and inactivity detection remain enabled and all interrupts must be serviced by a host processor; that is, a processor must read each interrupt before it is cleared and can be used again.

Loop mode operation is illustrated in the flowchart in Figure 32.

Linked Mode

In linked mode, activity and inactivity detection are linked to each other such that only one of the functions is enabled at any given time. As soon as activity is detected, the device is assumed to be moving (or awake) and stops looking for activity; rather, inactivity is expected as the next event. Therefore, only inactivity detection operates.

Similarly, when inactivity is detected, the device is assumed to be stationary (or asleep). Thus, activity is expected as the next event; therefore, only activity detection operates.

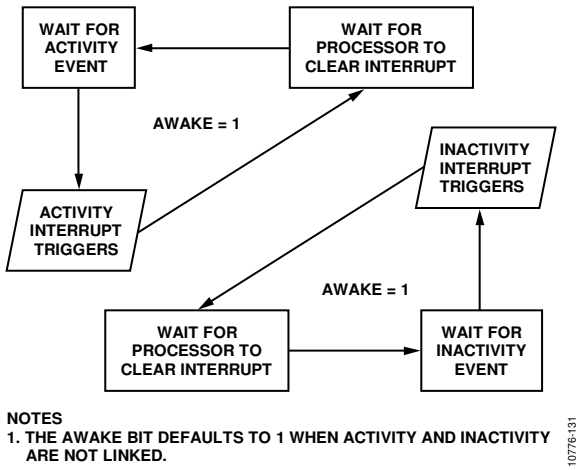

Figure 31. Flowchart Illustrating Activity and Inactivity Operation in Default Mode

In linked mode, each interrupt must be serviced by a host processor before the next interrupt is enabled.

Linked mode operation is illustrated in the flowchart in Figure 32.

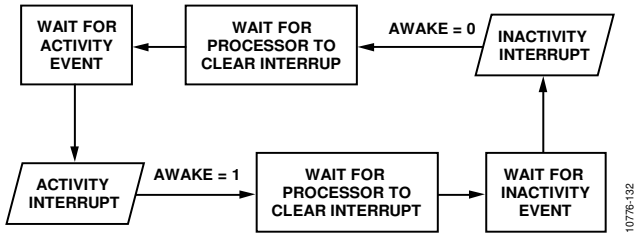

Figure 32. Flowchart Illustrating Activity and Inactivity Operation in Linked Mode

Loop Mode

In loop mode, motion detection operates as described in the Linked Mode section, but interrupts do not need to be serviced by a host processor. This configuration simplifies the implementation of commonly used motion detection and enhances power savings by reducing the amount of power used in bus communication.

Loop mode operation is illustrated in the flowchart in Figure 33.

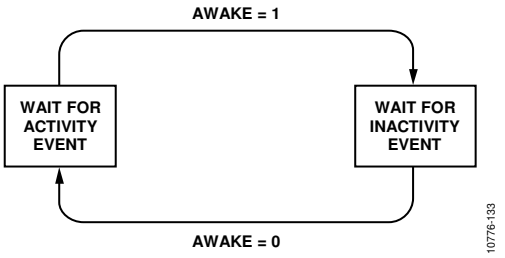

Figure 33. Flowchart Illustrating Activity and Inactivity Operation in Loop Mode

Autosleep

When in linked or loop mode, enabling autosleep causes the device to enter wake-up mode autonomously (see the Wake-Up Mode section) when inactivity is detected, and to reenter measurement mode when activity is detected.

The autosleep configuration is active only if linked or loop modes are enabled. In the default mode, the autosleep setting is ignored.

Using the AWAKE Bit

The AWAKE bit is a status bit that indicates whether the ADXL362 is awake or asleep. The device is awake when it has experienced an activity condition, and it is asleep when it has experienced an inactivity condition.

The awake signal can be mapped to the INT1 or INT2 pin, allowing the pin to serve as a status output to connect or disconnect power to downstream circuitry based on the awake status of the accelerometer. Used in conjunction with loop mode, this configuration implements a trivial, autonomous motion activated switch, as shown in Figure 43.

If the turn-on time of downstream circuitry can be tolerated, this motion switch configuration can save significant system level power by eliminating the standby current consumption of the remainder of the application. This standby current can often exceed the full operating current of the ADXL362.

FIFO

The ADXL362 includes a deep 512-sample first in, first out (FIFO) buffer. The FIFO provides benefits primarily in two ways, as follows.

System Level Power Savings

Appropriate use of the FIFO enables system level power savings by enabling the host processor to sleep for extended periods of time while the accelerometer autonomously collects data. Alternatively, using the FIFO to collect data can unburden the host while it tends to other tasks.

Data Recording/Event Context

The FIFO can be used in a triggered mode to record all data leading up to an activity detection event, thereby providing context for the event. In the case of a system that identifies impact events, for example, the accelerometer can keep the entire system off while it stores acceleration data in its FIFO and looks for an activity event. When the impact event occurs, data that was collected prior to the event is frozen in the FIFO. The accelerometer can then wake the rest of the system and transfer this data to the host processor, thereby providing context for the impact event.

Generally, the more context available, the more intelligent decisions a system can achieve, making a deep FIFO especially useful. The ADXL362 FIFO can store up to more than 13 seconds of data, providing a clear picture of events prior to an activity trigger.

All FIFO modes of operation, as well as the structure of the FIFO and instructions for retrieving data from it, are described in further detail in the FIFO Modes section of this data sheet.

COMMUNICATIONS

SPI Instructions

The digital interface of the ADXL362 is implemented with system level power savings in mind. The following features enhance power savings:

- Burst reads and writes reduce the number of SPI communication cycles required to configure the device and retrieve data.
- Concurrent operation of activity and inactivity detection enables "set it and forget it" operation. Loop mode further reduces communications power by enabling the clearing of interrupts without processor intervention.
- The FIFO is implemented such that consecutive samples can be read continuously via a multibyte read of unlimited length; thus, one read FIFO instruction can clear the entire contents of the FIFO. In many other accelerometers, each read instruction retrieves a single sample only. In addition, the ADXL362 FIFO construction allows the use of direct memory access (DMA) to read the FIFO contents.

Bus Keepers

The ADXL362 includes bus keepers on all pins that can be configured as digital inputs: MOSI, SCLK, $\overline{CS}$, INT1, and INT2. Bus keepers prevent tristate bus lines from floating when nothing is driving them, thus preventing through current in any gate inputs that are on the bus.

MSB Registers

Acceleration and temperature measurements are converted to 12-bit values and transmitted via SPI using two registers per measurement. To read a full sample set of 3-axis acceleration data, six registers must be read.

Many applications do not require the accuracy that 12-bit data provides and prefer, instead, to save system level power. The MSB registers XDATA, YDATA, and ZDATA enable this tradeoff. These registers contain the eight MSBs of the x-, y-, and z-axis acceleration data; reading them effectively provides 8-bit acceleration values. Importantly, only three (consecutive) registers must be read to retrieve a full data set, significantly reducing the time during which the SPI bus is active and drawing current.

12-bit and 8-bit data are available simultaneously so that both data formats can be used in a single application, depending on the needs of the application at a given time. For example, the processor can read 12-bit data when higher resolution is required, and switch to 8-bit data (simply by reading a different set of registers) when application requirements change.

ADDITIONAL FEATURES

FREE FALL DETECTION

Many digital output accelerometers include a built-in free fall detection feature. In the ADXL362, this function can be implemented using the inactivity interrupt. Refer to the Applications Information section for more details, including suggested threshold and timing values.

EXTERNAL CLOCK

The ADXL362 has a built-in 51.2 kHz (typical) clock that, by default, serves as the time base for internal operations.

ODR and bandwidth scale proportionally with the clock. The ADXL362 provides a discrete number of options for ODR, such as 100 Hz, 50 Hz, 25 Hz, and so forth, in factors of 2, (see the Filter Control Register section for a complete listing). To achieve data rates other than those provided, an external clock can be used at the appropriate clock frequency. The output data rate scales with the clock frequency, as shown in Equation 3.

$$ODR_{ACTUAL} = ODR_{SELECTED} \times \frac{f}{51.2\text{ kHz}} \quad (3)$$

For example, to achieve an 80 Hz ODR, select the 100 Hz ODR setting and provide a clock frequency that is 80% of nominal, or 41.0 kHz.

The ADXL362 can operate with external clock frequencies ranging from the nominal 51.2 kHz down to 25.6 kHz to allow the user to achieve any desired output data rate.

Alternatively, an external clock can improve clock frequency accuracy. The distribution of clock frequencies among a sampling of >1000 parts has a standard deviation of approximately 3%. To achieve tighter tolerances, a more accurate clock can be provided externally.

Bandwidth automatically scales to ½ or ¼ of the ODR (based on the HALF_BW setting), and this ratio is preserved, regardless of clock frequency. Power consumption also scales with clock frequency: higher clock rates increase power consumption. Figure 34 shows how power consumption varies with clock rate.

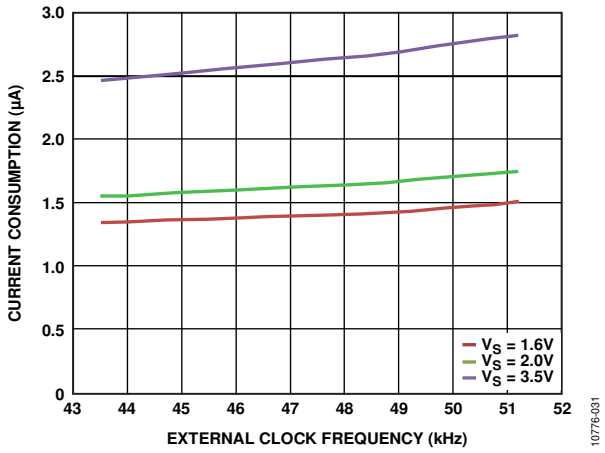

Figure 34. Current Consumption vs. External Clock Rate

SYNCHRONIZED DATA SAMPLING

For applications that require a precisely timed acceleration measurement, the ADXL362 features an option to synchronize acceleration sampling to an external trigger.

SELF TEST

The ADXL362 incorporates a self test feature that effectively tests its mechanical and electronic systems simultaneously. When the self test function is invoked, an electrostatic force is applied to the mechanical sensor. This electrostatic force moves the mechanical sensing element in the same manner as acceleration, and it is additive to the acceleration experienced by the device. This added electrostatic force results in an output change on all three axes.

USER REGISTER PROTECTION

The ADXL362 includes user register protection for single event upsets (SEUs). An SEU is a change of state caused by ions or electromagnetic radiation striking a sensitive node in a microelectronic device. The state change is a result of the free charge created by ionization in or close to an important node of a logic element (for example, a memory bit). The SEU, itself, is not considered permanently damaging to transistor or circuit functionality, but it can create erroneous register values. The ADXL362 registers that are protected from SEU are Register 0x20 to Register 0x2E.

SEU protection is implemented via a 99-bit error correcting (Hamming-type) code that detects both single- and double-bit errors. The check bits are recomputed any time a write to any of the protected registers occurs. At any time, if the stored version of the check bits is not in agreement with the current check bit calculation, the ERR_USER_REGS status bit is set.

The SEU bit in the status register is set on power-up prior to device configuration; it clears upon the first register write to that device.

TEMPERATURE SENSOR

The ADXL362 includes an integrated temperature sensor that can monitor internal system temperature or improve the temperature stability of the device via calibration. For example, acceleration outputs vary with temperature at a rate of ±0.5 mg/°C (typical), but the relationship to temperature is repeatable and can be calibrated.

To use the temperature sensor to monitor absolute temperature, it is recommended that its initial bias (its output at some known temperature) is measured and calibrated.

SERIAL COMMUNICATIONS

The ADXL362 communicates via a 4-wire SPI and operates as a slave. Ignore data that is transmitted from the ADXL362 to the master device during writes to the ADXL362.

As shown in Figure 36 to Figure 40, the MISO pin is in a high impedance state, held by a bus keeper, except when the ADXL362 is sending read data (to conserve bus power).

Wire the ADXL362 for SPI communication as shown in the connection diagram in Figure 35. The recommended SPI clock speeds are 1 MHz to 8 MHz, with 12 pF maximum loading.

The SPI timing scheme follows CPHA = CPOL = 0.

For correct operation of the device, the logic thresholds and timing parameters in Table 9 and Table 10 must be met at all times. Refer to Figure 41 and Figure 42 for visual diagrams of the timing parameters.

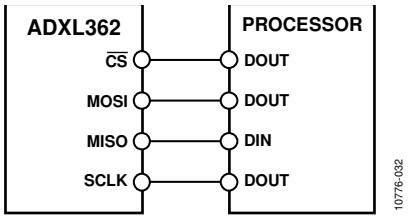

Figure 35. 4-Wire SPI Connection Diagram

SPI COMMANDS

The SPI port uses a multibyte structure wherein the first byte is a command. The ADXL362 command set is

- 0x0A: write register
- 0x0B: read register
- 0x0D: read FIFO

Read and Write Register Commands

The command structure for the read register and write register commands is as follows (see Figure 36 and Figure 37):

</CS down> <command byte (0x0A or 0x0B)> <address byte> <data byte> <additional data bytes for multi-byte> … </CS up>

The read and write register commands support multibyte (burst) read/write access. The waveform diagrams for multi-byte read and write commands are shown in Figure 38 and Figure 39.

Read FIFO Command

Reading from the FIFO buffer is a command structure that does not have an address.

</CS down> <command byte (0x0D)> <data byte> <data byte> … </CS up>

It is recommended that an even number of bytes be read (using a multibyte transaction) because each sample consists of two bytes: 2 bits of axis information and 14 bits of data. If an odd number of bytes is read, it is assumed that the desired data was read; therefore, the second half of the last sample is discarded so a read from the FIFO always starts on a properly aligned even-byte boundary. Data is presented least significant byte first, followed by the most significant byte.

MULTIBYTE TRANSFERS

Multibyte transfers, also known as burst transfers, are supported for all SPI commands: register read, register write, and FIFO read commands. It is recommended that data be read using multibyte transfers to ensure that a concurrent and complete set of x-, y-, and z-acceleration (and temperature, where applicable) data is read.

The FIFO runs on the serial port clock during FIFO reads and can sustain bursting at the SPI clock rate as long as the SPI clock is 1 MHz or faster.

Register Read/Write Auto-Increment

A register read or write command begins with the address specified in the command and auto-increments for each additional byte in the transfer. To avoid address wrapping and side effects of reading registers multiple times, the auto-increment halts at the invalid Register Address 63 (0x3F).

INVALID ADDRESSES AND ADDRESS FOLDING

The ADXL362 has a 6-bit address bus, mapping only 64 registers in the possible 256 register address space. The addresses do not fold to repeat the registers at addresses above 64. Attempted access to register addresses above 64 are mapped to the invalid register at 63 (0x3F) and have no functional effect.

Address 0x00 to Address 0x2E are for customer access, as described in the register map. Address 0x2F to Address 0x3F are reserved for factory use.

LATENCY RESTRICTIONS

Reading any of the data registers (0x08 to 0x0A or 0x0E to 0x15) clears the data ready interrupt. There can be as much as an 80 µs delay from reading a register to the clearing of the data ready interrupt.

Other register reads, register writes, and FIFO reads have no latency restrictions.

INVALID COMMANDS

Commands other than 0x0A, 0x0B, and 0x0D have no effect. The MISO output remains in a high impedance state, and the bus keeper holds the MISO line at its last value.

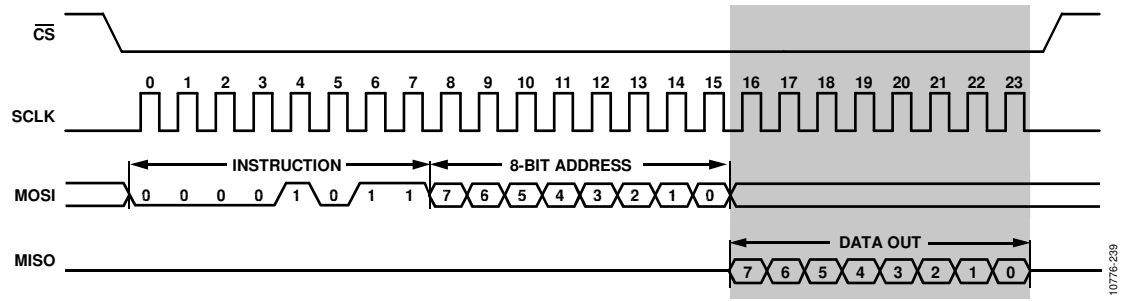

Figure 36. Register Read

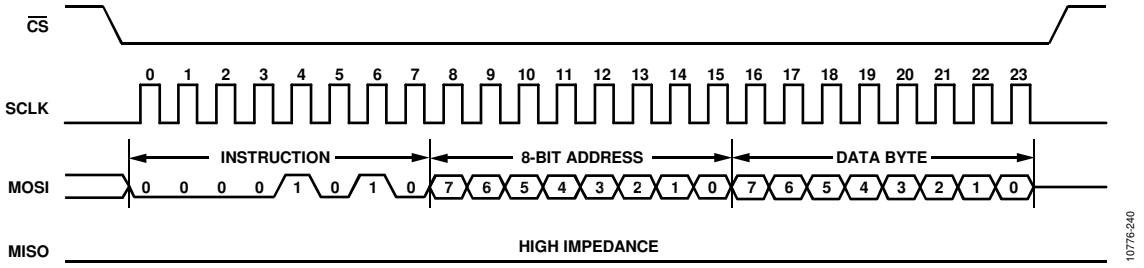

Figure 37. Register Write (Receive Instruction Only)

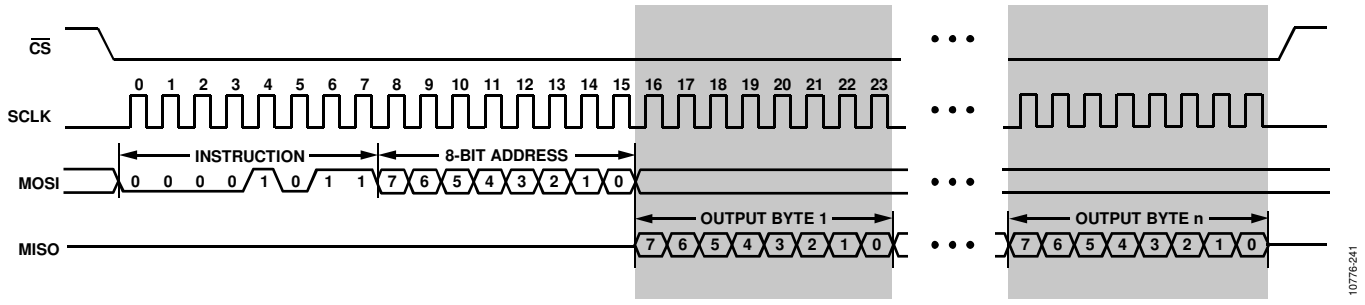

Figure 38. Burst Read

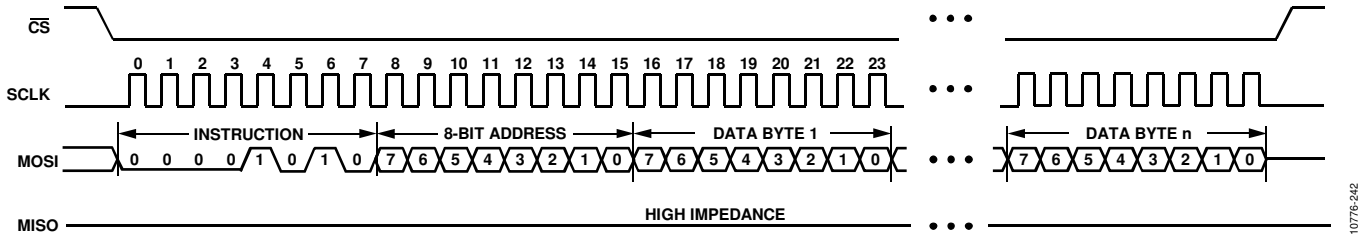

Figure 39. Burst Write (Receive Instruction Only)

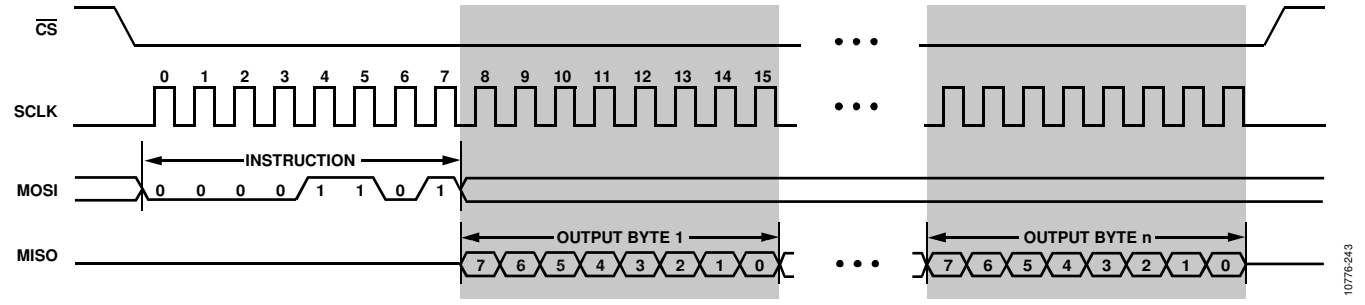

Figure 40. FIFO Read

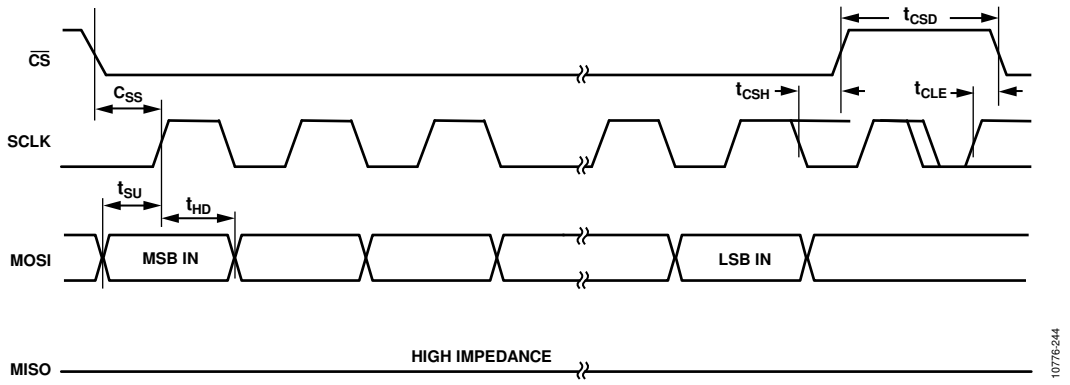

Figure 41. Timing Diagram for SPI Receive Instructions

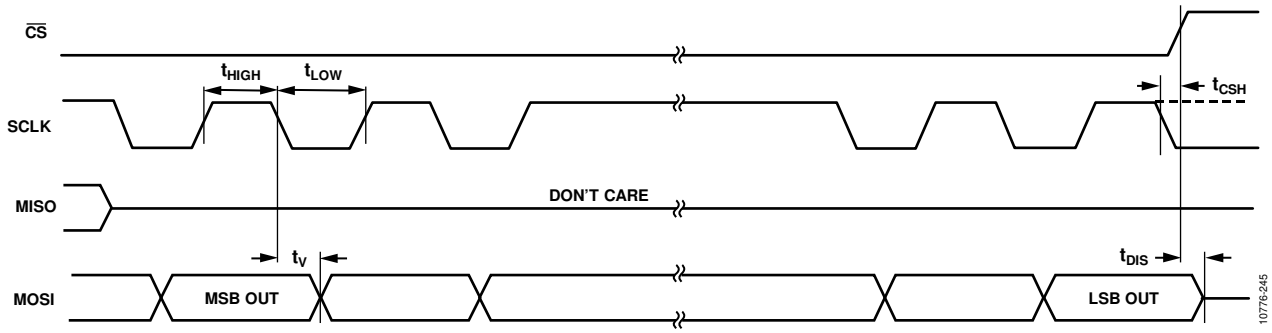

Figure 42. Timing Diagram for SPI Send Instructions (Shaded Portions of Figure 36, Figure 38, and Figure 40)

Table 9. SPI Digital Input/Output

Parameter	Test Conditions/Comments	Limit[1] Min	Limit[1] Max	Unit
Digital Input				
Low Level Input Voltage (V_{IL})			$0.3 \times V_{DD\ I/O}$	V
High Level Input Voltage (V_{IH})		$0.7 \times V_{DD\ I/O}$		V
Low Level Input Current (I_{IL})	$V_{IN} = V_{DD\ I/O}$		0.1	μA
High Level Input Current (I_{IH})	$V_{IN} = 0$ V	−0.1		μA
Digital Output				
Low Level Output Voltage (V_{OL})	$I_{OL} = 10$ mA		$0.2 \times V_{DD\ I/O}$	V
High Level Output Voltage (V_{OH})	$I_{OH} = -4$ mA	$0.8 \times V_{DD\ I/O}$		V
Low Level Output Current (I_{OL})	$V_{OL} = V_{OL,\ max}$	10		mA
High Level Output Current (I_{OH})	$V_{OH} = V_{OH,\ min}$		−4	mA

[1] Limits based on characterization results, not production tested.

Table 10. SPI Timing (T_A = 25°C, V_S = 2.0 V, $V_{DD\ I/O}$ = 2.0 V)

	Limit[1, 2]			
Parameter	**Min**	**Max**	**Unit**	**Description**
f_{CLK}[3]	2.4	8000	kHz	Clock Frequency
C_{SS}	100		ns	$\overline{CS}$ Setup Time
t_{CSH}	20		ns	$\overline{CS}$ Hold Time
t_{CSD}	20		ns	$\overline{CS}$ Disable Time
t_{SU}	20		ns	Data Setup Time
t_{HD}	20		ns	Data Hold Time
t_{HIGH}	50		ns	Clock High Time
t_{LOW}	50		ns	Clock Low Time
t_{CLE}	25		ns	Clock Enable Time
t_V	0	35	ns	Output Valid from Clock Low
t_{DIS}	0	25	ns	Output Disable Time

[1] Limits based on design targets; not production tested.
[2] The timing values are measured corresponding to the input thresholds (V_{IL} and V_{IH}) given in Table 9.
[3] The minimum limit is only necessary when using FIFO.

REGISTER MAP

Table 11. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	DEVID_AD	[7:0]	DEVID_AD[7:0]								0xAD	R
0x01	DEVID_MST	[7:0]	DEVID_MST[7:0]								0x1D	R
0x02	PARTID	[7:0]	PARTID[7:0]								0xF2	R
0x03	REVID	[7:0]	REVID[7:0]								0x01	R
0x08	XDATA	[7:0]	XDATA[7:0]								0x00	R
0x09	YDATA	[7:0]	YDATA[7:0]								0x00	R
0x0A	ZDATA	[7:0]	ZDATA[7:0]								0x00	R
0x0B	STATUS	[7:0]	ERR_USER_REGS	AWAKE	INACT	ACT	FIFO_OVER-RUN	FIFO_WATER-MARK	FIFO_READY	DATA_READY	0x40	R
0x0C	FIFO_ENTRIES_L	[7:0]	FIFO_ENTRIES_L[7:0]								0x00	R
0x0D	FIFO_ENTRIES_H	[7:0]	UNUSED						FIFO_ENTRIES_H[1:0]		0x00	R
0x0E	XDATA_L	[7:0]	XDATA_L[7:0]								0x00	R
0x0F	XDATA_H	[7:0]	SX				XDATA_H[3:0]				0x00	R
0x10	YDATA_L	[7:0]	YDATA_L[7:0]								0x00	R
0x11	YDATA_H	[7:0]	SX				YDATA_H[3:0]				0x00	R
0x12	ZDATA_L	[7:0]	ZDATA_L[7:0]								0x00	R
0x13	ZDATA_H	[7:0]	SX				ZDATA_H[3:0]				0x00	R
0x14	TEMP_L	[7:0]	TEMP_L[7:0]								0x00	R
0x15	TEMP_H	[7:0]	SX				TEMP_H[3:0]				0x00	R
0x16	Reserved	[7:0]	Reserved[7:0]								0x00	R
0x17	Reserved	[7:0]	Reserved[7:0]								0x00	R
0x1F	SOFT_RESET	[7:0]	SOFT_RESET[7:0]								0x00	W
0x20	THRESH_ACT_L	[7:0]	THRESH_ACT_L[7:0]								0x00	RW
0x21	THRESH_ACT_H	[7:0]	UNUSED					THRESH_ACT_H[2:0]			0x00	RW
0x22	TIME_ACT	[7:0]	TIME_ACT[7:0]								0x00	RW
0x23	THRESH_INACT_L	[7:0]	THRESH_INACT_L[7:0]								0x00	RW
0x24	THRESH_INACT_H	[7:0]	UNUSED					THRESH_INACT_H[2:0]			0x00	RW
0x25	TIME_INACT_L	[7:0]	TIME_INACT_L[7:0]								0x00	RW
0x26	TIME_INACT_H	[7:0]	TIME_INACT_H[7:0]								0x00	RW
0x27	ACT_INACT_CTL	[7:0]	RES		LINKLOOP		INACT_REF	INACT_EN	ACT_REF	ACT_EN	0x00	RW
0x28	FIFO_CONTROL	[7:0]	UNUSED				AH	FIFO_TEMP	FIFO_MODE		0x00	RW
0x29	FIFO_SAMPLES	[7:0]	FIFO_SAMPLES[7:0]								0x80	RW
0x2A	INTMAP1	[7:0]	INT_LOW	AWAKE	INACT	ACT	FIFO_OVER-RUN	FIFO_WATER-MARK	FIFO_READY	DATA_READY	0x00	RW
0x2B	INTMAP2	[7:0]	INT_LOW	AWAKE	INACT	ACT	FIFO_OVER-RUN	FIFO_WATER-MARK	FIFO_READY	DATA_READY	0x00	RW
0x2C	FILTER_CTL	[7:0]	RANGE		RES	HALF_BW	EXT_SAMPLE	ODR			0x13	RW
0x2D	POWER_CTL	[7:0]	RES	EXT_CLK	LOW_NOISE		WAKEUP	AUTOSLEEP	MEASURE		0x00	RW
0x2E	SELF_TEST	[7:0]	UNUSED							ST	0x00	RW

REGISTER DETAILS

This section describes the functions of the ADXL362 registers. The ADXL362 powers up with default register values in the as shown in the Reset column of Table 11 in the Register Map section.

Note that any changes to the registers before the POWER_CTL register (Register 0x00 to Register 0x2C) must be made with the device in standby. If changes are made while the ADXL362 is in measurement mode, they can be effective for only part of a measurement.

DEVICE ID REGISTER

Address: 0x00, Reset: 0xAD, Name: DEVID_AD

This register contains the Analog Devices device ID, 0xAD.

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	1	1	0	1

DEVICE ID: 0x1D REGISTER

Address: 0x01, Reset: 0x1D, Name: DEVID_MST

This register contains the Analog Devices MEMS device ID, 0x1D.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	1	1	1	0	1

PART ID: 0xF2 REGISTER

Address: 0x02, Reset: 0xF2, Name: PARTID

This register contains the device ID, 0xF2 (362 octal).

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	0	0	1	0

SILICON REVISION ID REGISTER

Address: 0x03, Reset: 0x01, Name: REVID

This register contains the product revision ID, beginning with 0x01 and incrementing for each subsequent revision.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	1

X-AXIS DATA (8 MSB) REGISTER

Address: 0x08, Reset: 0x00, Name: XDATA

This register holds the eight most significant bits of the x-axis acceleration data. This limited resolution data register is used in power conscious applications where eight bits of data are sufficient: energy can be conserved by reading only one byte of data per axis, rather than two.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0

Y-AXIS DATA (8 MSB) REGISTER

Address: 0x09, Reset: 0x00, Name: YDATA

This register holds the eight most significant bits of the y-axis acceleration data. This limited resolution data register is used in power conscious applications where eight bits of data are sufficient: energy can be conserved by reading only one byte of data per axis, rather than two.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0

Z-AXIS DATA (8 MSB) REGISTER

Address: 0x0A, Reset: 0x00, Name: ZDATA

This register holds the eight most significant bits of the z-axis acceleration data. This limited resolution data register is used in power conscious applications where eight bits of data are sufficient: energy can be conserved by reading only one byte of data per axis, rather than two.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0