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Micropower, 3-Axis, ±200 *g* Digital Output, MEMS

Data Sheet **ADXL372**

FEATURES

- **±200 *g* measurement range**
- **200 Hz to 3200 Hz user selectable bandwidth with 4-pole antialiasing filter**
- **Selectable oversampling ratio**
- **Adjustable high-pass filter**
- **Ultralow power**
  - **Power can be derived from a coin cell battery**
  - **22 µA at 3200 Hz ODR, 2.5 V supply**
  - **Low power, wake-up mode for low *g* activity detection**
  - **1.4 µA instant on mode with adjustable threshold**
  - **<0.1 µA standby mode**
- **Built in features for system level power savings**
  - **Autonomous interrupt processing without processor intervention**
  - **Deep embedded FIFO to minimize host processor load**
- **Ultralow power event monitoring detects impacts and wakes up fast enough to capture the transient events**
- **Ability to capture and store peak acceleration values of events**
- **Adjustable, low *g* threshold activity and inactivity detection**
- **Wide supply range: 1.6 V to 3.5 V**
- **Acceleration sample synchronization via external trigger**
- **SPI digital interface and limited I²C interface format support**
- **12-bit output at 100 mg/LSB scale factor**
- **Wide temperature range: −40°C to +105°C**
- **Small, thin, 3 mm × 3.25 mm × 1.06 mm package**

APPLICATIONS

- **Impact and shock detection**
- **Asset health assessment**
- **Portable Internet of Things (IoT) edge nodes**
- **Concussion and head trauma detection**

GENERAL DESCRIPTION

The ADXL372 is an ultralow power, 3-axis, ±200 *g* MEMS accelerometer that consumes 22 µA at a 3200 Hz output data rate (ODR). The ADXL372 does not power cycle its front end to achieve its low power operation and therefore does not run the risk of aliasing the output of the sensor.

In addition to its ultralow power consumption, the ADXL372 has many features to enable impact detection while providing system level power reduction. The device includes a deep multimode output first in, first out (FIFO), several activity detection modes, and a method for capturing only the peak acceleration of over threshold events.

Two additional lower power modes with interrupt driven, wake-up features are available for monitoring motion during periods of inactivity. In wake-up mode, acceleration data can be averaged to obtain a low enough output noise to trigger on low *g* thresholds. In instant on mode, the ADXL372 consumes 1.4 µA while continuously monitoring the environment for impacts. When an impact event that exceeds the internally set threshold is detected, the device switches to normal operating mode fast enough to record the event.

High *g* applications tend to experience acceleration content over a wide range of frequencies. The ADXL372 includes a 4-pole low-pass antialiasing filter to attenuate out of band signals that are common in high *g* applications. The ADXL372 also incorporates a high-pass filter to eliminate initial and slow changing errors, such as ambient temperature drift.

The ADXL372 provides 12-bit output data at 100 mg/LSB scale factor. The user can access configuration and data registers via the serial peripheral interface (SPI) or limited I²C protocol. The ADXL372 operates over a wide supply voltage range and is available in a 3 mm × 3.25 mm × 1.06 mm package.

Multifunction pin names may be referenced by their relevant function only.

FUNCTIONAL BLOCK DIAGRAM

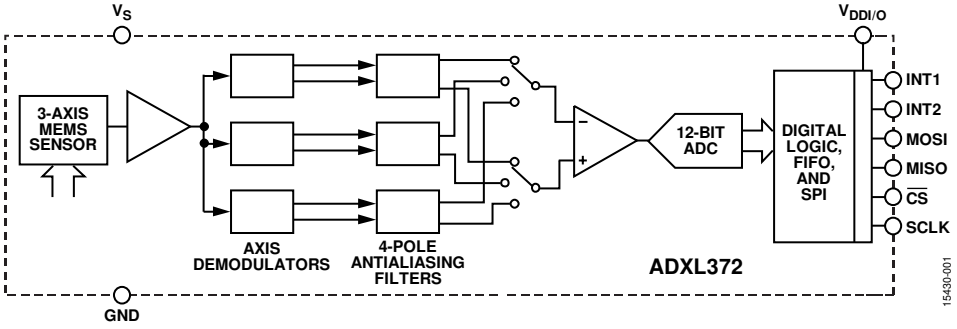

Figure 1.

Rev. 0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **Technical Support**

www.analog.com

ADXL372* PRODUCT PAGE QUICK LINKS

Last Content Update: 03/13/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- Ultralow Power, ±200 g Digital Accelerometer Breakout Board

DOCUMENTATION

Data Sheet

- ADXL372: Micropower, 3-Axis, ±200 g Digital Output, MEMS Data Sheet

User Guides

- UG-1113: Ultralow Power, ±200 g Digital Accelerometer Breakout Board

DESIGN RESOURCES

- ADXL372 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADXL372 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

3/2017—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 2.5 V, $V_{DDI/O}$ = 2.5 V, 3200 Hz ODR, 1600 Hz bandwidth, acceleration = 0 *g*, default register settings, unless otherwise noted. All minimum and maximum specifications are guaranteed. Typical specifications may not be guaranteed.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range			±200		*g*
Nonlinearity	Percentage of full scale		±0.5		%
Sensor Resonant Frequency			16		kHz
Cross Axis Sensitivity[1]			±2.5		%
OUTPUT RESOLUTION	Each axis				
All Operating Modes			12		Bits
SCALE FACTOR	Each axis				
Scale Factor Calibration Error				±10	%
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	Expressed in m*g*/LSB		100		m*g*/LSB
	Expressed in LSB/*g*		10		LSB/*g*
Scale Factor Change Due to Temperature[2]			0.1		%/°C
0 *g* OFFSET	Each axis				
0 *g* Output	X_{OUT}, Y_{OUT}, Z_{OUT}				
	At V_S = 2.5 V	−3	±1	+3	*g*
	1.6 V ≤ V_S ≤ 3.5 V	−7	±1	+7	*g*
0 *g* Offset vs. Temperature[2]					
Normal Operation	X_{OUT}, Y_{OUT}, Z_{OUT}		±50		m*g*/°C
Low Noise Mode	X_{OUT}, Y_{OUT}, Z_{OUT}		±35		m*g*/°C
NOISE PERFORMANCE					
RMS Noise	Each axis				
Normal Operation			3.5		LSB
Low Noise Mode			3		LSB
BANDWIDTH	User selectable				
ODR		400		6400	Hz
High-Pass Filter, −3 dB Corner[3]		0.24		30.48	Hz
Low-Pass (Antialiasing) Filter, −3 dB Corner[4]	4-pole low-pass filter	200		ODR/2	Hz
POWER SUPPLY					
Operating Voltage Range (V_S)		1.6	2.5	3.5	V
Input/Output Voltage Range ($V_{DDI/O}$)		1.6	2.5	V_S	V
Supply Current					
Measurement Mode	3200 Hz ODR				
Normal Operation			22		µA
Low Noise Mode			33		µA
Instant On Mode			1.4		µA
Wake-Up Mode	Varies with wake-up rate				
	At slowest wake-up rate		0.77		µA
Standby			<0.1		µA
Power Supply Rejection Ratio (PSRR)	C_S = 1.1 µF, C_{IO} = 1.1 µF, input is 100 mV sine wave on V_S				
Input Frequency					
100 Hz to 1 kHz			−20		dB
1 kHz to 250 kHz			−17		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Turn-On Time	3200 Hz ODR				
Power-Up to Standby	C_S = 1.1 µF, C_{IO} = 1.1 µF		5		ms
Measurement Mode Instruction to Valid Data	Filter settle bit = 1		370		ms
	Filter settle bit = 0		16		ms
Instant On ULP Monitoring to Full Bandwidth Data			1		ms
ENVIRONMENTAL TEMPERATURE					
Operating Temperature Range		−40		+105	°C

[1] Cross axis sensitivity is defined as coupling between any two axes.
[2] −40°C to +25°C or +25°C to +105°C.
[3] This parameter has an available corner frequency scale with the ODR setting.
[4] Bandwidth and ODR are set independent of each other.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	10000 *g*
Any Axis, Powered	10000 *g*
V_S	−0.3 V to +3.6 V
$V_{DDI/O}$	−0.3 V to +3.6 V
All Other Pins	−0.3 V to V_S
Output Short-Circuit Duration (Any Pin to Ground)	Indefinite
ESD, Human Body Model (HBM)	2000 V
Temperature Range (Storage)	−50°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3.

Package Type[1]	θ_{JA}	θ_{JC}	Unit	Device Weight
CC-16-4	150	85	°C/W	18 m*g*

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD51.

RECOMMENDED SOLDERING PROFILE

Figure 2 and Table 4 provide details about the recommended soldering profile.

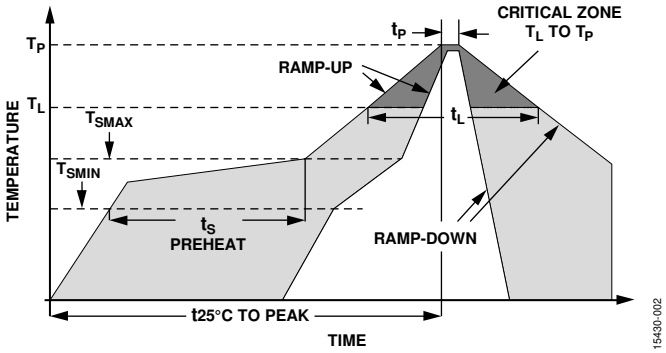

Figure 2. Recommended Soldering Profile

Table 4. Recommended Soldering Profile

	Condition	
Profile Feature	**Sn63/Pb37**	**Pb-Free**
Average Ramp Rate (T_L to T_P)	3°C/sec max	3°C/sec max
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time (T_{SMIN} to T_{SMAX}) (t_S)	60 sec to 120 sec	60 sec to 180 sec
T_{SMAX} to T_L		
Ramp-Up Rate	3°C/sec max	3°C/sec max
Time Maintained Above Liquidous (T_L)		
Liquidous Temperature (T_L)	183°C	217°C
Time (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_P)	240 + 0/−5°C	260 + 0/−5°C
Time Within 5°C of Actual Peak Temperature (t_P)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 minutes max	8 minutes max

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

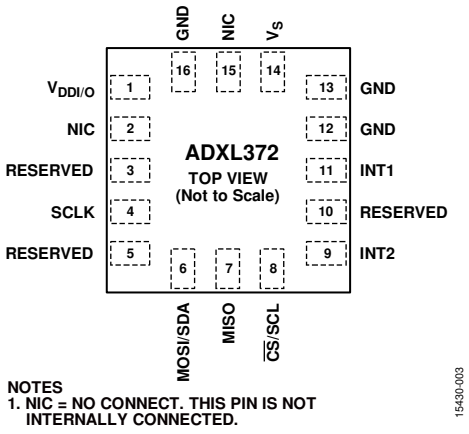

Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{DDI/O}$	Supply Voltage for Digital Input/Output.
2	NIC	No Connect. This pin is not internally connected.
3	RESERVED	Reserved. This pin may be left unconnected or connected to GND.
4	SCLK	SPI Serial Communications Clock.
5	RESERVED	Reserved. This pin may be left unconnected or connected to GND.
6	MOSI/SDA	SPI Master Output, Slave Input (MOSI). I^2C Serial Data (SDA).
7	MISO	SPI Master Input, Slave Output.
8	$\overline{CS}$/SCL	SPI Chip Select ($\overline{CS}$). I^2C Serial Communications Clock (SCL).
9	INT2	Interrupt 2 Output. This pin also serves as an input for synchronized sampling.
10	RESERVED	Reserved. This pin may be left unconnected or connected to GND.
11	INT1	Interrupt 1 Output. This pin also serves as an input for external clocking.
12	GND	Ground. This pin must be connected to ground.
13	GND	Ground. This pin must be connected to ground.
14	V_S	Supply Voltage.
15	NIC	No Connect. This pin is not internally connected.
16	GND	Ground. This pin must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

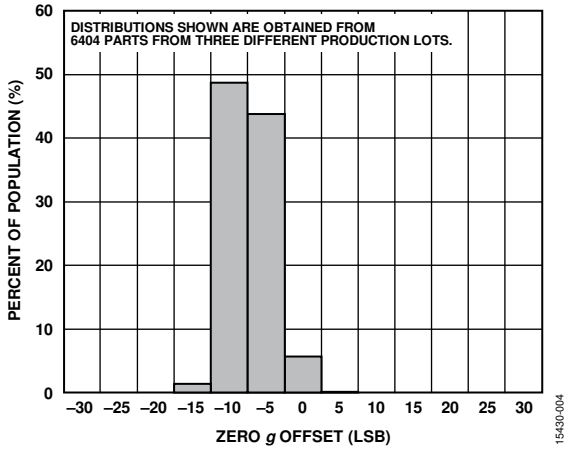

Figure 4. X-Axis Zero g Offset at 25°C, V_S = 2.5 V

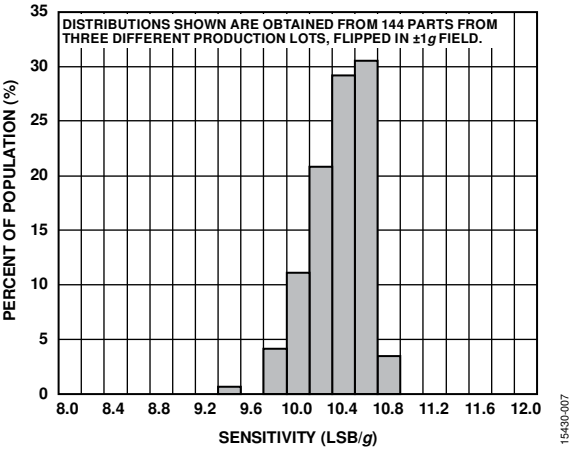

Figure 7. X-Axis Sensitivity at 25°C, V_S = 2.5 V

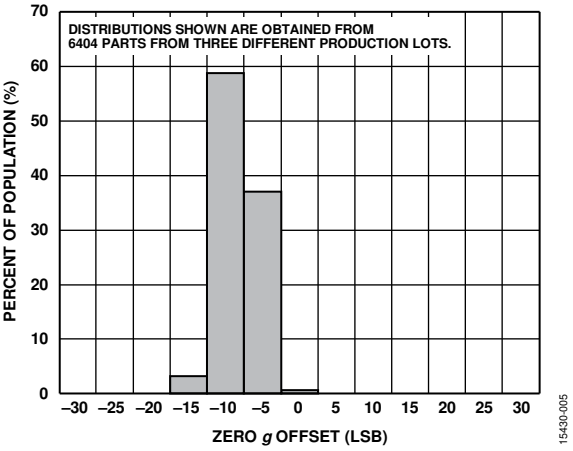

Figure 5. Y-Axis Zero g Offset at 25°C, V_S = 2.5 V

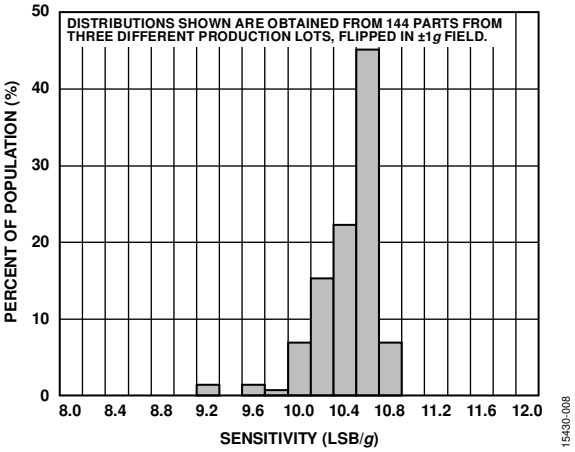

Figure 8. Y-Axis Sensitivity at 25°C, V_S = 2.5 V

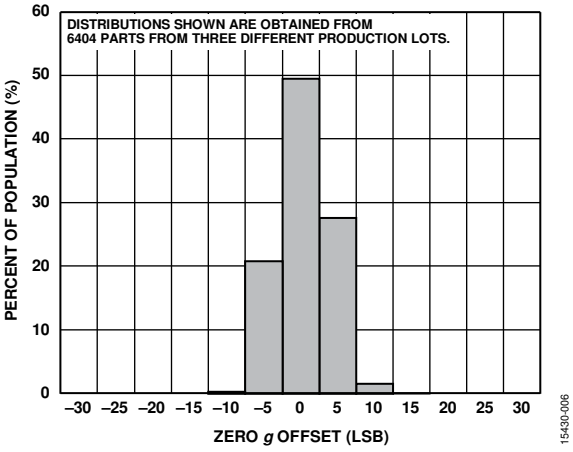

Figure 6. Z-Axis Zero g Offset at 25°C, V_S = 2.5 V

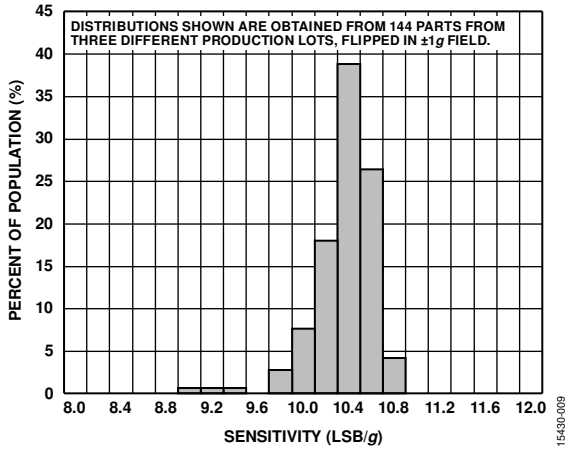

Figure 9. Z-Axis Sensitivity at 25°C, V_S = 2.5 V

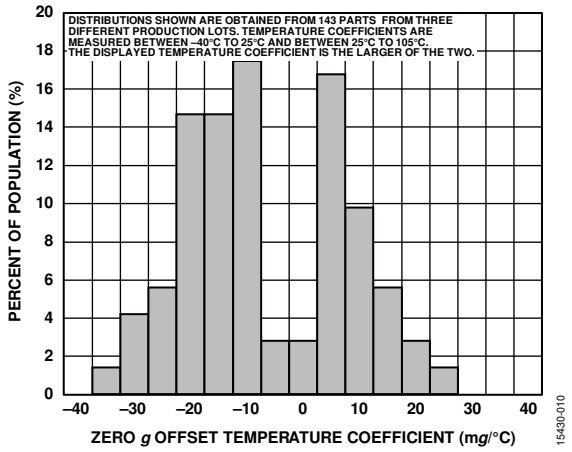

Figure 10. X-Axis Zero g Offset Temperature Coefficient, V_S = 2.5 V

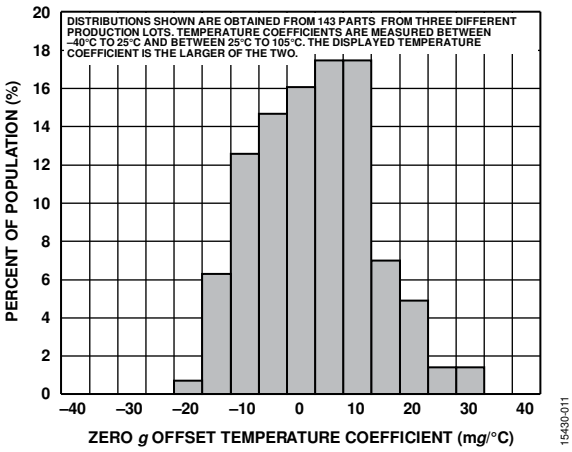

Figure 11. Y-Axis Zero g Offset Temperature Coefficient, V_S = 2.5 V

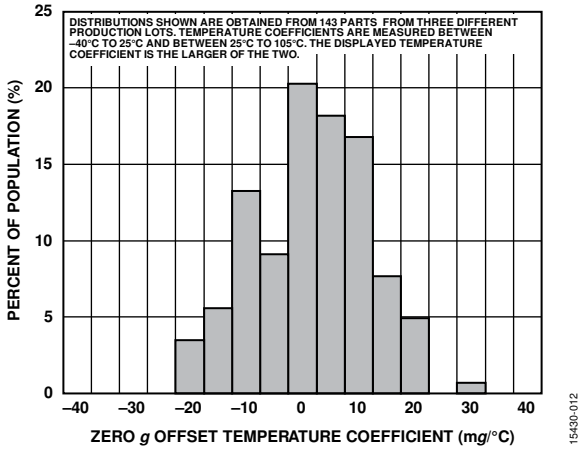

Figure 12. Z-Axis Zero g Offset Temperature Coefficient, V_S = 2.5 V

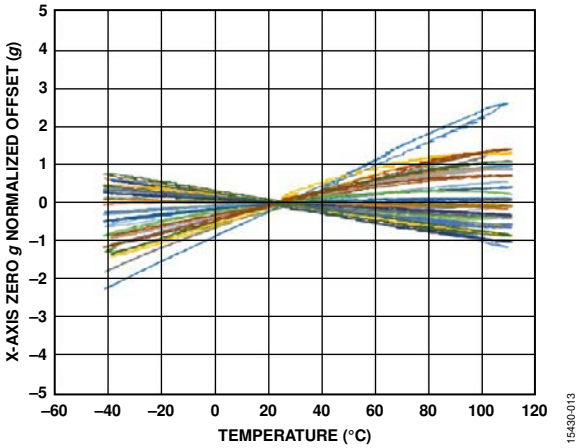

Figure 13. X-Axis Zero g Normalized Offset vs. Temperature, 36 Parts Soldered to PCB, ODR = 3200 Hz

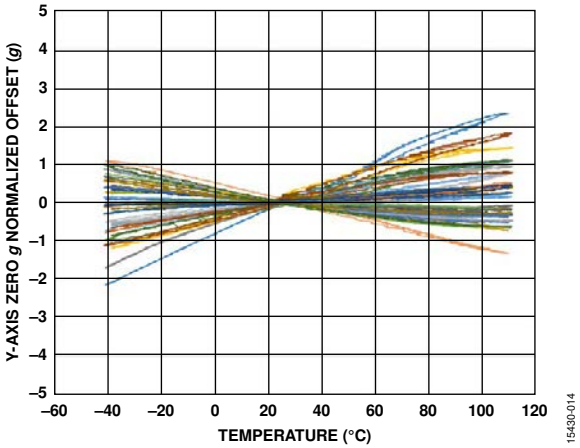

Figure 14. Y-Axis Zero g Normalized Offset vs. Temperature, 36 Parts Soldered to PCB, ODR = 3200 Hz

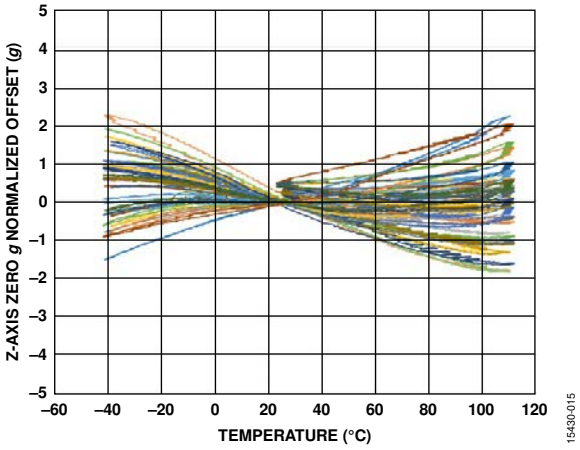

Figure 15. Z-Axis Zero g Normalized Offset vs. Temperature, 36 Parts Soldered to PCB, ODR = 3200 Hz

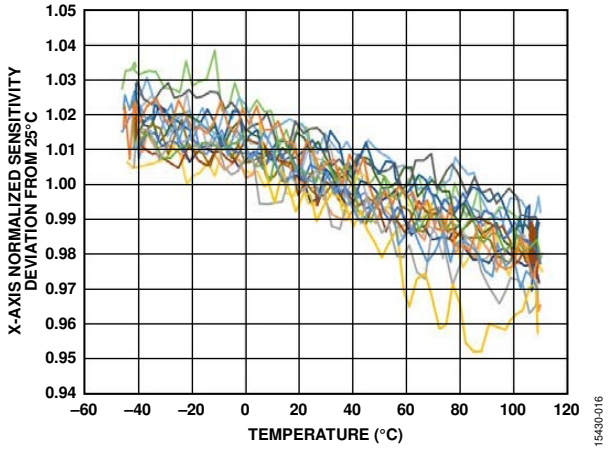

Figure 16. X-Axis Normalized Sensitivity Deviation from 25°C vs. Temperature, 18 Parts Soldered to PCB, ODR = 3200 Hz

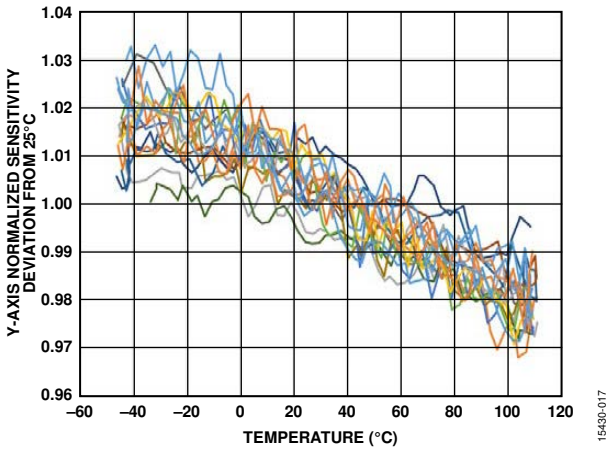

Figure 17. Y-Axis Normalized Sensitivity Deviation from 25°C vs. Temperature, 17 Parts Soldered to PCB, ODR = 3200 Hz

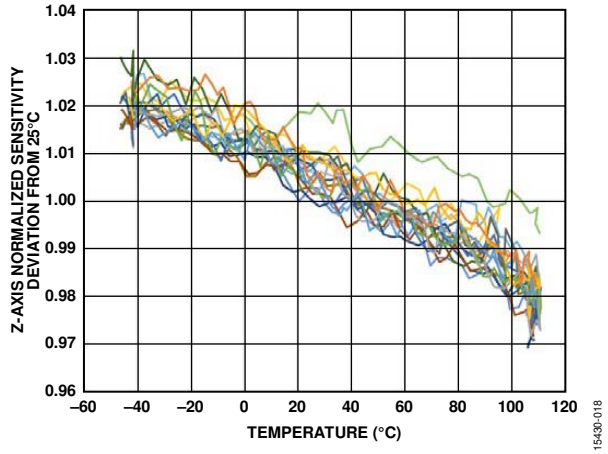

Figure 18. Z-Axis Normalized Sensitivity Deviation from 25°C vs. Temperature, 18 Parts Soldered to PCB, ODR = 3200 Hz

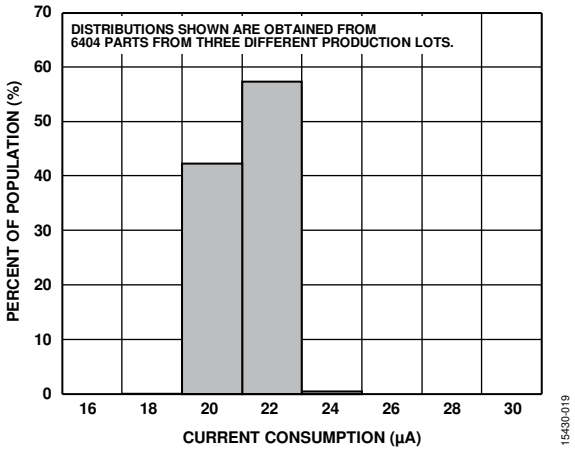

Figure 19. Current Consumption at 25°C, Normal Mode, 3200 Hz Output Data Rate, V_S = 2.5 V

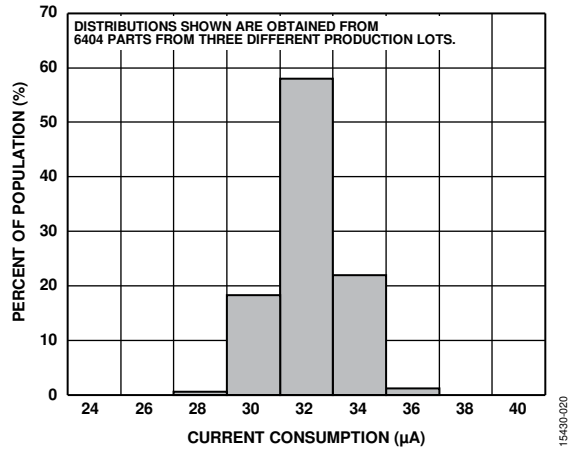

Figure 20. Current Consumption at 25°C, Low Noise Mode, 3200 Hz Output Data Rate, V_S = 2.5 V

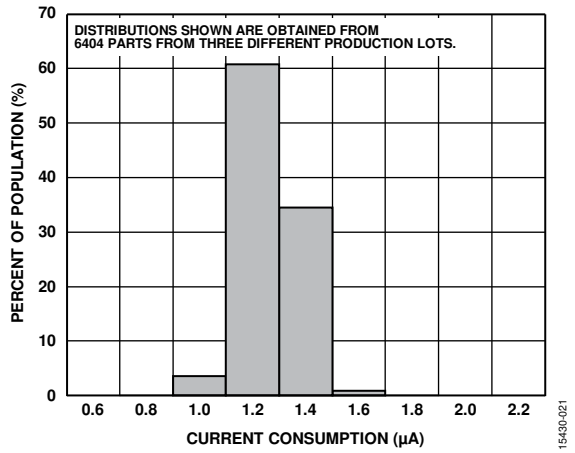

Figure 21. Current Consumption at 25°C, Instant On Mode, V_S = 2.5 V

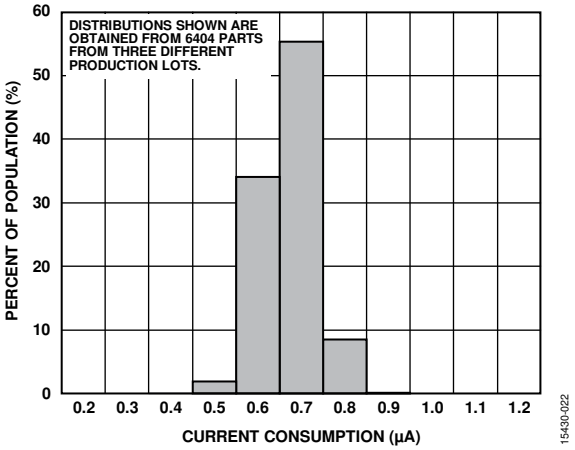

Figure 22. Current Consumption at 25°C, Wake-Up Mode, V_S = 2.5 V

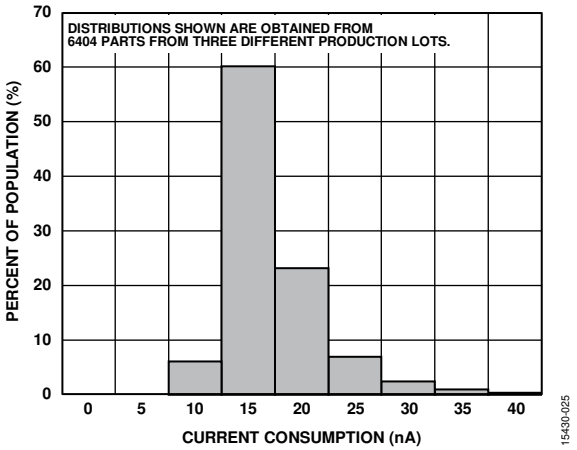

Figure 25. Current Consumption at 25°C, Standby Mode, V_S = 2.5 V

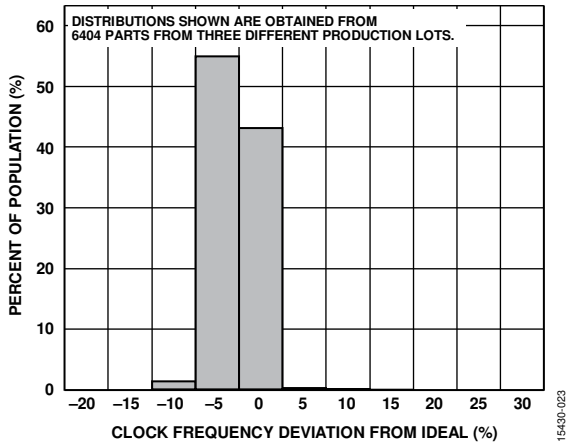

Figure 23. Clock Frequency Deviation from Ideal at 25°C, ODR = 3200 Hz, V_S = 2.5 V

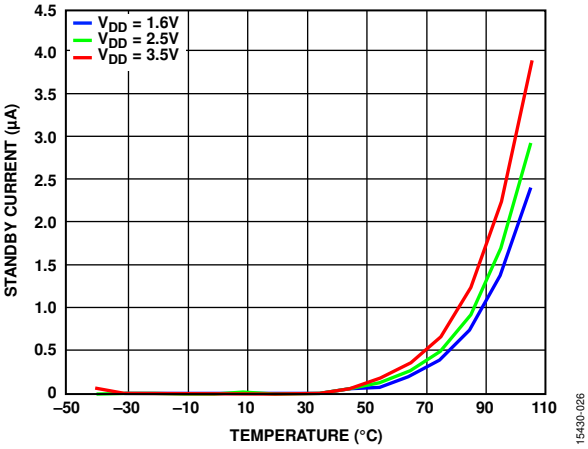

Figure 26. Standby Current vs. Temperature

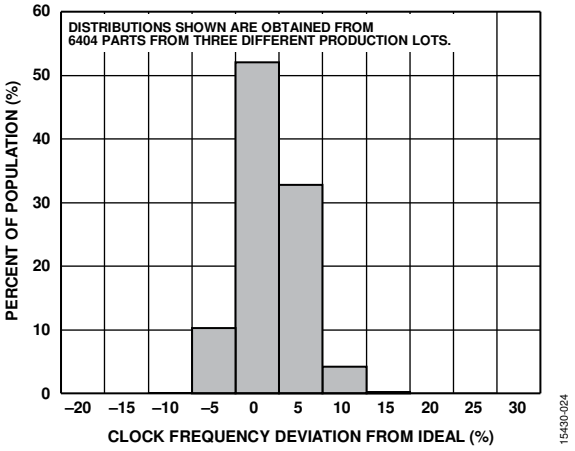

Figure 24. Clock Frequency Deviation from Ideal at 25°C, ODR = 6400Hz, V_S = 2.5 V

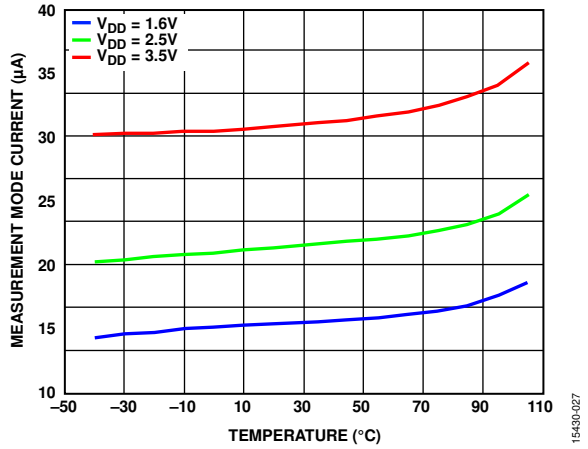

Figure 27. Measurement Mode Current vs. Temperature

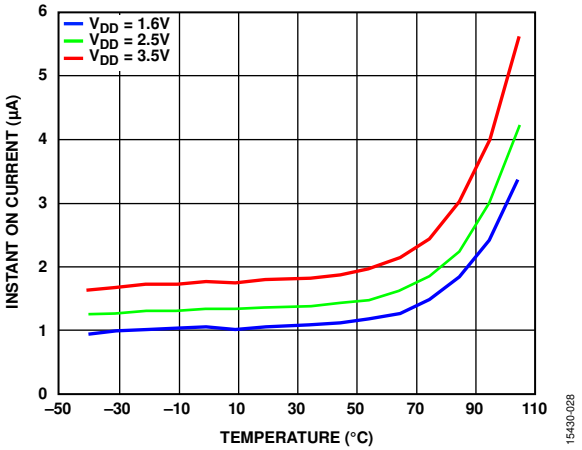

Figure 28. Instant On Current vs. Temperature

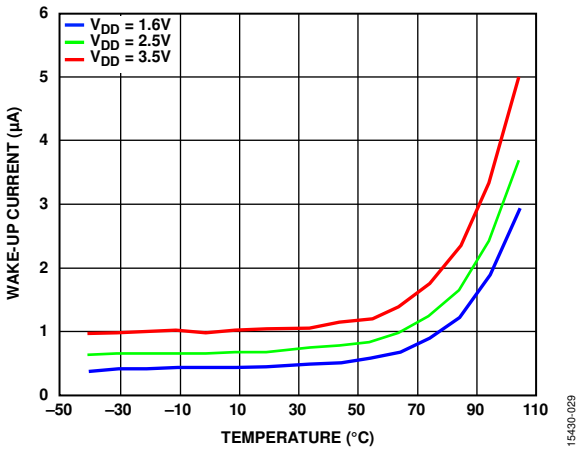

Figure 29. Wake-Up Current vs. Temperature

THEORY OF OPERATION

The ADXL372 is a complete 3-axis acceleration measurement system that operates at extremely low power levels. Acceleration is reported digitally, and the device communicates via the SPI and I²C protocols. Built in digital logic enables autonomous operation and implements functions that enhance system level power savings.

MECHANICAL DEVICE OPERATION

The moving component of the sensor is a polysilicon surface micromachined structure built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against acceleration forces.

Deflection of the structure is measured using differential capacitors that consist of independent fixed plates and plates attached to the moving mass. Acceleration deflects the structure and unbalances the differential capacitor, resulting in a sensor output whose amplitude is proportional to acceleration. Phase sensitive demodulation determines the magnitude and polarity of the acceleration.

OPERATING MODES

The ADXL372 has three operating modes: measurement mode for continuous, wide bandwidth sensing; an instant on mode for low power impact detection; and wake-up mode for limited bandwidth low *g* activity detection. Measurement can be suspended by placing the device in standby mode.

Measurement Mode

Measurement mode is the default operating mode of the ADXL372. In this mode, acceleration data is read continuously, and the accelerometer consumes 22 µA (typical) at an ODR of 3200 Hz using a 2.5 V supply. Actual current consumption is dependent on the ODR chosen. All features described in this data sheet are available when operating the ADXL372 in this mode.

Instant On Mode

Instant on mode enables extremely low power impact detection. In this mode, the accelerometer constantly monitors the environment while consuming a very low current of 1.4 µA (typical). When an event that exceeds an internal threshold is detected, the device switches into measurement mode to record the event. The target default threshold is 10 *g* to 15 *g*, but it can vary. A register option allows the threshold to be increased to a target of 30 *g* to 40 *g* if the default threshold is too low.

To save power, no new digital acceleration data is made available until the accelerometer switches into normal operation. However, all registers have normal read/write functionality.

Wake-Up Mode

Wake-up mode is ideal for simple detection of the presence or absence of motion at an extremely low power consumption. Wake-up mode is particularly useful for the implementation of a low *g* motion activated on/off switch, allowing the rest of the system to be powered down until sustained activity is detected.

In wake-up mode, the device is powered down for a duration of time equal to the wake-up timer, set by the WAKEUP_RATE bits in the TIMING register, and then turns on for a duration equal to the filter settling time (see the Filter Settling Time section). The current drawn in this mode is determined by both these parameters.

Table 6. Wake-Up Current in µA at Different Wake-Up Timer and Filter Settings

	Filter Settling Time	
Wake-Up Timer (ms)	**16 ms**	**370 ms**
52	5.8 µA	19.4 µA
104	3.6 µA	17.3 µA
208	2.3 µA	14.4 µA
512	1.4 µA	9.7 µA
2048	0.91 µA	4 µA
4096	0.83 µA	2.5 µA
8192	0.79 µA	1.7 µA
24576	0.77 µA	1.1 µA

If motion is detected, the accelerometer can respond autonomously in several ways, depending on the device configuration, such as the following:

- Switch into full bandwidth measurement mode.
- Signal an interrupt to a microcontroller.
- Wake up downstream circuitry.

While in wake-up mode, all registers and the FIFO have normal read/write functionality, and real-time data can be read from the data registers at the reduced wake-up rate. However, no new data is stored in the FIFO during wake-up mode, and there are no interrupts available in wake-up mode.

Standby

Placing the ADXL372 in standby mode suspends measurement and reduces current consumption to less than 100 nA. All interrupts are cleared, and no new interrupts are generated. The ADXL372 powers up in standby mode with all sensor functions turned off.

BANDWIDTH

Low-Pass Antialiasing Filter

High *g* events often include acceleration content over a wide range of frequencies. The analog-to-digital converter (ADC) of the ADXL372 samples the input acceleration at the user selected ODR. In the absence of antialiasing filters, input signals whose frequency is more than half the ODR alias or that fold into the measurement bandwidth can lead to inaccurate measurements. To mitigate this inaccuracy, a four-pole, low-pass filter is provided at the input of the ADC. The filter bandwidth is user selectable, and the default bandwidth is 200 Hz. The maximum bandwidth is constrained to at most half of the ODR, to ensure that the Nyquist criteria is not violated.

High-Pass Filter

The ADXL372 offers a one-pole, high-pass filter with a user selectable −3 dB frequency. Applications that do not require dc acceleration measurements can use the high-pass filter to minimize constant or slow varying offset errors including initial bias, bias drift due to temperature, and bias drift due to supply voltage.

The high-pass filter is a first-order infinite impulse response (IIR) filter. Table 7 lists the available −3 dB frequencies, which are user selectable and dependent on the output data rate. The high-pass and low-pass filters can be used simultaneously to set up a band-pass option.

Table 7. High-Pass Filter −3 dB Corner Frequencies

	ODR (Hz)				
Setting	**6400**	**3200**	**1600**	**800**	**400**
00	30.48	15.24	7.61	3.81	1.9
01	15.58	7.79	3.89	1.94	0.97
10	7.88	3.94	1.97	0.98	0.49
11	3.96	1.98	0.99	0.49	0.24

Filter Settling Time

After entering measurement mode, the first output value does not appear until after the filter settling time has passed. This time is selectable using the FILTER_SETTLE bit in the POWER_CTL register. The recommended (and default) settling time to acquire valid data when using either the high-pass filter or the low-pass activity detect filter is 370 ms. The filter settling time of 16 ms is ideal for when both the high-pass filter and low-pass activity detect filter are disabled.

Selectable ODR

The ADXL372 can report acceleration data at 400 Hz, 800 Hz, 1600 Hz, 3200 Hz, or 6400 Hz. The ODR is user selectable and the default is 400 Hz. In the event that the user selects an anti-aliasing filter bandwidth greater than half the ODR, the device defaults the bandwidth to half the ODR. Increasing or decreasing the ODR increases or decreases the current consumption accordingly, as shown in Figure 30.

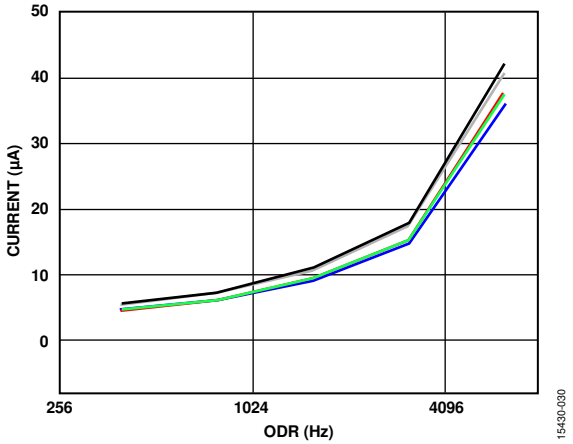

Figure 30. Measurement Mode Current vs. ODR for Five Parts

POWER/NOISE TRADE-OFF

The noise performance of the ADXL372 in normal operation, typically 3.5 LSB rms at 3200 Hz ODR and 1600 Hz bandwidth, is adequate for most applications, depending on bandwidth and the desired resolution. For cases where lower noise is needed, the ADXL372 provides a lower noise operating mode that trades reduced noise for a somewhat higher current consumption. In all cases, operating at a higher bandwidth setting increases the rms noise and operating with a lower bandwidth decreases the noise. Table 8 lists the current consumption and noise densities obtained for normal operation and the lower noise mode at a typical 2.5 V supply.

Operating the ADXL372 at a higher supply voltage also decreases noise. Table 9 lists the current consumption and noise densities obtained for normal operation and the lower noise mode at the highest recommended supply, 3.5 V.

Table 8. Noise and Current Consumption for V_S = 2.5 V

Mode	Typical RMS Noise (LSB)	Typical Current Consumption (µA)
Normal Operation[1]	3.5	22
Low Noise[1]	3	33

[1] V_S = 2.5 V, ODR = 3200 Hz, and bandwidth = 1600 Hz.

Table 9. Noise and Current Consumption for V_S = 3.5 V

Mode	Typical RMS Noise (LSB)	Typical Current Consumption (µA)
Normal Operation[1]	3	32
Low Noise[1]	2.5	44

[1] V_S = 3.5 V, ODR = 3200 Hz, and bandwidth = 1600 Hz.

POWER SAVINGS

The digital interface of the ADXL372 is implemented with system level power savings in mind. The following features enhance power savings:

- Burst reads and writes reduce the number of SPI communication cycles required to configure the device and retrieve data.
- Concurrent operation of activity and inactivity detection enables set it and forget it operation. Loop modes further reduce communications power by enabling the clearing of interrupts without processor intervention.
- The FIFO is implemented such that consecutive samples can be read continuously via a multibyte read of unlimited length; thus, one FIFO read instruction can clear the entire contents of the FIFO. The ADXL372 FIFO construction also allows the use of direct memory access (DMA) to read the FIFO contents.

AUTONOMOUS EVENT DETECTION

ACTIVITY AND INACTIVITY

The ADXL372 features built in logic that detects activity (defined as acceleration above a user set threshold) and inactivity (defined as acceleration below a user set threshold). Activity and inactivity events can be used as triggers to manage the accelerometer operating mode, trigger an interrupt to a host processor, and/or autonomously drive a motion switch.

Detection of an activity or inactivity event is indicated in the STATUS2 register and can be configured to generate an interrupt. In addition, the activity status of the device, that is, whether it is moving or stationary, is indicated by the AWAKE bit, described in the Using the AWAKE Bit section.

Activity and inactivity detection can be used when the accelerometer is in either measurement mode or wake-up mode. However, the activity and inactivity interrupts are not available in wake-up mode because the device is inherently looking for activity in this mode, and any changes to activity or inactivity detection features must be made while the device is in standby mode.

Low-Pass Activity Detect Filter

The ADXL372 combines high *g* impact detection and low *g* movement detection in one device. For low *g* detection, an internal low-pass filter with a −3 dB corner of approximately 10 Hz averages data to reduce the rms noise, allowing accurate detection of activity or inactivity thresholds as low as 500 mg. For high *g* impact detection, the low-pass activity detect filter can be turned off through a register setting. When using both the low-pass activity detect filter and the high-pass filter, the user must select a high-pass filter corner that does not exceed 10 Hz; otherwise, activity detection data is severely attenuated.

Activity Detection

An activity event is detected when acceleration in at least one enabled axis remains above a specified threshold for a specified time. Enabled axes, thresholds, and time are user selected. Each axis has its own activity threshold, but the activity timer is shared among all three axes. When multiple axes are selected, an over-threshold event on any one enabled axis triggers the activity detection.

Referenced and Absolute Configurations

Activity detection can be configured as referenced or absolute mode for all axes through the ACT_REF bit in the THRESH_ACT_X_L register.

When using absolute activity detection, acceleration samples are compared directly to a user set threshold to determine whether motion is present. For example, if a threshold of 0.5 *g* is set and the acceleration on the z-axis is 1 *g* longer than the user defined activity time, the activity status asserts.

In many applications, it is advantageous for activity detection to be based not on an absolute threshold, but on a deviation from a reference point or orientation. The referenced activity detection is particularly useful because it removes the effect on activity detection of the static 1 *g* imposed by gravity as well as any static offset errors, which can be up to several *g*. In absolute activity detection, when the threshold is set to less than 1 *g*, activity is immediately detected in this case.

In the referenced configuration, activity is detected when acceleration samples are above an internally defined reference by a user defined amount for the user defined amount of time, as described by

$$Abs(Acceleration - Reference) > Threshold$$

where *Abs* is the absolute value.

Consequently, activity is detected only when the acceleration has deviated sufficiently from the initial orientation. The default setting for the accelerometer is in absolute mode. After it is placed in referenced mode through the appropriate register setting, the reference for activity detection is calculated as soon as full bandwidth measurement mode is turned on. To reset the reference, it is necessary to put the device back into absolute mode and then back to referenced mode. The new reference is set as soon as the device enters full bandwidth measurement mode again. If using both activity and inactivity detection in referenced mode, both must be set back to absolute mode before the reference can be reset.

Activity Timer

Ideally, the intent of activity detection is to wake up a system only when motion is intentional, ignoring noise or small, unintentional movements. In addition to being sensitive to low *g* events, the ADXL372 activity detection algorithm is robust in filtering out undesired triggers.

The ADXL372 activity detection functionality includes a timer to filter out unwanted motion and ensure that only sustained motion is recognized as activity. The timer period depends on the ODR selected. At 3200 Hz and below, it is ~6.6 ms; at 6400 Hz, it is ~3.3 ms. For activity detection to trigger, above threshold activity must be sustained for a time equal to the number of activity timer periods specified in the activity time register. For example, a setting of 10 in this register means that above threshold activity must be sustained for 66 ms at 3200 Hz ODR. A register value of zero results in single sample activity detection. The maximum allowable activity time is ~1.68 sec (or 841.5 ms at 6400 Hz ODR). Note that the activity timer is operational in measurement mode only.

Activity Detection in Wake-Up Mode

If activity detection is enabled while the device is in wake-up mode, the device uses single sample activity detection, no matter the activity time register setting. If activity is detected, the device automatically returns to full bandwidth measurement mode. However, the activity interrupt is not generated unless the activity time setting is zero. If it is not zero, after entering measurement mode, the interrupt is not generated until the device sees sustained activity for the amount of time given in the activity time register. The awake interrupt automatically goes high upon entering measurement mode if the device is in default mode or autosleep mode. If it is in linked or loop mode (but not autosleep), it is linked to the activity interrupt, which behaves as previously mentioned.

After the device automatically enters measurement mode due to activity detection, if autosleep is not on, it must be placed manually back into wake-up mode.

Inactivity Detection

An inactivity event is detected when acceleration in all enabled axes remains below a specified threshold for a specified time. Enabled axes, threshold, and time are user selected. Each axis has its own inactivity threshold, but the inactivity timer is shared among all three axes. When multiple axes are selected, all enabled axes must stay under the threshold for the required amount of time to trigger inactivity detection.

Referenced and Absolute Configurations

Inactivity detection is also configurable as referenced or absolute through the INACT_REF bit in the THRESH_INACT_X_L register. When using absolute inactivity detection, acceleration samples are compared directly to a user set threshold for the user set time to determine the absence of motion. Inactivity is detected when enough consecutive samples are all below the threshold.

When using referenced inactivity detection, inactivity is detected when acceleration samples are within a user specified amount from an internally defined reference for a user defined amount of time.

$$Abs(Acceleration - Reference) < Threshold$$

Referenced inactivity, like referenced activity, is particularly useful for eliminating the effects of the static acceleration due to gravity, as well as other static offsets. With absolute inactivity, if the inactivity threshold is set lower than 1 *g*, a device resting motionless may never detect inactivity. With referenced inactivity, the same device under the same configuration detects inactivity. The default setting for the accelerometer is in absolute mode. After it is placed in referenced mode through the appropriate register setting, the reference for inactivity detection is calculated as soon as full bandwidth measurement mode is turned on. To reset the reference, it is necessary to put the device back into absolute mode and then back to referenced mode. The new reference is set as soon as the device enters full bandwidth measurement mode again. If using both inactivity and activity detection in referenced mode, both must be set back to absolute mode before the reference can be reset.

Inactivity Timer

The ADXL372 inactivity detect functionality includes a timer to allow detection of sustained inactivity. The timer period depends on the ODR selected. At 3200 Hz and below, it is ~26 ms; at 6400 Hz, it is ~13 ms. For inactivity detection to trigger, below threshold inactivity must be sustained for a time equal to the number of inactivity timer periods specified in the inactivity time registers. For example, a setting of 10 in these registers means that below threshold inactivity must be sustained for 260 ms at 3200 Hz ODR. A value of zero in these registers results in single sample, inactivity detection. The maximum allowable inactivity time is ~28.4 minutes at 3200 Hz ODR (or ~14.2 minutes at 6400 Hz ODR).

Linking Activity and Inactivity Detection

When in measurement mode or wake-up mode, the activity and inactivity detection functions can be used concurrently and processed manually by a host processor, or they can be configured to interact in several other ways, such as those that follow.

Default Mode

In default mode, activity and inactivity detection are both available simultaneously, and all interrupts must be serviced by a host processor; that is, a processor must read each interrupt before it is cleared and can be used again. Refer to the Interrupts section for information on clearing interrupts.

The flowchart in Figure 31 illustrates default mode operation.

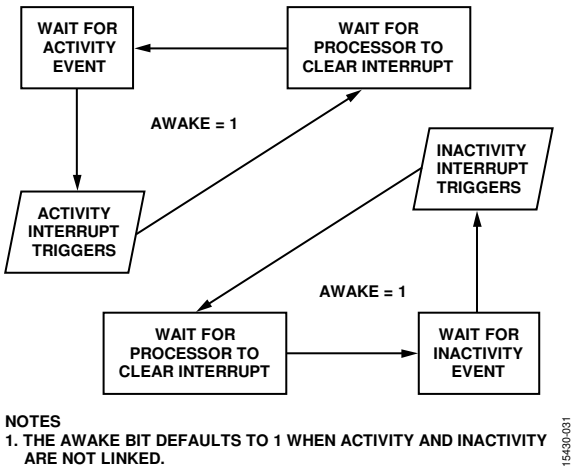

Figure 31. Flowchart Illustrating Activity and Inactivity Operation in Default Mode

Linked Mode

In linked mode, activity and inactivity detection are linked to each other such that only one of the functions is enabled at any given time. As soon as activity is detected, the device is assumed to be moving (or awake) and stops looking for activity; rather, inactivity is expected as the next event. Therefore, only inactivity detection operates.

Similarly, when inactivity is detected, the device is assumed to be stationary (or asleep). Thus, activity is expected as the next event; therefore, only activity detection operates.

In linked mode, each interrupt must be serviced by a host processor before the next interrupt is enabled.

The flowchart in Figure 32 illustrates linked mode operation.

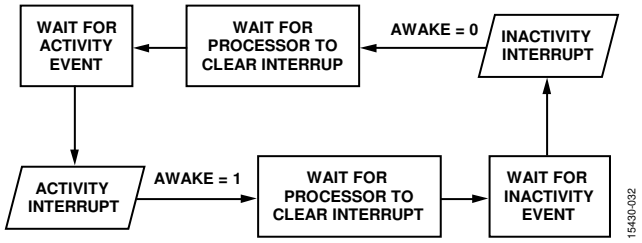

Figure 32. Flowchart Illustrating Activity and Inactivity Operation in Linked Mode

Loop Mode

In loop mode, motion detection operates as described in the Linked Mode section, but interrupts do not need to be serviced by a host processor. This configuration simplifies the implementation of commonly used motion detection and enhances power savings by reducing the amount of power used in bus communication.

The flowchart in Figure 33 illustrates loop mode operation.

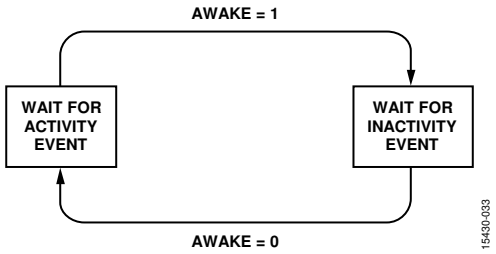

Figure 33. Flowchart Illustrating Activity and Inactivity Operation in Loop Mode

Autosleep

If autosleep is selected, after the device is placed in wake-up mode (see the Wake-Up Mode section), it automatically sets to loop mode and begins looking for activity. When activity is detected, the device automatically enters measurement mode and immediately begins looking for inactivity. When inactivity is detected, the device automatically re-enters wake-up mode. Note that the device must be manually placed in wake-up mode before autosleep can begin functioning. It does not automatically enter wake-up mode if the device is started up manually in measurement mode.

Using the AWAKE Bit

The AWAKE bit is a status bit that indicates whether the ADXL372 is awake or asleep. In default mode or autosleep mode, the AWAKE bit is high whenever the device is in measurement mode. In linked or loop mode, the AWAKE bit is high whenever the device experiences an activity condition, and it is low when the device experiences an inactivity condition.

The awake signal can be mapped to the INT1 or the INT2 pin allowing the pin to serve as a status output to connect or disconnect power to downstream circuitry based on the awake status of the accelerometer. Used in conjunction with loop mode, this configuration implements a simple, autonomous motion activated switch.

If the turn-on time of downstream circuitry can be tolerated, this motion switch configuration can save significant system level power by eliminating the standby current consumption of the remainder of the application circuit. This standby current can often exceed the full operating current of the ADXL372.

MOTION WARNING

In addition to the activity threshold previously described, the ADXL372 offers a secondary threshold. This second threshold, the motion warning threshold, can be set independently of the activity threshold. It does not have any functionality related to autosleep, linked, or loop mode, or the device awake status. The purpose of the motion warning functionality is to issue a notification to the system, via the status bit and/or interrupt, that the observed acceleration has exceeded the second threshold. It is controlled by the THRESH_ACT2_x_x registers, and by the ACTIVITY2 interrupt, which is sent only to the INT2 pin. Each axis has its own motion warning threshold. However, the motion warning activity interrupt does not have an activity timer. It is only used for single sample, activity detection. The motion warning threshold also shares the same referenced vs. absolute configuration as the primary activity detection.

IMPACT DETECTION FEATURES

Impact detection applications often require high *g* and high bandwidth acceleration measurements, and the ADXL372 is designed with these applications in mind. Several features are included that target impact detection and aim to simplify the system design.

WIDE BANDWIDTH

An impact is a transient event that produces an acceleration pulse with frequency content over a wide range. A sufficiently wide bandwidth is needed to capture the impact event because lowering bandwidth has the effect of reducing the magnitude of the recorded signal, resulting in measurement inaccuracy.

The ADXL372 can operate with bandwidths of up to 3200 Hz at extremely low power levels. A steep filter roll-off is also useful for effective suppression of out of band content, and the ADXL372 incorporates a four-pole, low-pass antialiasing filter for this purpose.

INSTANT ON IMPACT DETECTION

The ADXL372 instant on mode is an ultralow power mode that continuously monitors the environment for impact events that exceed a built in threshold. When an impact is detected, the device switches into full measurement mode and captures the impact profile.

No digital data is available in this mode of operation. The user can configure the device to detect an impact between a threshold level of either 10 *g* to 15 *g* or 30 *g* to 40 *g* by using the INSTANT_ON_ THRESH bit in the POWER_CTL register. When an impact beyond the selected threshold is detected, the ADXL372 switches to full bandwidth measurement mode and begins outputting digital data.

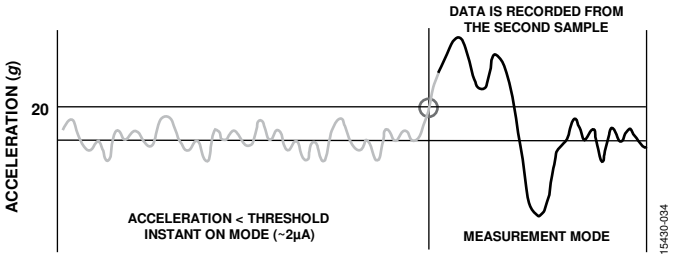

Figure 34. Instant On Mode Using Default Threshold

After the accelerometer is in full bandwidth measurement mode, it must be set back into instant on mode manually by first writing the device into full bandwidth measurement mode (or standby mode), and then back to instant on mode. It cannot return to instant on mode automatically.

CAPTURING IMPACT EVENTS

In certain applications, a single (3-axis) acceleration sample at the peak of an impact event contains sufficient information about the event, and the full acceleration history is not required. For these applications, the ADXL372 provides the capability to store only the peak acceleration of each over threshold event. The x, y, and z acceleration samples at the peak of the event can be stored in the FIFO. Applications that do not require the full event profile can greatly increase the time between FIFO reads by storing only peak acceleration information. A peak is defined as the x, y, and z acceleration sample that has the highest magnitude (root sum squared) of all other values within a particular over threshold event. In addition to recording the peak of each over threshold impact event in the FIFO, the ADXL372 can also keep track of the absolute highest peak recorded in separate registers.

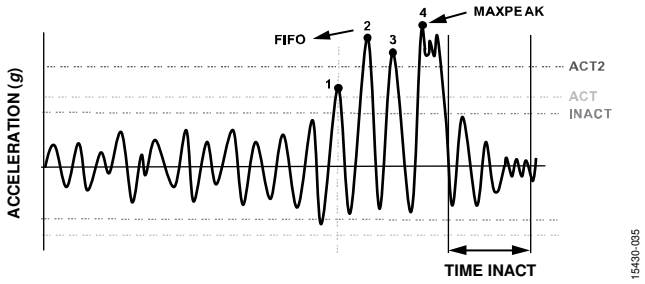

Figure 35. Capturing Impact Events

Enable peak detection by doing the following:

- Put the FIFO in peak detect and stream mode (b0011101x to Register 0x3A).
- Set the desired activity threshold and time settings (Register 0x23 to Register 0x29).
- Set the desired inactivity threshold and time settings (Register 0x2A to Register 0x31).
- Set the activity mode to linked or loop mode (Register 0x3E).

As soon as the activity interrupt is triggered, the device records the x, y, and z values of the peak acceleration event that occurs between the activity interrupt trigger and the next inactivity interrupt trigger, as shown in Figure 35 in the FIFO. It continues to do this for each period of activity between the triggering of the activity interrupt and consequent triggering of the inactivity interrupt. The process does work in linked mode, but the user must be clear each interrupt before the device looks for the next activity or inactivity interrupt. For as long as peak detect mode is selected, the device also stores the highest overall peak recorded in the MAXPEAK_x_x registers. When these values are read out of the registers, the register data is cleared, and the device begins looking for the new highest peak.

FIFO

The ADXL372 includes a deep, 512 sample FIFO buffer.

BENEFITS OF THE FIFO

The FIFO buffer is an important feature in ultralow power applications in two ways: system level power savings and data recording/event context.

System Level Power Savings

Appropriate use of the FIFO enables system level power savings by enabling the host processor to sleep for extended periods while the accelerometer autonomously collects data. Alternatively, using the FIFO to collect data can unburden the host while it tends to other tasks.

Data Recording/Event Context

The FIFO can be used in a triggered mode to record all data leading up to an activity detection event, thereby providing context for the event. In the case of a system that identifies impact events, for example, the accelerometer can keep the entire system off while it stores acceleration data in its FIFO and looks for an activity event. When the impact event occurs, data collected prior to the event is frozen in the FIFO. The accelerometer can now wake the rest of the system and transfer this data to the host processor, thereby providing context for the impact event.

Generally, the more context available, the more intelligent decisions a system can achieve, making a deep FIFO especially useful. For example, the ADXL372 FIFO can store up to 512 1-axis samples at 400 Hz ODR, providing a 1.28 sec window, or 170 3-axis samples at 3200 Hz to provide a 50 ms window, which is a typical duration for impact events.

USING THE FIFO

The FIFO is a 512 sample memory buffer that can save power, unburden the host processor, and autonomously record data.

FIFO operation is configured via Register 0x39 and Register 0x3A. The 512 FIFO samples can be allotted in several ways, such as the following:

- 170 sample sets of concurrent 3-axis data
- 256 sample sets of concurrent 2-axis data (user selectable)
- 512 sample sets of single-axis data
- 170 sets of impact event peak (x, y, z)

All FIFO modes must be configured while in standby mode. When reading data from multiple axes from the FIFO, to ensure that data is not overwritten and stored out of order, at least one sample set must be left in the FIFO after every read (therefore, a set of 3-axis data must have 169 samples at most).

The FIFO operates in one of the following four modes: FIFO disabled, oldest saved mode (first N), stream mode (last N), and triggered mode.

FIFO Disabled

When the FIFO is disabled, no new data is stored in it, and any data already in it is cleared.

The FIFO is disabled by setting the FIFO_MODE bits in the FIFO_CTL register (Register 0x3A) to 0b00.

Oldest Saved Mode (First N)

In oldest saved mode, the FIFO accumulates data until it is full and then stops. After reading the data, the FIFO must be disabled and re-enabled to save a new set of data. One possible use case for this mode is to enable it right after entering instant on mode. After a shock is detected, the data immediately stores in the FIFO to be read whenever convenient.

The FIFO is placed into oldest saved mode by setting the FIFO_MODE bits in the FIFO_CTL register (Register 0x3A) to 0b11.

Stream Mode (Last N)

In stream mode, the FIFO always contains the most recent data. The oldest sample is discarded when space is needed to make room for a newer sample.

Stream mode is useful for unburdening a host processor. The processor can tend to other tasks while data is being collected in the FIFO. When the FIFO fills to a certain number of samples (specified by the FIFO_SAMPLES register along with Bit 0 in the FIFO_CTL register), it triggers a watermark interrupt (if this interrupt is enabled). At this point, the host processor can read the contents of the entire FIFO and then return to its other tasks as the FIFO fills again.

The FIFO is placed into stream mode by setting the FIFO_MODE bits in the FIFO_CTL register (Register 0x3A) to 0b01.

Triggered Mode

In triggered mode, the FIFO operates as in stream mode until an activity detection event, after which it saves the samples surrounding that event. The operation is similar to a one-time run trigger on an oscilloscope. The number of samples to be saved after the activity event is specified in FIFO_SAMPLES (Register 0x39[7:0], along with Bit 0 in the FIFO_CTL register, Register 0x3A). For example if the FIFO_SAMPLE is set to 12, there are 500 samples before the trigger and 12 after the trigger. The trigger can be reset by clearing the activity interrupt and reading all 512 locations of the FIFO. If this is not complete, future FIFO data reads may contain invalid data. Place the FIFO into triggered mode by setting the FIFO_MODE bits in the FIFO_CTL register (Register 0x3A) to 0b10.

RETRIEVING DATA FROM FIFO

Access FIFO data by reading the FIFO_DATA register. A multibyte read to this register does not autoincrement the address, and instead continues to pop data from the FIFO. Data is left justified and formatted as shown in Table 10.

When reading data, the most significant byte (Bits[B15:B8]) is read first, followed by the least significant byte (Bits[B7:B0]). Bits[B15:B4] represent the 12-bit, twos complement acceleration data. Bit 0 serves as a series start indicator: only the first data byte of a series contains a 1 in this bit, and the remaining items contain a 0.

Table 10. FIFO Buffer Data Format

B15 (MSB)	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Data							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Data				Reserved			Series start indicator

INTERRUPTS

Several of the built in functions of the ADXL372 can trigger interrupts to alert the host processor of certain status conditions. The functionality of these interrupts is described in this section.

INTERRUPT PINS

Interrupts can be mapped to either (or both) of two designated output pins, INT1 and INT2, by setting the appropriate bits in the INT1_MAP register and INT2_MAP register, respectively. All functions can be used simultaneously. If multiple interrupts are mapped to one pin, the OR combination of the interrupts determines the status of the pin.

If no functions are mapped to an interrupt pin, that pin is automatically configured to a high impedance (high-Z) state. The pins are also placed in the high-Z state upon a reset.

When a certain status condition is detected, the pin that condition is mapped to is activated. The configuration of the pin is active high by default so when it is activated, the pin goes high. However, this configuration can be switched to active low by setting the INTx_LOW bit in the appropriate INTx_MAP register.

The INTx pins can connect to the interrupt input of a host processor where interrupts are responded to with an interrupt routine. Because multiple functions can be mapped to the same pin, the STATUS register can determine which condition caused the interrupt to trigger.

Interrupts are cleared in several of the following ways:

- Reading the STATUS2 register clears ACTIVITY and INACT interrupts. However, if activity detection is operating in default mode, and the activity or inactivity timers are set to 0, the only way to clear the activity or inactivity bits, respectively, is to set the device into standby mode and restart full bandwidth measurement mode.
- Setting the device into standby mode and back into full bandwidth measurement mode clears the ACTIVITY2 interrupt.
- Reading from the data registers clears the DATA_RDY interrupt.
- Reading enough data from the FIFO buffer so that interrupt conditions are no longer met, and then reading the STATUS register (Register 0x04) clears the FIFO_RDY, FIFO_FULL, and FIFO_OVR interrupts.

Both interrupt pins are push-pull low impedance pins with an output impedance of about 500 Ω (typical) and digital output specifications as shown in Table 11. Both have bus keepers that hold them to a valid logic state when they are in a high impedance mode.

To prevent interrupts from being falsely triggered during configuration, disable interrupts while their settings, such as thresholds, timings, or other values, are configured.

Alternate Functions

The INT1 and INT2 pins can be configured for use as input pins instead of for signaling interrupts. INT1 is used as an external clock input when the EXT_CLK bit in the TIMING register is set. INT2 is used as the trigger input for synchronized sampling when the EXT_SYNC bit in the TIMING register is set. One or both of these alternate functions can be used concurrently; however, if an interrupt pin is used for its alternate function, it cannot simultaneously be used to signal interrupts.

TYPES OF INTERRUPTS

Activity and Inactivity Interrupts

The ACTIVITY bit and INACT bit are set when activity and inactivity are detected, respectively. Detection procedures and criteria are described in the Autonomous Event Detection section.

Data Ready Interrupt

The DATA_RDY bit is set when new valid data is available, and it is cleared when no new data is available.

The DATA_RDY bit does not set while any of the data registers are being read. If DATA_RDY = 0 prior to a register read and new data becomes available during the register read, DATA_RDY remains 0 until the read is complete and only then sets to 1.

If DATA_RDY = 1 prior to a register read, it is cleared at the start of the register read.

If DATA_RDY = 1 prior to a register read and new data becomes available during the register read, DATA_RDY is cleared to 0 at the start of the register read and remains 0 throughout the read. When the read is complete, DATA_RDY is set to 1.

FIFO Interrupts

FIFO Watermark

The FIFO_FULL bit is set when the number of samples stored in the FIFO is equal to or exceeds the number specified in FIFO_SAMPLES (Register 0x39 together with Bit 0 in the FIFO_CTL register). The FIFO_FULL bit is cleared automatically when enough samples are read from the FIFO, such that the number of samples remaining is lower than that specified.

If the number of FIFO samples is set to 0, the watermark interrupt is set. To avoid unexpectedly triggering this interrupt, the default value of the FIFO_SAMPLES register is 0x80.

FIFO Ready

The FIFO_RDY bit is set when there is at least one valid sample available in the FIFO output buffer. This bit is cleared when no valid data is available in the FIFO. In FIFO triggered mode, it is only set after the activity interrupt is detected, and the data surrounding the event is saved in the FIFO.

Overrun

The FIFO_OVR bit is set when the FIFO has overrun or overflowed, such that new data replaces unread data, which may indicate a full FIFO that has not yet been emptied or a clocking error caused by a slow SPI transaction. If the FIFO is configured to oldest saved mode, an overrun event indicates that there is insufficient space available for a new sample.

The FIFO_OVR bit is cleared when both the contents of the FIFO and the STATUS register are read. It is also cleared when the FIFO is disabled.

Table 11. Interrupt Pin Digital Output

Parameter	Test Conditions	Limit[1]		Unit
		Min	Max	
Digital Output				
Low Level Output Voltage (V_{OL})	I_{OL} = 500 µA		0.2 × $V_{DDI/O}$	V
High Level Output Voltage (V_{OH})	I_{OH} = −300 µA	0.8 × $V_{DDI/O}$		V
Low Level Output Current (I_{OL})	V_{OL} = $V_{OL, MAX}$	500		µA
High Level Output Current (I_{OH})	V_{OH} = $V_{OH, MIN}$		−300	µA
Pin Capacitance	f_{IN} = 1 MHz, V_{IN} = 2.0 V		8	pF
Rise/Fall Time				
Rise Time (t_R)[2]	C_{LOAD} = 150 pF		210	ns
Fall Time (t_F)[3]	C_{LOAD} = 150 pF		150	ns

[1] Limits based on characterization results, not production tested.
[2] Rise time is measured as the transition time from $V_{OL, MAX}$ to $V_{OH, MIN}$ of the interrupt pin.
[3] Fall time is measured as the transition time from $V_{OH, MIN}$ to $V_{OL, MAX}$ of the interrupt pin.

ADDITIONAL FEATURES

USING AN EXTERNAL CLOCK

When operating at 3200 Hz ODR or lower, the ADXL372 has a built in 307.2 kHz (typical) clock that, by default, serves as the time base for internal operations. At 6400 Hz ODR, this clock speed increases to 614.4 kHz (typical). If desired, an external clock can be provided instead, for either improved clock frequency accuracy or for control of the output data rate. To use an external clock, set the EXT_CLK bit (Bit 1) in the TIMING register (Register 0x3D) and apply a clock to the INT1 pin.

The external clock can operate at the nominal 307.2 kHz or slower (when using ODR ≤ 3200 Hz), or 614.4 kHz or slower (when using ODR = 6400 Hz) to allow the user to achieve any desired output data rate. Lower external clock rates must be used with caution because it may result in aliasing of high frequency signals that may be present in certain applications.

ODR and bandwidth scale proportionally with the clock. The ADXL372 provides a discrete number of options for ODR. ODRs other than those provided are achieved by selecting an appropriate clock frequency. For example, to achieve a 2560 Hz ODR, use the 3200 Hz setting with a clock frequency that is 80% of nominal, or 245.76 kHz. Bandwidth also scales by the same ratio, so if a 400 Hz bandwidth is selected, the resulting bandwidth is 320 Hz.

SYNCHRONIZED DATA SAMPLING

For applications that require a precisely timed acceleration measurement, the ADXL372 features an option to synchronize acceleration sampling to an external trigger. The EXT_SYNC bit in the TIMING register enables this feature. When the EXT_SYNC bit is set to 1, the INT2 pin automatically reconfigures for use as the sync trigger input.

When external triggering is enabled, it is up to the system designer to ensure that the sampling frequency meets system requirements. Sampling too infrequently causes aliasing. Noise can be lowered by oversampling; however, sampling at too high a frequency may not allow enough time for the accelerometer to process the acceleration data and convert it to valid digital output data.

When the Nyquist criterion is met, signal integrity is maintained. An internal antialiasing filter is available in the ADXL372 and can assist the system designer in maintaining signal integrity. To prevent aliasing, set the filter bandwidth to a frequency no greater than half the sampling rate. For example, when sampling at 1600 Hz, set the filter bandwidth to no higher than 800 Hz.

Because of internal timing requirements, the maximum allowable external trigger frequencies are as follows:

- 1-axis data = 3100 Hz
- 2-axis data = 2700 Hz
- 3-axis data = 2200 Hz

These values are doubled when an ODR rate of 6400 Hz is selected. Additionally, the trigger signal applied to the INT2 pin must meet the following criteria:

- The trigger signal must be active high.
- The pulse width of the trigger signal must be at least 53 µs.
- The minimum sampling frequency is set only by system requirements. Samples need not be polled at any minimum rate; however, if samples are polled at a rate lower than the bandwidth set by the antialiasing filter, aliasing may occur.

The EXT_SYNC is an active high signal. Due to the asynchronous nature of the internal clock and external sync, there may be a one ODR clock cycle difference between consecutive external sync pulses. The external sync sets the ODR of the system. For example, if sending an external sync at a 2 kHz rate, all 3 axes (if enabled) are sampled in that 2 kHz window.

SELF TEST

The ADXL372 incorporates a pass or fail self test feature that effectively tests its mechanical and electronic systems simultaneously. When the self test function is invoked, an electrostatic force is applied to the mechanical sensor. This electrostatic force moves the mechanical sensing element in the same manner as acceleration, and the acceleration experienced by the device increases because of this force.

Self Test Procedure

The self test function is enabled via the ST bit in the SELF_TEST register, Register 0x40. The recommended procedure for using the self test functionality is as follows:

1. Place the device into measurement mode.
2. Make sure the low-pass activity filter is enabled.
3. Assert self test by setting the ST bit in the SELF_TEST register (Register 0x40).

Read the self test status bits, ST_DONE and USER_ST, after approximately 300 ms to check the pass or fail condition.