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3-Axis, ±200 *g* Digital MEMS Accelerometer

Data Sheet

ADXL375

FEATURES

- Low power: as low as 35 µA in measurement mode and 0.1 µA in standby mode at V_S = 2.5 V
- Power consumption scales automatically with bandwidth
- Embedded, 32-level FIFO buffer minimizes processor load
- Bandwidth of up to 1 kHz
  - Bandwidth selectable via serial command
- Shock event detection
- Activity/inactivity monitoring
- Supply voltage range: 2.0 V to 3.6 V
- I/O voltage range: 1.7 V to V_S
- SPI (3- or 4-wire) and I^2C digital interfaces
- Wide temperature range: −40°C to +85°C
- 10,000 *g* shock survival
- Pb free/RoHS compliant
- Small and thin: 3 mm × 5 mm × 1 mm LGA package

APPLICATIONS

- Concussion and head trauma detection
- High force event detection

GENERAL DESCRIPTION

The ADXL375 is a small, thin, 3-axis accelerometer that provides low power consumption and high resolution measurement up to ±200 *g*. The digital output data is formatted as 16-bit, twos complement data and is accessible through a SPI (3- or 4-wire) or I^2C digital interface.

An integrated memory management system with a 32-level first in, first out (FIFO) buffer can be used to store data to minimize host processor activity and lower overall system power consumption.

Low power modes enable intelligent motion-based power management with threshold sensing and active acceleration measurement at extremely low power dissipation.

The ADXL375 is supplied in a small, thin, 3 mm × 5 mm × 1 mm, 14-lead LGA.

FUNCTIONAL BLOCK DIAGRAM

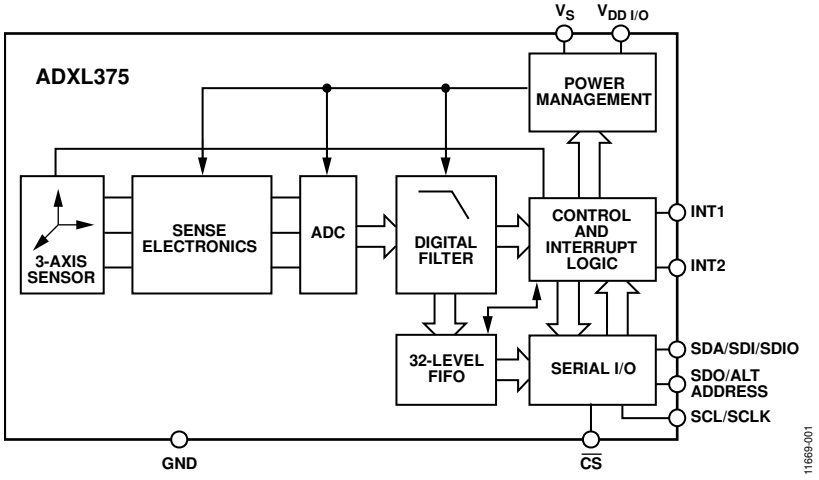

Figure 1.

Rev. B

Document Feedback

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADXL375Z Evaluation Board
- Real Time Eval System for Digital Output Sensor

DOCUMENTATION

Application Notes

- AN-1266: Autonomous Shock Event Monitoring with the ADXL375

Data Sheet

- ADXL375: 3-Axis, ±200 g Digital MEMS Accelerometer Data Sheet

User Guides

- UG-598: 3-Axis, ±200 g Digital Accelerometer Evaluation Board for ADXL375

REFERENCE MATERIALS

Press

- Analog Devices' 3-axis High-g MEMS Accelerometer Enables Highly Accurate Impact, Shock, and Concussive Detection Systems

DESIGN RESOURCES

- ADXL375 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADXL375 EngineerZone Discussions.

SAMPLE AND BUY

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Submit a technical question or find your regional support number.

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REVISION HISTORY

4/14—Rev. A to Rev. B

Changes to Figure 24 ... 15
Changes to Register 0x1E, Register 0x1F, Register 0x20—OFSX, OFSY, OFSZ (Read/Write) Section ... 21

9/13—Rev. 0 to Rev. A

Added MEMS to Product Title ... 1

8/13—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 2.5 V, $V_{DD\ I/O}$ = 2.5 V, acceleration = 0 *g*, C_S = 10 µF tantalum, $C_{I/O}$ = 0.1 µF, output data rate (ODR) = 800 Hz, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ[1]	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range[2]		±180	±200		*g*
Nonlinearity	Percentage of full scale		±0.25		%
Cross-Axis Sensitivity[3]			±2.5		%
SENSITIVITY	Each axis				
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}[2, 4]	ODR ≤ 800 Hz	18.4	20.5	22.6	LSB/*g*
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}[2, 4]	ODR ≤ 800 Hz	44	49	54	mg/LSB
Sensitivity Change Due to Temperature			±0.02		%/°C
0 *g* OFFSET	Each axis				
0 *g* Output for X_{OUT}, Y_{OUT}, Z_{OUT}		−6000	±400	+6000	m*g*
0 *g* Offset vs. Temperature			±10		mg/°C
NOISE	X-, y-, and z-axes		5		mg/√Hz
OUTPUT DATA RATE AND BANDWIDTH[5]	User selectable				
Output Data Rate (ODR)[4, 6]		0.1		3200	Hz
SELF-TEST[7]					
Output Change in Z-Axis			6.4		*g*
POWER SUPPLY					
Operating Voltage Range (V_S)		2.0	2.5	3.6	V
Interface Voltage Range ($V_{DD\ I/O}$)		1.7	1.8	V_S	V
Supply Current					
Measurement Mode	ODR ≥ 100 Hz		145		µA
	ODR ≤ 3 Hz		35		µA
Standby Mode			0.1		µA
Turn-On and Wake-Up Time[8]	ODR = 3200 Hz		1.4		ms
TEMPERATURE					
Operating Temperature Range		−40		+85	°C
WEIGHT					
Device Weight			30		mg

[1] Typical specifications are for at least 68% of the population of parts and are based on the worst case of mean ± 1 σ distribution, except for sensitivity, which represents the target value.
[2] Minimum and maximum specifications represent the worst case of mean ± 3 σ distribution and are not guaranteed in production.
[3] Cross-axis sensitivity is defined as coupling between any two axes.
[4] The output format for the 1600 Hz and 3200 Hz output data rates is different from the output format for the other output data rates. For more information, see the Data Formatting at Output Data Rates of 3200 Hz and 1600 Hz section.
[5] Bandwidth is the −3 dB frequency and is half the output data rate: bandwidth = ODR/2.
[6] Output data rates < 6.25 Hz exhibit additional offset shift with increased temperature.
[7] Self-test change is defined as the output (*g*) when the SELF_TEST bit = 1 (DATA_FORMAT register, Address 0x31) minus the output (*g*) when the SELF_TEST bit = 0. Due to device filtering, the output reaches its final value after 4 × τ when enabling or disabling self-test, where τ = 1/(data rate). For the self-test to operate correctly, the part must be in normal power operation (LOW_POWER bit = 0 in the BW_RATE register, Address 0x2C).
[8] Turn-on and wake-up times are determined by the user-defined bandwidth. At a 100 Hz data rate, the turn-on and wake-up times are each approximately 11.1 ms. For other data rates, the turn-on and wake-up times are each approximately τ + 1.1 ms, where τ = 1/(data rate).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Acceleration, Any Axis	
Unpowered	10,000 *g*
Powered	10,000 *g*
V_S	−0.3 V to +3.9 V
$V_{DD\ I/O}$	−0.3 V to +3.9 V
Digital Pins	−0.3 V to $V_{DD\ I/O}$ + 0.3 V or 3.9 V, whichever is less
Output Short-Circuit Duration (Any Pin to Ground)	Indefinite
Temperature Range	
Powered	−40°C to +105°C
Storage	−40°C to +105°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Unit
14-Terminal LGA	150	85	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SOLDERING PROFILE

Figure 2 and Table 4 provide information about the recommended soldering profile.

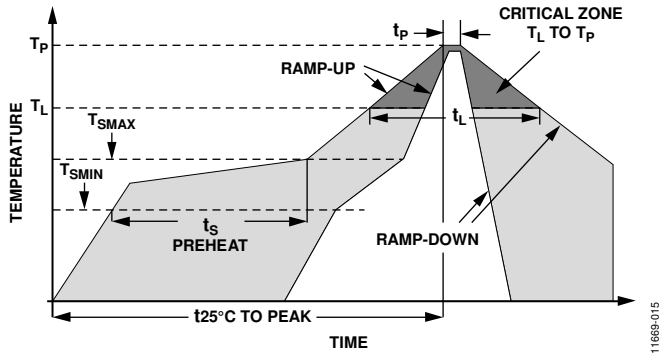


Figure 2. Recommended Soldering Profile

Table 4. Recommended Soldering Profile Limits[1, 2]

Profile Feature	Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)	3°C/sec maximum	3°C/sec maximum
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time from T_{SMIN} to T_{SMAX} (t_S)	60 sec to 120 sec	60 sec to 180 sec
Ramp-Up Rate (T_{SMAX} to T_L)	3°C/sec maximum	3°C/sec maximum
Liquidous Temperature (T_L)	183°C	217°C
Time Maintained Above T_L (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_P)	240°C +0°C/−5°C	260°C +0°C/−5°C
Time Within 5°C of Actual T_P (t_P)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec maximum	6°C/sec maximum
Time 25°C (t25°C) to Peak Temperature	6 minutes maximum	8 minutes maximum

[1] Based on JEDEC Standard J-STD-020D.1.
[2] For best results, the soldering profile should be in accordance with the recommendations of the manufacturer of the solder paste used.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

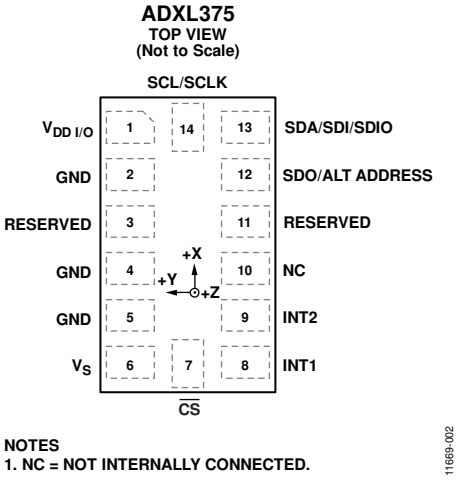


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{DD\ I/O}$	Digital Interface Supply Voltage.
2	GND	Ground. This pin must be connected to ground.
3	RESERVED	Reserved. This pin must be connected to V_S or left open.
4	GND	Ground. This pin must be connected to ground.
5	GND	Ground. This pin must be connected to ground.
6	V_S	Supply Voltage.
7	$\overline{CS}$	Chip Select.
8	INT1	Interrupt 1 Output.
9	INT2	Interrupt 2 Output.
10	NC	Not Internally Connected.
11	RESERVED	Reserved. This pin must be connected to ground or left open.
12	SDO/ALT ADDRESS	SPI 4-Wire Serial Data Output (SDO)/I^2C Alternate Address Select (ALT ADDRESS).
13	SDA/SDI/SDIO	I^2C Serial Data (SDA)/SPI 4-Wire Serial Data Input (SDI)/SPI 3-Wire Serial Data Input and Output (SDIO).
14	SCL/SCLK	I^2C Serial Communications Clock (SCL)/SPI Serial Communications Clock (SCLK).

TYPICAL PERFORMANCE CHARACTERISTICS

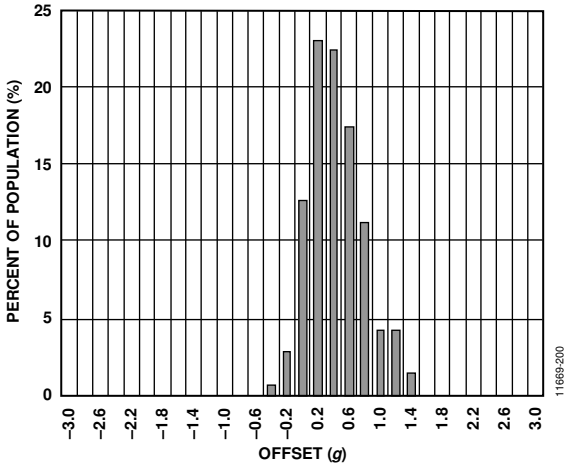


Figure 4. X-Axis Zero g Offset at 25°C, V_S = 2.5 V

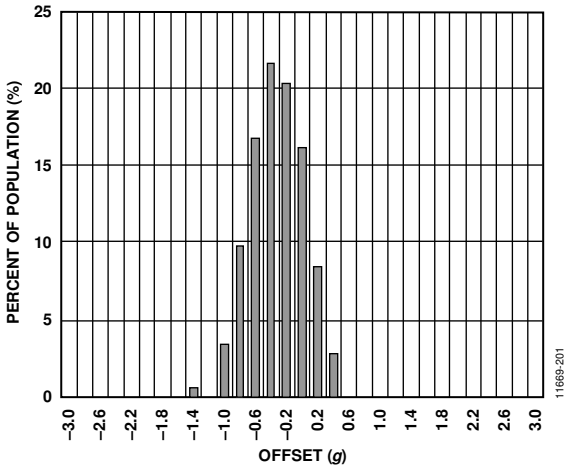


Figure 5. Y-Axis Zero g Offset at 25°C, V_S = 2.5 V

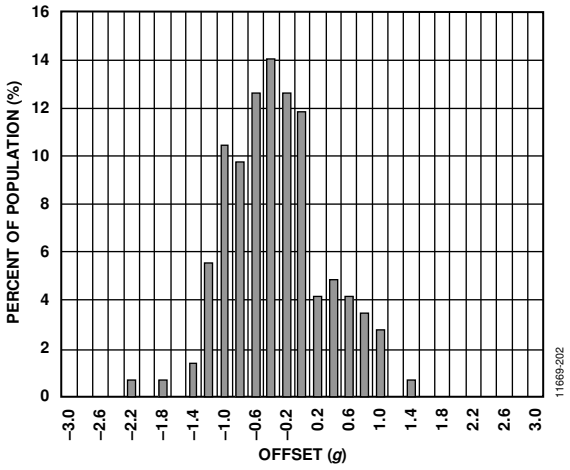


Figure 6. Z-Axis Zero g Offset at 25°C, V_S = 2.5 V

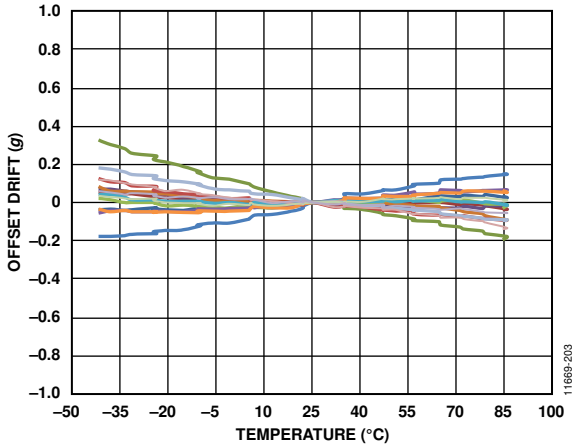


Figure 7. X-Axis Offset Drift, 15 Parts Soldered to PCB, V_S = 2.5 V

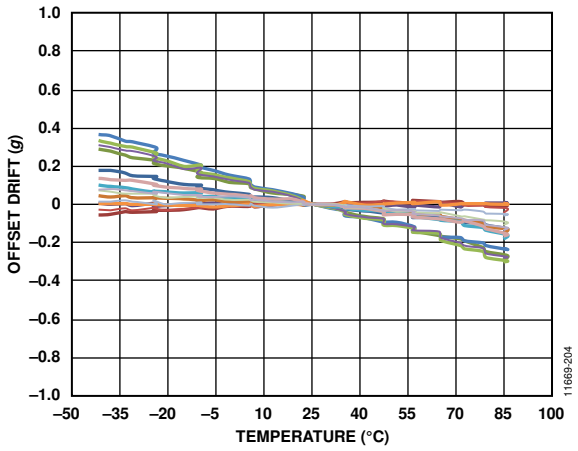


Figure 8. Y-Axis Offset Drift, 15 Parts Soldered to PCB, V_S = 2.5 V

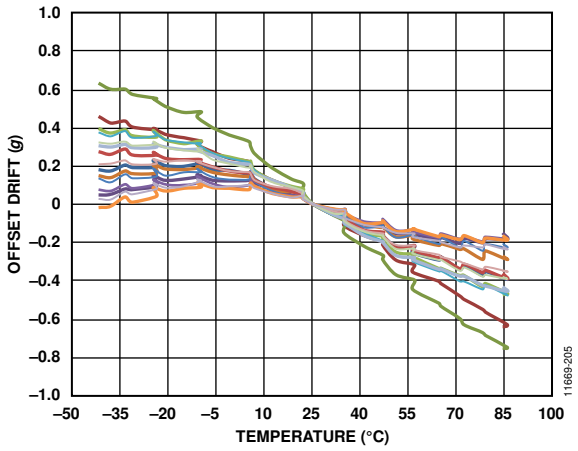


Figure 9. Z-Axis Offset Drift, 15 Parts Soldered to PCB, V_S = 2.5 V

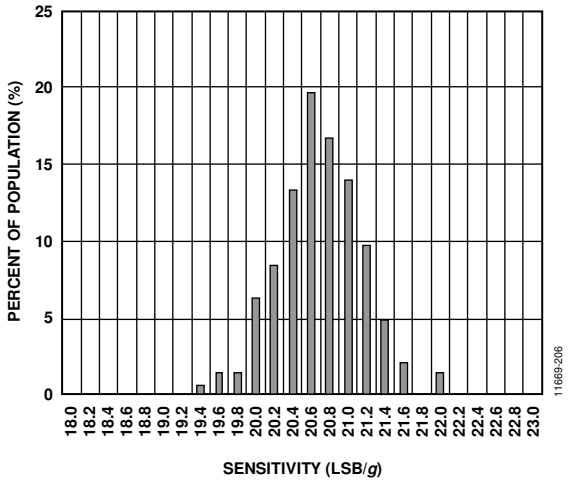


Figure 10. X-Axis Sensitivity at 25°C, V_S = 2.5 V

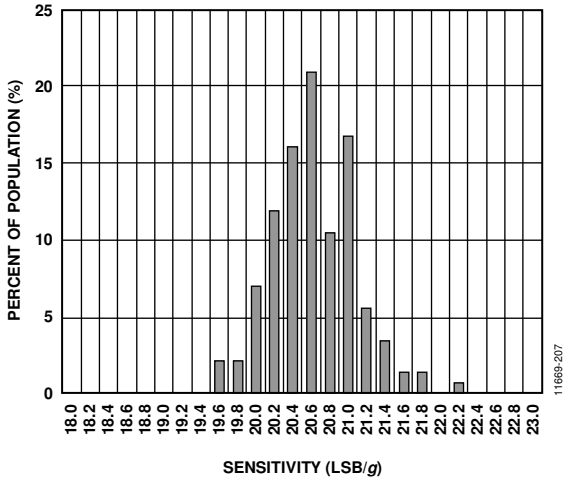


Figure 11. Y-Axis Sensitivity at 25°C, V_S = 2.5 V

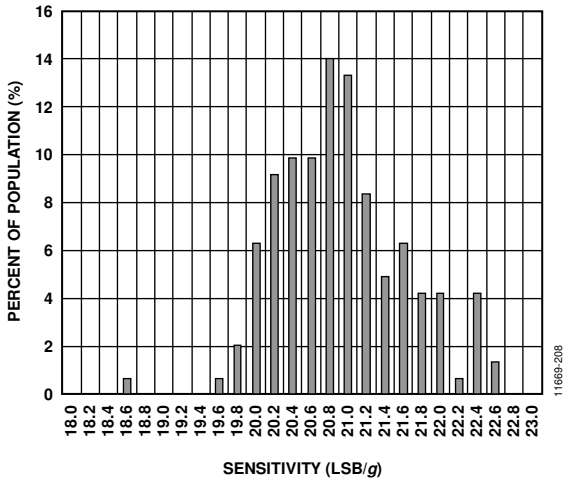


Figure 12. Z-Axis Sensitivity at 25°C, V_S = 2.5 V

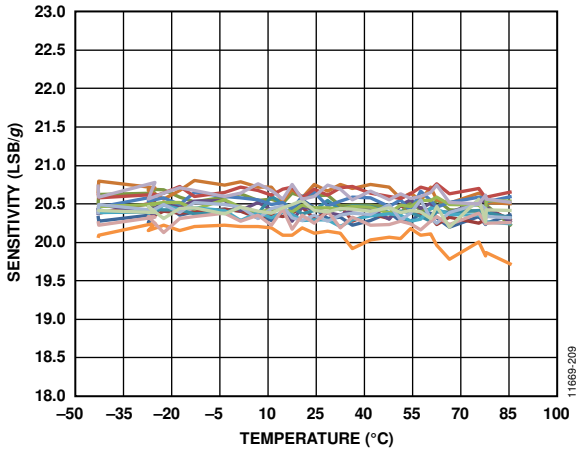


Figure 13. X-Axis Sensitivity vs. Temperature, 16 Parts Soldered to PCB, V_S = 2.5 V

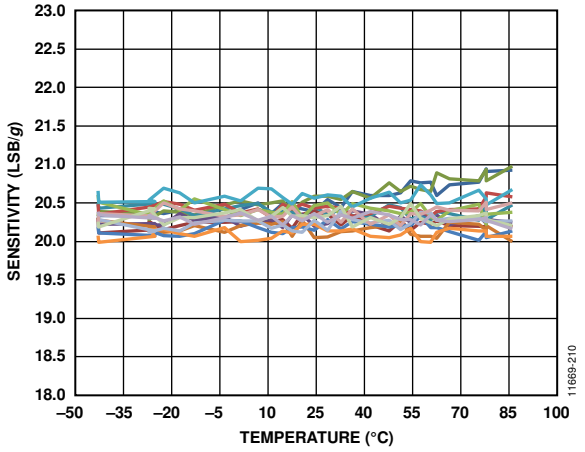


Figure 14. Y-Axis Sensitivity vs. Temperature, 16 Parts Soldered to PCB, V_S = 2.5 V

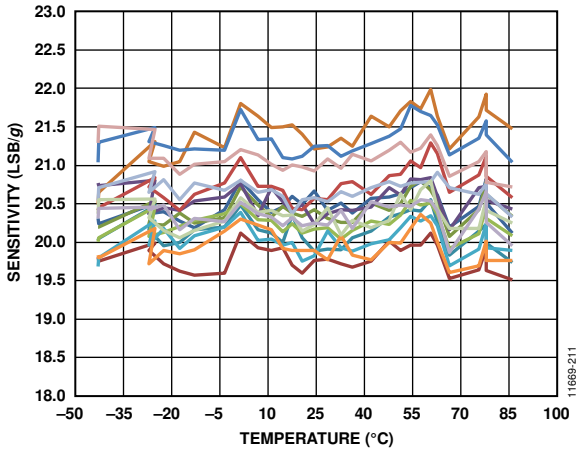


Figure 15. Z-Axis Sensitivity vs. Temperature, 16 Parts Soldered to PCB, V_S = 2.5 V

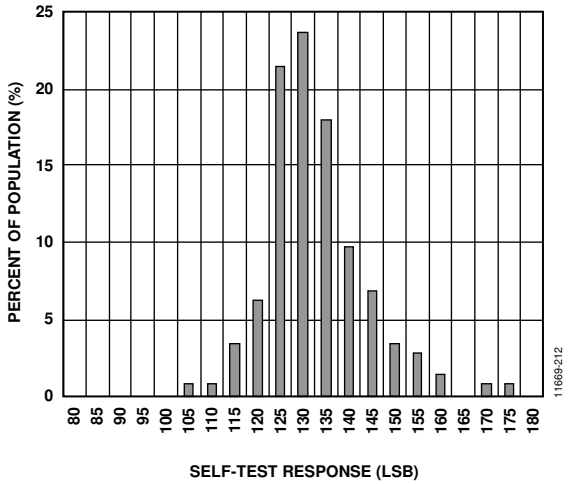


Figure 16. Z-Axis Self-Test Response at 25°C, V_S = 2.5 V

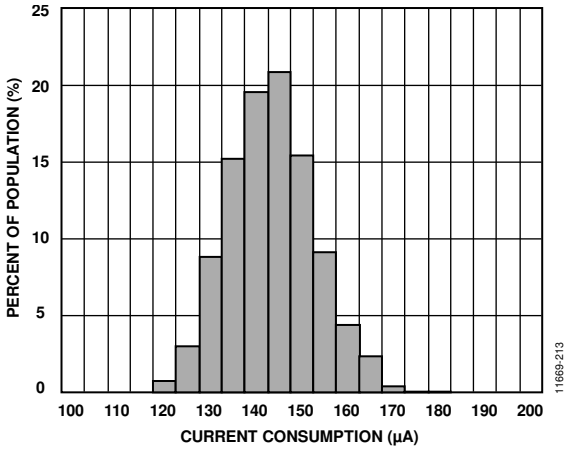


Figure 17. Current Consumption at 25°C, 100 Hz Output Data Rate, V_S = 2.5 V

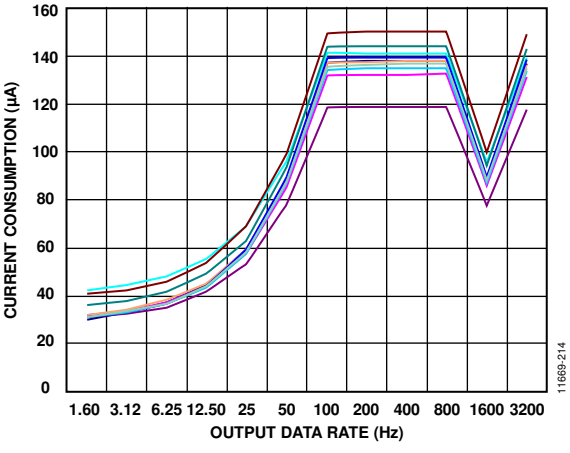


Figure 18. Current Consumption vs. Output Data Rate at 25°C, 10 Parts Soldered to PCB, V_S = 2.5 V

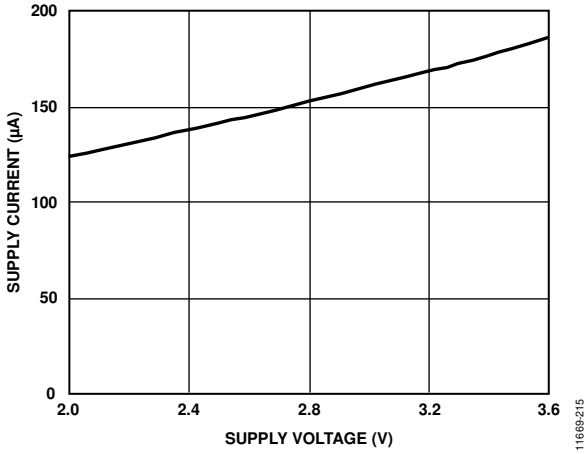


Figure 19. Supply Current vs. Supply Voltage (V_S) at 25°C

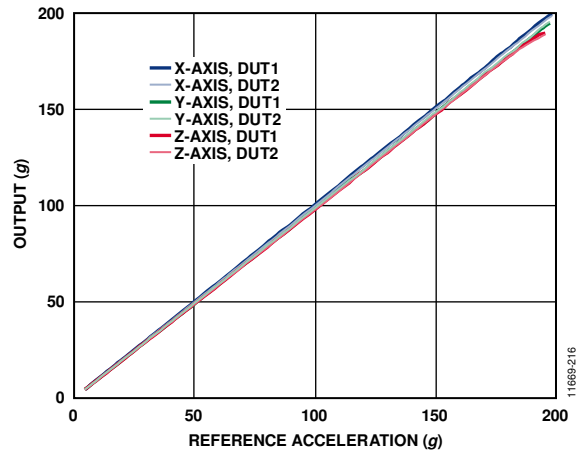


Figure 20. Output Linearity over the Dynamic Range

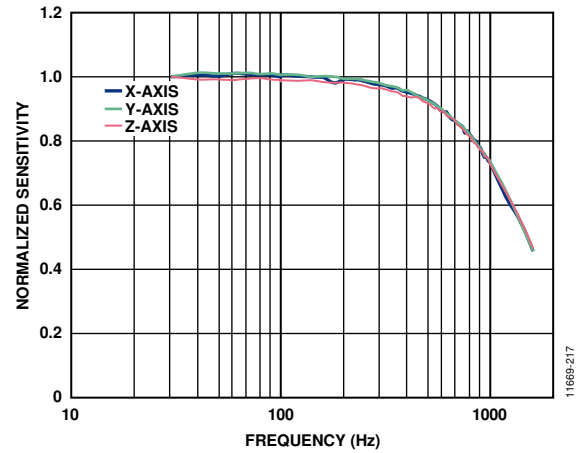


Figure 21. Frequency Response

THEORY OF OPERATION

The ADXL375 is a complete 3-axis acceleration measurement system with a measurement range of ±200 *g*. It measures both dynamic acceleration resulting from motion or shock and static acceleration, such as gravity.

The sensor is a polysilicon surface-micromachined structure built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide resistance against forces due to applied acceleration.

Deflection of the structure is measured using differential capacitors that consist of independent fixed plates and plates attached to the moving mass. Acceleration deflects the proof mass and unbalances the differential capacitor, resulting in a sensor output whose amplitude is proportional to acceleration. Phase sensitive demodulation is used to determine the magnitude and polarity of the acceleration.

POWER SEQUENCING

Power can be applied to V_S or $V_{DD\ I/O}$ in any sequence without damaging the ADXL375. Table 7 provides a description of all the power modes. The interface voltage level is set using the interface supply voltage, $V_{DD\ I/O}$, which must be present to ensure that the ADXL375 does not create a conflict on the communication bus. For single-supply operation, $V_{DD\ I/O}$ can be the same as the main supply, V_S. In a dual-supply application, however, $V_{DD\ I/O}$ can differ from V_S to accommodate the desired interface voltage, as long as V_S is greater than or equal to $V_{DD\ I/O}$.

After V_S is applied, the device enters standby mode. In standby mode, power consumption is minimized; the device waits for $V_{DD\ I/O}$ to be applied and for the command to enter measurement mode. This command can be initiated by setting the measure bit (Bit D3) in the POWER_CTL register (Address 0x2D).

When the device is in standby mode, any register can be written to or read from. It is recommended that the device be configured in standby mode before enabling measurement mode. Clearing the measure bit returns the device to standby mode.

CURRENT CONSUMPTION AND OUTPUT DATA RATE

The ADXL375 automatically modulates its current consumption in proportion to its output data rate (see Table 6). The device bandwidth and output data rate are specified using the rate bits (Bits[D3:D0]) in the BW_RATE register (Address 0x2C).

Table 6. Typical Current Consumption vs. Data Rate (T_A = 25°C, V_S = 2.5 V, $V_{DD\ I/O}$ = 1.8 V)

Rate Bits	Output Data Rate (Hz)	Bandwidth (Hz)	I_{DD} (μA)
1111	3200	1600	145
1110	1600	800	90
1101	800	400	140
1100	400	200	140
1011	200	100	140
1010	100	50	140
1001	50	25	90
1000	25	12.5	60
0111	12.5	6.25	50
0110	6.25	3.13	40
0101	3.13	1.56	35
0100	1.56	0.78	35
0011	0.78	0.39	35
0010	0.39	0.20	35
0001	0.20	0.10	35
0000	0.10	0.05	35

Table 7. Power Modes

Power Mode	V_S	$V_{DD\ I/O}$	Description
Power Off	Off	Off	The device is completely off, but it is still possible for the device to create a conflict on the communication bus.
Bus Disabled	On	Off	The device is on in standby mode, but communication is unavailable and the device can create a conflict on the communication bus. Minimize the duration of the bus disabled state during power-up to prevent a conflict on the communication bus.
Bus Enabled	Off	On	No functions are available, but the device does not create a conflict on the communication bus.
Standby or Measurement	On	On	At power-up, the device is in standby mode, awaiting a command to enter measurement mode, and all sensor functions are off. After the device is instructed to enter measurement mode, all sensor functions are available.

POWER SAVING MODES

Low Power Mode

A low power mode is available for additional power savings. In low power mode, the internal sampling rate is reduced, allowing for power savings in the 12.5 Hz to 400 Hz data rate range at the expense of slightly greater noise. To enter low power mode, set the LOW_POWER bit (Bit D4) in the BW_RATE register (Address 0x2C). Table 8 shows the current consumption in low power mode for output data rates where there is an advantage to using low power mode.

Table 8. Typical Current Consumption vs. Data Rate, Low Power Mode (T_A = 25°C, V_S = 2.5 V, $V_{DD\ I/O}$ = 1.8 V)

Rate Bits	Output Data Rate (Hz)	Bandwidth (Hz)	I_{DD} (μA)
1100	400	200	90
1011	200	100	60
1010	100	50	50
1001	50	25	45
1000	25	12.5	40
0111	12.5	6.25	35

For data rates not shown in Table 8, the use of low power mode does not provide any advantage over normal power mode. Therefore, it is recommended that low power mode be used only for the data rates shown in Table 8.

Autosleep Mode

Additional power can be saved if the ADXL375 automatically switches to sleep mode during periods of inactivity. To enable the autosleep mode feature,

1. Set the THRESH_INACT register (Address 0x25) and the TIME_INACT register (Address 0x26) to values that signify inactivity. The appropriate values depend on the application.
2. Set the AUTO_SLEEP bit (Bit D4) and the link bit (Bit D5) in the POWER_CTL register (Address 0x2D).

Current consumption at the sub-12.5 Hz data rates that are used in autosleep mode is typically 35 μA for V_S = 2.5 V.

For information about the advantages of using low power mode vs. autosleep mode, see the Sleep Mode vs. Low Power Mode section.

Standby Mode

For even lower power operation, standby mode can be used. In standby mode, current consumption is reduced to 0.1 μA (typical). In this mode, no measurements are made, but the contents of the FIFO buffer are preserved. To enter standby mode, clear the measure bit (Bit D3) in the POWER_CTL register (Address 0x2D).

FIFO BUFFER

The ADXL375 contains patented technology for an embedded memory management system with a 32-level FIFO buffer that can be used to minimize host processor burden. This buffer has four modes: bypass, FIFO, stream, and trigger. Each mode can be selected by setting the FIFO_MODE bits (Bits[D7:D6]) in the FIFO_CTL register (Address 0x38; see Table 9).

Table 9. FIFO Modes (FIFO_CTL Register, Address 0x38)

Setting		FIFO	
D7	D6	Mode	Description
0	0	Bypass	FIFO buffer is bypassed.
0	1	FIFO	FIFO buffer collects up to 32 samples and then stops collecting data, collecting new data only when the buffer is not full.
1	0	Stream	FIFO buffer holds the last 32 samples. When the buffer is full, the oldest data is overwritten with newer data.
1	1	Trigger	FIFO buffer holds the last samples before the trigger event and continues to collect data until full. New data is collected only when the buffer is not full.

For an in-depth description of the FIFO buffer and FIFO modes, see the AN-1025 Application Note, *Utilization of the First In, First Out (FIFO) Buffer in Analog Devices, Inc., Digital Accelerometers*.

Bypass Mode

In bypass mode, the FIFO buffer is not operational and, therefore, remains empty.

FIFO Mode

In FIFO mode, data from measurements of the x-, y-, and z-axes is stored in the FIFO buffer. When the number of samples in the FIFO buffer equals the level specified by the samples bits of the FIFO_CTL register (Address 0x38), the watermark interrupt is set (see the Watermark Bit section). The FIFO buffer continues to accumulate samples until it is full (32 samples from measurements of the x-, y-, and z-axes) and then stops collecting data.

After the FIFO buffer stops collecting data, the device continues to operate; therefore, features such as shock detection can be used after the FIFO buffer is full. The watermark interrupt bit remains set until the number of samples in the FIFO buffer is less than the value stored in the samples bits of the FIFO_CTL register.

Stream Mode

In stream mode, data from measurements of the x-, y-, and z-axes is stored in the FIFO buffer. When the number of samples in the FIFO buffer equals the level specified by the samples bits of the FIFO_CTL register (Address 0x38), the watermark interrupt is set (see the Watermark Bit section). The FIFO buffer continues to accumulate samples; the buffer stores the latest 32 samples from measurements of the x-, y-, and z-axes, discarding older data as new data arrives. The watermark interrupt bit remains set until the number of samples in the FIFO buffer is less than the value stored in the samples bits of the FIFO_CTL register.

Trigger Mode

In trigger mode, the FIFO buffer accumulates samples, storing the latest 32 samples from measurements of the x-, y-, and z-axes. After a trigger event occurs, an interrupt is sent to the INT1 or INT2 pin (determined by the trigger bit in the FIFO_CTL register), and the FIFO_TRIG bit (Bit D7) is set in the FIFO_STATUS register (Address 0x39).

The FIFO buffer keeps the last n samples (n is the value specified by the samples bits in the FIFO_CTL register) and then operates in FIFO mode, collecting new samples only when the FIFO buffer is not full. A delay of at least 5 µs must elapse between the occurrence of the trigger event and the start of data readback from the FIFO buffer to allow the buffer to discard and retain the necessary samples.

Additional trigger events cannot be recognized until the part is reset to trigger mode. To reset the part to trigger mode,

1. If desired, read data from the FIFO buffer (see the Retrieving Data from the FIFO Buffer section).
   Before resetting the part to trigger mode, read back the FIFO data; placing the device into bypass mode clears the FIFO buffer.
2. Configure the device for bypass mode by setting Bits[D7:D6] at Address 0x38 to 00.
3. Configure the device for trigger mode by setting Bits[D7:D6] at Address 0x38 to 11.

Retrieving Data from the FIFO Buffer

When the FIFO buffer operates in FIFO, stream, or trigger mode, FIFO data can be read from the data registers (Address 0x32 to Address 0x37). Each time data is read from the FIFO buffer, the oldest x-, y-, and z-axis data is moved into the DATAX, DATAY, and DATAZ registers.

If a single-byte read operation is performed, the remaining bytes of data for the current FIFO sample are lost. Therefore, data for all axes of interest must be read in a burst (multiple-byte) read operation. To ensure that the FIFO buffer is empty (that is, all new data has moved into the data registers), an interval of at least 5 µs must elapse between the end of the readback from the data registers and the start of a new read of the data registers or the FIFO_STATUS register (Address 0x39). The end of a read operation from the data registers is signified by the transition from Register 0x37 to Register 0x38 or by the $\overline{CS}$ pin going high.

When SPI operation is enabled at a frequency of 1.6 MHz or lower, the register addressing portion of the transmission provides a sufficient delay to ensure that the FIFO buffer has completely emptied. When SPI operation is enabled at a frequency higher than 1.6 MHz, the $\overline{CS}$ pin must be deasserted to ensure a total delay of 5 µs; otherwise, the delay is not sufficient. When SPI operation is enabled at 5 MHz, the total delay necessary is at most 3.4 µs.

When I^2C mode is enabled on the part, the communication rate is low enough to ensure a sufficient delay between FIFO reads.

SELF-TEST

The ADXL375 incorporates a self-test feature that effectively tests its mechanical and electronic systems simultaneously. When the self-test function is enabled (via the SELF_TEST bit in the DATA_FORMAT register, Address 0x31), an electrostatic force is exerted on the mechanical sensor.

This electrostatic force moves the mechanical sensing element in the same manner as acceleration, and it is additive to the external acceleration experienced by the device. This added electrostatic force results in an output change in the x-, y-, and z-axes. Because the electrostatic force is proportional to V_S^2, the output change varies with V_S.

The self-test response in the x- and y-axes exhibits bimodal behavior and, therefore, is not always a reliable indicator of sensor health or potential shift in device sensitivity. For this reason, perform the self-test check in the z-axis.

Use of the self-test feature at data rates of less than 100 Hz or at 1600 Hz may yield values outside the limits shown in Figure 16. For the self-test function to operate correctly, the part must be in normal power operation (LOW_POWER bit = 0 in the BW_RATE register, Address 0x2C) and be configured for a data rate from 100 Hz to 800 Hz, or for a data rate of 3200 Hz (see Table 6).

For more information about the self-test feature, see the Using Self-Test section.

INTERRUPTS

The ADXL375 provides two output pins for driving interrupts: INT1 and INT2. Both interrupt pins are push-pull, low impedance pins (see Table 10 for output specifications). The default configuration of the interrupt pins is active high. The polarity can be changed to active low by setting the INT_INVERT bit (Bit D5) in the DATA_FORMAT register (Address 0x31). All interrupt functions can be enabled simultaneously, but some functions may need to share the same interrupt pin.

ENABLING AND DISABLING INTERRUPTS

Interrupts are enabled by setting the appropriate bits in the INT_ENABLE register (Address 0x2E); the interrupt is mapped to the INT1 pin or the INT2 pin based on the contents of the INT_MAP register (Address 0x2F). When the user configures the interrupt pins for the first time, it is recommended that the functions and interrupt mapping be configured before the interrupts are enabled.

When changing the configuration of an interrupt, follow this procedure.

1. Disable the interrupt by clearing the bit corresponding to the function in the INT_ENABLE register.
2. Reconfigure the interrupt function.
3. Reenable the interrupt in the INT_ENABLE register.

Configuration of the functions while the interrupts are disabled helps to prevent the accidental generation of an interrupt.

CLEARING INTERRUPTS

The interrupt functions are latched and can be cleared as follows:

1. Read the data registers (Address 0x32 to Address 0x37) to clear the data-related interrupts.
2. Read the INT_SOURCE register (Address 0x30) to clear the remaining interrupts.

BITS IN THE INTERRUPT REGISTERS

This section describes the interrupts that can be set in the INT_ENABLE register (Address 0x2E) and monitored in the INT_SOURCE register (Address 0x30).

For an in-depth description of the FIFO buffer and the interrupt bits, see the AN-1025 Application Note, *Utilization of the First In, First Out (FIFO) Buffer in Analog Devices, Inc., Digital Accelerometers*.

DATA_READY Bit

The DATA_READY bit is set when new data is available and is cleared when no new data is available.

SINGLE_SHOCK Bit

The SINGLE_SHOCK bit is set when a single acceleration event that is greater than the value in the THRESH_SHOCK register (Address 0x1D) occurs for less time than is specified by the DUR register (Address 0x21). For more information, see the Shock Detection section.

DOUBLE_SHOCK Bit

The DOUBLE_SHOCK bit is set when two acceleration events that are greater than the value in the THRESH_SHOCK register (Address 0x1D) occur for less time than is specified by the DUR register (Address 0x21). The second shock event starts after the time specified by the latent register (Address 0x22) but within the time specified by the window register (Address 0x23). For more information, see the Shock Detection section.

Activity Bit

The activity bit is set when acceleration greater than the value stored in the THRESH_ACT register (Address 0x24) is experienced on any participating axis. Participating axes are specified by the ACT_INACT_CTL register (Address 0x27).

Table 10. Interrupt Pin Digital Output Specifications

Parameter	Test Conditions/Comments	Limit[1]		Unit
		Min	Max	
DIGITAL OUTPUT				
Low Level Output Voltage (V_{OL})	I_{OL} = 300 µA		0.2 × $V_{DD\ I/O}$	V
High Level Output Voltage (V_{OH})	I_{OH} = −150 µA	0.8 × $V_{DD\ I/O}$		V
Low Level Output Current (I_{OL})	V_{OL} = $V_{OL,\ MAX}$	300		µA
High Level Output Current (I_{OH})	V_{OH} = $V_{OH,\ MIN}$		−150	µA
PIN CAPACITANCE	f_{IN} = 1 MHz, V_S = 2.5 V		8	pF
RISE/FALL TIME	C_{LOAD} = 150 pF			
Rise Time (t_R)[2]			210	ns
Fall Time (t_F)[3]			150	ns

[1] Limits based on characterization results; not production tested.
[2] Rise time is measured as the transition time from $V_{OL,\ MAX}$ to $V_{OH,\ MIN}$ of the interrupt pin.
[3] Fall time is measured as the transition time from $V_{OH,\ MIN}$ to $V_{OL,\ MAX}$ of the interrupt pin.

Inactivity Bit

The inactivity bit is set when acceleration less than the value stored in the THRESH_INACT register (Address 0x25) is experienced for more time than is specified by the TIME_INACT register (Address 0x26) on all participating axes. Participating axes are specified by the ACT_INACT_CTL register (Address 0x27). The maximum value for TIME_INACT is 255 sec.

Watermark Bit

The watermark bit is set when the number of samples in the FIFO buffer equals the value stored in the samples bits (Bits[D4:D0]) of the FIFO_CTL register (Address 0x38). The watermark bit is cleared automatically when the FIFO buffer is read and the FIFO contents return to a value below the value specified by the samples bits.

Overrun Bit

The overrun bit is set when new data replaces unread data. The precise operation of the overrun function depends on the FIFO mode (see the FIFO Buffer section).

- In bypass mode, the overrun bit is set when new data replaces unread data in the data registers (Address 0x32 to Address 0x37).
- In FIFO mode, stream mode, and trigger mode, the overrun bit is set when the FIFO buffer is full.

The overrun bit is automatically cleared when the FIFO buffer contents are read.

SERIAL COMMUNICATIONS

The ADXL375 supports I²C and SPI digital communications. In both cases, the ADXL375 operates as a slave device. When the $\overline{CS}$ pin is tied high to $V_{DD\ I/O}$, I²C mode is enabled. The $\overline{CS}$ pin must be tied high to $V_{DD\ I/O}$ or be driven by an external controller. If the $\overline{CS}$ pin is left unconnected, the user may not be able to communicate with the part. In SPI mode, the $\overline{CS}$ pin is controlled by the bus master. In both SPI and I²C modes of operation, ignore data transmitted from the ADXL375 to the master device during writes to the ADXL375.

SPI MODE

The ADXL375 can be configured for 3-wire SPI mode or 4-wire SPI mode, as shown in Figure 22 and Figure 23. Clearing the SPI bit (Bit D6) in the DATA_FORMAT register (Address 0x31) selects 4-wire mode; setting the SPI bit selects 3-wire mode. The maximum SPI clock speed is 5 MHz with 100 pF maximum loading. The timing scheme requires clock polarity (CPOL) = 1 and clock phase (CPHA) = 1. If power is applied to the ADXL375 before the clock polarity and phase of the host processor are configured, take the $\overline{CS}$ pin high before changing the clock polarity and phase. When using 3-wire SPI mode, it is recommended that the SDO pin be either pulled up to $V_{DD\ I/O}$ or pulled down to GND via a 10 kΩ resistor.

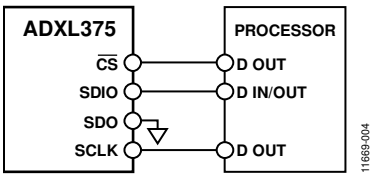


Figure 22. 3-Wire SPI Connection Diagram

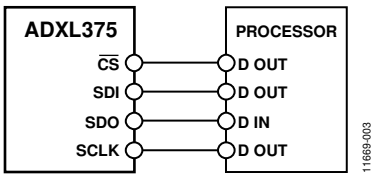


Figure 23. 4-Wire SPI Connection Diagram

$\overline{CS}$ is the serial port enable line and is controlled by the SPI master. This line must go low at the start of a transmission and high at the end of a transmission, as shown in Figure 25 to Figure 27. SCLK is the serial port clock and is supplied by the SPI master. SCLK should idle high during a period of no transmission. In 4-wire SPI mode, SDI and SDO are the serial data input and output, respectively. In 3-wire SPI mode, SDIO functions as both the serial data input and output. Data is updated on the falling edge of SCLK and should be sampled on the rising edge of SCLK.

To read or write multiple bytes in a single transmission, the multiple-byte bit (MB in Figure 25 to Figure 27), located after the R/$\overline{W}$ bit in the first byte transfer, must be set. After the register address byte and the first byte of data, each subsequent set of eight clock pulses causes the ADXL375 to point to the next register for a read or write. This shifting continues until the clock pulses cease and $\overline{CS}$ is deasserted. To perform reads or writes on different, nonsequential registers, $\overline{CS}$ must be deasserted between transmissions and the new register must be addressed separately.

Figure 25 and Figure 26 show the timing diagrams for 4-wire SPI writes and reads, respectively. Figure 27 shows the timing diagram for 3-wire SPI reads or writes. For correct operation of the part, the logic thresholds and timing parameters in Table 11 and Table 12 must be met at all times.

Use of the 3200 Hz and 1600 Hz output data rates is recommended only with SPI communication speeds greater than or equal to 2 MHz. The 800 Hz output data rate is recommended only with communication speeds greater than or equal to 400 kHz, and the remaining data rates scale proportionally. For example, the minimum recommended communication speed for a 200 Hz output data rate is 100 kHz. Operation at an output data rate above the recommended maximum value may result in undesirable effects on the acceleration data, including missing samples or additional noise.

Preventing Bus Traffic Errors

The ADXL375 $\overline{CS}$ pin is used both for initiating SPI transactions and for enabling I²C mode. When the ADXL375 is used on a SPI bus with multiple devices, its $\overline{CS}$ pin is held high while the master communicates with the other devices. There may be conditions where a SPI command transmitted to another device looks like a valid I²C command. In this case, the ADXL375 interprets this command as an attempt to communicate in I²C mode and may interfere with other bus traffic. Unless bus traffic can be adequately controlled to ensure that such a condition never occurs, it is recommended that a logic gate be added in front of Pin 13 (SDA/SDI/SDIO), as shown in Figure 24. This OR gate holds the SDA line high when $\overline{CS}$ is high to prevent SPI bus traffic at the ADXL375 from appearing as an I²C start command.

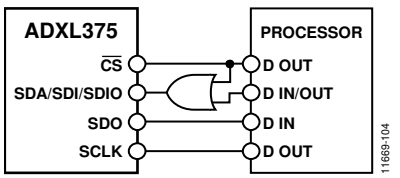


Figure 24. Recommended SPI Connection Diagram When Using Multiple SPI Devices on a Single Bus

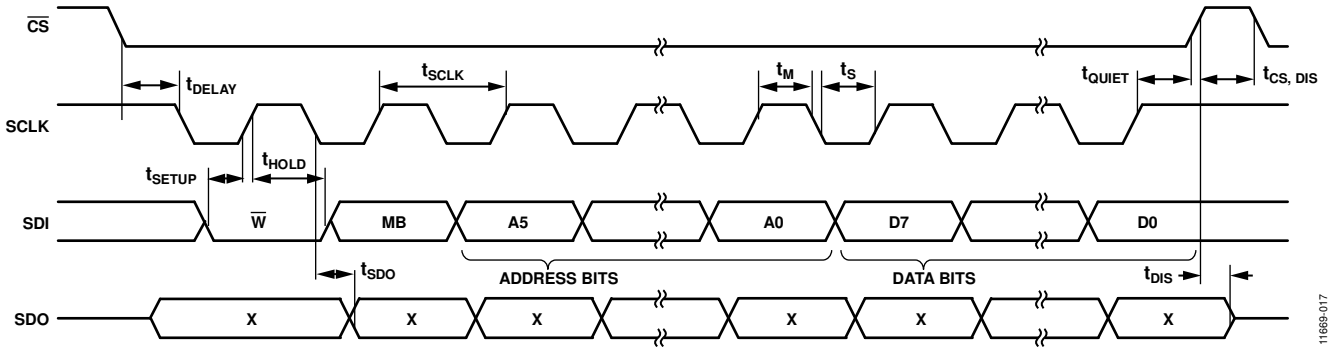


Figure 25. SPI 4-Wire Write Timing Diagram

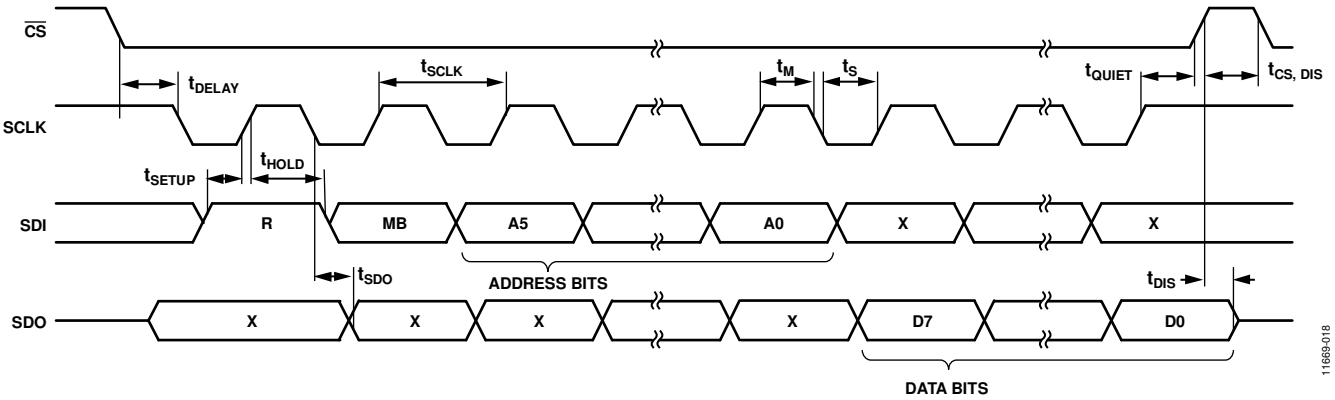
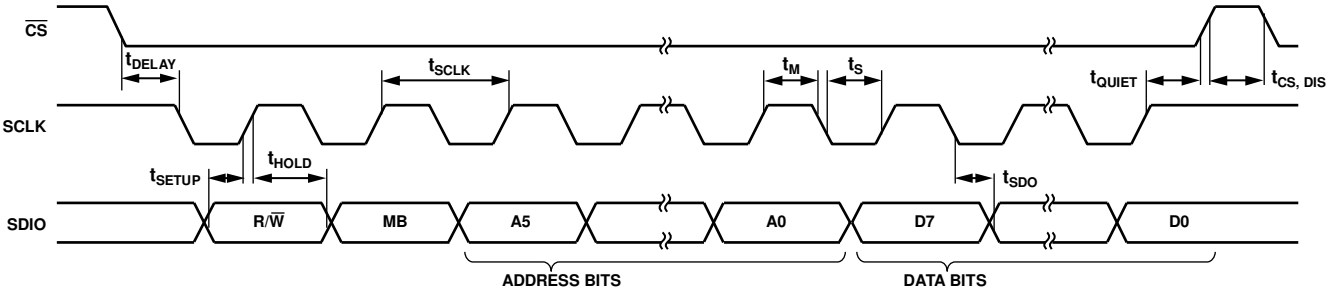


Figure 26. SPI 4-Wire Read Timing Diagram



NOTES
1. t_{SDO} IS ONLY PRESENT DURING READS.

Figure 27. SPI 3-Wire Read/Write Timing Diagram

Table 11. SPI Digital Input/Output Specifications

Parameter	Test Conditions/Comments	Limit[1]		Unit
		Min	Max	
DIGITAL INPUT				
Low Level Input Voltage (V_{IL})			$0.3 \times V_{DD\ I/O}$	V
High Level Input Voltage (V_{IH})		$0.7 \times V_{DD\ I/O}$		V
Low Level Input Current (I_{IL})	$V_S = V_{DD\ I/O}$		0.1	μA
High Level Input Current (I_{IH})	$V_S = 0$ V	−0.1		μA
DIGITAL OUTPUT				
Low Level Output Voltage (V_{OL})	$I_{OL} = 10$ mA		$0.2 \times V_{DD\ I/O}$	V
High Level Output Voltage (V_{OH})	$I_{OH} = -4$ mA	$0.8 \times V_{DD\ I/O}$		V
Low Level Output Current (I_{OL})	$V_{OL} = V_{OL,\ MAX}$	10		mA
High Level Output Current (I_{OH})	$V_{OH} = V_{OH,\ MIN}$		−4	mA
PIN CAPACITANCE	$f_{IN} = 1$ MHz, $V_S = 2.5$ V		8	pF

[1] Limits based on characterization results; not production tested.

Table 12. SPI Timing ($T_A = 25°C$, $V_S = 2.5$ V, $V_{DD\ I/O} = 1.8$ V)[1]

Parameter	Limit[2, 3]		Unit	Description
	Min	Max		
f_{SCLK}		5	MHz	SPI clock frequency
t_{SCLK}	200		ns	Mark-space ratio (1/(SPI clock frequency)) for the SCLK input is 40/60 to 60/40
t_{DELAY}	5		ns	$\overline{CS}$ falling edge to SCLK falling edge
t_{QUIET}	5		ns	SCLK rising edge to $\overline{CS}$ rising edge
t_{DIS}		10	ns	$\overline{CS}$ rising edge to SDO/SDIO disabled
$t_{CS,\ DIS}$	150		ns	$\overline{CS}$ deassertion between SPI communications
t_S	$0.3 \times t_{SCLK}$		ns	SCLK low pulse width (space)
t_M	$0.3 \times t_{SCLK}$		ns	SCLK high pulse width (mark)
t_{SETUP}	5		ns	SDI/SDIO valid before SCLK rising edge
t_{HOLD}	5		ns	SDI/SDIO valid after SCLK rising edge
t_{SDO}		40	ns	SCLK falling edge to SDO/SDIO output transition
t_R[4]		20	ns	SDO/SDIO output high to output low transition
t_F[4]		20	ns	SDO/SDIO output low to output high transition

[1] The $\overline{CS}$, SCLK, SDI, and SDO pins are not internally pulled up or down; they must be driven for proper operation.
[2] Limits based on characterization results, with $f_{SCLK} = 5$ MHz and bus load capacitance of 100 pF; not production tested.
[3] The timing values are referred to the input thresholds (V_{IL} and V_{IH}) given in Table 11.
[4] Output rise and fall times measured with capacitive load of 150 pF. t_R and t_F are not shown in Figure 25 to Figure 27.

I²C MODE

When the $\overline{CS}$ pin is tied high to $V_{DD\ I/O}$, the ADXL375 is configured for I²C mode. I²C mode requires a simple 2-wire connection, as shown in Figure 28. The ADXL375 conforms to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007, available from NXP Semiconductors. The ADXL375 supports standard (100 kHz) and fast (400 kHz) data transfer modes if the bus parameters given in Table 13 and Table 14 are met.

Single- or multiple-byte reads and writes are supported, as shown in Figure 29. When the ALT ADDRESS pin (Pin 12) is tied high to $V_{DD\ I/O}$, the 7-bit I²C address for the device is 0x1D, followed by the R/$\overline{W}$ bit. In this configuration, the write address is 0x3A, and the read address is 0x3B. An alternate I²C address of 0x53 can be selected by grounding the ALT ADDRESS pin (see Figure 28). In this configuration, the write address is 0xA6, and the read address is 0xA7.

Unused pins have no internal pull-up or pull-down resistors; therefore, the $\overline{CS}$ and ALT ADDRESS pins have no known state or default state if the pins are left floating or unconnected. When using I²C mode, it is required that the $\overline{CS}$ pin be connected to $V_{DD\ I/O}$ and that the ALT ADDRESS pin be connected to either $V_{DD\ I/O}$ or GND.

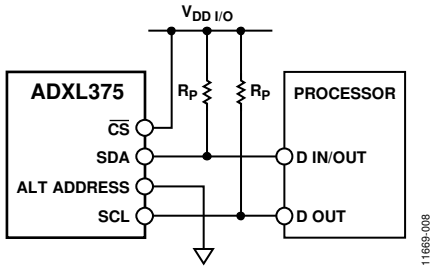


Figure 28. I²C Connection Diagram (Address 0x53)

Due to communication speed limitations, the maximum output data rate when using 400 kHz I²C mode is 800 Hz, which scales linearly with a change in the I²C communication speed. For example, using I²C mode at 100 kHz limits the maximum ODR to 200 Hz. Operation at an output data rate above the recommended maximum value may result in undesirable effects on the acceleration data, including missing samples or additional noise.

If other devices are connected to the same I²C bus, the nominal operating voltage level of the other devices cannot exceed $V_{DD\ I/O}$ by more than 0.3 V. External pull-up resistors, R_P, are necessary for proper I²C operation (see Figure 28). To ensure proper operation, refer to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007, when selecting pull-up resistor values.

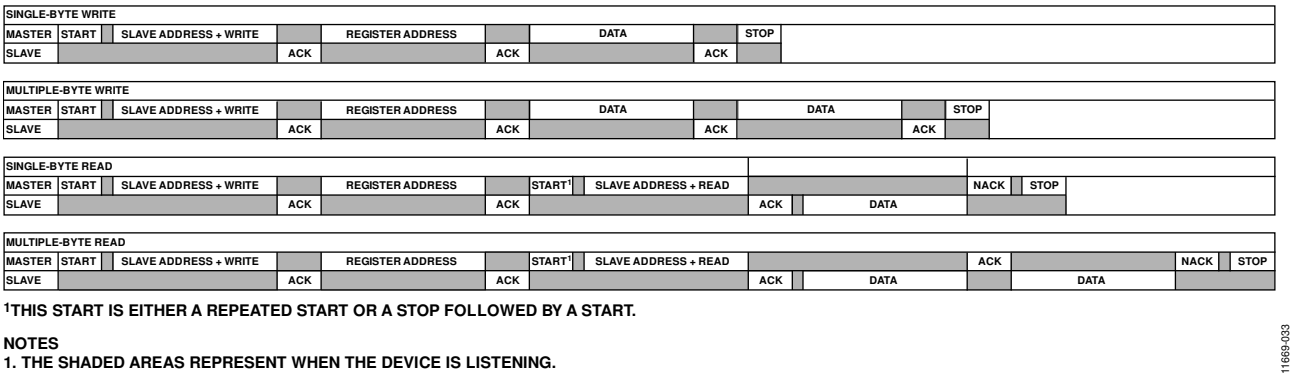


Figure 29. I²C Device Addressing

Table 13. I²C Digital Input/Output Specifications

Parameter	Test Conditions/Comments	Limit[1]		Unit
		Min	Max	
DIGITAL INPUT				
Low Level Input Voltage (V_{IL})			0.3 × $V_{DD\ I/O}$	V
High Level Input Voltage (V_{IH})		0.7 × $V_{DD\ I/O}$		V
Low Level Input Current (I_{IL})	$V_S = V_{DD\ I/O}$		0.1	µA
High Level Input Current (I_{IH})	V_S = 0 V	−0.1		µA
DIGITAL OUTPUT				
Low Level Output Voltage (V_{OL})	$V_{DD\ I/O}$ < 2 V, I_{OL} = 3 mA		0.2 × $V_{DD\ I/O}$	V
	$V_{DD\ I/O}$ ≥ 2 V, I_{OL} = 3 mA		400	mV
Low Level Output Current (I_{OL})	$V_{OL} = V_{OL,\ MAX}$	3		mA
PIN CAPACITANCE	f_{IN} = 1 MHz, V_S = 2.5 V		8	pF

[1] Limits based on characterization results; not production tested.

Table 14. I²C Timing (T_A = 25°C, V_S = 2.5 V, $V_{DD\ I/O}$ = 1.8 V)

	Limit[1, 2]			
Parameter	**Min**	**Max**	**Unit**	**Description**
f_{SCL}		400	kHz	SCL clock frequency
t_1	2.5		µs	SCL cycle time
t_2	0.6		µs	SCL high time
t_3	1.3		µs	SCL low time
t_4	0.6		µs	Hold time for start/repeated start condition
t_5	100		ns	Data setup time
t_6[3, 4, 5]	0	0.9	µs	Data hold time
t_7	0.6		µs	Setup time for repeated start condition
t_8	0.6		µs	Setup time for stop condition
t_9	1.3		µs	Bus-free time between a stop condition and a start condition
t_{10}		300	ns	Rise time of SCL and SDA when receiving
	0		ns	Rise time of SCL and SDA when receiving or transmitting
t_{11}		300	ns	Fall time of SCL and SDA when receiving
		250	ns	Fall time of SCL and SDA when transmitting
C_b		400	pF	Capacitive load for each bus line

[1] Limits based on characterization results, with f_{SCL} = 400 kHz and a 3 mA sink current; not production tested.
[2] The timing values are referred to the input thresholds (V_{IL} and V_{IH}) given in Table 13.
[3] t_6 is the data hold time that is measured from the falling edge of SCL. It applies to data during the transmission and acknowledge phases.
[4] To bridge the undefined region of the falling edge of SCL, a transmitting device must internally provide an output hold time of at least 300 ns for the SDA signal (with respect to $V_{IH, MIN}$ of the SCL signal).
[5] The maximum value for t_6 must be met only if the device does not stretch the low period (t_3) of the SCL signal. The maximum value for t_6 is a function of the clock low time (t_3), the clock rise time (t_{10}), and the minimum data setup time ($t_{5(MIN)}$). This value is calculated as $t_{6(MAX)} = t_3 - t_{10} - t_{5(MIN)}$.

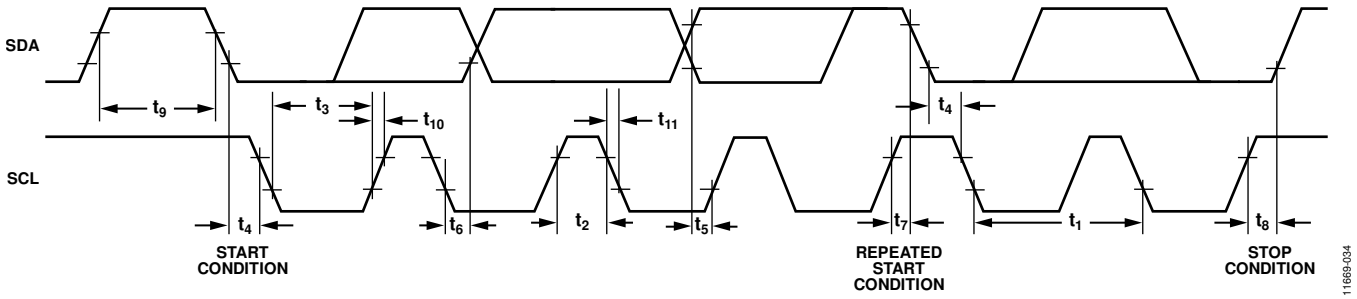


Figure 30. I²C Timing Diagram

REGISTER MAP

All registers in the ADXL375 are eight bits in length.

Table 15. Register Map

Address					
Hex	**Decimal**	**Register Name**	**Access Type**	**Reset Value**	**Description**
0x00	0	DEVID	R	11100101	Device ID
0x01 to 0x1C	1 to 28	Reserved	N/A	N/A	Reserved; do not access
0x1D	29	THRESH_SHOCK	R/$\overline{W}$	00000000	Shock threshold
0x1E	30	OFSX	R/$\overline{W}$	00000000	X-axis offset
0x1F	31	OFSY	R/$\overline{W}$	00000000	Y-axis offset
0x20	32	OFSZ	R/$\overline{W}$	00000000	Z-axis offset
0x21	33	DUR	R/$\overline{W}$	00000000	Shock duration
0x22	34	Latent	R/$\overline{W}$	00000000	Shock latency
0x23	35	Window	R/$\overline{W}$	00000000	Shock window
0x24	36	THRESH_ACT	R/$\overline{W}$	00000000	Activity threshold
0x25	37	THRESH_INACT	R/$\overline{W}$	00000000	Inactivity threshold
0x26	38	TIME_INACT	R/$\overline{W}$	00000000	Inactivity time
0x27	39	ACT_INACT_CTL	R/$\overline{W}$	00000000	Axis enable control for activity and inactivity detection
0x2A	42	SHOCK_AXES	R/$\overline{W}$	00000000	Axis control for single shock/double shock
0x2B	43	ACT_SHOCK_STATUS	R	00000000	Source of single shock/double shock
0x2C	44	BW_RATE	R/$\overline{W}$	00001010	Data rate and power mode control
0x2D	45	POWER_CTL	R/$\overline{W}$	00000000	Power saving features control
0x2E	46	INT_ENABLE	R/$\overline{W}$	00000000	Interrupt enable control
0x2F	47	INT_MAP	R/$\overline{W}$	00000000	Interrupt mapping control
0x30	48	INT_SOURCE	R	00000010	Interrupt source
0x31	49	DATA_FORMAT	R/$\overline{W}$	00000000	Data format control
0x32	50	DATAX0	R	00000000	X-Axis Data 0
0x33	51	DATAX1	R	00000000	X-Axis Data 1
0x34	52	DATAY0	R	00000000	Y-Axis Data 0
0x35	53	DATAY1	R	00000000	Y-Axis Data 1
0x36	54	DATAZ0	R	00000000	Z-Axis Data 0
0x37	55	DATAZ1	R	00000000	Z-Axis Data 1
0x38	56	FIFO_CTL	R/$\overline{W}$	00000000	FIFO control
0x39	57	FIFO_STATUS	R	00000000	FIFO status

REGISTER DESCRIPTIONS

All registers in the ADXL375 are eight bits in length.

Register 0x00—DEVID (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	0	1	0	1

The read-only DEVID register holds the fixed device ID code of 0xE5 (345 octal).

Register 0x1D—THRESH_SHOCK (Read/Write)

The THRESH_SHOCK register contains the unsigned threshold value for shock interrupts. The magnitude of the shock event is compared with the value in the THRESH_SHOCK register for shock detection. The scale factor is 780 mg/LSB. A value of 0 may result in undesirable behavior if single shock/double shock interrupts are enabled.

Register 0x1E, Register 0x1F, Register 0x20—OFSX, OFSY, OFSZ (Read/Write)

The OFSX, OFSY, and OFSZ registers contain user-configured offset adjustments in twos complement format with a scale factor of 0.196 *g*/LSB. The value stored in the offset registers is automat-ically added to the acceleration data, and the resulting value is stored in the output data registers (Address 0x32 to Address 0x37). For more information about offset calibration and the use of the offset registers, see the Offset Calibration section.

Register 0x21—DUR (Read/Write)

The DUR register contains an unsigned time value representing the maximum time that an event must be above the THRESH_SHOCK threshold to qualify as a shock event. The scale factor is 625 µs/LSB. A value of 0 disables the single shock and double shock functions.

Register 0x22—Latent (Read/Write)

The latent register contains an unsigned time value representing the wait time from the detection of a shock event to the start of the time window (specified by the window register) during which a possible second shock event can be detected. The scale factor is 1.25 ms/LSB. A value of 0 disables the double shock function.

Register 0x23—Window (Read/Write)

The window register contains an unsigned time value representing the amount of time after the expiration of the latency time (specified by the latent register) during which a second valid shock can begin. The scale factor is 1.25 ms/LSB. A value of 0 disables the double shock function.

Register 0x24—THRESH_ACT (Read/Write)

The THRESH_ACT register contains the unsigned threshold value for detecting activity. The magnitude of the activity event is compared with the value in the THRESH_ACT register. The scale factor is 780 mg/LSB. A value of 0 may result in undesirable behavior if the activity interrupt is enabled.

Register 0x25—THRESH_INACT (Read/Write)

The THRESH_INACT register contains the unsigned threshold value for detecting inactivity. The magnitude of the inactivity event is compared with the value in the THRESH_INACT register. The scale factor is 780 mg/LSB. A value of 0 may result in undesirable behavior if the inactivity interrupt is enabled.

Register 0x26—TIME_INACT (Read/Write)

The TIME_INACT register contains an unsigned time value representing the amount of time that acceleration must be less than the value in the THRESH_INACT register for inactivity to be detected. The scale factor is 1 sec/LSB. Unlike the other interrupt functions, which use unfiltered output data (see the Threshold Detection and Bandwidth section), the inactivity function uses filtered output data.

At least one output sample must be generated for the inactivity interrupt to be triggered. For this reason, the inactivity function may appear to be unresponsive if the TIME_INACT register is set to a value less than the time constant of the output data rate. A value of 0 results in an interrupt when the output data is less than the value in the THRESH_INACT register. The maximum value for TIME_INACT is 255 sec.

Register 0x27—ACT_INACT_CTL (Read/Write)

D7	D6	D5	D4
ACT AC/DC	ACT_X enable	ACT_Y enable	ACT_Z enable
D3	**D2**	**D1**	**D0**
INACT AC/DC	INACT_X enable	INACT_Y enable	INACT_Z enable

The ACT_INACT_CTL register selects dc-coupled or ac-coupled operation and selects the axes that participate in activity and inactivity detection.

ACT AC/DC and INACT AC/DC Bits

A setting of 0 for the ACT AC/DC and INACT AC/DC bits selects dc-coupled operation; a setting of 1 selects ac-coupled operation. In dc-coupled operation, the current acceleration magnitude is compared directly with the values in the THRESH_ACT and THRESH_INACT registers to determine whether activity or inactivity is detected.

In ac-coupled operation for activity detection, the acceleration value at the start of activity detection is taken as a reference value. New samples of acceleration data are then compared to this reference value and, if the magnitude of the difference exceeds the THRESH_ACT value, an activity interrupt is triggered.

Similarly, in ac-coupled operation for inactivity detection, a reference value is used for comparison and is updated whenever the device exceeds the inactivity threshold. After the reference value is selected, the device compares the magnitude of the difference between the reference value and the current acceleration with the THRESH_INACT value. If the difference is less than the value in the THRESH_INACT register for the time specified in the TIME_INACT register, the device is considered inactive, and the inactivity interrupt is triggered.

ACT_x Enable and INACT_x Enable Bits

A setting of 1 for the ACT_x enable and INACT_x enable bits enables x-, y-, or z-axis participation in detecting activity or inactivity. A setting of 0 excludes the selected axis from participation. If all axes are excluded, the function is disabled. For activity detection, all participating axes are logically OR'ed, causing the activity function to be triggered when any participating axis exceeds the activity threshold. For inactivity detection, all participating axes are logically AND'ed, causing the inactivity function to be triggered only if all participating axes are below the inactivity threshold for the specified time.

Register 0x2A—SHOCK_AXES (Read/Write)

D7	D6	D5	D4
0	0	0	0
D3	**D2**	**D1**	**D0**
Suppress	SHOCK_X enable	SHOCK_Y enable	SHOCK_Z enable

The SHOCK_AXES register specifies the participation of each of the three axes in single shock/double shock detection.

Suppress Bit

Setting the suppress bit suppresses double shock detection if acceleration greater than the value in the THRESH_SHOCK register is present during the latency time between shocks. For more information, see the Shock Detection section.

SHOCK_x Enable Bits

A setting of 1 in the SHOCK_X enable, SHOCK_Y enable, or SHOCK_Z enable bit enables x-, y-, or z-axis participation in shock detection. A setting of 0 excludes the selected axis from participation in shock detection.

Register 0x2B—ACT_SHOCK_STATUS (Read Only)

D7	D6	D5	D4
0	ACT_X source	ACT_Y source	ACT_Z source
D3	**D2**	**D1**	**D0**
Asleep	SHOCK_X source	SHOCK_Y source	SHOCK_Z source

The read-only ACT_SHOCK_STATUS register indicates the first axis involved in an activity or shock event.

ACT_x Source and SHOCK_x Source Bits

The ACT_x source and SHOCK_x source bits indicate the first axis involved in an activity or shock event. A setting of 1 corresponds to involvement in the event; a setting of 0 corresponds to no involvement. When new data is available, these bits are not cleared but are overwritten by the new data. Read the ACT_SHOCK_STATUS register before clearing the interrupt. Disabling an axis from participation in activity or shock events clears the corresponding source bit in this register when the next activity or single shock/double shock event occurs.

Asleep Bit

A setting of 1 in the asleep bit indicates that the part is asleep; a setting of 0 indicates that the part is not asleep. This bit toggles only if the device is configured for autosleep. For more information about the autosleep mode, see the AUTO_SLEEP Bit section.

Register 0x2C—BW_RATE (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	LOW_POWER	Rate			

The BW_RATE register configures the device bandwidth and output data rate; this register also enables and disables low power mode.

LOW_POWER Bit

A setting of 0 in the LOW_POWER bit selects normal operation; a setting of 1 selects reduced power operation, which has somewhat higher noise. For more information, see the Low Power Mode section.

Rate Bits

The rate bits select the device bandwidth and output data rate (see Table 6 and Table 8). The default value for these bits is 0x0A, which translates to a 100 Hz output data rate. The selected output data rate must be appropriate for the communication protocol and frequency selected. Selecting an output data rate that is too high for the communication speed may result in samples being discarded (for more information, see the Serial Communications section).

Register 0x2D—POWER_CTL (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	Link	AUTO_SLEEP	Measure	Sleep	Wakeup	

The POWER_CTL register can be used to configure the device for autosleep mode; this register is also used to set the device to measurement mode or standby mode.

Link Bit

The link bit serially links the activity and inactivity functions. If both the activity and inactivity functions are enabled, a setting of 1 in the link bit delays the start of the activity detection function until inactivity is detected. After activity is detected, inactivity detection begins, preventing the detection of activity. When this bit is set to 0, the inactivity and activity functions are concurrent. For more information about the link feature, see the Link Mode section.

Before clearing the link bit, it is recommended that the part be placed in standby mode (set the measure bit, Bit D3, to 0). After clearing the link bit, reset the part to measurement mode (set the measure bit, Bit D3, to 1). This configuration sequence ensures that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the link bit is cleared may have additional noise, especially if the device is asleep when the bit is cleared.

AUTO_SLEEP Bit

If the link bit is set, a setting of 1 in the AUTO_SLEEP bit enables the autosleep function. In autosleep mode, the ADXL375 automatically switches to sleep mode if the inactivity function is enabled and inactivity is detected (that is, when acceleration is below the THRESH_INACT value for at least the time specified by the TIME_INACT value). If activity detection is also enabled, the ADXL375 automatically wakes up from sleep after detecting activity and returns to operation at the output data rate set in the BW_RATE register. A setting of 0 in the AUTO_SLEEP bit disables automatic switching to sleep mode.

If the link bit is not set, the AUTO_SLEEP feature is disabled and setting the AUTO_SLEEP bit has no effect on device operation. For more information about the link feature, see the Link Bit section and the Link Mode section. For more information about autosleep mode, see the Autosleep Mode section.

Before clearing the AUTO_SLEEP bit, it is recommended that the part be placed in standby mode (set the measure bit, Bit D3, to 0). After clearing the AUTO_SLEEP bit, reset the part to measurement mode (set the measure bit, Bit D3, to 1). This configuration sequence ensures that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the AUTO_SLEEP bit is cleared may have additional noise, especially if the device is asleep when the bit is cleared.

Measure Bit

A setting of 0 in the measure bit places the part into standby mode; a setting of 1 places the part into measurement mode. The ADXL375 powers up in standby mode with minimum power consumption (see the Power Sequencing section).

Sleep Bit

A setting of 0 in the sleep bit places the part into the normal mode of operation; a setting of 1 places the part into sleep mode. Sleep mode suppresses the DATA_READY interrupt, stops transmission of data to the FIFO buffer, and switches the sampling rate to the rate specified by the wakeup bits (Bits[D1:D0]). In sleep mode, only the activity function can be used. When the DATA_READY interrupt is suppressed, the output data registers (Register 0x32 to Register 0x37) are still updated at the sampling rate set by the wakeup bits.

Before clearing the sleep bit, it is recommended that the part be placed in standby mode (set the measure bit, Bit D3, to 0). After clearing the sleep bit, reset the part to measurement mode (set the measure bit, Bit D3, to 1).

Wakeup Bits

The wakeup bits control the sampling rate during sleep mode (see Table 16).

Table 16. Sampling Rate in Sleep Mode

Setting		
D1	**D0**	**Frequency (Hz)**
0	0	8
0	1	4
1	0	2
1	1	1

Register 0x2E—INT_ENABLE (Read/Write)

D7	**D6**	**D5**	**D4**
DATA_READY	SINGLE_SHOCK	DOUBLE_SHOCK	Activity
D3	**D2**	**D1**	**D0**
Inactivity	0	Watermark	Overrun

A setting of 1 for any bit in the INT_ENABLE register enables the specified function to generate interrupts; a setting of 0 for any bit in this register prevents the function from generating interrupts. The DATA_READY, watermark, and overrun bits enable only the interrupt output; the functions are always enabled. It is recommended that interrupts be configured in Register 0x2F before their outputs are enabled in this register. For more information about the interrupts, see the Bits in the Interrupt Registers section.

Register 0x2F—INT_MAP (Read/Write)

D7	**D6**	**D5**	**D4**
DATA_READY	SINGLE_SHOCK	DOUBLE_SHOCK	Activity
D3	**D2**	**D1**	**D0**
Inactivity	0	Watermark	Overrun

A setting of 0 for any bit in the INT_MAP register causes the specified interrupt to be sent to the INT1 pin; a setting of 1 for any bit in this register causes the specified interrupt to be sent to the INT2 pin. All selected interrupts for a given pin are OR'ed.

Register 0x30—INT_SOURCE (Read Only)

D7	**D6**	**D5**	**D4**
DATA_READY	SINGLE_SHOCK	DOUBLE_SHOCK	Activity
D3	**D2**	**D1**	**D0**
Inactivity	X[1]	Watermark	Overrun

[1] X = ignore this bit.

A setting of 1 for any bit in the INT_SOURCE register indicates that the specified function has triggered an interrupt; a setting of 0 for any bit in this register indicates that the specified function has not triggered an interrupt. The DATA_READY, watermark, and overrun bits are always set if the corresponding interrupt occurs, regardless of the settings in the INT_ENABLE register; these bits are cleared by reading data from the data registers (Address 0x32 to Address 0x37). The DATA_READY and watermark bits may require multiple reads to be cleared. Other bits, and their corresponding interrupts, are cleared by reading the INT_SOURCE register.

Register 0x31—DATA_FORMAT (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
SELF_TEST	SPI	INT_INVERT	0	1	Justify	1	1

The DATA_FORMAT register controls the presentation of data to Register 0x32 through Register 0x37.

SELF_TEST Bit

A setting of 1 in the SELF_TEST bit applies a self-test force to the sensor, causing a shift in the output data. A value of 0 disables the self-test force. For more information about the self-test function, see the Self-Test section and the Using Self-Test section.

SPI Bit

A value of 1 in the SPI bit configures the device for 3-wire SPI mode; a value of 0 configures the device for 4-wire SPI mode.

INT_INVERT Bit

A value of 0 in the INT_INVERT bit sets the polarity of the interrupt pins to active high; a value of 1 sets the polarity of the interrupt pins to active low.

Justify Bit

A setting of 1 in the justify bit selects left justified (MSB) mode; a setting of 0 selects right justified (LSB) mode with sign extension.

Register 0x32 to Register 0x37—DATAX0, DATAX1, DATAY0, DATAY1, DATAZ0, DATAZ1 (Read Only)

These six bytes (Register 0x32 to Register 0x37) are each eight bits in length and contain the output data for each axis.

- Register 0x32 and Register 0x33 contain the output data for the x-axis.
- Register 0x34 and Register 0x35 contain the output data for the y-axis.
- Register 0x36 and Register 0x37 contain the output data for the z-axis.

The output data is in twos complement format. DATAx0 is the least significant byte, and DATAx1 is the most significant byte (x represents X, Y, or Z). The DATA_FORMAT register (Address 0x31) controls the format of the data. It is recommended that a multiple-byte read of all six registers be performed to prevent a change in data between reads of sequential registers.

When using the 3200 Hz or 1600 Hz output data rate, the LSB of the output data-word is always 0. When the data is right justified, the LSB corresponds to Bit D0 of the DATAx0 register; when the data is left justified, the LSB corresponds to Bit D3 of the DATAx0 register.

Register 0x38—FIFO_CTL (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
FIFO_MODE		Trigger	Samples				

The FIFO_CTL register is used to configure the FIFO buffer for the device. For more information, see the FIFO Buffer section.

For an in-depth description of the FIFO buffer, see the AN-1025 Application Note, *Utilization of the First In, First Out (FIFO) Buffer in Analog Devices, Inc., Digital Accelerometers*.

FIFO_MODE Bits

These bits set the FIFO mode, as described in Table 17.

Table 17. FIFO Modes

Setting		FIFO	
D7	D6	Mode	Description
0	0	Bypass	FIFO buffer is bypassed.
0	1	FIFO	FIFO buffer collects up to 32 samples and then stops collecting data, collecting new data only when the buffer is not full.
1	0	Stream	FIFO buffer holds the last 32 samples. When the buffer is full, the oldest data is overwritten with newer data.
1	1	Trigger	FIFO buffer holds the last samples before the trigger event and continues to collect data until full. New data is collected only when the buffer is not full.

Trigger Bit

A value of 0 in the trigger bit links the trigger event of trigger mode to the INT1 pin, and a value of 1 links the trigger event to the INT2 pin.

Samples Bits

The function of the samples bits depends on the FIFO mode selected (see Table 18). Entering a value of 0 in the samples bits immediately sets the watermark bit in the INT_SOURCE register, regardless of the FIFO mode selected. Undesirable operation may occur if a value of 0 is used for the samples bits when trigger mode is used.

Table 18. Samples Bits Functions

FIFO Mode	Samples Bits Function
Bypass	None.
FIFO	Specifies how many FIFO entries are needed to trigger a watermark interrupt.
Stream	Specifies how many FIFO entries are needed to trigger a watermark interrupt.
Trigger	Specifies how many FIFO samples are retained in the FIFO buffer before a trigger event.