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High Performance, SPI Digital Output, Angular Rate Sensor

Data Sheet

ADXRS810

FEATURES

Excellent null offset stability over temperature
High vibration rejection over a wide frequency range
2000 *g* powered shock survivability
SPI digital output with 16-bit data-word
Low noise
Continuous self-test
Fail-safe functions
Temperature sensor
3.3 V and 5 V operation
–40°C to +105°C operation
Small, low profile, industry standard SOIC package provides yaw rate (Z-axis) response
Qualified for automotive applications

APPLICATIONS

Car navigation

GENERAL DESCRIPTION

The ADXRS810 is an angular rate sensor (gyroscope) intended for automotive navigation applications. An advanced, differential, quad-sensor design rejects the influence of linear acceleration, enabling the ADXRS810 to operate in exceedingly harsh environments where shock and vibration are present.

The ADXRS810 uses an internal, continuous self-test architecture. The integrity of the electromechanical system is checked by applying a high frequency electrostatic force to the sense structure to generate a rate signal that can be differentiated from the baseband rate data and internally analyzed.

The ADXRS810 is capable of sensing an angular rate of up to ±300°/sec. Angular rate data is presented as a 16-bit word, as part of a 32-bit SPI message.

The ADXRS810 is available in a cavity plastic 16-lead SOIC and is capable of operating across both a wide voltage range (3.3 V to 5 V) and temperature range (−40°C to 105°C).

FUNCTIONAL BLOCK DIAGRAM

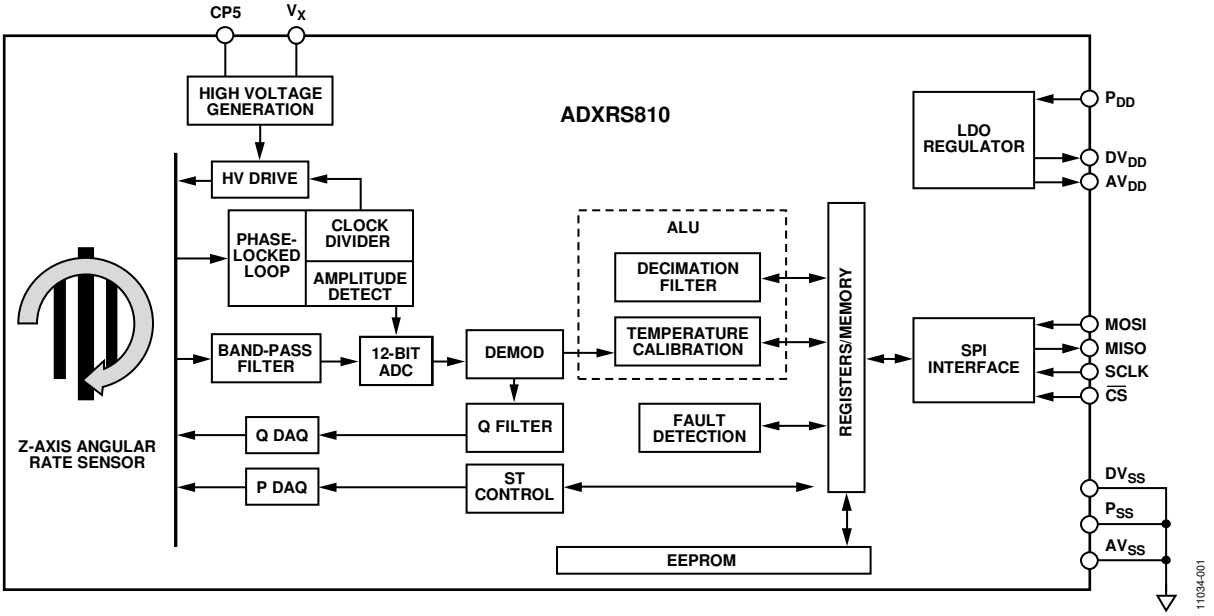

Figure 1.

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- ADXRS810: High Performance, SPI Digital Output, Angular Rate Sensor Data Sheet

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- ADXRS810 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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TABLE OF CONTENTS

REVISION HISTORY

10/12—Revision 0: Initial Version

SPECIFICATIONS

Specification conditions at T_A = 25°C, P_{DD} = 5 V, angular rate = 0°/sec, bandwidth = f_0/200, ±1 *g*, continuous self-test on.

Table 1.

Parameter	Test Conditions/Comments	Symbol	Min	Typ	Max	Unit
MEASUREMENT RANGE	Full-scale range	FSR	±300			°/sec
SENSITIVITY	See Figure 2					
Nominal Sensitivity				80		LSB/°/sec
Sensitivity Tolerance	At 25°C			±1		%
Sensitivity Temperature Drift	From −40°C to +25°C or 25°C to 85°C		−3		+3	%
Nonlinearity[1]	Best fit straight line			0.05		% FSR rms
Cross-Axis Sensitivity[2]				±3		%
NULL						
Null Accuracy	At 25°C			±2		°/sec
Null Temperature Drift	−40°C to +25°C or 25°C to 85°C		−4		+4	°/sec
Overall Null Accuracy[1]	−40°C to +85°C		−8		+8	°/sec
Null Drift Gradient	−40°C to +85°C		−0.1		+0.1	°/s/°C
NOISE PERFORMANCE						
Rate Noise Density	T_A = 25°C			0.015		°/sec/√Hz
	T_A = −40°C to 105°C			0.020		°/sec/√Hz
LOW-PASS FILTER						
Cut-Off (−3 dB) Frequency	f_0/200, see Figure 10	f_{LP}		77.5		Hz
Group Delay[3]	Frequency = 0 Hz	t_{LP}	3.25	4	4.75	ms
SENSOR RESONANT FREQUENCY		f_0	13	15.5	19	kHz
SHOCK AND VIBRATION IMMUNITY						
Sensitivity-to-Linear Acceleration	DC to 5 kHz			0.03		°/sec/*g*
SELF-TEST	See the Continuous Self-Test section					
Magnitude				2559		LSBs
Fault Register Threshold	Compared to LOCST data		2239		2879	LSBs
Sensor Data Status Threshold	Compared to LOCST data		1279		3839	LSBs
Frequency	f_0/32	f_{ST}		485		Hz
ST Low-Pass Filter −3 dB Frequency	f_0/8000			1.95		Hz
ST Low-Pass Filter Group Delay[3]				64		ms
SPI COMMUNICATIONS						
Clock Frequency		f_{OP}			8.08	MHz
Voltage Input High	MOSI, $\overline{CS}$, SCLK	V_{IH}	0.85 × P_{DD}		P_{DD} + 0.3	V
Voltage Input Low	MOSI, $\overline{CS}$, SCLK	V_{IL}	−0.3		P_{DD} × 0.15	V
Output Voltage Low	MISO, current = 3 mA	V_{OL}			0.5	V
Output Voltage High	MISO, current = −2 mA	V_{OH}	P_{DD} − 0.5			V
Input/Output Leakage Current	MISO, MOSI, SCLK, V_{OL} = 0 V	I_{IL}	−0.1		0	µA
	MISO, MOSI, SCLK, V_{OL} = P_{DD}	I_{IH}	0		0.1	µA
Internal Pull-Up Current	$\overline{CS}$, P_{DD} = 3.3 V, $\overline{CS}$ = 0.15 × P_{DD}	I_{PU}		60	200	µA
	$\overline{CS}$, P_{DD} = 5 V, $\overline{CS}$ = 0.15 × P_{DD}			80	300	µA
TEMPERATURE SENSOR						
Value at 45°C				0		LSB
Scale Factor				5		LSB/°C

Parameter	Test Conditions/Comments	Symbol	Min	Typ	Max	Unit
POWER SUPPLY						
Supply Voltage		P_{DD}	3.15		5.25	V
Quiescent Supply Current		I_{DD}		6	10	mA
Turn-On Time	Power on to ½°/sec of final or within 1% of final value (whichever comes first)			100	500	ms
SWITCHING REGULATOR	See the Application Circuit section					
Required CP5 Supply Current		I_{CP5}	0.1		1	mA
Internal Operating Voltage		V_{CP5}	22		25	V
Internal Resistance		R_{on}				
5 V Supply				50		Ω
3.3 V Supply				75		Ω
Required Current	Current requirement for external inductor	I_{typ}				
5 V Supply				35		mA
3.3 V Supply				20		mA
TEMPERATURE RANGE		T_{MIN}, T_{MAX}	−40		+105	°C

[1] Minimum/maximum limit is at least ±4 sigma based on characterization.
[2] Cross-axis sensitivity specification does not include effects due to device mounting on a PCB.
[3] Minimum/maximum limits are guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Acceleration (Any Axis, Unpowered, 0.5 ms)	2000 *g*
Acceleration (Any Axis, Powered, 0.5 ms)	2000 *g*
Supply Voltage (P_{DD})	−0.3 V to +6.0 V
Output Short-Circuit Duration (Any Pin to Common)	Indefinite
Operating Temperature Range	−40°C to +125°C
Storage Temperature	−40°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead SOIC	191.5	25	°C/W

RATE SENSITIVE AXIS

The ADXRS810 is available in a SOIC package. The device transmits a positive-going LSB count for clockwise rotation about the axis normal to the package top. Conversely, a negative-going LSB count is transmitted for counterclockwise rotation about the Z-axis.

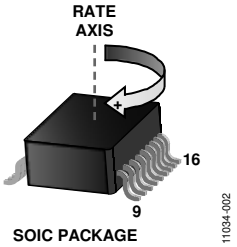

Figure 2. RATEOUT Signal Increases with Clockwise Rotation

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

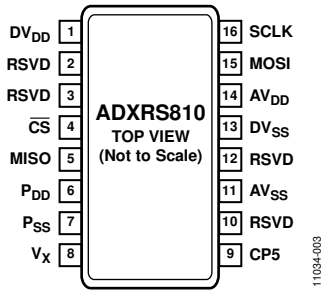

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DV_{DD}	Digital Regulated Voltage Output. See the Application Circuit section.
2, 3, 10, 12	RSVD	Reserved for Analog Devices, Inc., Use Only. Connect to GND.[1]
4	$\overline{CS}$	Chip Select.
5	MISO	Master In/Slave Out.
6	P_{DD}	Supply Voltage.
7	P_{SS}	Switching Regulator Ground (GND).
8	V_X	High Voltage Switching Node. See the Application Circuit section.
9	CP5	High Voltage Supply. See the Application Circuit section.
11	AV_{SS}	Analog Ground (GND).
13	DV_{SS}	Digital Signal Ground (GND).
14	AV_{DD}	Analog Regulated Voltage Output. See the Application Circuit section.
15	MOSI	Master Out/Slave In.
16	SCLK	SPI Clock.

[1] The RSVD pins must be connected to PCB ground. For enhanced product diagnosis, make this connection through a trace and not directly through the package footprint. See the Suggested PCB Layout section for proper connection to the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

N > 1000, unless otherwise noted.

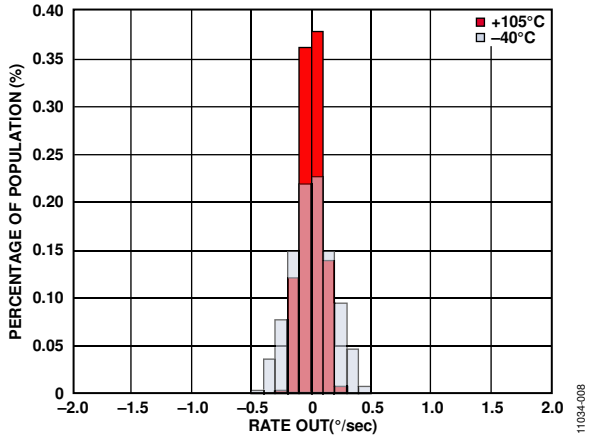

Figure 4. Initial Null Output

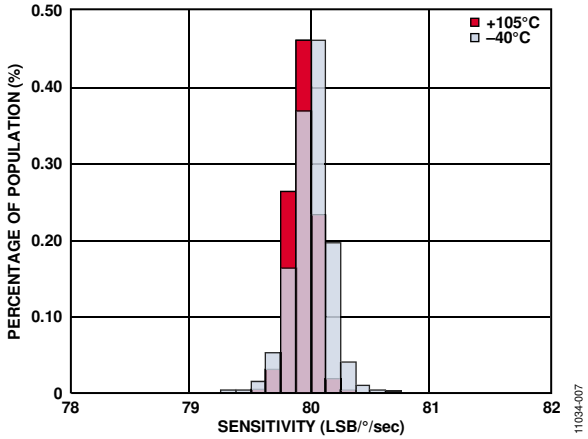

Figure 7. Sensitivity

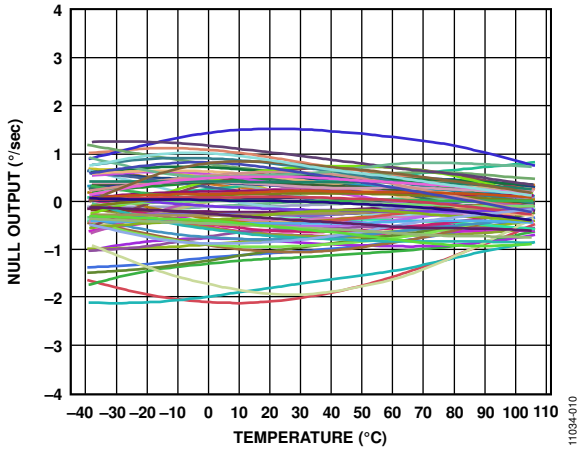

Figure 5. Typical Null Output Response over Temperature (N > 100)

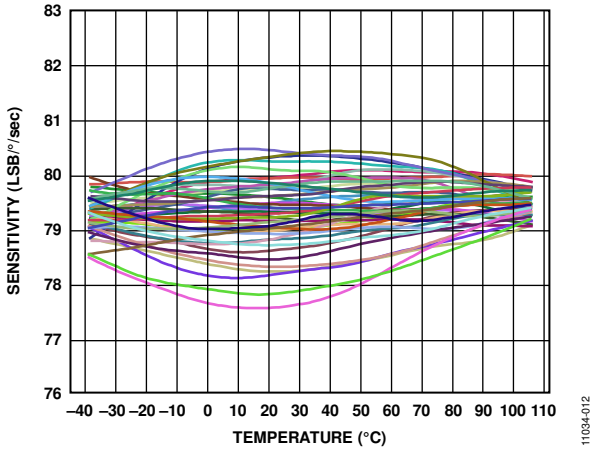

Figure 8. Sensitivity over Temperature (N > 100)

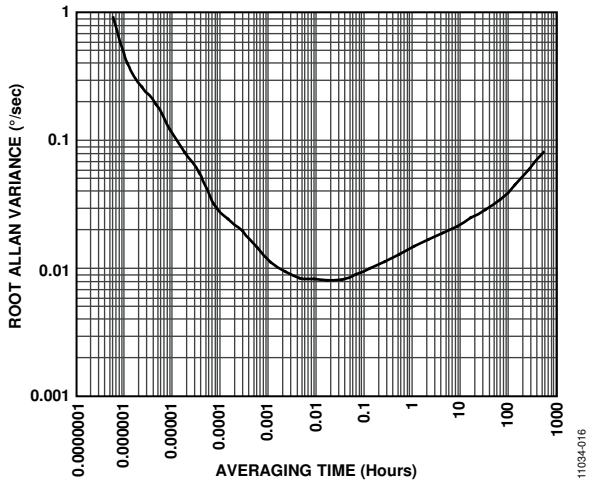

Figure 6. Typical Root Allan Variance at 105°C

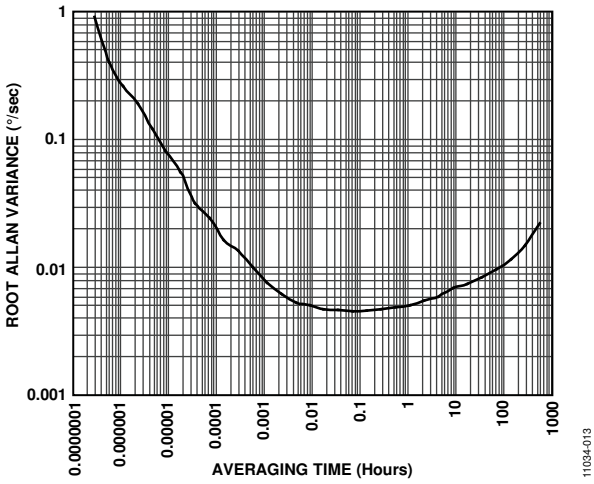

Figure 9. Typical Root Allan Variance at –40°C

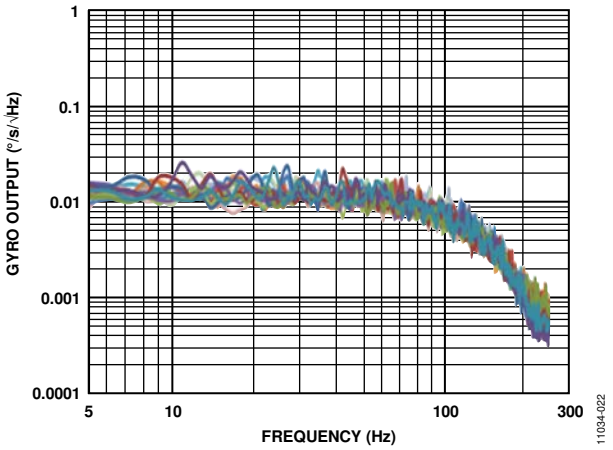

Figure 10. DUT Typical Response to Random Vibration (5 Hz to 5 kHz at 15 g RMS)

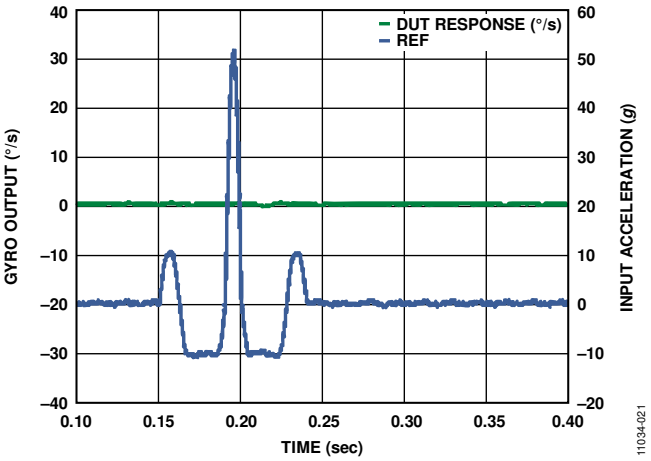

Figure 11. DUT Typical Response to 50 g, 10 ms Half-Sine Shock Test

THEORY OF OPERATION

The ADXRS810 operates on the principle of a resonator gyro. Figure 12 presents a simplified illustration of one of four polysilicon sensing structures. Each sensing structure contains a dither frame that is electrostatically driven to resonance. This produces the necessary velocity element to produce a Coriolis force when experiencing angular rate. The ADXRS810 is designed to sense Z-axis (yaw) angular rate.

When the sensing structure is exposed to angular rate, the resulting Coriolis force is coupled into an outer sense frame, which contains movable fingers that are placed between fixed pickoff fingers. This forms a capacitive pickoff structure that senses Coriolis motion. The resulting signal is fed to a series of gain and demodulation stages that produce the electrical rate signal output. The quad-sensor design rejects linear and angular acceleration, including external *g*-forces and vibration. This is achieved by mechanically coupling the four sensing structures such that external *g*-forces appear as common-mode signals that can be removed by the fully differential architecture implemented in the ADXRS810.

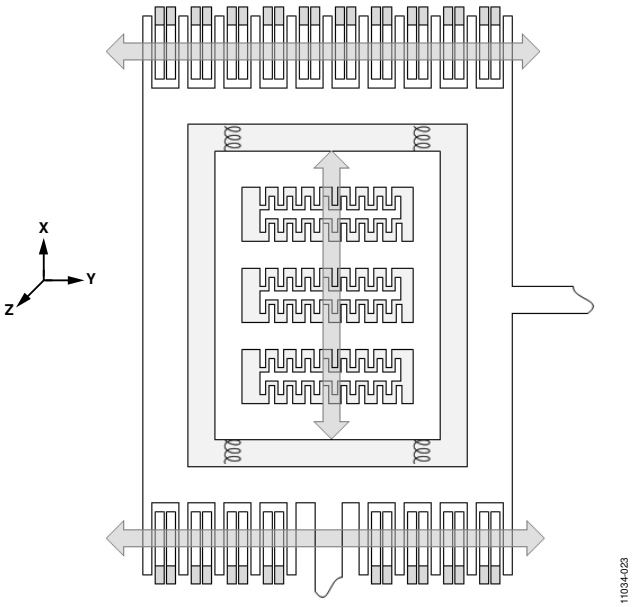

Figure 12. Simplified Gyro Sense Structure

The resonator requires 22.5 V (typical) for operation. Because only 5 V is typically available in most applications, a switching regulator is included on-chip. If an external high voltage supply is available, the inductor and diode can be omitted, and this supply can be connected to CP5. See the Application Circuit section.

CONTINUOUS SELF-TEST

The ADXRS810 gyroscope uses a complete electromechanical self-test. An electrostatic force is applied to the gyroscope frame, resulting in a deflection of the capacitive sense fingers. This deflection is exactly equivalent to deflection that occurs as a result of the external rate input. The output from the beam structure is processed by the same signal chain as a true rate output signal, providing complete coverage of both the electrical and mechanical components.

The electromechanical self-test is performed continuously during operation at a rate higher than the output bandwidth of the device. The self-test routine generates equivalent positive and negative rate deflections. This information can then be filtered such that there is no overall effect on the demodulated rate output.

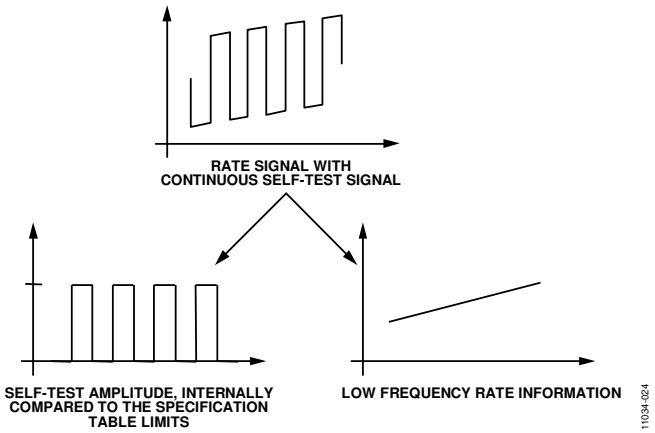

Figure 13. Continuous Self-Test Demodulation

The difference amplitude between the positive and negative self-test deflections is filtered to $f_0/8000$ (~1.95 Hz) and continuously monitored and compared to hardcoded self-test limits. If the measured amplitude exceeds these limits (listed in the Specifications table), one of two error conditions is asserted, depending on the magnitude of self-test error. For less severe self-test error magnitudes, the CST bit of the fault register is asserted; however, the status bits (ST[1:0]) in the sensor data response remain set to 0b01 for valid sensor data. For more severe self-test errors, the CST bit of the fault register is asserted, and the status bits (ST[1:0]) in the sensor data response are set to 0b00 for invalid sensor data. The thresholds for both failure conditions are listed in the Specifications table. The user can access the self-test information by issuing a read command to the self-test memory register (Address 0x04). See the SPI Communication Protocol—Applications section for more information about error reporting.

APPLICATIONS INFORMATION

CALIBRATED PERFORMANCE

Each ADXRS810 gyroscope uses internal EEPROM memory to store its temperature calibration information. The calibration information is encoded into the device during factory testing. The calibration data is used to perform offset, gain, and self-test corrections over temperature. Storing this information internally removes the burden from the customer of performing system level temperature calibration.

MECHANICAL CONSIDERATIONS FOR MOUNTING

Mount the ADXRS810 in a location close to a hard mounting point of the printed circuit board (PCB) to the case. Mounting the ADXRS810 at an unsupported PCB location (that is, at the end of a lever or in the middle of a trampoline), as shown in Figure 14, may result in apparent measurement errors because the gyroscope is subject to the resonant vibration of the PCB. Locating the gyroscope near a hard mounting point helps ensure that any PCB resonances at the gyroscope are above the frequency at which harmful aliasing with the internal electronics can occur. To ensure that aliased signals do not couple into the baseband measurement range, it is recommended that the module be designed such that the first system level resonance occurs at a frequency higher than 800 Hz.

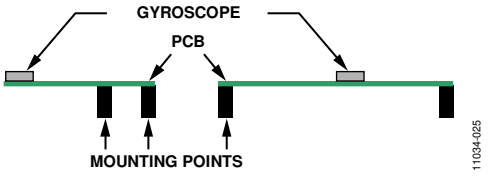

Figure 14. Where Not to Mount a Gyroscope

APPLICATION CIRCUIT

Figure 15 and Figure 16 show the recommended application circuits for the ADXRS810 gyroscope. These application circuits provide a connection reference for the SOIC package. Note that DV_{DD}, AV_{DD}, and P_{DD} are all individually connected to ground through 1 µF capacitors. Do not connect these supplies together. Additionally, an external diode and inductor must be connected for proper operation of the internal shunt regulator. These components allow for the internal resonator drive voltage to reach its required level, as listed in the Specifications table.

Figure 16 presents an alternate method of operation for the ADXRS810 gyroscope. If the user has access to a power source that is capable of supplying a current of between 0.1 mA and 1 mA to the CP5 pin, this alternate source can be used to drive the internal regulator. In this application circuit, the external diode and inductor can be omitted and V_X left as a no connect.

The required supply current to the CP5 pin can be met in one of two ways. Either a current source can be connected to CP5, such that the stated current requirement is satisfied, or a high voltage supply can be connected to CP5 through a resistor. For both methods, take precautions such that variations to the supply do not result in the current exceeding the 0.1 mA to 1 mA limits. See the Specifications table for a complete description of the parameters related to the shunt regulator.

Table 5.

Component	Qty	Description
Inductor	1	470 µH (560 µH)
Diode	1	>24 V breakdown voltage
Capacitor	3	1 µF
Capacitor	1	100 nF

Note the following schematic recommendations:

- Leakage current on the CP5 pin should be kept to a minimum. All sources of leakage, including reverse leakage current through the diode and PCB surface leakage, should account for not more than 70 µA. For most applications, the diode is the primary source of leakage current.
- Applications that operate at 3.3 V should use an inductor value of 560 µH to ensure proper operation of the internal boost regulator. For all applications, the inductor must be capable for 50 mA of peak current.

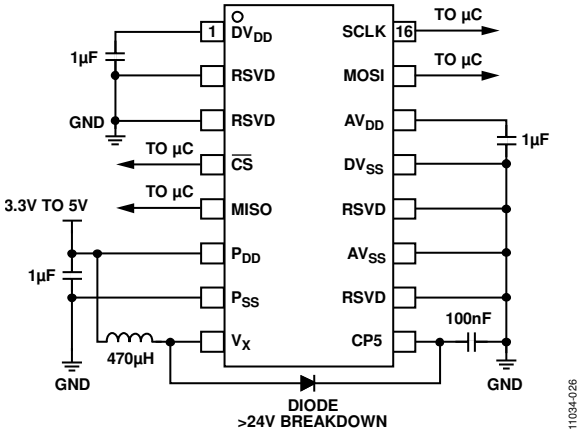

Figure 15. Recommended ADXRS810 Application Circuit

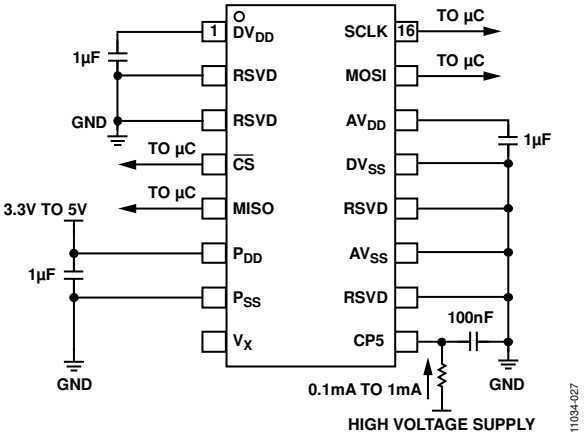

Figure 16. ADXRS810 Alternate Application Circuit

ADXRS810 SIGNAL CHAIN TIMING

The ADXRS810 primary signal chain is in Figure 17. It is the series of necessary functional circuit blocks through which the rate data is generated and processed. This sequence of electromechanical elements determines how quickly the device is capable of translating an external rate input stimulus into an SPI word to be sent to the master device. The group delay, which is a function of the filter characteristic, is the time required for the output of the low-pass filter to be within 10% of the external rate input and is seen to be ~4 ms. Additional delay can be observed due to the timing of SPI transactions and the population of the rate data into the internal device registers. This delay is broken down in Figure 17 such that the delay through each element of the signal chain is presented.

The transfer function for the rate data low-pass filter (LPF) is given as

$$\left[\frac{1-Z^{-64}}{1-Z^{-1}}\right]^2$$

where:

$$T=\frac{1}{f_0}=\frac{1}{15.2\text{ kHz (typ)}}$$

And the transfer function for the continuous self-test LPF is given as

$$\frac{1}{64-63\,Z^{-1}}$$

where:

$$T=\frac{16}{f_0}=\frac{16}{15.2\text{ kHz}}\text{(typ)}$$

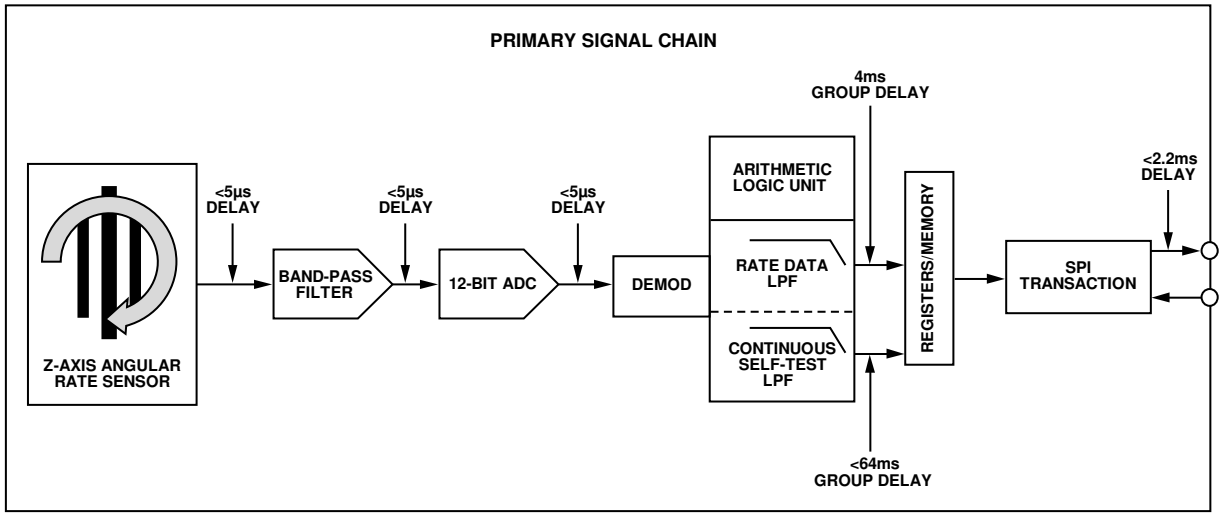

Figure 17. ADXRS810 Primary Signal Chain and Associated Delays

SPI COMMUNICATIONS CHARACTERISTICS

The following conditions apply to the SPI command and response timing characteristics in Table 6:

- All timing parameters are guaranteed through characterization.
- All timing is shown with respect to 10% of P_{DD} and 90% of the actual delivered voltage waveform.
- Parameters are valid for 3.0 V ≤ P_{DD} ≤ 5.5 V.
- Capacitive load for all signals is assumed to be ≤80 pF.
- Ambient temperature is −40°C ≤ T_A ≤ +105°C.
- The MISO pull-up load is 47 kΩ or 110 µA.

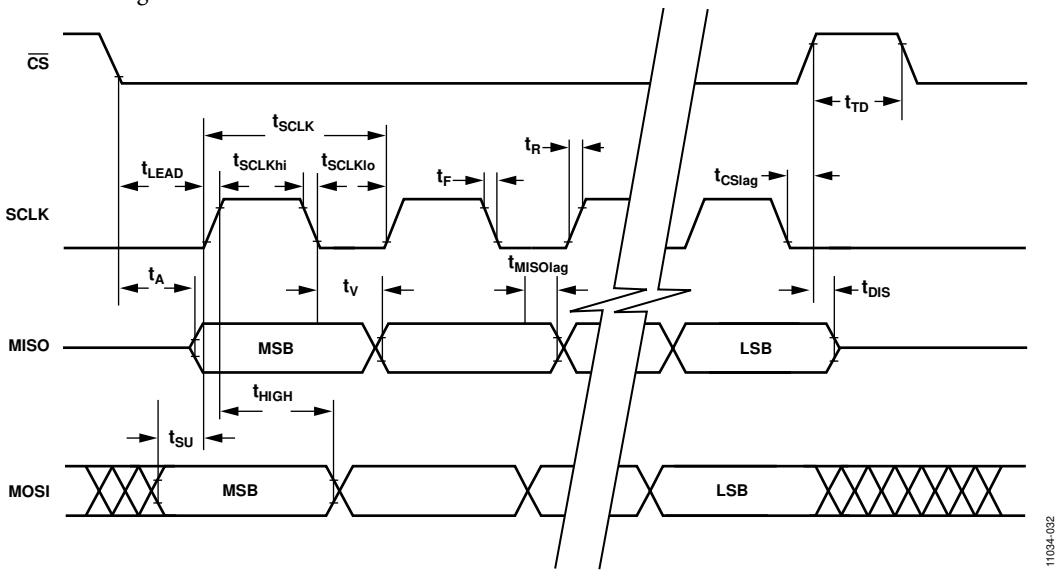

Figure 18. SPI Timings Drawing

Table 6. SPI Command/Response Timing Characteristics

Symbol	Function	Min	Max	Unit
f_{OP}	SPI operating frequency		8.08	MHz
$t_{SCLKLhi}$	Clock (SCLK) high time	½ t_{SCLK} − 13		ns
t_{SCLKlo}	Clock (SCLK) low time	½ t_{SCLK} − 13		ns
t_{SCLK}	SCLK period	123.7		ns
t_F	Clock (SCLK) fall time	5.5	13	ns
t_R	Clock (SCLK) rise time	5.5	13	ns
t_{SU}	Data input (MOSI) setup time	37		ns
t_{HIGH}	Data input (MOSI) hold time	49		ns
t_A	Data output (MISO) access time		20	ns
t_V	Data output (MISO) valid after SCLK		32.5	ns
$t_{MISOlag}$	Data output (MISO) lag time	0		ns
t_{DIS}	Data output (MISO) disable time		40	ns
t_{LEAD}	Enable ($\overline{CS}$) lead time	½ t_{SCLK}		ns
t_{CSlag}	Enable ($\overline{CS}$) lag time	½ t_{SCLK}		ns
t_{TD}	Sequential transfer delay	0.1		µs

SPI COMMUNICATION PROTOCOL—APPLICATIONS

DEVICE DATA LATCHING

To allow for rapid acquisition of data from the ADXRS810, device data latching is implemented as shown in Figure 19. Upon assertion of chip select, the data in the device is latched into memory. When the full MOSI command is received, and chip select deasserted, the appropriate data is shifted into the SPI port registers in preparation for the next sequential command/response exchange. This allows for an exceedingly fast sequential transfer delay of 0.1 µs (see Table 6). As a design precaution, it should be noted that the transmitted data is only as recent as the sequential transmission delay implemented by the system. Conditions that result in a sequential transfer delay of several seconds cause the next sequential device response to contain data that is several seconds old.

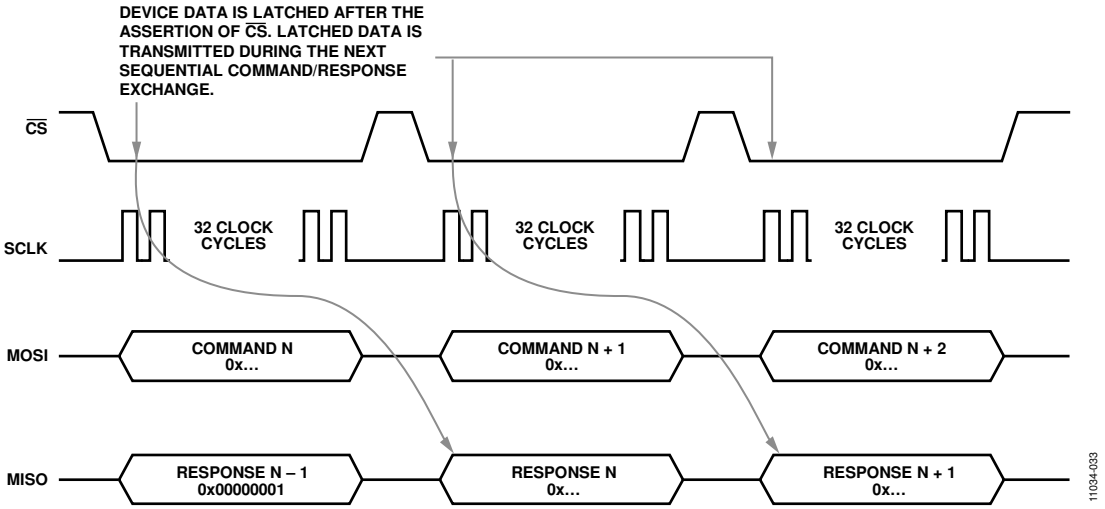

Figure 19. Device Data Latching

COMMAND/RESPONSE

Input/output is handled through a 32-bit command/response SPI interface. The command/response SPI interface is structured such that the response to a command is issued during the next sequential SPI exchange. As shown in Figure 20, the response (Response N) to a specific command (Command N) is issued upon receipt of the next command (Command N + 1).

For the ADXRS810, the clock phase = clock polarity = 0. Additionally, the device response to the initial command is 0x00000001. This prevents the transmission of random data to the master device upon the initial command/response exchange.

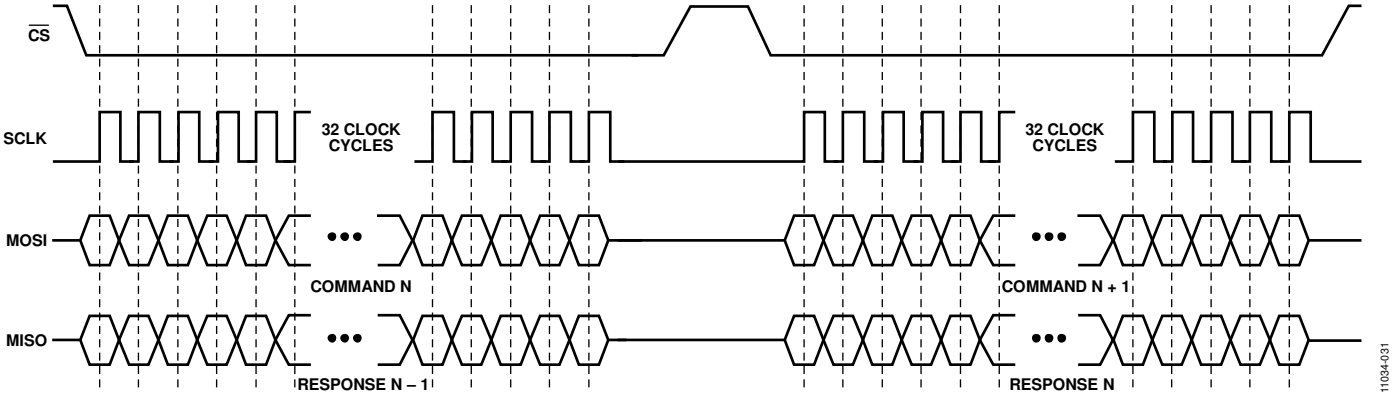

Figure 20. SPI Protocol

SPI COMMUNICATION PROTOCOL—BIT DEFINITIONS

Table 7. SPI Signals

Signal	Symbol	Description
Serial Clock	SCLK	Exactly 32 clock cycles when $\overline{CS}$ is active
Chip Select	$\overline{CS}$	Active low
Master Out/Slave In	MOSI	Data sent to the gyro device from the main controller
Master In/Slave Out	MISO	Data sent to the main controller from the gyro

Table 8. SPI Commands

	Bit																															
Command	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Sensor Data	SQ1	SQ0	1	SQ2																											CHK	P
Read	1	0	0	SM2	SM1	SM0	A8	A7	A6	A5	A4	A3	A2	A1	A0																	P
Write	0	1	0	SM2	SM1	SM0	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

Table 9. SPI Responses

	Bit																															
Command	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Sensor Data	SQ2	SQ1	SQ0	P0	ST1	ST0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			PLL	Q	NVM	POR	PWR	CST	CHK	P1
Read	0	1	0	P0	1	1	1	0	SM2	SM1	SM0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0					P1
Write	0	0	1	P0	1	1	1	0	SM2	SM1	SM0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0					P1
R/W Error	0	0	0	P0	1	1	1	0	SM2	SM1	SM0	0	0	SPI	RE	DU									PLL	Q	NVM	POR	PWR	CST	CHK	P1

COMMAND/RESPONSE BIT DESCRIPTIONS

Table 10. Quick Guide—Bit Definitions for the SPI Interface

Bit	Description
[SQ2:SQ0]	Sequence bits (from master)
[A8:A0]	Register address
[D15:D0]	Data
P	Command odd parity
SPI	SPI command/response
RE	Request error
[SM2:SM0]	Sensor module bits (from master)
DU	Data unavailable
[ST1:ST0]	Status bits
P0	Response, odd parity, Bits[31:16]
P1	Response, odd parity, Bits[31:0]

SQ2:SQ0

This field provides the system with a means of synchronizing the data samples received from multiple sensors. To facilitate correct synchronization, the ADXRS810 gyroscope includes the SQ[2:0] field in the response as it was received in the request.

SM2:SM0

Sensor module bits from the master device. These bits are not implemented in the ADXRS810 but are hardcoded to 000 for all occurrences.

A8:A0

These bits represent the memory address from which device data is read or to which information is written. These bits should be supplied by the master only when the memory registers are being accessed and are ignored for all sensor data requests. See the Memory Register Definitions section for a complete description of the available memory registers.

D15:D0

These 16 bits of device data can contain any of the following:

- Master: data to be written to a memory register as specified in A8:A0.
- Slave: sensor rate output data.
- Slave: device data read from the memory register specified in A8:A0, as well as data from the next sequential register.
- Slave: for a write command, the 16-bit data that is written to the specified memory register is reflected back to the master device for correlation.

SPI

The SPI bit is set when any of the following occurs:

- Too many/too few bits are transmitted
- A message from the control module contains a parity error

The occurrence of a SPI error results in the device issuing a R/W error response (see Table 9), regardless of the SPI command type (see Table 8) issued by the master device.

ST1:ST0

The ST1 and ST0 status bits are used to signal to the master device the type of data contained in the response message. The status bits are decoded as shown in Table 11.

Table 11.

ST[1:0]	Content in Bits[D15:D0]
00	Error data for sensor data response
01	Valid sensor data
10	Sensor self-test data
11	Read/write response

There are two independent conditions that can result in the ST bits being set to 0b00 during a sensor data response.

- The self-test response is sufficiently different from its nominal value. See the Specifications table for the appropriate limits.
- A PLL fault is active.

P

Parity bit required for all master-to-slave data transmissions. Communications protocol requires one parity bit to achieve odd parity for the entire 32-bit command. Bits that are in don't care positions are still factored into the parity calculation.

P0

Parity bit that establishes odd parity for Bits[31:16] of the device response.

P1

Parity bit that establishes odd parity for the entire 32-bit device response.

RE

Communications error bit transmitted from the ADXRS810 device to the control module. Request errors can occur when

- An invalid command is sent from the control module
- A read/write command specifies an invalid memory register
- A write command attempted to write to a nonwritable memory register

DU

Once the chip select pin ($\overline{CS}$) is deasserted, wait 0.1 µs before reasserting the chip select pin ($\overline{CS}$) and initiating another command/response frame with the device. Failure to adhere to this timing specification may result in a data unavailable (DU) error.

ADXRS810 FAULT REGISTER BIT DEFINITIONS

Table 12 describes the bits available for signaling faults to the user.

Table 12. Quick Guide—Fault Register Bit Definitions

Bit	Description
PLL	PLL failure
Q	Quadrature error
NVM	NVM memory fault
POR	Power-on/reset failed to initialize
UV	Regulator undervoltage
AMP	Amplitude detection failure
PWR	Power regulation failed: overvoltage/undervoltage
CST	Continuous self-test failure
CHK	Check; generate faults
OV	Regulator overvoltage
FAIL	Failure that sets the ST[1:0] bits to 0b00

The individual bits of the fault register are updated asynchronously, depending on their respective detection criteria; however, it is recommended that the fault register be read at a rate of at least 100 Hz. Once asserted, individual status bits are not deasserted until they are read by the master device. If the error persists after a fault register read, the status bit immediately reasserts and remains asserted until the next sequential command/response exchange. The FAULT0 register is appended to every sensor data request. The remaining fault information can be accessed by issuing a read command to Address 0x0A.

PLL

This bit indicates that the device had a failure in the phase lock loop functional circuit block, which occurs when the PLL fails to achieve sync with the resonator structure. If the PLL status flag is active, the ST bits of the sensor data response are set to 0b00, indicating that the response contains potentially invalid rate data.

Q

A Q fault can be asserted based on two independent quadrature calculations. Located in the QUAD1 memory register (Address 0x08) is a value corresponding to the total instantaneous quadrature present in the device. If this value exceeds 4096 LSBs, a Q fault is issued. Separately, an internal quadrature accumulator records the amount of quadrature correction performed by the ADXRS810. A Q fault is issued after the quadrature error present in the device contributes to an equivalent of 4°/sec (typical) of rate offset.

NVM

An NVM error is transmitted to the control module if the internal NVM data fails a checksum calculation. This check is performed once every 50 µs and does not include the PID memory register.

POR

An internal check is performed on device startup to ensure that the volatile memory of the device is functional. This is accomplished by programming a known value from the device's ROM into a volatile memory register. This value is continuously compared to the known value in ROM every 1 µs for the duration of the device operation. If the value stored in the volatile memory changes, or does not match the value stored in ROM, the POR error flag is asserted. The value stored in ROM is rewritten to the volatile memory upon a device power cycle.

PWR

The device performs a continuous check of the internal 3 V regulated voltage level. If either an overvoltage (OV) or undervoltage (UV) fault is asserted, the PWR bit is asserted as well. These conditions occur when the regulated voltage is observed to be either more than 3.3 V or less than 2.77 V. An internal low-pass filter removes high frequency glitching effects so that the PWR bit is not asserted unnecessarily. To determine if the fault is a result of an overvoltage or undervoltage condition, the OV and UV fault bits must be analyzed.

CST

The ADXRS810 is designed with continuous self-test functionality. Measured self-test amplitudes are compared against the limits presented in the Specifications table. Deviation from this value results in a reported self-test error. There are two thresholds for a self-test failure.

- A self-test value > ±320 LSBs from nominal results in an assertion of the self-test flag in the fault register.
- A self-test value > ±1280 LSBs from nominal results in both an assertion of the self-test flag in the fault register and setting of the ST[1:0] bits to 0b00, indicating that the rate data contained in the sensor data response is potentially invalid.

CHK

The CHK bit is transmitted by the control module to the ADXRS810 as a method of generating faults. By asserting the CHK bit, the device creates conditions that result in the generation of all faults represented through the fault register. For example, the self-test amplitude is deliberately altered so that it exceeds the fault detection threshold, resulting in a self-test error. In this way, the device is capable of checking both its ability to detect a fault condition and its ability to report that fault to the control module.

The fault conditions are initiated nearly simultaneously; however, the timing for receiving fault codes when the CHK bit is asserted is dependent upon the time required to generate each unique fault. It takes not more than 50 ms for all of the internal faults to be generated and the fault register to be updated to reflect the condition of the device. Until the CHK bit is cleared, the ST[1:0] status bits are set to 0b10, indicating that the data should be interpreted by the control module as self-test data. After the CHK bit is deasserted, the fault conditions require an additional 50 ms to decay and the device to return to normal operation. See Figure 21 for the proper methodology for asserting the CHK bit.

OV

The OV fault bit asserts when the internally regulated voltage (nominally 3 V) is observed to exceed 3.3 V. This measurement is low pass filtered to prevent artifacts such as noise spikes from asserting a fault condition. When an OV fault occurs, the PWR fault bit is asserted simultaneously. Because the OV fault bit is not transmitted as part of a sensor data request, it is recommended that the user read back the FAULT1 and FAULT0 memory registers upon the assertion of a PWR error. This allows the user to determine the specific error condition.

UV

The UV fault bit asserts when the internally regulated voltage (nominally 3 V) is observed to be less than 2.77 V. This measurement is low pass filtered to prevent artifacts such as noise spikes from asserting a fault condition. When a UV fault occurs, the PWR fault bit is asserted simultaneously. Because the UV fault bit is not transmitted as part of a sensor data request, it is recommended that the user read back the FAULT1 and FAULT0 memory registers upon the assertion of a PWR error. This allows the user to determine the specific error condition.

FAIL

The fail flag is asserted when a condition arises such that the ST[0:1] bits are set to 0b00. This indicates that the device has experienced a gross failure and that the sensor data could potentially be invalid.

AMP

The AMP fault bit is asserted when the measured amplitude of the silicon resonator has been significantly reduced. This condition can occur if the voltage supplied to CP5 has fallen below the requirements of the internal voltage regulator. This fault bit is OR'ed with the CST fault such that during a sensor data request the CST bit position represents either an AMP failure or a CST failure. The full fault status register, FAULT0, can then be read from memory to validate the specific failure.

CHK BIT ASSERTION: RECOMMENDED START-UP ROUTINE

Figure 21 illustrates a recommended start-up routine that can be implemented by the user. Alternate start-up sequences can be employed; however, take care that the response from the ADXRS810 is handled correctly. If implemented immediately after power is applied to the device, the total time to implement the following fault detection routine is approximately 200 ms. As described in the Device Data Latching section, the data present in the device upon the assertion of the $\overline{CS}$ signal is used in the next sequential command/response exchange. This results in an apparent one transaction delay before the data resulting from the assertion of the CHK bit is reported by the device. For all other read/write interactions with the device, no such delay exists, and the MOSI command is serviced during the next sequential command/ response exchange. Note that when the CHK bit is deasserted, if the user tries to obtain data from the device before the CST fault flag has cleared, the device reports the data as error data.

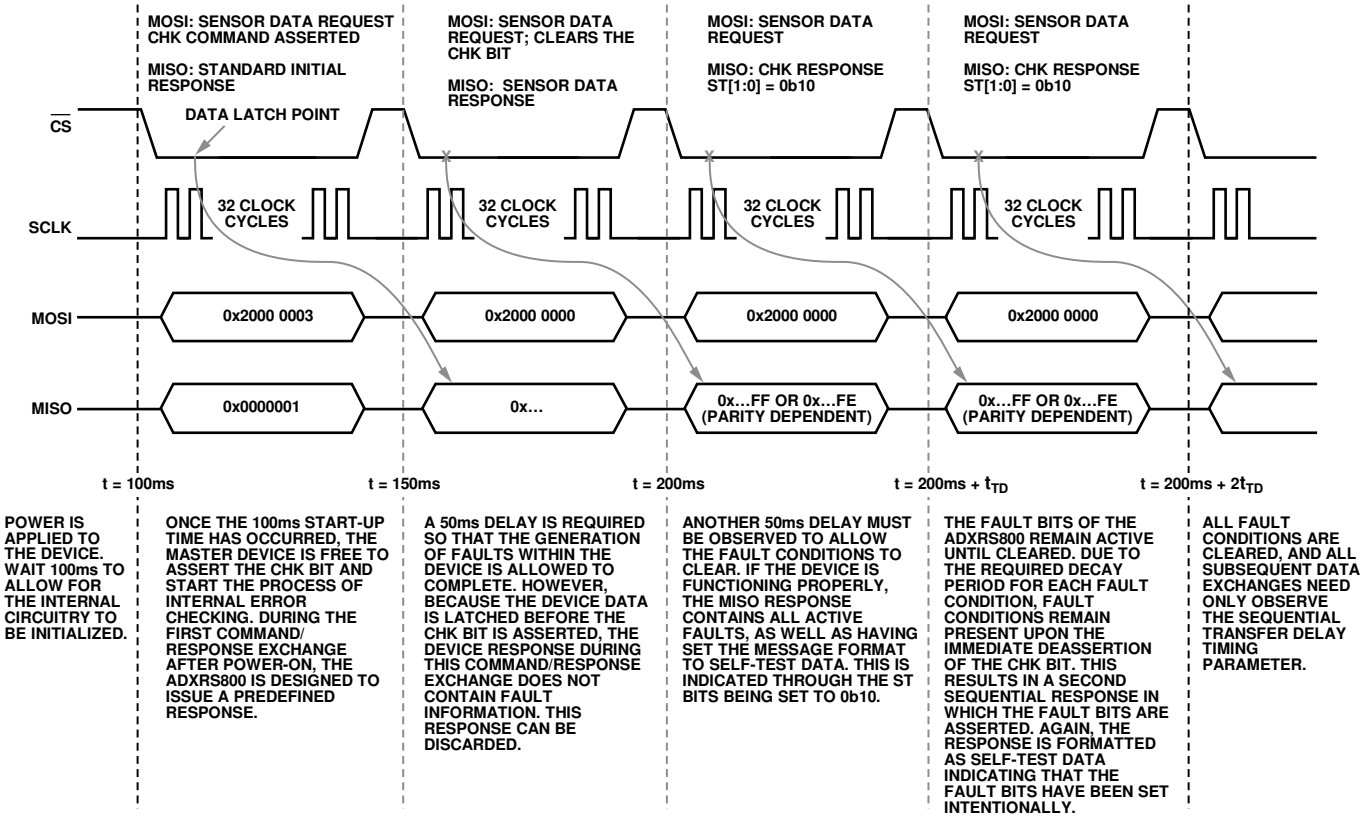

Figure 21. Recommended Start-Up Sequence

SPI RATE DATA FORMAT

The ADXRS810 gyroscope transmits rate data in a 16-bit format as part of a 32-bit SPI data frame. See Table 9 for the full 32-bit format of the sensor data request response. The rate data is transmitted MSB first, from D15 to D0. The data is formatted as a twos complement number, with a scale factor of 80 LSBs/°/sec. Therefore, the highest obtainable value for positive (clockwise) rotation is 0x7FFF (decimal +32,767) and for counterclockwise rotation is 0x8000 (decimal −32,768). Performance of the device is not guaranteed above ±24,000 LSBs (±300°/sec).

Table 13. ADXRS810 Rate Data Table

14-Bit Rate Data			
Decimal (LSBs)	**Hex (D15:D0)**	**Data Type**	**Description**
32,767	0x7FFF	Rate data (not guaranteed)	Maximum possible positive data value
…	…	…	…
24,000	0x5DC0	Rate data	300°/sec rotation (positive FSR)
…	…	…	…
10,000	0x2710	Rate data	125°/sec rotation
…	…	…	…
1000	0x03E8	Rate data	12.5°/sec rotation
…	…	…	…
100	0x0064	Rate data	1.25°/sec rotation
…	…	…	…
12	0x000C	Rate data	0.15°/sec rotation
11	0x000B	Rate data	0.1375°/sec rotation
10	0x000A	Rate data	0.125°/sec rotation
…	…	…	…
3	0x0003	Rate data	0.015°/sec rotation
2	0x0002	Rate data	0.01375°/sec rotation
1	0x0001	Rate data	0.0125°/sec rotation
0	0x0000	Rate data	0 rotation value
−1	0xFFFF	Rate data	−0.0125°/sec rotation
−2	0xFFFE	Rate data	−0.01375°/sec rotation
−3	0xFFFD	Rate data	−0.015°/sec rotation
…	…	…	…
−10	0xFFF6	Rate data	−0.125°/sec rotation
−11	0xFFF5	Rate data	−0.1375°/sec rotation
−12	0xFFF4	Rate data	−0.15°/sec rotation
…	…	…	…
−100	0xFF9C	Rate data	−1.25°/sec rotation
…	…	…	…
−1000	0xFC18	Rate data	−12.5°/sec rotation
…	…	…	…
−10, 000	0xD8F0	Rate data	−125°/sec rotation
…	…	…	…
−24,000	0xA240	Rate data	−300°/sec rotation (negative FSR)
…	…	…	…
−32,768	0x8000	Rate data (not guaranteed)	Maximum possible negative data value

ADXRS810 MEMORY MAP

Table 14 contains a list of the memory registers that are available to be read by the user. See the Command/Response section for the proper input sequence to read a specific memory register. Each memory register comprises eight bits of data; however, when a read request is performed, the data is always returned as a 16-bit message. This is accomplished by appending the data from the next sequential register to the memory address that is specified. Data is transmitted MSB first. For proper acquisition of data from the memory register, the read request should be made to the even numbered register address only. The memory map registers are described in the Memory Register Definitions section.

Table 14. ADXRS810 Memory Map[1]

Addr	Name	MSB							LSB
0x00	RATE1	RTE15	RTE14	RTE13	RTE12	RTE11	RTE10	RTE9	RTE8
0x01	RATE0	RTE7	RTE6	RTE5	RTE4	RTE3	RTE2	RTE1	RTE0
0x02	TEM1	TEM9	TEM8	TEM7	TEM6	TEM5	TEM4	TEM3	TEM2
0x03	TEM0	TEM1	TEM0	X	X	X	X	X	X
0x04	LOCST1	LCST15	LCST14	LCST13	LCST12	LCST11	LCST10	LCST9	LCST8
0x05	LOCST0	LCST7	LCST6	LCST5	LCST4	LCST3	LCST2	LCST1	LCST0
0x06	HICST1	HCST15	HCST14	HCST13	HCST12	HCST11	HCST10	HCST9	HCST8
0x07	HICST0	HCST7	HCST6	HCST5	HCST4	HCST3	HCST2	HCST1	HCST0
0x08	QUAD1	QAD15	QAD14	QAD13	QAD12	QAD11	QAD10	QAD9	QAD8
0x09	QUAD0	QAD7	QAD6	QAD5	QAD4	QAD3	QAD2	QAD1	QAD0
0x0A	FAULT1	X	X	X	X	FAIL	AMP	OV	UV
0x0B	FAULT0	PLL	Q	NVM	POR	PWR	CST	CHK	0
0x0C	PID1	PIDB15	PIDB14	PIDB13	PIDB12	PIDB11	PIDB10	PIDB9	PIDB8
0x0D	PID0	PIDB7	PIDB6	PIDB5	PIDB4	PIDB3	PIDB2	PIDB1	PIDB0
0x0E	SN3	SNB31	SNB30	SNB29	SNB28	SNB27	SNB26	SNB25	SNB24
0x0F	SN2	SNB23	SNB22	SNB21	SNB20	SNB19	SNB18	SNB17	SNB16
0x10	SN1	SNB15	SNB14	SNB13	SNB12	SNB11	SNB10	SNB9	SNB8
0x11	SN0	SNB7	SNB6	SNB5	SNB4	SNB3	SNB2	SNB1	SNB0

[1] X = don't care.

MEMORY REGISTER DEFINITIONS

The SPI-accessible memory registers are described in this section. As described in the previous section, when requesting data from a memory register, only the first sequential memory address need be addressed. The data returned by the device contains 16 bits of memory register information. Bits[15:8] contain the MSB of the requested information, and Bits[7:0] contain the LSB.

In each of the following register sections, the update rate and scale factors are called out for convenience.

0x00 RATE1, 0x01 RATE0

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Register Update Rate: $f_0/32$ (~485 Hz)
Scale Factor: 80 LSBs/°/sec

The rate registers contain the temperature compensated rate output of the device filtered to $f_0/200$ (~77.5Hz). This data can also be accessed by issuing a sensor data read request to the device. The data is presented as a 16-bit, twos complement number.

0x02 TEM1, 0x03 TEM0

MSB[1]							LSB
D9	D8	D7	D6	D5	D4	D3	D2
D1	D0	X	X	X	X	X	X

[1] X = don't care.

Register Update Rate: $f_0/32$ (~485 Hz)
Scale Factor: 5 LSBs/°C

The TEMx registers contain a value corresponding to the temperature of the device. The data is presented as a 10-bit, twos complement number. 0 LSBs corresponds to a temperature of approximately 45°C.

Table 15.

Temperature	Value of TEM1:TEM0[1]
45°C	0000 0000 00XX XXXX
85°C	0011 0010 00XX XXXX
0°C	1100 0111 11XX XXXX

[1] X = don't care.

0x04 LOCST1, 0x05 LOCST0

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Register Update Rate: $f_0/16$ (~970 Hz)
Scale Factor: 80 LSBs/°/sec

The LOCSTx memory registers contain the value of the temperature compensated and low pass filtered continuous self-test delta. This value is a measure of the difference between the positive and negative self-test deflections and corresponds to the values presented in the Specifications table. The device issues a CST error when the value of the self-test exceeds the established self-test limits. The self-test data is filtered to $f_0/8000$ (~1.95 Hz) to prevent false triggering of the CST fault bit. The data is presented as a 16-bit, twos complement number, with a scale factor of 80 LSBs/°/sec.

0x06 HICST1, 0x07 HICST0

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Register Update Rate: $f_0/16$ (~970 Hz)
Scale Factor: 80 LSBs/°/sec

The HICSTx registers contain the unfiltered self-test information. The HICSTx data can be used to supplement fault diagnosis in safety critical applications as sudden shifts in the self-test response are detected. However, the CST bit of the fault register is not set when the HICSTx data is observed to exceed the self-test limits. Only the LOCSTx memory register, which is designed to filter noise and the effects of sudden, temporary self-test spiking due to external disturbances, controls the assertion of the CST fault bit. The data is presented as a 16-bit, twos complement number.

0x08 QUAD1, 0x09 QUAD0

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Register Update Rate: $f_0/64$ (~240 Hz)
Scale Factor: 80 LSBs/°/sec equivalent

The QUADx memory registers contain a value corresponding to the amount of quadrature error present in the device at a given time. Quadrature can be likened to a measurement of the error of the motion of the resonator structure and can be caused by stresses and aging effects. The quadrature data is filtered to $f_0/200$ (~77.5Hz) and can be read frequently to detect sudden shifts in the level of quadrature. The data is presented as a 16-bit, twos complement number.

0x0A FAULT1, 0x0B FAULT0

MSB[1]							LSB
X	X	X	X	FAIL	AMP	OV	UV
PLL	Q	NVM	POR	PWR	CST	CHK	0

[1] X = don't care.

Register Update Rate: N/A
Scale Factor: N/A

The FAULTx registers contain the state of the error flags in the device. The FAULT0 register is appended to the end of every device data transmission (see Table 12); however, this register can also be accessed independently through its memory location. The individual fault bits are updated asynchronously, requiring <5 µs to activate, once the fault condition exists on-chip. Once toggled, each fault bit remains active until the fault register is read or a sensor data command is received. If the fault is still active after the bit is read, the fault bit immediately reasserts itself.

0X0C PID1, 0X0D PID0

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Register Update Rate: N/A
Scale Factor: N/A

The PIDx (part ID) registers contain a 16-bit number identifying the version of the ADXRS810. Combined with the serial number, this information allows for a higher degree of device individualization and tracking. The initial product ID is 0x5201. 0x52 can be interpreted as the ASCII value for the R character, with 0x01 signifying the first revision. Subsequent versions of silicon can increment this value to R02 (0x5202), R03 (0x5203), and so on.

0x0E SN3, 0x0F SN2, 0x10 SN1, 0x11 SN0

MSB							LSB
D31	D30	D29	D28	D27	D26	D25	D24
D23	D22	D21	D20	D19	D18	D17	D16
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Register Update Rate: N/A
Scale Factor: N/A

The SNx (serial number) registers contain a 32-bit identification number that uniquely identifies the device. To read the entire serial number, two memory read requests must be initiated. The first read request to Address 0x0E returns the upper 16 bits of the serial number, and the second read request to Address 0x10 returns the lower 16 bits of the serial number.

SUGGESTED PCB LAYOUT

Figure 22 and Figure 23 show a suggested board layout for the SOIC package, and Figure 24 shows a sample solder pad layout. The board layout is intended for a 2-layer PCB design. While this exact layout need not be followed, the user should adhere to the following guidelines:

- Locate C1, C2, and C3 as close as possible to their respective package pin.
- Connect all Analog Devices reserved pins to GND through a trace and not directly through the pad itself.
- Keep the trace from the V_X package pin to L1/D1 as short as possible. It is acceptable to locate either L1 or D1 on the back side of the PCB to shorten this trace.
- Figure 22 and Figure 23 show the use of a top-layer metal GND plane for all GND connections. The use of a power plane is not recommended.
- For the SOIC package, it is not recommended to route the SPI interface traces under the device without proper shielding, such as a filled ground plane (used in Figure 22 and Figure 23).
- The PDD trace is widened compared to other signal traces for improved noise performance.
- Note that the L1 and D1 footprints change according to the user's selection of inductor and diode component.

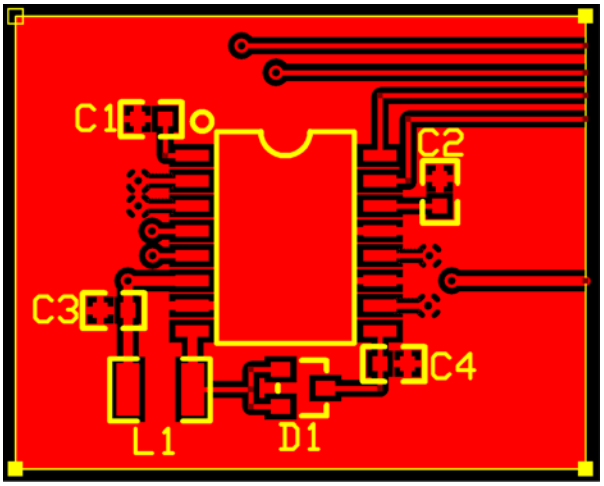

Figure 22. SOIC PCB Layout Top Layer Metal

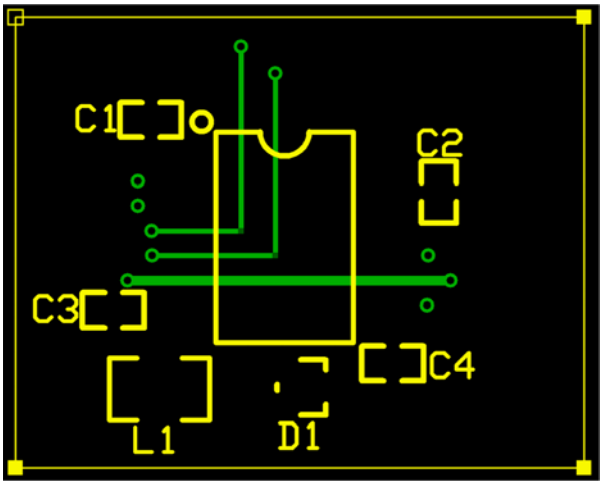

Figure 23. SOIC PCB Layout Bottom Layer Metal (Silkscreen Is shown as a Reference Only and Is Not Present on the Back Side of the PCB.)

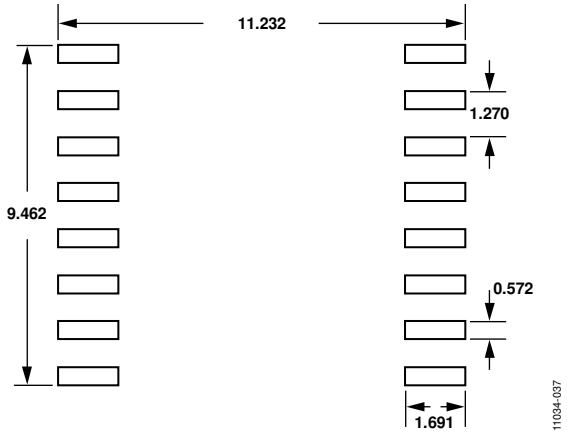

Figure 24. Sample SOIC Solder Pad Layout (Land Pattern); Dimensions Shown in Millimeters