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AFBR-775BxxxZ / AFBR-785BxxxZ

Twelve-Channel Transmitter and Receiver
Pluggable, Parallel-Fiber-Optics Modules

Data Sheet

Description

The AFBR-775BxxxZ Twelve-Channel, Pluggable, Parallel-Fiber-Optics Transmitter and AFBR-785BxxxZ Twelve-Channel, Pluggable, Parallel-Fiber-Optics Receiver are high performance fiber optics modules for short-range parallel multi-lane data communication and interconnect applications. The modules operate at 5.0Gbps per channel over multimode fiber systems using a nominal wavelength of 850 nm. Aggregate bandwidth per transmitter-receiver link is 60G. The electrical interface uses a 10x10 MEG-Array® low-profile mezzanine connector. The optical interface uses a MTP® (MPO) 1x12 ribbon cable connector. The thermal interface can be a factory installed heatsink for air-cooled systems or thermal seating plane for user flexibility. The modules incorporate high performance, highly reliable, short wavelength optical devices coupled with proven circuit technology to provide long life and consistent service.

Applications

- High Performance and High Productivity computer interconnects
- InfiniBand 12X DDR SX interconnects
- Datacom switch and router backplane connections
- Telecom switch and router backplane connections
- Dense 4 Gbps Fibre Channel compatible architectures
- Reach extensions for various protocols including PCI Express, HyperTransport and Serial RapidIO

Part Number Ordering Options

Transmitter Part Numbers	
With fin heat sink / no EMI nose clip	AFBR-775BZ
With fin heat sink / EMI nose clip	AFBR-775BEZ
With pin heat sink / no EMI nose clip	AFBR-775BPZ
With pin heat sink / EMI nose clip	AFBR-775BEPZ
With no heat sink / no EMI nose clip	AFBR-775BHZ
With no heat sink / with EMI nose clip	AFBR-775BEHZ
Receiver Part Numbers	
With fin heat sink / no EMI nose clip	AFBR-785BZ
With fin heat sink / EMI nose clip	AFBR-785BEZ
With pin heat sink / no EMI nose clip	AFBR-785BPZ
With pin heat sink / EMI nose clip	AFBR-785BEPZ
With no heat sink / no EMI nose clip	AFBR-785BHZ
With no heat sink / with EMI nose clip	AFBR-785BEHZ

Patent - www.avagotech.com/patents

Features

- High Channel Capacity: 60 Gbps per module
- High port density: 19 mm lateral port pitch; < 0.51 mm/Gbps for Tx–Rx pair
- Low power consumption per Gbps: < 53 mW/Gb/s for Tx–Rx pair
- Based on industry-standard, pluggable, SNAP12 form factor with upgraded pinout for improved signal integrity and keyed to prevent mis-plugging with first generation SNAP12 devices
- Backed by PPOD MSA to enable multiple sources of supply
- Twelve independent channels per module
- Separate transmitter and receiver modules
- 850 nm VCSEL array in transmitter; PIN array in receiver
- Operates up to 5.0 Gbps with 8b/10b compatible coded data
- Links up to 150 m at 5.0 Gbps with 2000 MHz·km 50 um MMF
- Two power supplies, 2.5 V and 3.3 V, for low power consumption
- Dedicated signals for module address, module reset and host interrupt.
- Two Wire Serial (TWS) interface with maskable interrupt for expanded functionality including:
  - o Individual channel functions: disable, squelch disable, lane polarity inversion, margin
  - o Programmable equalization integrated with DC blocking caps at transmitter data input
  - o Programmable receiver output swing and de-emphasis level
  - o A/D readback: module temperature and supply voltages, per channel laser current and laser power, or received power
  - o Status: per channel Tx fault, electrical (transmitter) or optical (receiver) LOS, and alarm flags
- 0 to 80 °C case temperature operating range

Transmitter Module

The optical transmitter module (see Figure 1) incorporates a 12-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 12-channel input buffer and laser driver, diagnostic monitors, control and bias blocks. The transmitter is designed for IEC-60825 and CDRH eye safety compliance; Class 1M out of the module. The Tx Input Buffer provides CML compatible differential inputs (presenting a nominal differential input impedance of 100 Ohms and a nominal common mode impedance to signal ground of 25 Ohms) for the high speed electrical interface that can operate over a wide common mode range without requiring DC blocking capacitors. For module control and interrogation, the control interface (LVTTL compatible) incorporates a Two Wire Serial (TWS) interface of clock and data signals and dedicated signals for host interrupt, module address setting and module reset. Diagnostic monitors for VCSEL bias, light output (LOP), temperature, both supply voltages and elapsed operating time are implemented and results are available through the TWS interface.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential inputs, de-activate channels, place channels into margin mode, disable the squelch function and program input equalization levels to reduce the effect of long PCB traces. A reset for the control registers is available. Serial ID information and alarm thresholds are provided. To reduce the need for polling, the TWS interface is augmented with an interrupt signal for the host.

Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of input signal (LOS) and transmitter fault conditions. All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset by reading the appropriate flag register. The optical output will squelch for loss of input signal unless squelch is disabled. Fault detection or channel deactivation through the TWS interface will disable the channel. Status, alarm and fault information are available via the TWS interface. The interrupt signal (selectable via the TWS interface as a pulse or static level) is provided to inform hosts of an assertion of an alarm, LOS and/or Tx fault.

Receiver Module

The optical receiver module (see Figure 2) incorporates a 12-channel PIN photodiode array, a 12-channel preamplifier and output buffer, diagnostic monitors, control and bias blocks. The Rx Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 Ohms to AC ground and 100 Ohms differentially that should be differentially terminated with 100 Ohms. DC blocking capacitors may be required. For module control and interrogation, the control interface (LVTTL compatible) incorporates a Two Wire Serial (TWS) interface of clock and data signals and dedicated signals for host interrupt, module address setting and module reset. Diagnostic monitors for optical input power, temperature, both supply voltages and elapsed operating time are implemented and results are available through the TWS interface.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential outputs, de-activate channels, disable the squelch function, program output signal amplitude and de-emphasis and change receiver bandwidth. A reset for the control registers is available. Serial ID information and alarm thresholds are provided. To reduce the need for polling, the TWS interface is augmented with an interrupt signal for the host.

Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of optical input signal (LOS). All flags are latched and will remain set even if the condition initiating the latch clears and operation

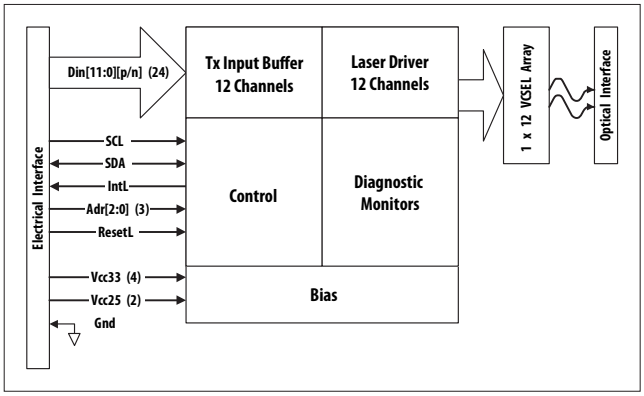


Figure 1. Transmitter Block Diagram

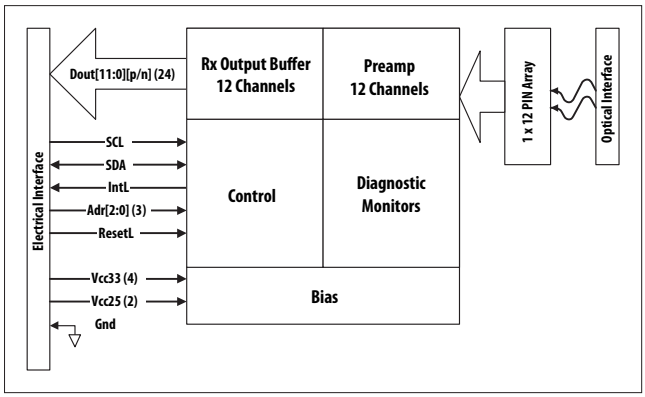


Figure 2. Receiver Block Diagram

resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register. The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through TWS interface. Status and alarm information are available via the TWS interface. The interrupt signal (selectable via the TWS interface as a pulse or static level) is provided to inform hosts of an assertion of an alarm and/or LOS.

High Speed Signal Interface

Figure 3 shows the interface between an ASIC/SerDes and the fiber optics modules. For simplicity, only one channel is shown. As shown in the Figure 3, the compliance points are on the host board side of the electrical connectors. Sets of s-parameters are defined for the transmitter and receiver interfaces. The transmitter and receiver are designed, when operating within Recommended Operating Conditions, to provide a robust eye-opening at the receiver outputs. See the Recommended Operating Conditions and the Receiver Electrical Characteristics for details.

Unused inputs and outputs should be terminated with 100 Ω differential loads.

The transmitter inputs support a wide common mode range and DC blocking capacitors may not be needed – none are shown in Figure 3. Depending on the common mode range tolerance of the ASIC/SerDes inputs, DC blocking capacitors may be required in series with the receiver. Differential impedances are nominally 100 Ω. The common mode output impedance for the receiver is nominally 25 Ω while the nominal common mode input impedance of the transmitter is 25 Ω.

Transmitter Input Equalization

Transmitter inputs can be programmed for one of several levels of equalization. See Figure 4. The default case provides a flat gain-frequency response in the inputs. Different levels of compensation can be selected to equalize skin-effect losses across the host circuit board. See Tx Memory Map 01h Upper Page section addresses 228 - 233 for programming details.

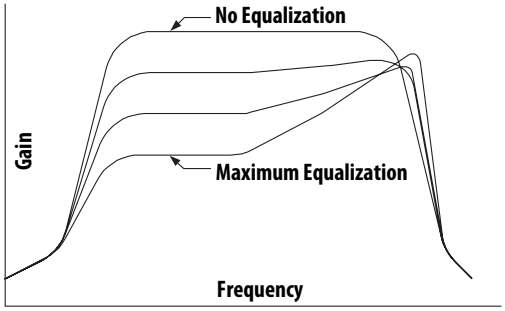


Figure 4. Input Equalization

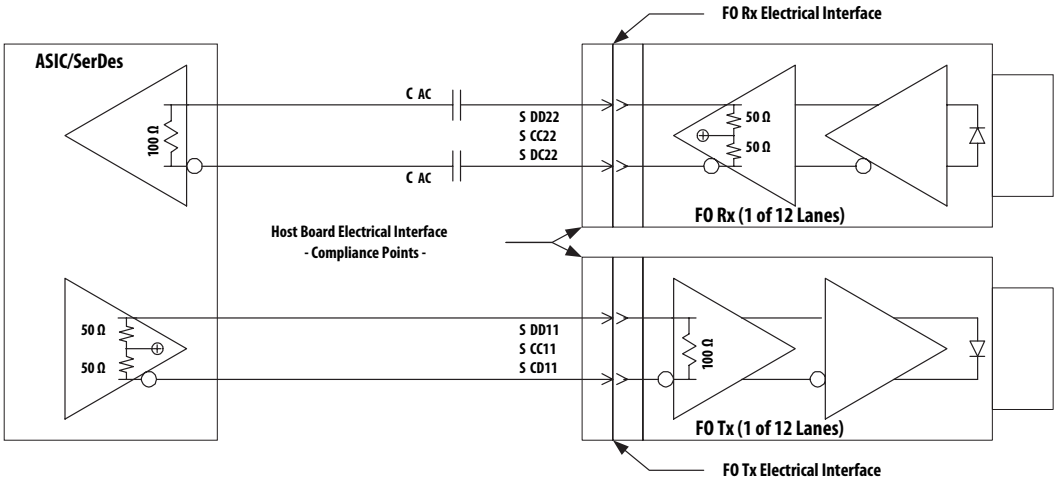


Figure 3. Application Reference Diagram

Receiver Output Amplitude and De-emphasis

Receiver outputs can be programmed to provide several levels of amplitude and de-emphasis. See Figure 5 for de-emphasis definition. The user can program for peak-to-peak amplitude and then a de-emphasis level. If zero de-emphasis is selected, then the signal steady state equals the peak-to-peak level. For other levels of de-emphasis the selected de-emphasis reduces the steady-state from the peak-to-peak level. The change from peak-to-peak level to steady-state occurs within a bit time. See Rx Memory Map 01h Upper Page section addresses 228 - 233 for amplitude programming details and addresses 234 – 239 for de-emphasis programming details.

Control Signal Interface

The control interface includes dedicated signals for address inputs, interrupt output and reset input and bidirectional clock and data lines for a two-wire serial access (TWS interface) to control and status and information registers. The TWS interface is compatible with industry standard two-wire serial protocol scaled for 3.3 volt LVTTL. It is implemented as a slave device. Signal and timing characteristics are further defined in the Control Characteristics and Control Interface & Memory Map sections.

The registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Regulatory & Compliance Issues

Various standard and regulations apply to the modules. These include eye-safety, EMC, ESD and RoHS. See the Regulatory Section for details regarding these and component recognition. Please note the transmitter module is a Class 1M laser product – DO NOT VIEW RADIATION DIRECTLY WITH OPTICAL INSTRUMENTS. See Regulatory Compliance Table for details.

Package Outline

The module is designed to meet the package outline defined in the PPOD MSA. This MSA follows the outline of the SNAP12 MSA except for the position of the MEG-Array® connector and pin assignments. See the package outline and host board footprint figures (Figures 23 -26) for details.

Handling and Cleaning

The transmitter and receiver modules can be damaged by exposure to current surges and over voltage events. Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Wave soldering, reflow soldering and/or aqueous wash process with the modules on board are not recommended. Normal handling precautions for electrostatic discharge sensitive devices should be observed.

Each module is supplied with an inserted port plug for protection of the optical ports. This plug should always be in place whenever a fiber cable is not inserted.

The optical connector includes recessed elements that are exposed whenever a cable or port plug is not inserted. Prior to insertion of a fiber optic cable, it is recommended that the cable end be cleaned to avoid contamination from the cable plug. The port plug ensures the optics remain clean and no addition cleaning should be needed. In the event of contamination, dry nitrogen or clean dry air at less than 20 psi can be used to dislodge the contamination. The optical port features (e.g. guide pins) preclude use of a solid instrument. Liquids are also not advised.

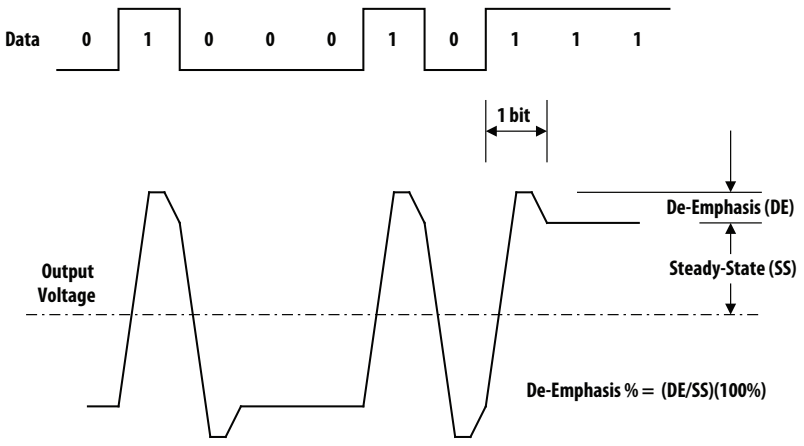


Figure 5. Definition of De-emphasis and Steady State

Link Model and Reference Channel

Performance specifications for the AFBR-775BxxxZ Transmitter and AFBR-785BxxxZ Receiver are based on a reference channel model. A reference channel model provides the basis for inter-operability between independently produced transmitter and receiver modules. The reference model used for the AFBR-775BxxxZ Transmitter and AFBR-785BxxxZ Receiver is based on the industry standard 10GbE link model (10GEPBud3_1_16a.xls available at the IEEE P802.3ae 10Gb/s Ethernet Task Force Serial PMD Documents website http://www.ieee802.org/3/ae/public/adhoc/serial_pmd/documents/).

As shown in Figure 6, a channel for a fiber optic link comprises a transmitter, receiver and cable plant with inputs at test point TP1 and outputs at test point TP4. The test points TP1 and TP4 coincide with the compliance points defined in Figure 3. The cable plant here includes the fiber and two inline connectors.

A reference channel permits the effect of various channel attributes to be referred to different points in the channel and accumulated. For example, in the GbE (All_1250.xls available at the IEEE website http://grouper.ieee.org/groups/802/3/10G_study/public/email_attach/All_1250.xls) and 10 GbE models all signal impairments are captured and translated into power penalties. Also, the effect of transmitter and fiber attributes are also captured and referred to TP3 to define stressed receiver test criteria. Similarly, all effects upstream of TP4 can be captured and referred to TP4 and combined at this point into a figure of merit. Since the signal at TP4 is electrical and not optical there are advantages for this.

To ensure inter-operability among independently produced transmitters and receivers, definition of acceptable devices is required. This can be accomplished on an individual parameter basis by setting min/max limits or with aggregates of attributes by establishing a figure of merit. Referring again to the 10GbE link model, the entity 'margin at target distance' is an aggregate figure of merit of all link attributes. There a set of link attributes will yield a specific link margin and a worst case set of link attributes can be defined for a minimum level of performance. Instead of placing a maximum or minimum limit on each attribute, it is possible to allow elements in the set to shift (i.e. tradeoff with others within the set) as long as the desired margin is achieved. Further, if 'margin at target distance' can be translated into eye opening at TP4, the aggregate figure of merit is directly measurable. To preserve independence for transmitter, receiver and fibers, it is required that transmitter attributes only trade-off with other transmitter attributes and, similarly, receiver attributes can only trade-off with other receiver attributes.

In this data sheet, a minimum eye width at TP4 for a specified maximum BER is the figure of merit used to define acceptable link performance. Additional inputs and calculations have been added to the 10GbE link model to calculate eye closure and the effects of all impairments are referred to TP4 and combined as elements of eye closure. The minimum eye width at TP4 is included in tables, Transmitter Optical Characteristics and Receiver Electrical Characteristics, as minimum "Reference Link Output Eye Width'.

Note:

1. The Recommended Operating Conditions table and those for transmitter and receiver characteristics provide the necessary attributes to define the worst case set for the reference channel. Various elements of this worst case set are labeled 'Informative' and are allowed to range outside the maximum or minimum limit for the individual element when there is a compensating improvement in others of the worst case subset. Transmitter attribute tradeoffs are limited to the transmitter subset and receiver tradeoffs are limited to the receiver subset.

The following two tables summarizes the practical tradeoffs between different informative transmitter parameters, as well as different informative receiver parameters, respectively. Although the wavelength and spectral width can also trade off with each other, they are not included here for interoperability reason.

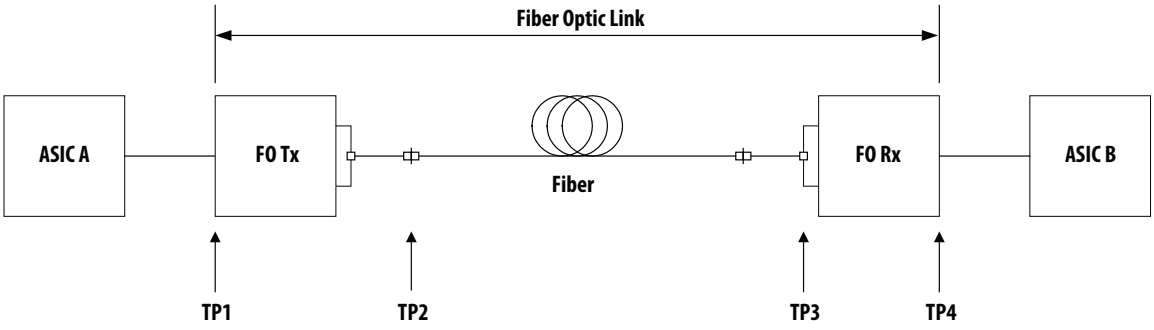


Figure 6. Fiber Optic Link

Informative TX parameters trading off each other while guaranteeing TP2 & TP4 performance

Parameter	Symbol
Extinction Ratio	ER
Output Optical Modulation Amplitude	OMA
Output Rise/Fall Time	
Relative Intensity Noise OMA	RIN12OMA
Accumulated Deterministic Jitter	
Accumulated Total Jitter	

Informative RX parameters trading off each other while guaranteeing TP4 performance

Parameter	Symbol
Receiver Bandwidth (BW)	
Input Optical Power Sensitivity (OMA)	

The reference model for testing transmitters consists of a pattern generator, fiber optic test cable, attenuator, test receiver and BERT. See Figure 7 for the evolution of a reference channel to a transmitter test channel. Differences between the worst case values for attributes in the reference model and those in the test equipment set can be compensated by an added attenuator (note that the 10GbE model translates all impairments into power penalties) and adjustments in TJ criteria at TP4. Differences in the TP1 input jitter between the defined conditions, TJ r and DJ r, for the reference channel and actually provided in the test channel, TJ t and DJ t, can also be accommodated by adjustments to TP4 test criteria (TJ r becomes TJ t). The extended 10GbE Link model is used to determine the compensating attenuation and TP4 criteria adjustments.

The reference for testing receivers consists of a pattern generator, test transmitter, fiber optic test cable, attenuator and BERT. See Figure 8 for the evolution of a reference channel to a receiver test channel. In a similar manner as with the transmitter, all differences between the test equipment and worst case channel are compensated with an attenuator and adjustments in the TP4 criteria.

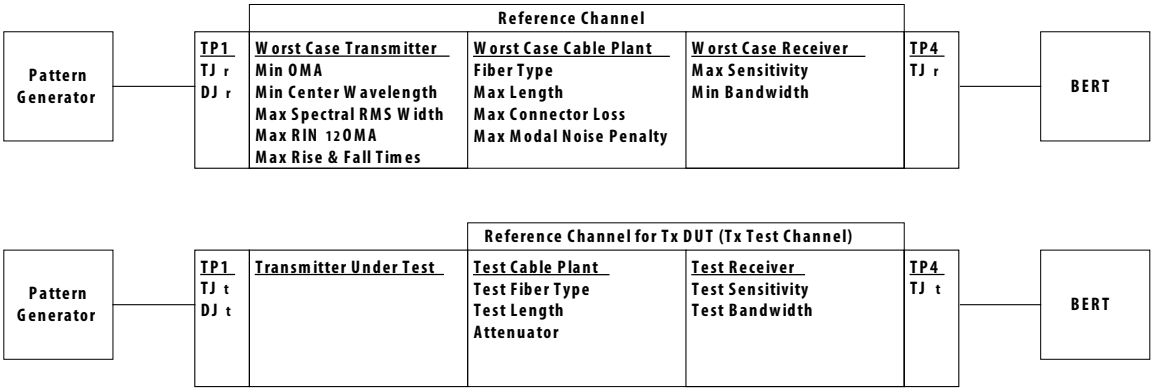


Figure 7. Reference and Test Channels for Transmitter

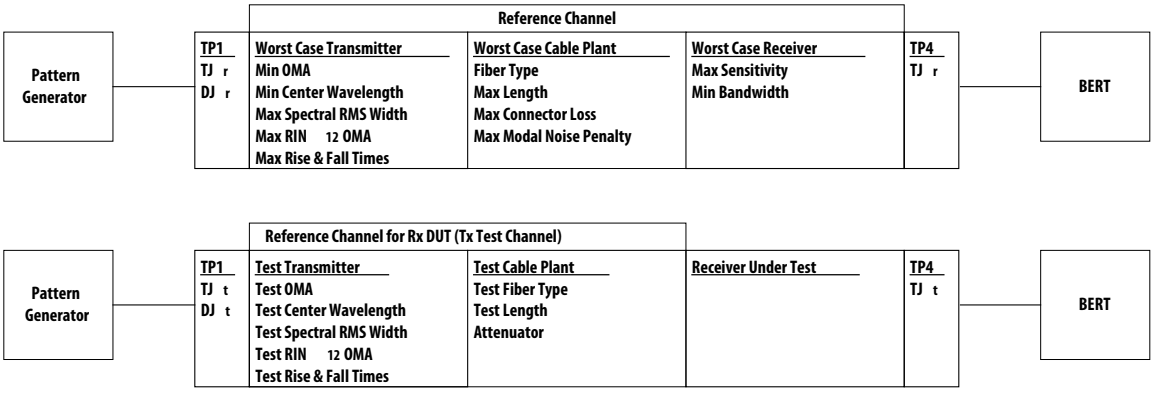


Figure 8. Reference and Test Channels for Receiver

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operation Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_s	-40	100	°C	
Case Temperature - Operating	$T_{C\ AMR}$	-20	90	°C	1
2.5 V Power Supply Voltage	Vcc25	-0.5	3.0	V	
3.3 V Power Supply Voltage	Vcc33	-0.5	3.6	V	
Data Input Voltage – Single Ended		-0.5	Vcc33+0.5, Vcc25+0.5	V	2
Data Input Voltage – Differential	$\lvert V_{DIp} - V_{DIn} \rvert$		1.0	V	3
Control Input Voltage	Vi	-0.5	Vcc33+0.5, 3.6	V	4
Control Output Current	Io	-20	20	mA	
Relative Humidity	RH	5	95	%	

Notes:

1. The position for case temperature measurement is shown in Figure 11. Operation at or above the maximum Absolute Maximum Case Temperature for extended periods may adversely affect reliability. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions.
2. The maximum limit is the lesser of Vcc33 + 0.5 V or Vcc25+ 0.5 V..
3. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry.
4. The maximum limit is the lesser of Vcc33 + 0.5 V or 3.6 V.

Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Case Temperature	Tc	0	40	80	°C	
2.5 V Power Supply Voltage	Vcc25	2.375	2.5	2.625	V	Figures 12, 13
3.3 V Power Supply Voltage	Vcc33	3.135	3.3	3.465	V	Figures 12, 13
Signal Rate per Channel		2.5		5.0	GBd	
Data Input Differential Peak-to-Peak Voltage Swing	$\Delta V_{DI\ pp}$	175		1400	mVpp	3, Figure 14
Data Input Common Mode Voltage	$V_{DI\ CM}$	0.35		Vcc33-0.35	V	4
Data Input Rise & Fall Times (20% - 80%)		30		48	ps	
Data Input Deterministic Jitter				32	ps	5
Data Input Total Jitter				66	ps	6
Control* Input Voltage High	V_{ih}	2		Vcc33	V	
Control* Input Voltage Low	V_{il}	GND		0.8	V	
Two Wire Serial Interface Clock Rate				400	kHz	Figure 17
Reset Pulse Width	$t_{RSTL\ PW}$	10			µs	Figure 19
Power Supply Noise				100	mVpp	7500 Hz to 2.7 GHz
Receiver Differential Data Output Load			100		Ohms	Figure 3
AC Coupling Capacitors – Receiver Data Outputs	Cac		0.1		µF	8, Figure 3
Fiber Length: 500 MHz·km 50µm MMF		0.5		75	m	9
Fiber Length: 2000 MHz·km 50µm MMF		0.5		150	m	

Notes:

* Control signals, LVTTL (3.3 V) compatible, include Adr[2:0], IntL, ResetL, SCL and SDA.

1 The position for case temperature measurement is shown in Figure 11. Continuous operation at the maximum Recommended Operating Case Temperature should be avoided in order not to degrade reliability. Modules will function (degraded performance may result) where operated with case temperatures below the minimum Recommended Operating Case Temperature.

2. While operation for various codes, e.g. 8b10b, are supported, certain parameters, jitter and sensitivity, are defined for specific operating conditions of 5.0 GBd and 8b10b equivalent test patterns. The receiver has a low frequency -3dB corner near 100 kHz.

3. Data inputs are CML compatible. Minimum input requirement holds for default input equalization settings. Data Input Differential Peak to Peak Voltage Swing is defined as follows: $\Delta V_{DI\ pp} = \Delta VD_{IH} - \Delta VD_{IL}$ where ΔVD_{IH} = High State Differential Data Input Voltage and ΔVD_{IL} = Low State Differential Data Input Voltage.

4. Data Input Common Mode Voltage is defined as follows: $VD_{ICM} = (VD_{inp} + VD_{inn})/2$.

5. Deterministic Jitter, D_J, conforms to the dual-Dirac model where $T_{J(BER)} = DJ + 2Q(BER)RJ_{rms}$ and RJ_{rms} is the width of the Gaussian component. Here BER = 10^{-12}. D_J is measured with the same conditions as T_J. Effects of impairments in the test signal due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.

6. Total Jitter, T_J, defined for a BER of 10^{-12}, is measured at the 50% signal level using a 5.0 GBd Pseudo Random Bit Sequence of length 2^7-1 (PRBS7), or equivalent, test pattern. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.

7. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figures 12 and 13 for recommended power supply filters.

8. For data pattern with restricted run lengths and disparity, e.g. 8b10b, smaller value capacitors may provide acceptable results.

9. Channel insertion loss includes 3.5 dB/km attenuation, 1.5 dB connector loss and 0.3 dB modal noise penalty allocations.

Transmitter Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40˚C, Vcc33 = 3.3 V and Vcc25 = 2.5 V.

Parameter	Symbols	Min	Typ	Max	Units	Reference
Power Consumption				2.4	W	
Power Supply Current - Vcc25				370	mA	1
Power Supply Current - Vcc33				425	mA	2
Differential Input Impedance		80		120	Ω	Informative
Differential Input Reflection Coefficient	S_{DD11}		-8		dB	3, Figure 3
Common Mode Input Reflection Coefficient	S_{CC11}		-6		dB	4, Figure 3
Differential to CM Input Reflection Coefficient	S_{CD11}		-35		dB	5, Figure 3
LOS Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	$\Delta V_{DI\ PP\ LOS}$	58	120	156	mVpp	
LOS Hysteresis: Tx Data Input		1		4	dB	6
Power On Initialization Time	$t_{PWR\ INIT}$			2000	ms	7, Figure 18

Notes:

* For control signal timing including Adr[2:0], IntL, ResetL, SCL and SDA see Control Characteristics: Transmitter/Receiver.

1. Supply current includes that of all Vcc25 contacts.
2. Supply current includes that of all Vcc33 contacts.
3. Measured over the range 100 MHz to 3.75 GHz with reference differential impedance of 100 Ω
4. Measured over the range 100 MHz to 3.75 GHz with reference common mode impedance of 25 Ω
5. Measured over the range 100 MHz to 3.75 GHz with reference differential impedance of 100 Ω
6. LOS Hysteresis is defined as 20 Log(LOS De-assert Level / LOS Assert Level).
7. Power On Initialization Time is the time from when the supply voltages reach and remain above the minimum Recommended Operating Conditions to the time when the module enables TWS access. The module at that point is fully functional.

Receiver Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40˚C, Vcc33 = 3.3 V and Vcc25 = 2.5 V.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Power Consumption				2	W	1
Power Supply Current (Vcc25)				670	mA	2
Power Supply Current (Vcc33)				200	mA	3
Data Output Differential Peak-to-Peak Voltage Swing (Zero De-emphasis)	$\Delta V_{DO\ pp}$	775	850	925	mVpp	4 , Figure 14, 100 Ω Load Full Scale Setting
		415	490	565		Default Amplitude Setting
Data Output Common Mode Voltage	$V_{DO\ CM}$	1.785		2.540	V	5, Figure 14, Over Amplitude Setting Range
Data Output Off State Differential Voltage	$\Delta V_{DO\ OFF}$			20	mVpp	
Data Output Off Common Mode Voltage	$V_{DO\ OFF\ CM}$			Vcc25	V	
Output Rise/Fall time (20-80%)				80	ps	6
Receiver BW		3.125			GHz	Informative, Linear stages, Default Rate Select
LOS to Data Output Squelch Assert Time	$t_{SQ\ ON}$			80	µs	7, Figure 22
Data Output Squelch De-assert Time	$t_{SQ\ OFF}$			300	µs	8, Figure 22
Reference Link Output Deterministic Jitter				66	ps	9, Informative
Reference Link Output Total Jitter				130	ps	10
Reference Link Output Eye Width	$t_{EYE\ LINK}$	70			ps	11
Differential Output Impedance		80		120	Ω	Informative
Differential Output Reflection Coefficient	S_{DD22}		-10		dB	12, Figure 3
Common Mode Output Reflection Coefficient	S_{CC22}		-8		dB	13, Figure 3
CM to Differential Output Reflection Coefficient	S_{DC22}		-35		dB	14, Figure 3
Power On Initialization Time	$t_{PWR\ INIT}$			2000	ms	15, Figure 18
Inter-channel Skew				150	ps	16
Rx Input-Output Latency				600	ps	Informative

Notes:

* For control signal timing including Adr[2:0], IntL, ResetL, SCL and SDA see Control Characteristics: Transmitter/Receiver.

1. Max conditions includes default output amplitude and de-emphasis programming.
2. Supply current includes that of all Vcc25 contacts. Max conditions include maximum output amplitude and de-emphasis programming.
3. Supply current includes that of all Vcc33 contacts. Max conditions include maximum output amplitude and de-emphasis programming.
4. Data outputs are CML compatible. Data Output Differential Peak to Peak Voltage Swing is defined as follows: $\Delta V_{DO\ pp} = \Delta V_{DOH} - \Delta V_{DOL}$ where ΔV_{DOH} = High State Differential Data Output Voltage and ΔV_{DOL} = Low State Differential Data Output Voltage. Impairments in measurements due to the test system are removed.
5. Data Output Common Mode Voltage is defined as follows: $V_{DO\ CM} = (VD_{outp} + VD_{outn})/2$.
6. These are unfiltered rise and fall times without de-emphasis measured between the 20% and 80% levels using a 500 MHz square wave test pattern. Impairments in measurements due to the test system are removed.
7. This is the module response time from fall of Rx input to less than Rx input LOS threshold to squelch of Rx outputs.
8. This is the module response time from rise of Rx input to greater than Rx input LOS threshold to resumption of Rx outputs.
9. Deterministic Jitter, D_J, conforms to the dual-Dirac model where $T_{J(BER)} = D_J + 2Q(BER)RJ_{rms}$ and RJ_{rms} is the width of the Gaussian component. Here BER = 10^{-12}. D_J is measured with the same conditions as T_J. The receiver output is measured with default de-emphasis. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with test patterns at an input signal 6 dB above maximum Receiver Sensitivity.
10. Total Jitter, T_J, defined for BER of 10^{-12}, is measured at the 50% signal level using a 5.0 GBd Pseudo Random Bit Sequence of length 2^7-1 (PRBS7), or equivalent, test pattern with characteristics that are equivalent to that of an AFBR 775B transmitter module and maximum cable length operating per the Recommended Operation Conditions as the test source. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.
11. Eye Opening is defined as the unit interval less T_J for the same test pattern and conditions as T_J.
12. Measured over the range 100 MHz to 3.75 GHz with reference differential impedance of 100 Ω
13. Measured over the range 100 MHz to 3.75 GHz with reference common mode impedance 25 Ω
14. Measured over the range 100 MHz to 3.75 GHz with reference differential impedance 100 Ω
15. Power On Initialization Time is the time from when the supply voltages reach and remain within Recommended Operating Conditions to the time when the module enables TWS access. The module at that point is fully functional.
16. Inter-Channel Skew is defined for the condition of equal amplitude, zero ps skew input signals.

Control Characteristics: Transmitter/Receiver

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40˚C, Vcc33 = 3.3 V and Vcc25 = 2.5 V.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Control* Input Voltage Hysteresis LVTTL	V_{hys}		0.4		V	
Control* Input Current LVTTL	I_{in}	-125		125	µA	0 V < Vin < Vcc33
Control* Output Voltage Low LVTTL	V_{ol}			0.4	V	I_{ol} = 2mA
Control* Output Current High-Z	I_{oh}	-10		10	µA	0 V < Vin < Vcc33
Address Assert Time				100	ms	1
Interrupt Assert Time	$t_{INTL\ ON}$			200	ms	2, Figure 20
Interrupt Pulse Width	$t_{INTL\ PW}$	5			µs	3, Figure 20
Interrupt De-assert Time	$t_{INTL\ OFF}$			500	µs	4, Figure 20
Reset Assert Time	$t_{RSTL\ ON}$			100	µs	5, Figure 19
Reset De-assert Time	$t_{RSTL\ OFF}$			2000	ms	6, Figure 19
Initialization Time TWS Interfaces				2000	ms	Figure 18
TWS Data In Set Up Time	$t_{SU:SDA}$			0.10	µs	7, Figure 17
TWS Data In Hold Time	$t_{HD:SDA}$			0	µs	8, Figure 17
TWS Clock Low to Data Out Valid	t_{AA}	0.10		0.90	µs	9, Figure 17
TWS Data Out Hold Time	t_{DH}	50			ns	10, Figure 17
TWS Data Output Rise Time	tr_{SDA}			0.30	µs	Figure 17, Measured between 0.8V and 2.0V
TWS Data Output Fall Time	tf_{SDA}			0.30	µs	
TWS Interface Timing						See Atmel Two-Wire Serial EEPROM, e.g. AT24C01A

Notes:

* Control signals include Adr[2:0], IntL, ResetL, SCL and SDA.

1. This is the module response time from a change in module address, Adr[2:0], to response to TWS communication using the new address.
2. This is the module response time from occurrence of interrupt generating event to IntL assertion, $V_{out:IntL} = V_{ol}$.
3. Pulse or static level can be selected for IntL. Pulse mode is default. See Memory Map.
4. This is the module response time from clear on read operation, measured from falling SCL edge after stop bit of read transaction, until $V_{out:IntL} = V_{oh}$ where IntL is in static mode.
5. Assertion of ResetL activates a complete module reset, i.e. module returns to factory default and non-volatile control settings. While ResetL is Low, Tx and Rx outputs are disabled and the module does not respond to the TWS interface.
6. This is the response time from ResetL de-assertion to resumption of operation.
7. Data In Set Up Time is measured from $V_{il(max)SDA}$ or $V_{ih(min)SDA}$ to $V_{il(max)SCL}$.
8. Data In Hold Time is measured from $V_{il(max)SCL}$ to $V_{il(max)SDA}$ or $V_{ih(min)SDA}$.
9. Clock Low to Data Out Time is measured from $V_{il(max)SCL}$ to $V_{ol(max)SDA}$ or $V_{oh(min)SDA}$.
10. Data Out Hold Time is measured from $V_{il(max)SCL}$ to $V_{ol(max)SDA}$ or $V_{oh(min)SDA}$.

Transmitter Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40˚C, Vcc33 = 3.3 V and Vcc25 = 2.5 V.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Output Optical Power: Average	PO AVE			-1.5	dBm	
Output Optical Power: Disabled	PO OFF			-30	dBm	
Extinction Ratio	ER	3			dB	Informative
Output Optical Modulation Amplitude	OMA	-5.7			dBm	Informative
Output OMA: Squelched				-27	dBm	
Encircled Flux						1
Center Wavelength		830		860	nm	
Spectral Width - rms				0.85	nm	
Output Rise/Fall Time				50	ps	2, Informative
Power On Initialization Time Tx Outputs	$t_{PWR\ INIT}$			2000	ms	Figure 18
Reset Assert Time Tx Outputs	$t_{RSTL\ ON}$			2000	ms	Figure 19
Reset De-assert Re-initialization Time Tx Outputs	$t_{RSTL\ OFF}$			2000	ms	Figure 19
Output Disable Assert Time for Fault	$t_{DIS\ ON}$			100	ms	Figure 21
Output Squelch Assert Time for LOS	$t_{SQ\ ON}$			80	µs	Figure 22
Output Squelch De-assert Time for LOS	$t_{SQ\ OFF}$			80	µs	Figure 22
Inter-channel Skew				150	ps	3
Channel Latency			400		ps	Informative
Relative Intensity Noise OMA	RIN12OMA			-124	dB/Hz	Informative
Accumulated Deterministic Jitter				54	ps	4, Informative
Accumulated Total Jitter				101	ps	5, Informative
Reference Link Output Eye Width	$t_{EYE\ REF}$	70			ps	

Notes:

1. The transmitter launch condition meets the requirements of 10 Gigabit Ethernet multimode fiber as detailed in TIA 492AAC.
2. These are unfiltered rise and fall times measured between the 20% and 80% levels using a 500 MHz square wave test pattern. Impairments in measurements due to the test system are removed.
3. Inter-Channel Skew is defined for the condition of equal amplitude, zero ps skew input signals.
4. Deterministic Jitter, DJ, conforms to the dual-Dirac model where $T_{J(BER)} = D_J + 2Q(BER)RJ_{rms}$ and RJ_{rms} is the width of the Gaussian component. Here BER = 10^{-12}. DJ is measured with the same conditions as T_J. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.
5. Total Jitter, T_J, defined for BER of 10^{-12}, is measured at the 50% signal level using a 5.0 GBd Pseudo Random Bit Sequence of length 27^{-1} (PRBS7), or equivalent, test pattern with test source characteristics per the Recommended Operation Conditions. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.
6. Eye Opening is defined as the unit interval less T_J for the same test pattern and conditions as T_J. Measurement is made at the output, TP4, of the Reference Channel. See Link Model and Reference Channel section and Receiver Electrical Characteristics.

Receiver Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40˚C, Vcc33 = 3.3 V and Vcc25 = 2.5 V.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Input Optical Power Sensitivity (OMA)				-13.85	dBm	1, Informative, Default Signal Rate
Input Optical Power Saturation	$P_{SAT\ AVE}$	-1.0			dBm	2
Operating Center Wavelength		830		860	nm	
Return Loss		12			dB	
LOS Asserted Threshold - OMA	P_{LOS} OMA	-26	-19		dBm	
LOS De-asserted - OMA			-17	-14	dBm	
LOS Hysteresis		0.5	2		dB	3

Notes:

1. Sensitivity is defined as the input OMA needed to produce a BER ≤10^{-12} at the center of the signal period using a 5.0 GBd Pseudo Random Bit Sequence of length 27^{-1} (PRBS7), or equivalent, test pattern. Effects of impairments in the test signal due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns and input signals 6 dB above PIN MIN.
2. Saturation is defined as the average input power (ER = 6 dB) that at the receiver output produces an eye width less than the Reference Link Output Eye Width Minimum ($t_{EYE\ LINK}$) for a BER ≤10^{-12} using a 5.0 GBd Pseudo Random Bit Sequence of length 27^{-1} (PRBS7), or equivalent, test pattern. Effects of impairments in the test signal due to the test system are removed from the measurement.
3. Signal Detect Hysteresis is defined as 10 Log(LOS De-assert Level / LOS Assert Level).than the Reference Link Output Eye Width Minimum ($t_{EYE\ LINK}$) for a BER ≤10^{-12} using a 5.0 GBd Pseudo Random Bit Sequence of length 27^{-1} (PRBS7), or equivalent, test pattern. Effects of impairments in the test signal due to the test system are removed from the measurement.
   Signal Detect Hysteresis is defined as 10 Log(LOS De-assert Level / LOS Assert Level).

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B) JEDEC Machine Model (MM) (JESD22-A115-A)	Transmitter module withstands minimum 2000 V Receiver module withstands minimum 2000 V Transmitter module withstands minimum 100 V Receiver module withstands minimum 100 V
Electrostatic Discharge (ESD) to Optical Connector Receptacle	Variation of IEC 61000-4-2	Typically withstands at least 6 kV air discharge with module biased
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	Typically passes with 10 dB margin. Actual performance dependent on enclosure design.
Immunity	Variation of IEC 61000-4-3	Typically minimal effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing	IEC 60825-1 Amendment 2 CFR 21 Section 1040	Pout: IEC AEL & US FDA CDRH Class 1M CDRH Accession Number: 9720151-074 TUV Certificate Number: 72060862
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File Number: E173874
RoHS Compliance		Less than 100 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl esters.

Transmitter Module Contact Assignment and Signal Description

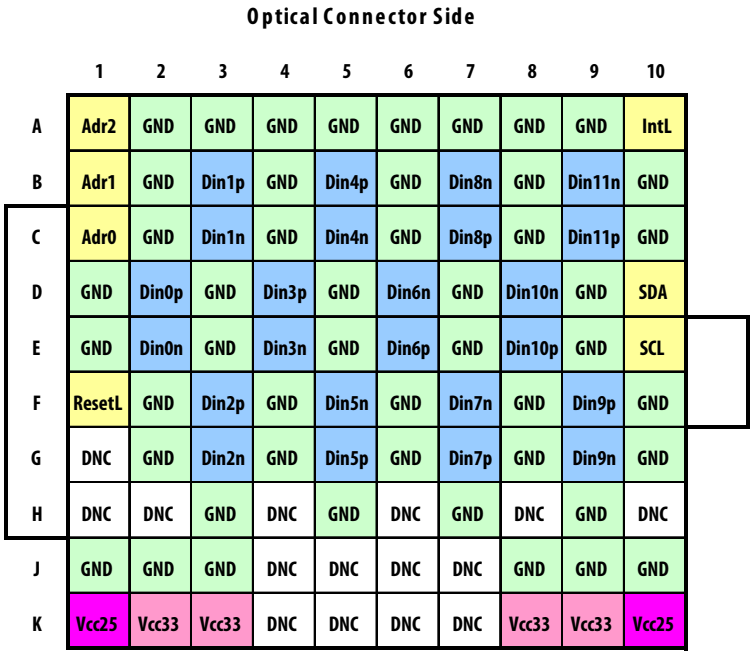


Figure 9. Host Board Pattern for Transmitter Connector – Top View

Signal Name	Signal Description	I/O	Type
Adr[2:0]	TWS Module Bus Address bits: Address has the form 0101hjkx where Adr2, Adr1 & Adr0 correspond to h, j & k respectively and x corresponds to the R/W command.	I	3.3V LVTTL
Din[11:0]p	Transmitter Data Non-inverting Input for channels 11 through 0	I	CML
Din[11:0]n	Transmitter Data Inverting Input for channels 11 through 0	I	CML
DNC	Reserved – Do Not Connect to any electrical potential on Host PCB		
GND	Signal Common: All module voltages are referenced to this potential unless otherwise stated. Connect these pins directly to the host board signal ground plane.		
IntL	Interrupt signal to Host, Asserted Low: An interrupt is generated in response to any Tx Fault condition, loss of input signal or assertion of any monitor Flag. It may be programmed through the TWS interface to generate either a pulse or static level with pulse mode as default. This output presents a High-Z condition when IntL is de-asserted and requires a pull-up on the Host board. Pull-up to the Host 3.3 V supply is recommended.	O	3.3V LVTTL, high-Z or driven to 0 level
ResetL	Reset signal to module, Asserted Low: When asserted the optical outputs are disabled, TWS interface commands are inhibited, and the module returns to default and non-volatile settings. An internal pullup biases the input High if the input is open.	I	3.3V LVTTL
SDA	TWS interface data signal: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is recommended.	I/O	3.3V LVTTL/ Open-Drain
SCL	TWS interface clock signal l: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is recommended.	I	3.3V LVTTL
Vcc25	2.5V Power supply, External common connection of pins required – not common internally		
Vcc33	3.3 V Power supply, External common connection of pins required – not common internally		
Case Common	Not accessible in connector. Case common incorporates exposed conductive surfaces including threaded bosses and is electrically isolated from signal common, i.e. GND. Connect as appropriate for EMI shield integrity. See EMI clip and bezel cutout recommendation.		

Receiver Module Contact Assignment and Signal Description

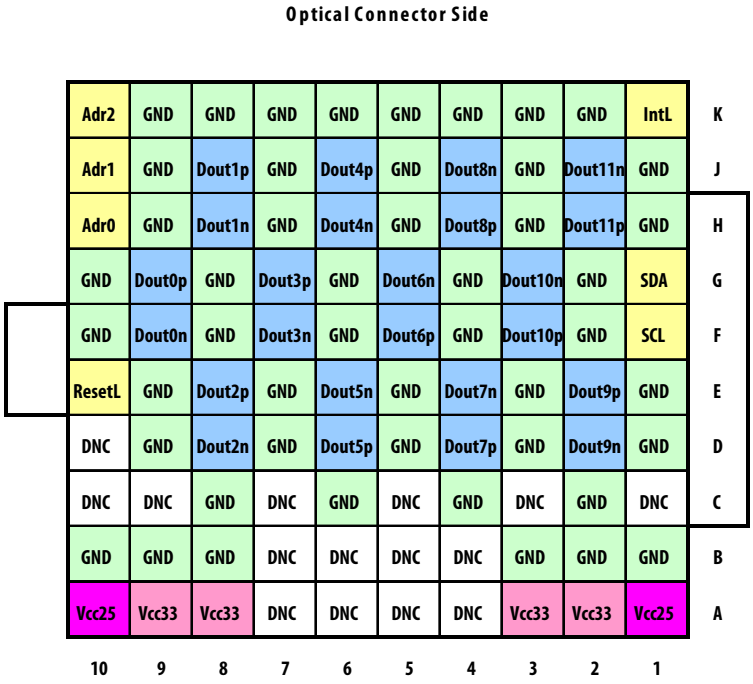


Figure 10. Host Board Pattern for Receiver Connector – Top View

PIN name	Functional descriptions	I/O	Type
Adr[2:0]	TWS Module Bus Address bits: Address has the form 0101hjkx where Adr2, Adr1 & Adr0 correspond to h, j & k respectively and x corresponds to the R/W command.	I	3.3V LVTTL
Dout[11:0]p	Receiver Data Non-inverting Output for channels 11 through 0	O	CML
Dout[11:0]n	Receiver Data Inverting Output for channels 11 through 0	O	CML
DNC	Reserved – Do Not Connect to any electrical potential on Host PCB		
GND	Signal Common: All module voltages are referenced to this potential unless otherwise stated. Connect these pins directly to the host board signal ground plane.		
IntL	Interrupt signal to Host, Asserted Low: An interrupt is generated in response to loss of input signal or assertion of any monitor Flag. It may be programmed through the TWS interface to generate either a pulse or static level with pulse mode as default. This output presents a High-Z condition when IntL is de-asserted and requires a pull-up on the Host board. Pull-up to the Host 3.3 V supply is recommended.	O	3.3V LVTTL, high-Z or driven to 0 level
ResetL	Reset signal to module, Asserted Low: When asserted the data outputs, Dout[11:0]p/n are squelched, TWS interface commands are inhibited, and the module returns to default and non-volatile settings. An internal pullup biases the input High if the input is open.	I	3.3V LVTTL
SDA	TWS interface data signal: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is recommended.	I/O	3.3V LVTTL/ Open-Drain
SCL	TWS interface clock signal: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is recommended.	I	3.3V LVTTL
Vcc25	2.5V Power supply, External common connection of pins required – not common internally	P	
Vcc33	3.3 V Power supply, External common connection of pins required – not common internally	P	
Case Common	Not accessible in connector. Case common incorporates exposed conductive surfaces including threaded bosses and is electrically isolated from signal common, i.e. GND. Connect as appropriate for EMI shield integrity. See EMI clip and bezel cutout recommendation.		

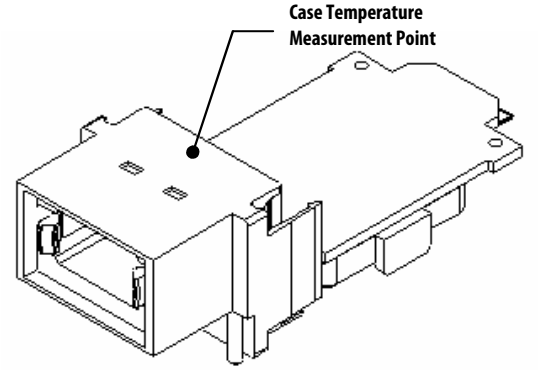


Figure 11. Case Temperature Measurement Point

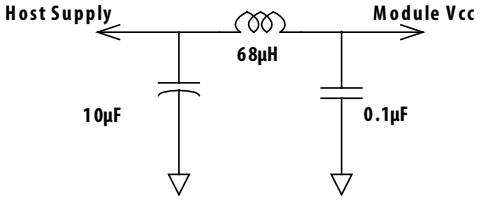


Figure 12. Recommended Tx Power Supply Filter

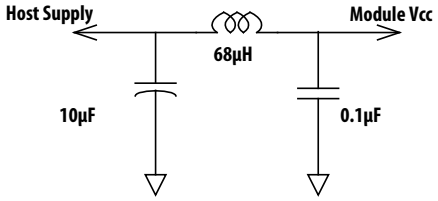


Figure 13. Recommended Rx Power Supply Filter

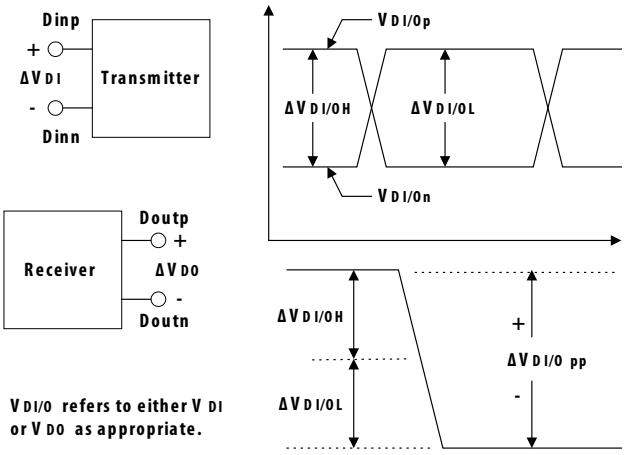


Figure 14. Differential Signal Definitions

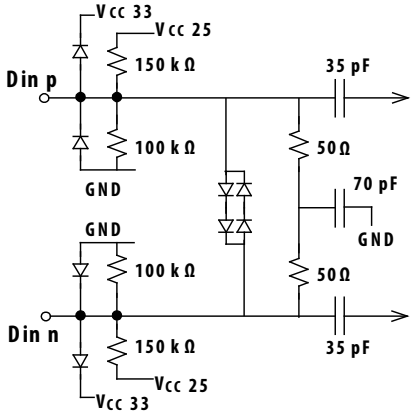


Figure 15. Transmitter Data Input Equivalent Circuit

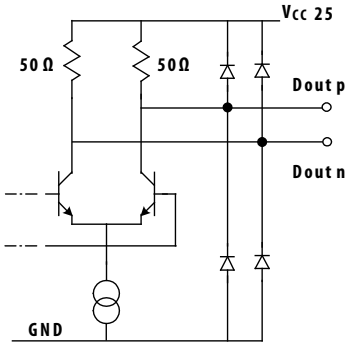


Figure 16. Receiver Data Output Equivalent Circuit

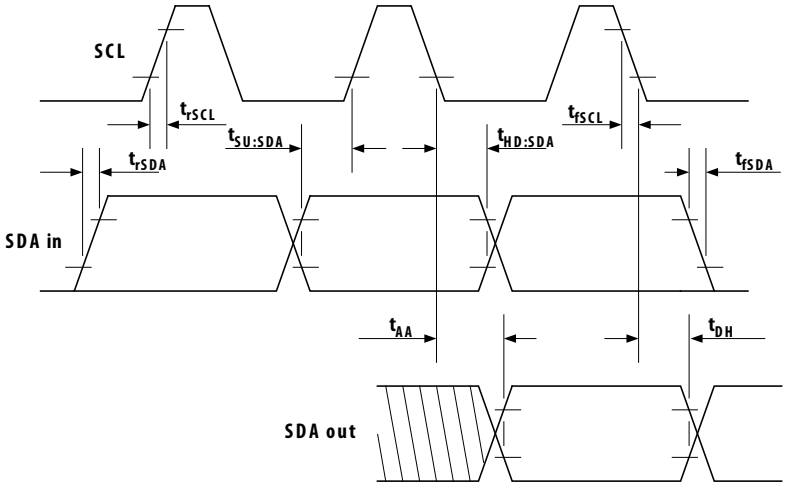


Figure 17. TWS Interface Bus Timing

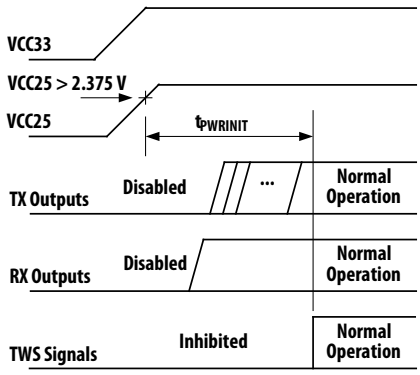


Figure 18. Power-up Sequence

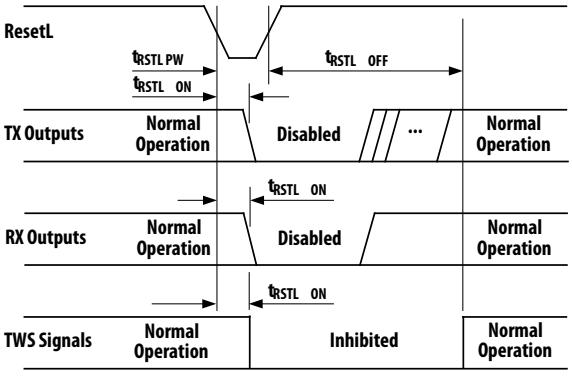


Figure 19. ResetL Sequence

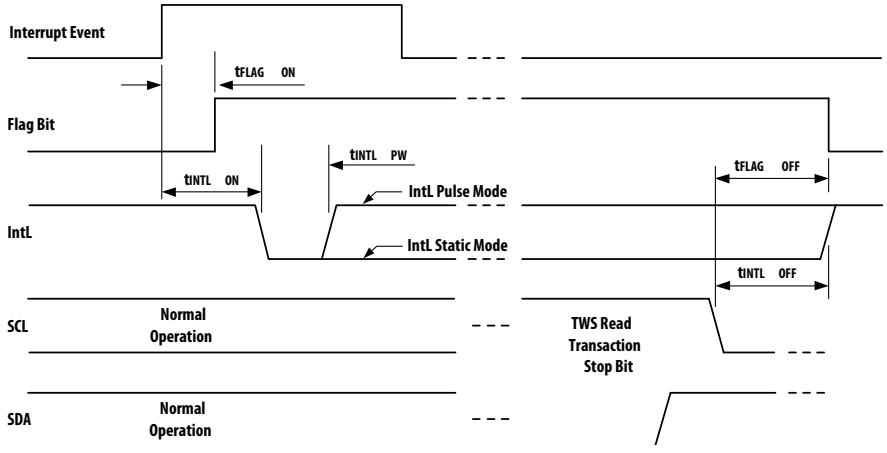


Figure 20. Interrupt Sequence

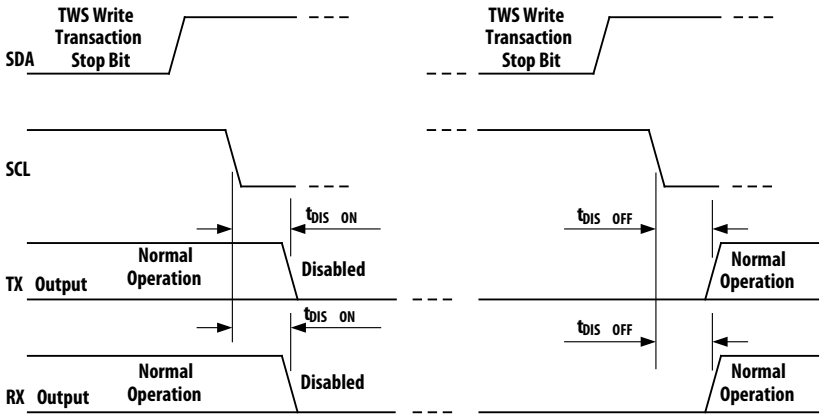


Figure 21. Channel Disable Sequence

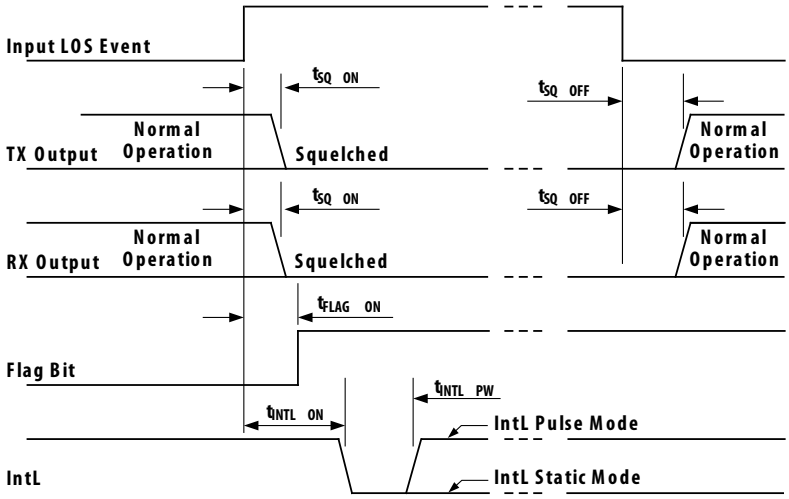


Figure 22. LOS Squelch Sequence

Package Outline, Host PCB Footprint and Panel Cutout

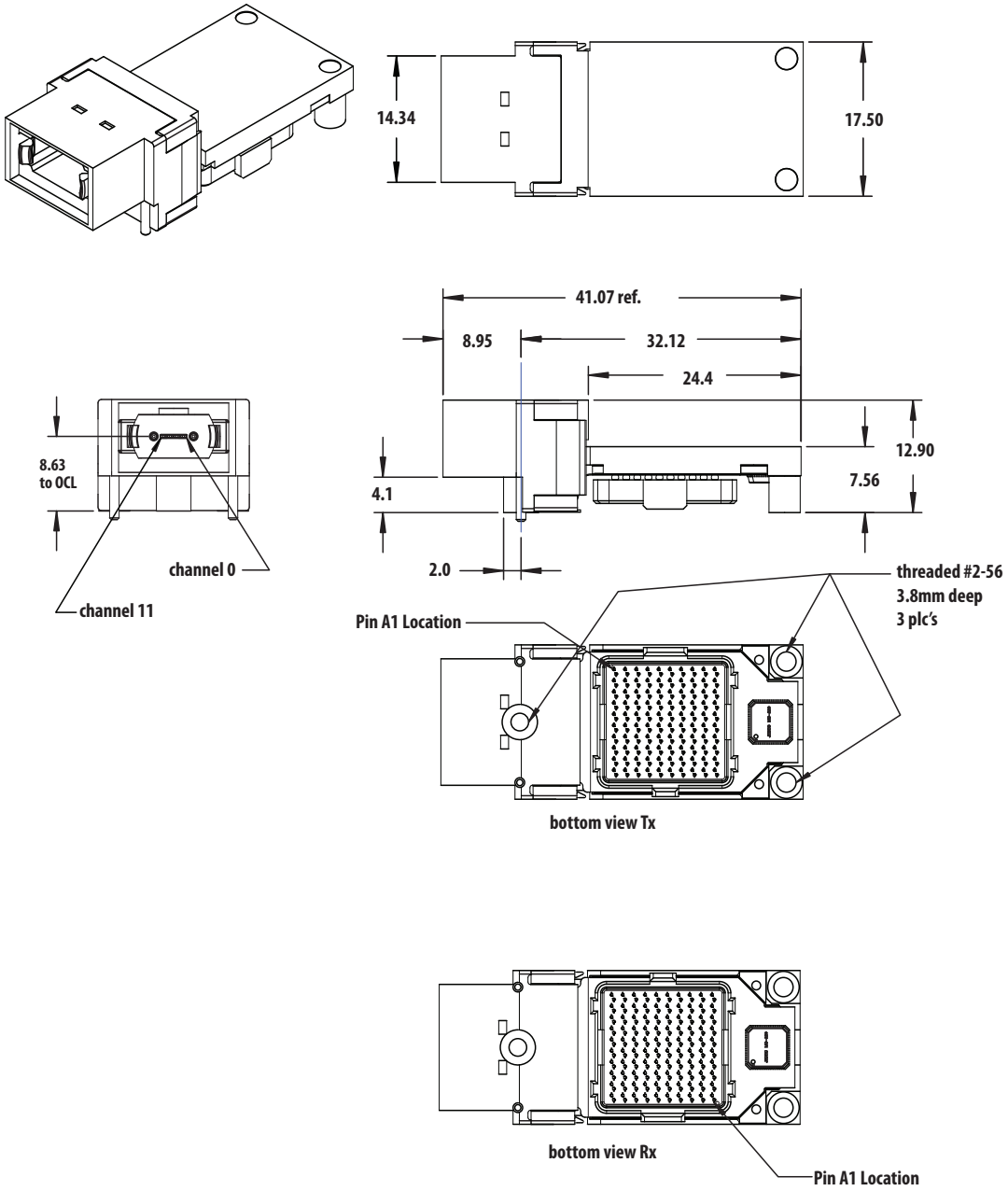


Figure 23. Package Outline AFBR-775BHZ and AFBR-785BHZ

Package outline dimensions are nominal expressed in mm unless otherwise stated. The mating host PCB mounted electrical connector is a 100 position FCI MEG-Array® Plug (FCI PN: 84512-102) or equivalent.

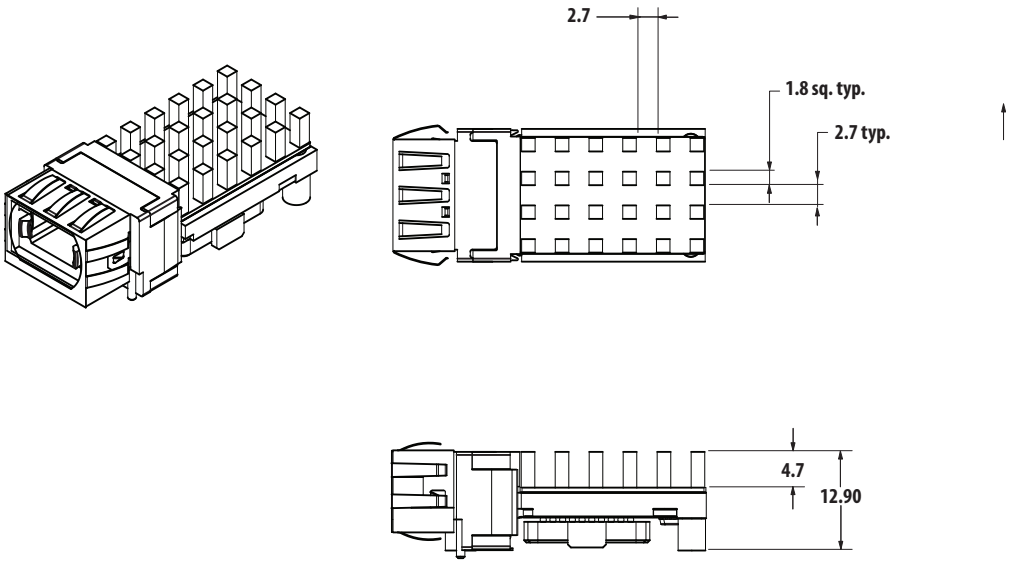


Figure 24. Package Outline AFBR-775BEPZ and AFBR-785BEPZ

Package outline dimensions are nominal expressed in mm unless otherwise stated. The mating host PCB mounted electrical connector is a 100 position FCI MEG-Array® Plug (FCI PN: 84512-102) or equivalent.

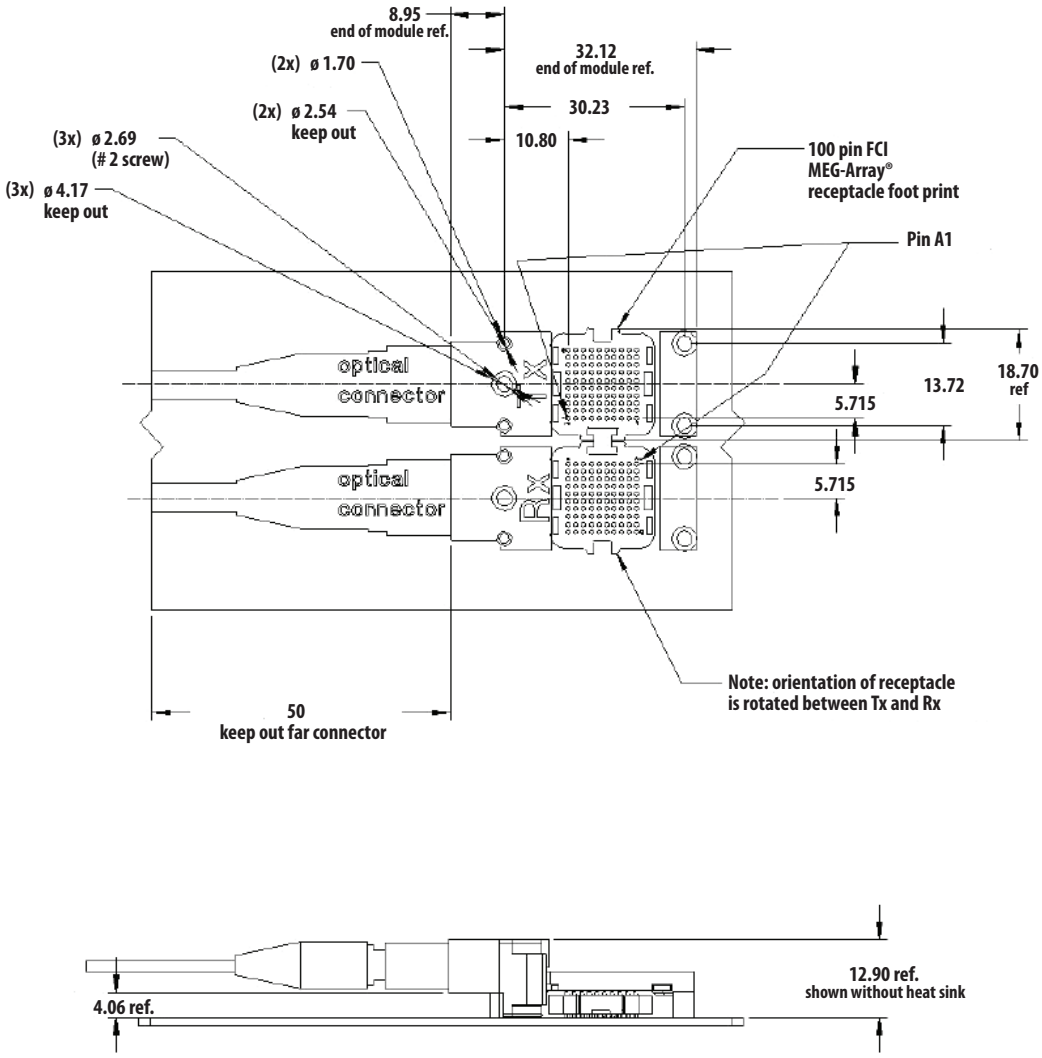


Figure 25. Host Board Module Footprint (Top View) and Module (Side View) – Mid-Plane Mount

Dimensions are nominal expressed in mm unless otherwise stated. The mating host PCB mounted electrical connector is a 100 position FCI MEG Array® Plug (FCI PN: 84512-102) or equivalent.

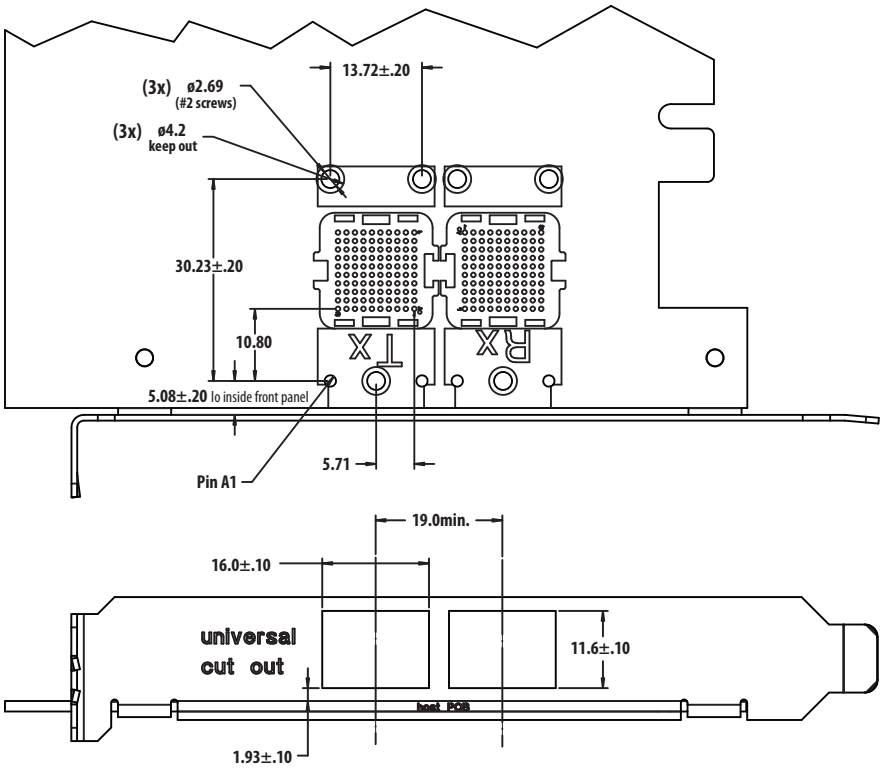


Figure 26. Host Board Module Footprint (Top and Side Views) – Panel Mount

Dimensions are nominal expressed in mm unless otherwise stated. The mating host PCB mounted electrical connector is a 100 position FCI MEG Array® Plug (FCI PN: 84512-102) or equivalent.

Control Interface & Memory Map

The control interface combines dedicated signal lines for address inputs, Adr[2:0], interrupt output, IntL, and reset input, ResetL, with two-wire serial, TWS, interface clock, SCL, and data, SDA, signals to provide users rich functionality over an efficient and easily used interface. The TWS interface is implemented as a slave device and compatible with industry standard two-wire serial protocol. It is scaled for 3.3 volt LVTTL. Outputs are high-z in the high state to support busing of these signals. Signal and timing characteristics are further defined in the Control I/O Characteristics section. In general, TWS bus timing and protocols follow the implementation popularized in Atmel Two-wire Serial EEPROMs. For additional details see, e.g., Atmel AT24C01A.

The address signals, Adr2, Adr1 and Adr0, provide the ability to program the TWS bus address of the module. The module address has the binary form 0101hjkx, where h, j and k correspond to Adr2, Adr1 and Adr0, respectively and x corresponds to the Read/Write command bit. Modules will respond to TWS bus addresses in the range of 50h to 5Fh (hereafter 5ih) depending upon the state of Adr2, Adr1 and Adr0. The address B0(h) should be avoided on the TWS bus where these modules are used.

An interrupt signal, IntL, is used to alert the host of a loss of input signal (LOS), transmitter fault conditions and/or assertion of any monitor flag. This reduces the need for dedicated status signal lines and polling the status and monitor registers while maintaining timely alerts to significant events. IntL can be programmed (page 01h byte 225 bit 0) to either pulse or static mode with pulse as the default mode.

A dedicated module reset signal, ResetL, is provided in case the TWS interface becomes dysfunctional. When ResetL is asserted, the outputs are disabled, TWS interface commands are inhibited and the module returns to factory default settings except Non-volatile Read-Write (RWn) registers which retain the last write. A module register (memory map except the non-volatile registers) reset can also be initiated over the TWS interface (page 5ih byte 91, bit 0). A TWS reset can be initiated by nine SLA clock cycles with SDA high in each cycle and creating a start condition.

With the TWS interface the user can read a status register (page 5ih byte 2) to see if data is available in the monitor registers, if the module has generated an IntL that has not been cleared and global status reports for loss of signal and fault conditions.

LOS, Tx fault and/or monitor flag registers can be accessed to check the status of individual channels or which channel may have generated a recent IntL. LOS, Tx fault and flag bits remain set (latched) after assertion even in the event the condition changes and operation resumes until cleared by the read operation of the associated registers or reset by ResetL or the TWS module reset function.

The user can read the present value of the various monitors. For transmitters and receivers, internal module temperature and supply voltages are reported. For transmitters, monitors provide for each channel laser bias current and laser light output power (LOP) information. For receivers, input power (Pave) is monitored for each channel. In addition, elapsed operating time is reported. All monitor items are two-byte fields and to maintain coherency, the host must access these with single two-byte read sequences. For each monitored item, alarm thresholds are established. If an item moves past a threshold, a flag is set, and, provided the item is not masked, IntL is asserted. The threshold settings are available in the upper memory page, 01h.

The user can select either a pulse or static mode for the interrupt signal IntL and initiate a module register reset. The user is provided the ability to disable individual channels. For transmitters, equalization levels can be independently set for individual channels. For receivers, output signal amplitude, de-emphasis levels and rate select can be independently set for individual channels. In the upper page, 01h, control field the user can invert the truth of the differential inputs for individual transmitter channel and for the differential outputs of individual receiver channels. In addition, the user can disable the output squelch function on an individual channel basis for both transmitters and receivers. For transmitters the user can, on an individual channel basis, activate a margin mode that reduces the output optical modulation amplitude for the channel.

All non-volatile control registers are located in the upper page 01(h). Non-volatile functions include the IntL mode selection bit, input and output polarity flip bits, transmitter equalization control bits, receiver output amplitude control and receiver output de-emphasis control. Entries into these registers will retain the last write for supply voltage cycles and for ResetL and module register resets.

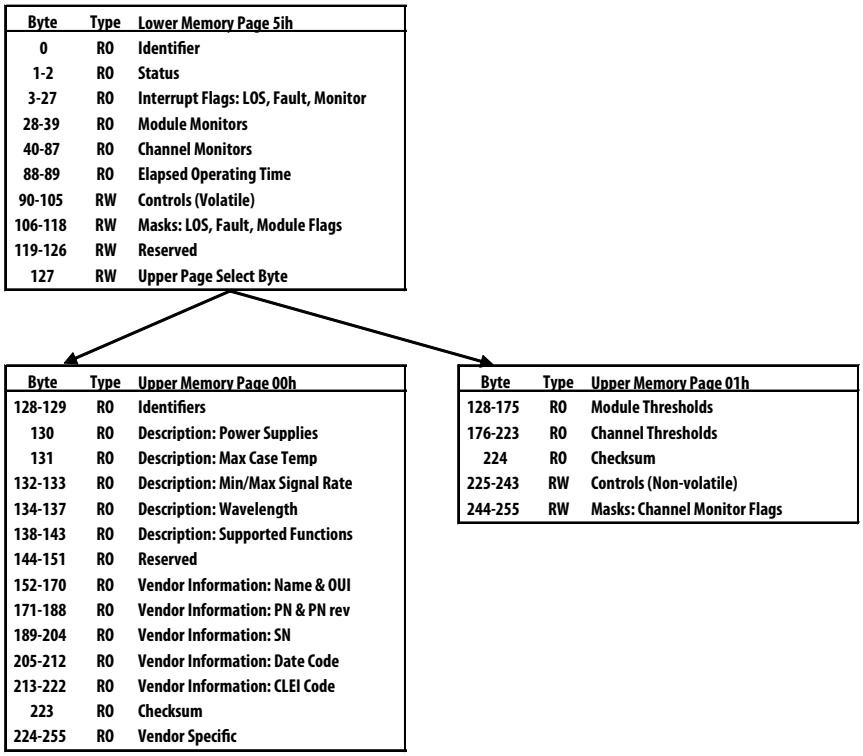
Volatile functions include module register reset, channel disable, squelch disable and margin activation.

A mask bit that can be set to prevent assertion of IntL for the individual item exists for every LOS, Tx fault and monitor flag. Mask fields for LOS, Tx fault and module monitors are in the lower memory page, 5ih, and the mask field for the channel monitors are in the upper page 01h. Entries in the mask fields are volatile.

Page 00h, based on the Serial ID pages of XFP and QSFP, provides module identity and information regarding the capabilities of the module.

Memory Map Overview

The memory is structured as a single address, multiple page approach after that in the XFP MSA and adapted by QSFP MSA for multi-channel transceivers. Figure 27 presents an overview of the memory structure showing a lower page (5ih) and two upper pages (00h and 01h). As with XFP and QSFP, time sensitive, dynamic and/or high interest information are contained in the base, i.e. lower, page. Here the upper page 00h contains the serial id information, again following the style of XFP and QSFP. The 01h upper table contains static threshold information, configuration controls and flag masks.



Byte	Type	Lower Memory Page 5ih
0	RO	Identifier
1-2	RO	Status
3-27	RO	Interrupt Flags: LOS, Fault, Monitor
28-39	RO	Module Monitors
40-87	RO	Channel Monitors
88-89	RO	Elapsed Operating Time
90-105	RW	Controls (Volatile)
106-118	RW	Masks: LOS, Fault, Module Flags
119-126	RW	Reserved
127	RW	Upper Page Select Byte

Byte	Type	Upper Memory Page 00h
128-129	RO	Identifiers
130	RO	Description: Power Supplies
131	RO	Description: Max Case Temp
132-133	RO	Description: Min/Max Signal Rate
134-137	RO	Description: Wavelength
138-143	RO	Description: Supported Functions
144-151	RO	Reserved
152-170	RO	Vendor Information: Name & OUI
171-188	RO	Vendor Information: PN & PN rev
189-204	RO	Vendor Information: SN
205-212	RO	Vendor Information: Date Code
213-222	RO	Vendor Information: CLEI Code
223	RO	Checksum
224-255	RO	Vendor Specific

Byte	Type	Upper Memory Page 01h
128-175	RO	Module Thresholds
176-223	RO	Channel Thresholds
224	RO	Checksum
225-243	RW	Controls (Non-volatile)
244-255	RW	Masks: Channel Monitor Flags

Figure 27 Two-Wire Serial Address 5ih Page Structure

Unless otherwise stated all reserved bytes are coded 00h and all reserved bits are coded 0b. Non-volatile read-write bits are labeled RWn and volatile read-write bits are labeled RWv.