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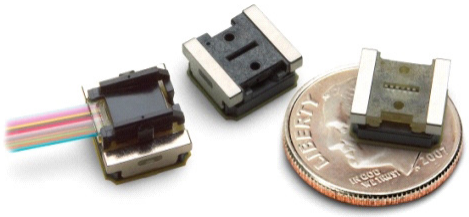
MicroPOD™
AFBR-77D13SZ, AFBR-78D13SZ
10 Gbps/Channel
Twelve Channel Parallel Fiber Optics Modules

Data Sheet



Description

The AFBR-77D13SZ Twelve Channel, Pluggable, Parallel Fiber Optics Transmitter and AFBR-78D13SZ Twelve Channel, Pluggable, Parallel Fiber Optics Receiver are high performance fiber optics modules for short-range parallel multi-lane data communication and interconnect applications. The high density optical modules are designed to operate over multimode fiber systems using a nominal wavelength of 850 nm.

The optical interface requires the user to provide a custom designed optical turn 1×12 ribbon cable PRIZM® LightTurn® connector.

Applications

- 100GbE, 10GbE and IB-QDR/ IB-DDR/ IB-SDR interconnects
- Data Aggregation, Backplane and Proprietary Protocol and Density Applications
- High Performance and High Productivity computer interconnects
- Switch Fabric interconnects

Part Number Ordering Options

	Base Part Number	
Modules for use with Flat Ribbon Jumper Cable	**Transmitter**	AFBR-77D13SZ
	Receiver	AFBR-78D13SZ
MicroPOD Evaluation Board (Tx)		AFBR- 77EVB
MicroPOD Evaluation Board (Rx)		AFBR- 78EVB

Where:
77 = Transmitter;
78 = Receiver

Features

- Compliant to IEEE 802.3ba 100GbE (100GBASE-SR10 and nPPI) per lane and compatible with 10GBASE-SR
- Compliant to 12×QDR Infiniband
- Operates at 10.3125 Gbps per channel with 64b/66b encoded data for 100GbE application and with 8b/10b for 10GbE applications. Supports 10 Gbps with 8b/10b for IB-QDR applications
- High Aggregate bandwidth: 120 Gbps per module
- High density footprint: 7.8 mm × 8.2 mm × 3.9 mm size
- Separate transmitter and receiver modules;
- 850 nm VCSEL array in transmitter; PIN array in receiver
- 10.3125 Gbps links up to 300 m & 400 m with OM3 & OM4 4700 MHz·km 50 µm MMF
- Optical Interface: PRIZM™ LightTurn® optical turn 1×12 ribbon fiber connector
- Electrical interface: 9×9 micro-LGA with 0.7424 mm pitch
- Low Power consumption: 3.0 W Max per Transmitter / Receiver pair (0 °C to 70 °C operating range)
- Dedicated signals for module address, module reset and host interrupt
- Two Wire Serial (TWS) interface with maskable interrupt for expanded functionality including:
  - Individual channel functions: disable, squelch disable, lane polarity inversion, TX eye margin enable
  - A/D read back: module temperature and supply voltages, per channel laser current and laser power, or received power
  - Status: per channel Tx fault, electrical (transmitter) or optical (receiver) LOS, and alarm flags
  - Programmable equalization integrated with DC blocking caps at transmitter data input
  - Programmable receiver output swing and de-emphasis level
  - Field-upgradable firmware capability
- 0 °C to 70 °C case temperature continuous operating range. 85 °C supported for short durations

Patent - www.avagotech.com/patents

Transmitter Module

The optical transmitter module (see Figure 1) incorporates a 12-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 12-channel input buffer and laser driver, diagnostic monitors, control and bias blocks. The transmitter is designed for EN-60825 and CDRH eye safety compliance; Class 3R out of the module. When fully assembled with the PRIZM LightTurn optical connector class 1M is achieved. The Tx Input Buffer provides CML compatible differential inputs (presenting a nominal differential input impedance of 100Ω and a nominal common mode impedance to signal ground of 25 Ω) for the high speed electrical interface that can operate over a wide common mode range without requiring external DC blocking capacitors. For module control and interrogation, the control interface incorporates a Two Wire Serial (TWS) interface of clock and data signals and dedicated signals for host interrupt, module address setting and module reset. Diagnostic monitors for VCSEL bias, light output power (LOP), temperature, both supply voltages and elapsed operating time are implemented and results are available through the TWS interface.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential inputs, deactivate channels, place channels into margin mode (system level diagnostic mode where TX OMA is reduced by ~1 dB), disable the squelch function and program input equalization levels to reduce the effect of long PCB traces. A reset for the control registers is available. Serial ID information and alarm thresholds are provided. To reduce the need for polling, the TWS interface is augmented with an interrupt signal for the host.

Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of input signal (LOS) and transmitter fault conditions. All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset by reading the appropriate flag register. The optical output will squelch for loss of input signal unless squelch is disabled. Fault detection or channel deactivation through the TWS interface will disable the channel. Status, alarm and fault information are available via the TWS interface. The interrupt signal (selectable via the TWS interface as a pulse or static level) is provided to inform hosts of an assertion of an alarm, LOS and/or Tx fault.

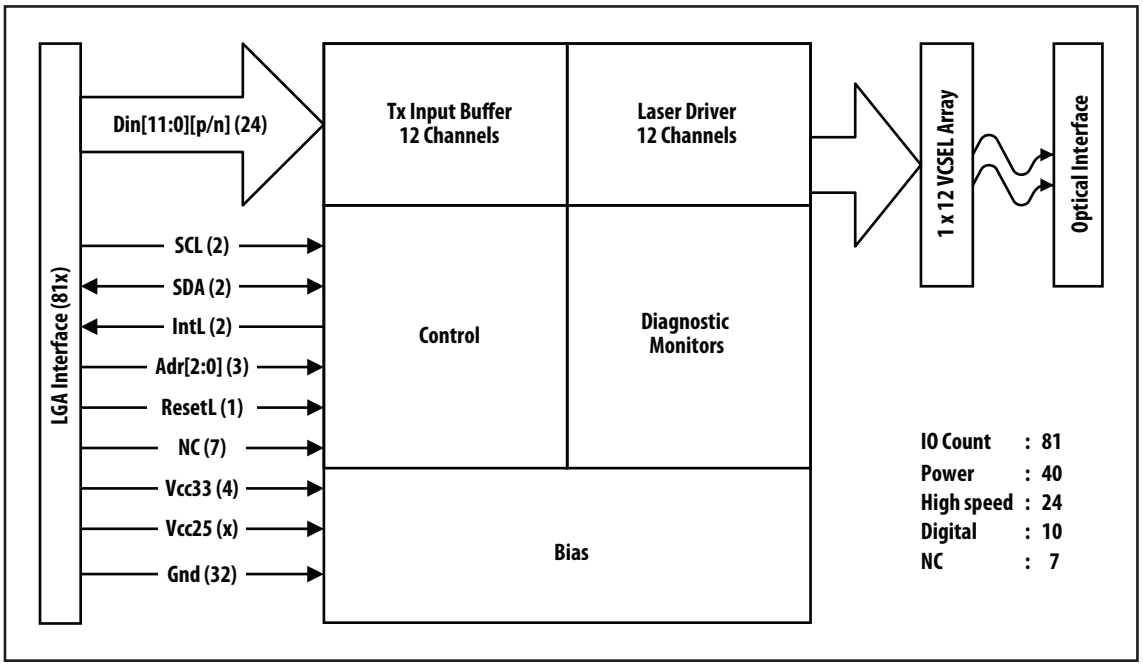


Figure 1. Transmitter Block Diagram

Receiver Module

The optical receiver module (see Figure 2) incorporates a 12-channel PIN photodiode array, a 12-channel pre-amplifier and output buffer, diagnostic monitors, control and bias blocks. The Rx Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50Ω to AC ground and 100Ω differentially that should be differentially terminated with 100 Ω. External DC blocking capacitors are required. For module control and interrogation, the control interface incorporates a Two Wire Serial (TWS) interface of clock and data signals and dedicated signals for host interrupt, module address setting and module reset. Diagnostic monitors for optical input power, temperature, both supply voltages and elapsed operating time are implemented and results are available through the TWS interface.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential outputs, deactivate channels, disable the squelch function, program output signal amplitude and de-emphasis and change receiver bandwidth. A reset for the control registers is available. Serial ID information and alarm thresholds are provided. To reduce the need for polling, the TWS interface is augmented with an interrupt signal for the host.

Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of optical input signal (LOS). All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register. The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through TWS interface. Status and alarm information are available via the TWS interface. The interrupt signal (selectable via the TWS interface as a pulse or static level) is provided to inform hosts of an assertion of an alarm and/or LOS.

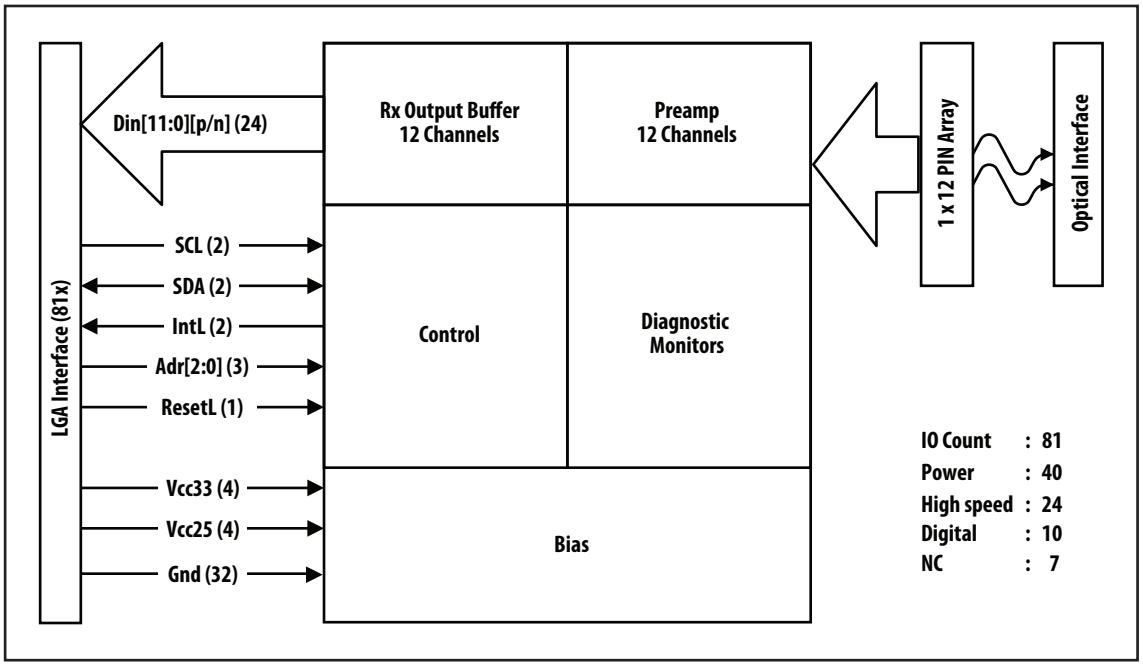


Figure 2. Receiver Block Diagram

High Speed Signal Interface

Figure 3 shows the interface between an ASIC/SerDes and the fiber optics modules. For simplicity, only one channel is shown. As shown in Figure 3, the compliance points are on the host board side of the electrical connectors. Sets of s-parameters are defined for the transmitter and receiver interfaces. The transmitter and receiver are designed, when operating within Recommended Operating Conditions, to provide a robust eye-opening at the receiver outputs. See the Recommended Operating Conditions and the Receiver Electrical Characteristics for details.

Unused inputs and outputs should be terminated with 100 Ω differential loads.

The transmitter inputs support a wide common mode range and DC blocking capacitors are not needed (internal capacitors are not shown in Figure 3). Depending on the common mode range tolerance of the ASIC/SerDes inputs, DC blocking capacitors may be required in series with the receiver; in this case 100nF capacitors are recommended. Differential impedances are nominally 100 Ω. The common mode output impedance for the receiver is nominally 25 Ω while the nominal common mode input impedance of the transmitter is 25 Ω.

Transmitter Input Equalization

Transmitter inputs can be programmed for one of several levels of equalization. See Figure 4. The default case provides a flat gain-frequency response in the inputs. Different levels of compensation can be selected to equalize skin-effect losses across the host circuit board. See Tx Memory Map 01h Upper Page section addresses 228 - 233 for programming details.

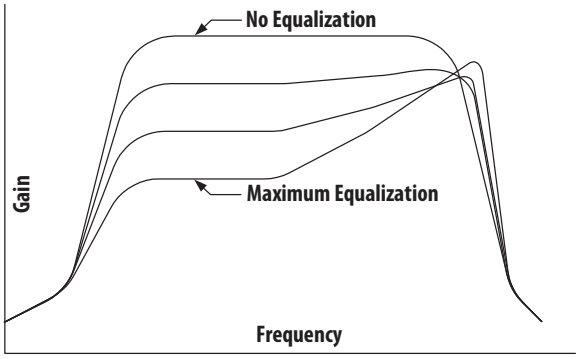


Figure 4. Transmitter Input Equalization

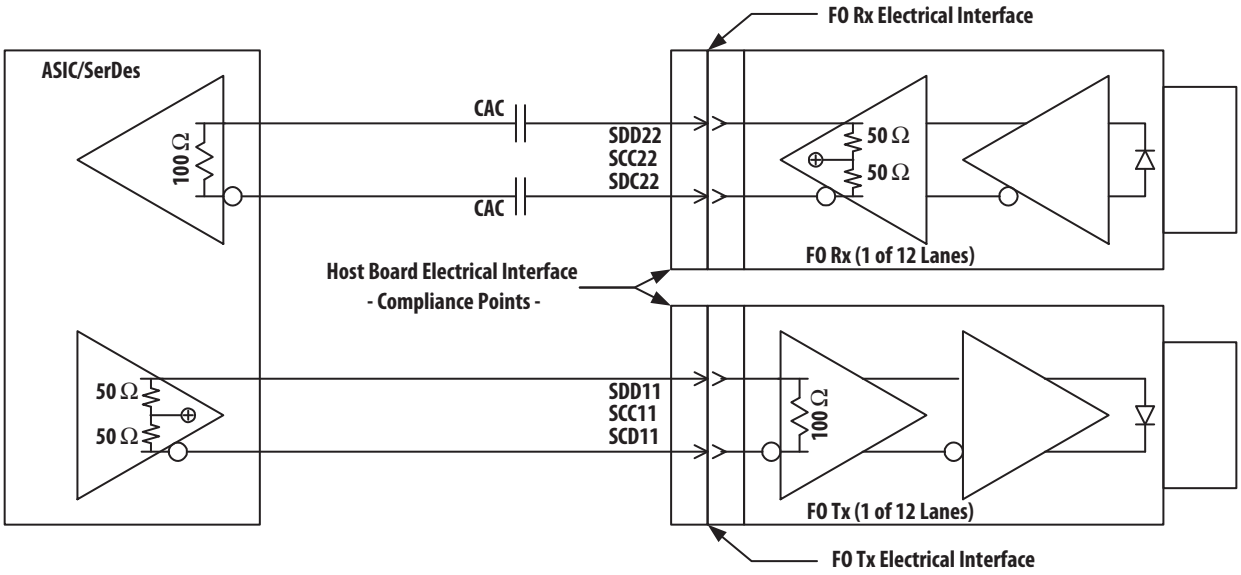


Figure 3. Application Reference Diagram

Receiver Output Amplitude and De-emphasis

Receiver outputs can be programmed to provide several levels of amplitude and de-emphasis. See Figure 5 for de-emphasis definition. The user can program for peak-to-peak amplitude and then a de-emphasis level. If zero de-emphasis is selected, then the signal steady state equals the peak-to-peak level. For other levels of de-emphasis the selected de-emphasis reduces the steady-state from the peak-to-peak level. The change from peak-to-peak level to steady-state occurs within a bit time. See Rx Memory Map 01h Upper Page section addresses 228 - 233 for amplitude programming details and addresses 234 – 239 for de-emphasis programming details.

Control Signal Interface

The control interface includes dedicated signals for address inputs, interrupt output and reset input, and bidirectional clock and data lines, for a two-wire serial access (TWS interface) to control, status and information registers. The TWS interface is compatible with industry standard two-wire serial protocol. The MicroPOD module is implemented as a slave device. Signal and timing characteristics are further defined in the Control Characteristics and Control Interface and Memory Map sections.

The registers of the serial interface memory are defined in the Control Interface and Memory Map section.

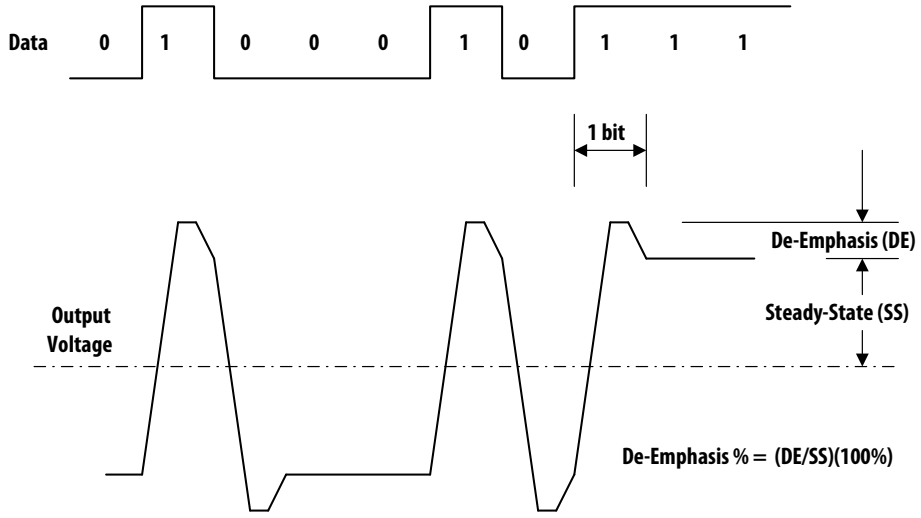


Figure 5. Definition of De-emphasis and Steady State

Link Model and Reference Channel

Performance specifications for the MicroPOD modules based on IEEE 802.3ba 100GBASE-SR10.

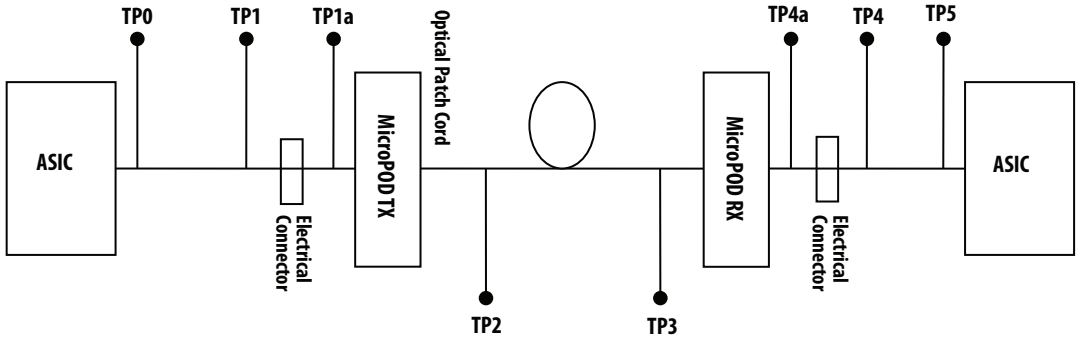


Figure 6. Link Model test point definitions

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operation Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

The TX and RX modules are not hermetically packaged, exposure to a condensing environment is not allowed.

Notice that both TX and RX Cu blocks (heat sink) are electrically connected to signal GND. There is no separated module case GND. Care must be taken when handling the modules.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_s	-40	85	°C	
Absolute Maximum Operating Temperature		-20	85	°C	Note 1
2.5 V Power Supply Voltage	V_{cc25}	-0.5	3.0	V	
3.3 V Power Supply Voltage	V_{cc33}	-0.5	4.0	V	
Data Input Voltage – Single Ended		-0.5	V_{cc33}+0.5, V_{cc25}+0.5, 4.0	V	Least of the three
Data Input Voltage – Differential	$\|V_{DIp} - V_{DIn}\|$		1.0	V	Note 2
Control Input Voltage	V_i	-0.5	V_{cc33}+0.5, 4.0	V	Note 3
Control Output Current	I_o	-20	20	mA	
Relative Humidity	RH	5	95	%	Note 4
Receiver Damage Threshold	Rx_P_{MAX}		+4	dBm	

Notes:
1. The position for case temperature measurement is shown in Figure 22. Electro-optical specifications are not guaranteed outside the recommended operating temperature range. Operation above the Absolute Maximum Case Temperature for extended periods may adversely affect reliability.
2. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry.
3. The maximum limit is the lesser of V_{cc} + 0.5 V or 4.0 V. SDA and SCL may be forced to <=4V for any V_{cc33} value. Note that both 1.2V CMOS and LVTTL logic is tolerant of voltage up to V_{cc33}+0.5.
4. Exposure to a condensing environment is not allowed.

Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Case Temperature	T_c	0		70	°C	Note 1
Case Temperature (short term)	T_{c_ext}	70		85	°C	Note 2
2.5 V Power Supply Voltage	V_{cc25}	2.375	2.5	2.625	V	Note 3
3.3 V Power Supply Voltage	V_{cc33}	3.135	3.3	3.465	V	
Signal Rate per Channel (rates < 3.125 Gb/s must be 8b/10b encoded)		1.25		10.3125	GBd	Note 4
Host Electrical Compliance		Per IEEE 802.3ba-2010 TP1a and TP4 nPPI specifications for host				
Control Input Voltage High	V_{ih}	2.3		3.6	V	
Control Input Voltage Low	V_{il}	-0.3		0.4	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Two Wire Serial Interface Write Cycle Time (up to 2 sequential bytes)	t_{WC}	100			ms	
Reset Pulse Width	$t_{RSTL\ PW}$	10			µs	
Power Supply Noise				100	mVpp	Note 5, 500 Hz to 5.4 GHz
Receiver Differential Data Output Load			100		Ω	Figure 3
AC Coupling Capacitors – Receiver Data Outputs	C_{ac}		0.1		µF	Note 6, Figure 3
Fiber Length: 4700 MHz·km 50 µm MMF (OM4) 2000 MHz·km 50 µm MMF (OM3)		0.5 0.5		400 300	m m	Note 7
Fiber Pull Force (long duration**)				0.98	N	
Fiber Pull Force (short duration*)				2.2	N	
PRIZM Insertion Force (short duration*)				40	N	

* Short duration is <15 seconds.

** Long duration (>5 minutes), exceeding this force long term could cause the optical light output power to drop or Rx sensitivity to diminish, which is not recoverable.

Notes:

1. Continuous operation above 70 °C should be avoided in order not to degrade reliability. The position for case temperature measurement is shown in Figure 22.
2. Short term is defined per section 4.1.2 of Telcordia GR-63-CORE Issue 3, March 2006 and corresponds to a period of not more than 96 consecutive hours and a total of not more than 15 days in 1 year (This refers to a total of 360 hours in any given year, but no more than 15 occurrences during that 1-year period).
3. There are no restrictions to the 2.5 V and 3.3 V power supply sequencing.
4. Higher data rates are possible. For further details, contact your Avago sales representative.
5. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 8 for recommended power supply filters.
6. For data pattern with restricted run lengths and disparity, e.g., 8b10b, smaller value capacitors may provide acceptable results.
7. Channel insertion loss includes 3.5 dB/km attenuation, 1.5 dB connector loss and 0.3 dB modal noise penalty allocations.

Transmitter Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_c = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V. Note: The TX output performance is only guaranteed when measured with a differential input that meets the recommended operating conditions. A link driven with a single-ended signal will degrade the jitter performance.

Parameter	Symbols	Min	Typ	Max	Units	Reference
Power Consumption (Max EQ)			1.2	1.6	W	Note 1
Power Supply Current - V_{cc25}			280	365	mA	Note 2
Power Supply Current - V_{cc33}			105	185	mA	Note 3
Differential Input Impedance		85	100	115		Informative
LOS Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	$\Delta V_{DI\ PP\ LOS}$	50			mVpp	Informative
LOS De-Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	$\Delta V_{DI\ PP\ LOS}$			210	mVpp	Note 4, Informative
LOS Hysteresis		0.5		4	dB	
Power On Initialization Time	$t_{PWR\ INIT}$		350	2000	ms	Note 5
Parameter	**Test Point**	**Min**	**Typ**	**Max**	**Units**	**Reference**
Single ended input voltage tolerance	TP1a	-0.3		4.0	V	Note 6
AC common mode input voltage tolerance	TP1a	15			mV	RMS
Differential input return loss	TP1				dB	Note 7, 10 MHz to 11.1 GHz
Differential to common-mode input return loss	TP1	10			dB	10 MHz to 11.1 GHz
J2 Jitter tolerance	TP1a	0.17			UI	Defined in 802.3ba
J9 Jitter tolerance	TP1a	0.29			UI	Defined in 802.3ba
Data Dependent Pulse Width Shrinkage (DDPWS) tolerance	TP1a	0.07			UI	Defined in 802.3ba
Eye Mask Coordinates: X1, X2, Y1, Y2	TP1a		 0.11, 0.31 95, 350		 UI mV	Note 8, Hit Ratio = $5x10^{-5}$

* For control signal timing including Adr[2:0], IntL, ResetL, SCL and SDA see Control Characteristics: Transmitter/Receiver.

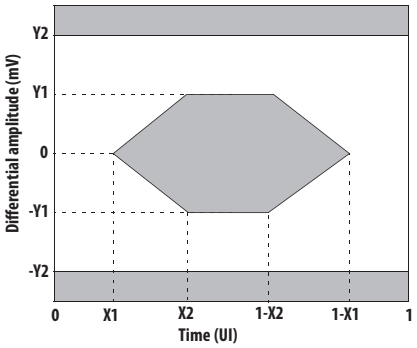
Notes:

1. Max power is 1.7 W above 70 °C, to 85 °C case temperature.
2. Supply current includes that of all V_{cc25} contacts.
3. Supply current includes that of all V_{cc33} contacts. Max current is 210 mA above 70 °C, to 85 °C case temperature.
4. Tx data input must conform to IEEE 802.3ba-2010 TP1a electrical host compliance specification.
5. Power On Initialization Time is the time from when the supply voltages reach and remain above the minimum Recommended Operating Conditions to the time when the module enables TWS access. The module at that point is fully functional.
6. Referred to TP1 signal common; The single-ended input voltage tolerance is the allowable range of the instantaneous input signals.
7. From 10 MHz to 11.1 GHz, the magnitude in decibels of the module differential input return loss at TP1 and the host differential output return loss at TP1a shall not exceed the limit given in Equation

   Return_loss (f) ≥ 12 – 2√(f) 0.01 ≤ f < 4.1 dB

   ≥ 6.3 – 13log10(f/5.5) 4.11 ≤ f < 11.1 dB

   Return_loss (f) is the return loss at frequency f

   f is the frequency in GHz
8. 

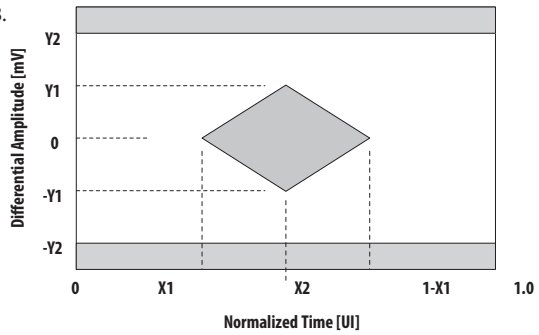
Tx Electrical Eye Mask Coordinates (TP1a) at Hit ratio 5 x 10^{-5} hits per sample

Receiver Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_c = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V. Note: The RX output performance is only guaranteed when measured with a differential output that meets the recommended operating conditions. A link driven with a single-ended signal will degrade the jitter performance.

Parameter	Test Point	Min	Typ	Max	Units	Reference
Power Consumption			1.1	1.4	W	Note 1
Power Supply Current (V_{cc25}) - @ Default De-emphasis / Default output swing			350	425	mA	Note 2
Power Supply Current (V_{cc33}) - @ Default De-emphasis / Default output swing			48	90	mA	Note 3
Power Supply Current (V_{cc25}) - @ Max De-emphasis/Max output swing			430	525	mA	Note 2
Power Supply Current (V_{cc33}) - @ Max De-emphasis/Max output swing			48	90	mA	Note 3
Data Output Differential Peak-to-Peak Voltage Swing (Default De-emphasis)	TP4	400	500	600	mVpp	Note 4, 100 Ω Load (default setting)
Data Output Common Mode Voltage	TP4	2.0		2.540	V	Over Amplitude Range
AC common-mode output voltage (RMS)	TP4			7.5	mV	
Termination mismatch at 1 MHz	TP4			5	%	
Differential Output Impedance	TP4	85		115		Informative
Differential Output Return Loss, 10M-11.1 GHz	TP4				dB	Note 5
CM to Differential Mode Conversion, 0.1G-11.1 GHz	TP4				dB	Note 6
Power On Initialization Time			288	2000	ms	
Output transition time (20% to 80%)	TP4	28			ps	
J2 Jitter Output	TP4			0.42	UI	Defined in 802.3ba
J9 Jitter Output	TP4			0.65	UI	Defined in 802.3ba
Data Dependent Pulse Width Shrinkage	TP4			0.34	UI	Defined in 802.3ba
Inter-channel Skew	TP4			11	ns	
Inter-channel Skew Variation	TP4		100		ps	Note 7
			Specification Values			
Eye Mask Coordinates: X1, X2, Y1, Y2	TP4		0.29, 0.5 150, 425		UI mV	Note 8, Hit Ratio = $5x10^{-5}$

Notes:

1. Max conditions include default output amplitude and de-emphasis programming.
2. Supply current includes that of all V_{cc25} contacts.
3. Supply current includes that of all V_{cc33} contacts.
4. See section on page 47 "Receiver Output Amplitude Control Code Description" for range of voltages defined in the receiver upper page 01h, address range 228 to 233. Data outputs are CML compatible. Data Output Differential Peak to Peak Voltage Swing is defined as follows: ΔVDO pp = ΔVDOH - ΔVDOL where ΔVDOH = High State Differential Data Output Voltage and ΔVDOL = Low State Differential Data Output Voltage. Output voltage swing is adjustable via TWS interface.
5. From 10MHz to 11.1 GHz. The magnitude in decibels of the module differential output return loss at TP4 and the host differential input return loss at TP4a shall not exceed the limit given in Equation
   Return_loss (f) 12 -2√(f) 0.01 ≤ f < 4.1 dB
   ≥ 6.3 - 13log10(f/5.5) 4.11 ≤ f < 11.1 dB
6. From 10 MHz to 11.1 GHz. The magnitude in decibels of the host common mode output return loss at TP4 shall not exceed the limit given in Equation:
   Return_loss (f) ≥ 7 - 1.6f 0.01 ≤ f < 2.5 dB
   ≥ 3 2.5 ≤ f < 11.1 dB
   f is the frequency in GHz
7. Inter-Channel Skew is defined for the condition of equal amplitude, zero ps skew input signals at TP1a.
8. 

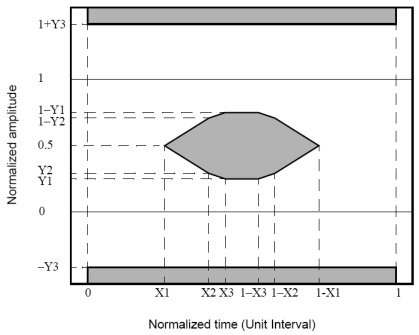
Rx Electrical Eye Mask Coordinates (TP4) at Hit ratio 5 x 10^{-5} hits per sample

Transmitter Optical Characteristics [1]

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_c = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V. Test point = TP2. Note that the TX output performance is only guaranteed with a differential input that meets the recommended operating conditions. A link driven with a single-ended signal will degrade the jitter performance.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Center Wavelength	λ_c	840	850	860	nm	
RMS spectral width			0.35	0.65	nm	Note 2
Average launch Power, each lane	$P_{O\ AVE}$	-7.6		2.4	dBm	
Output Optical Power: Disabled	$P_{O\ OFF}$			-30	dBm	
Extinction Ratio	ER	3			dB	
Optical Modulation Amplitude, each lane	OMA	-4.3		2.4	dBm	Note 3
Output Power (Squelched OMA)		-2.4			dBm	AC Squelch
Tx Mask Margin	Tx_MM		10%			
Difference in launch power between any two lanes (OMA)				4	dB	
Peak power, each lane				4	dBm	
Launch Power in OMA minus TDP, each lane	Po - TDP	-6.5			dBm	
Transmitter and Dispersion Penalty, each lane	TDP			3.5	dB	
Optical return loss tolerance				12	dB	
Encircled flux			≥ 86% at 19 µm, ≤ 30% at 4.5 µm			Note 4
			Specification Values			
Eye mask coordinates: X1, X2, X3 Y1, Y2, Y3			0.23, 0.34, 0.43 0.27, 0.35, 0.4		UI	Note 5, Hit ratio = $5x10^{-5}$ per sample
Power On Initialization Time Tx Outputs	$t_{PWR\ INIT}$		350	2000	ms	
Reset De-assert Re-initialization Time Tx Outputs	$t_{RSTL\ OFF}$		350	2000	ms	
Output Disable Assert Time for Fault	$t_{DIS\ ON}$		9	100	ms	
Output Squelch Assert Time for LOS	$t_{SQ\ ON}$		52	80	µs	
Output Squelch De-assert Time for LOS	$t_{SQ\ OFF}$		49	80	µs	

Notes:
1. These optical specifications are dependent upon the performance of the PRIZM LightTurn to cable assembly, which assumes a maximum of 2 dB insertion loss. More details are provided on the PRIZM LightTurn cable assembly specification. Please contact your Avago sales representative to receive this specification.
2. RMS spectral width is the standard deviation of the spectrum.
3. Output of user provided fiber connector. Even if the TDP<0.9 dB, the OMA must exceed this minimum value. Power exceeds IEEE802.3ae but Avago SFP+ transceivers are compatible with this higher receiver input power. Note the possibility of high optical power DMI alarms on SFP+ Receivers
4. Compliance assured up to 10.3125 Gbps.



Mask Coordinates

X1 = 0.23
X2 = 0.34
X3 = 0.43
Y1 = 0.27
Y2 = 0.35
Y3 = 0.40

Transmitter eye mask definitions (TP2) at Hit ratio 5 x 10^{-5} hits per sample

Receiver Optical Characteristics [1]

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_c = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V.

Parameter	Test Point	Min	Typ	Max	Units	Reference
Optical Modulation Amplitude (OMA), each lane	TP3			+3	dBm	
Stressed Sensitivity (OMA), each lane	TP3			-5.4	dBm	Note 2
Receiver Sensitivity (OMA)	TP3	-12			dBm	Informative
Operating Center Wavelength	TP3	840		860	nm	
Receiver Reflectance	TP3			-12	dB	
Peak Power, each lane	TP3			+4	dBm	
Output Rise/Fall time (20-80%)	TP3	25	40	50	ps	Note 3
LOS to Data Output Squelch Assert Time	TP3			80	µs	Note 4
Data Output Squelch De-assert Time	TP3			80	µs	Note 5
LOS ASSERT Threshold (OMA)	TP3	-30	-14		dBm	
LOS De-ASSERT Threshold (OMA)	TP3		-12.4	-8	dBm	
LOS Hysteresis	TP3	0.5	1.6		dB	

Notes:
1. These optical specifications are dependent upon the performance of the PRIZM LightTurn cable assembly, which assumes a maximum of 2 dB insertion loss. More details are provided on the PRIZM LightTurn cable assembly specification. Please contact your Avago sales representative to receive this specification.
2. Measured with conformance test signal at TP3 for BER = 10e-12.
3. These are unfiltered rise and fall times without de-emphasis measured between the 20% and 80% levels using a 500 MHz square wave test pattern. Impairments in measurements due to the test system are removed. Specifications are for information only.
4. This is the module response time from fall of Rx input to less than Rx input LOS threshold to squelch of Rx outputs.
5. This is the module response time from rise of Rx input to greater than Rx input LOS threshold to resumption of Rx outputs.

100GBASE-SR10 Illustrative Link Power Budgets

Parameter	OM3	OM4	Units	Reference
Effective Modal Bandwidth at 850 nm	2000	4700	MHz•km	
Launch Power in OMA minus TDP, each lane	-6.5		dBm	
Transmitter and Dispersion Penalty, each lane	3.5		dB	
Receiver Sensitivity (OMA)	-11.3		dBm	
Power Budget (for maximum TDP)	8.3		dB	
Operating Distance	0.5 to 100	0.5 to 150	m	
Channel Insertion Loss	1.9	1.5	dB	
Allocation for Penalties (for max. TDP)	6.4	6.5	dB	
Unallocated Margin	0	0.3	dB	
Additional Insertion Loss Allowed	0		dB	

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	Transmitter and Receiver modules withstand minimum 1000 V on all pins.
	JEDEC Machine Model (MM) (JESD22-A115-A)	Transmitter and Receiver modules withstand minimum 50 V on all pins.
Immunity	Variation of EN 61000-4-3	Typically minimum effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing	EN 60825-1:2007 CFR21 section 1040	P_{out}: IEC AEL and US FDA CDRH Class 3R* without optical connector, Class 1M with optical connector. CDRH Accession Number: 1020008-001 TUV Certificate Number: R72131700
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File Number: E173874
RoHS Compliance (RoHS Directive 2002/95/EC issued January 27, 2003)	BS EN 1122:2001 Mtd B by ICP for Cadmium, EPA Method 3051A by ICP for Lead and Mercury, EPA Method 3060A and 7196A by UV/Vis Spectrophotometry for Hexavalent Chromium. EPA Method 3540C/3550B by GC/MS for PPB and PBDE BS EN method by ICP and EPA methods by ICP, UV/Vis Spectrophotometry and GC/MS.	Less than 100 ppm of cadmium, Less than 1000 ppm lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl esters.

The following regulatory compliance depends on customer system design. It is the customer's responsibility to guarantee the performance at the system level.

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to Optical Connector Receptacle	Variation of IEC 61000-4-2	Not applicable. Actual performance dependent on user system design.
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	Not applicable. Actual performance dependent on enclosure design.
Immunity	Variation of IEC 61000-4-3	Not applicable. Actual performance dependent on enclosure design.

WARNING:

CAUTION! Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure

CAUTION! Laser Class 3R for laser module assembly without fiber optic cable attachment.

INVISIBLE LASER RADIATION, AVOID DIRECT EYE EXPOSURE!
CLASS 3R LASER PRODUCT WITHOUT OPTIC CABLE ASSEMBLY

IEC IEC60825-1:2007
COMPLIES WITH 21 CFR 1040.10 AND 1040.11
EXCEPT FOR DEVIATIONS PERSUANT TO LASER NOTICE NO. 50, DATED JUNE 24, 2007

WARNING:

CAUTION! Laser Class 1 Classification for laser module assembly including fiber optic cable attachment. Safe to view laser output with the naked eye or with the aid of typical magnifying optics (e.g., telescope or microscope).

INVISIBLE LASER RADIATION, DO NOT VIEW DIRECTLY WITH OPTICAL INSTRUMENTS.
CLASS 1 LASER PRODUCT WITH OPTIC CABLE ASSEMBLY.

Note: Standard used for classification: EN 60825-1:2007

Transmitter / Receiver Module Contact Assignment and Signal Description

Optical Fiber Exit Side

	1	2	3	4	5	6	7	8	9
A	GND	D2+	GND	D4+	GND	D6+	GND	D8+	GND
B	GND	D2-	GND	D4-	GND	D6-	GND	D8-	GND
C	GND	GND	ADR<2>	Vcc33	NC<3>	Vcc33	NC<2>	GND	GND
D	D0+	D0-	Vcc33	SDA	INTL	SDA	Vcc33	D10-	D10+
E	GND	GND	ADR<1>	SCL	NC<4>	SCL	NC<1>	GND	GND
F	D1+	D1-	Vcc25	RESET	INTL	NC<6>	Vcc25	D11-	D11+
G	GND	GND	ADR<0>	Vcc25	NC<5>	Vcc25	NC<0>	GND	GND
H	GND	D3-	GND	D5-	GND	D7-	GND	D9-	GND
J	GND	D3+	GND	D5+	GND	D7+	GND	D9+	GND

Figure 7. TX / RX Host Board Pattern – Top View

Signal Name	Signal Description	I/O	Type
Adr[2:0]	TWS Module Bus Address bits: Address has the form 0101hjkx where Adr2, Adr1 and Adr0 correspond to h, j and k respectively and x corresponds to the R/W command (0 for Write, and 1 for Read). Adr[2], Adr[1] and Adr[0] are pulled down to GND through 40 to 125 µA current source inside TX module.	I	3.3 V LVTTL
D[11:0]+	Module Data Non-inverting Input / Output for channels 11 through 0	I	CML
D[11:0]-	Module Data Inverting Input/ Output for channels 11 through 0	I	CML
NC<6:0>	Reserved – Do Not Connect to any electrical potential on Host PCB		
GND	Signal Common: All module voltages are referenced to this potential unless otherwise stated. Connect these pins directly to the host board signal ground plane.		
IntL	Interrupt signal to Host, Asserted Low: An interrupt is generated in response to any Fault condition, loss of input signal or assertion of any monitor Flag. It may be programmed through the TWS interface to generate either a pulse or static level with static mode as default. This output presents a High-Z condition when IntL is de-asserted and requires a pull-up on the Host board. Pull-up to the Host 3.3 V supply is required.	O	3.3 V LVTTL, high-Z or driven to 0 level
ResetL	Reset signal to module, Asserted Low: When asserted the optical outputs are disabled, TWS interface commands are inhibited, and the module returns to default and non-volatile settings. An internal pull-up biases the input High if the input is open.	I	3.3 V LVTTL
SDA	TWS interface data signal: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is required.	I/O	3.3 V LVTTL high-Z or driven to 0 level
SCL	TWS interface clock signal I: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is required.	I	3.3 V LVTTL
V_{cc25}	2.5 V Power supply, External common connection of pins required – not common internally		
V_{cc33}	3.3 V Power supply, External common connection of pins required – not common internally		
Case Common	Not accessible in connector. Case common incorporates exposed thermally conductive surfaces and is electrically isolated from signal common, i.e. GND.		

Recommended Power Supply Filtering

It is recommended to use separate power supply filters for V_{cc33} and V_{cc25} as in Figure 8. This filter is similar to other module specifications, such as SFF-8431 Rev 3.0 section D17 Figure 56.

Separate power supply filters shall be used for TX and RX modules.

The host power supply noise level compliance point is at point X.

The host power supply voltage level compliance point is at point Y, and host must take into account of the possible power supply drop due to the LGA interface.

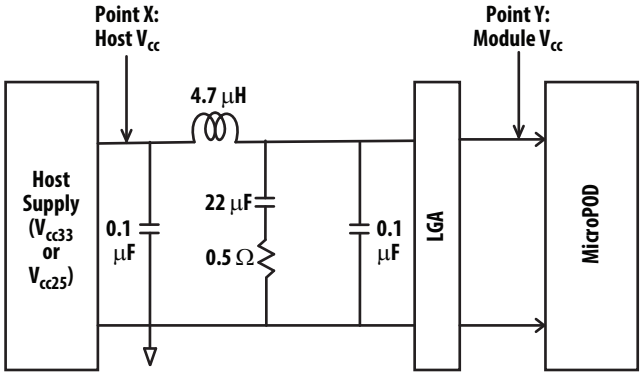


Figure 8. Recommended TX and RX Power Supply Filter

Power Supply Sequence

TX and RX Modules Power Supplies

There is no special requirement in the order of V_{cc33} and V_{cc25} power supply up/down sequence for TX or RX modules. However, it is recommended that

- Upon power down, the V_{cc33} and V_{cc25} shall be within 0 mV to +50 mV. If the residual voltage is larger than 50 mV, it can cause the TX or RX module to fail to start up.

Host ASIC Power Supplies

It is required that

- The maximum delay of power up/down between host ASIC and TX or RX module shall be shorter than 1 s to avoid any potential reliability damage to the modules.

It is recommended that: [1]

- The host ASIC power supply shall be turned on no later than TX or RX module power supplies (3.3 V and 2.5 V).
- The host ASIC power supply shall be turned off no earlier than module power supplies (3.3 V and 2.5 V).

If this condition cannot be met in the system design, the following shall be taken into account in the ASIC design. In the case when the RX module is powered on, host ASIC is power off, the host ASIC electrical input ESD diodes can be forward-biased through a 50 Ω resistor to the V_{cc25} supply (see Figure 10). The host ASIC ESD diodes shall be designed to tolerate such forward biasing.

High Speed and Low Speed IOs

The power supply sequence and the ramp rate shall be designed by the user to meet the absolute maximum specifications as in "Data Input Voltage – Single Ended" and "Control Input Voltage".

It is required that:

- Data signal shall NOT be presented at TX high speed inputs before both V_{cc33} and V_{cc25} are turned on for the TX module; and data signal shall be turned off at TX high speed inputs before both V_{cc33} and V_{cc25} are turned off for the TX module.

It is recommended that:

- The low speed inputs are pulled down when the TX and RX V_{cc33} or V_{cc25} are off.

Note:

1. In the case when host ASIC is turned on and the module power supply is off, the TX high speed input (if DC coupled to ASIC) and TX/RX low speed IO ESD diodes can be forward-biased by the ASIC. The following design shall take care of the potential latch up or reliability issues:
   - The TX high speed ESD diodes are designed to tolerate a minimum of 10 mA forward biasing current assuming ASIC is CML driver
   - The host system or ASIC low speed IO pull-ups shall be sufficient to limit the forward biasing current in the low speed IO ESD diodes.

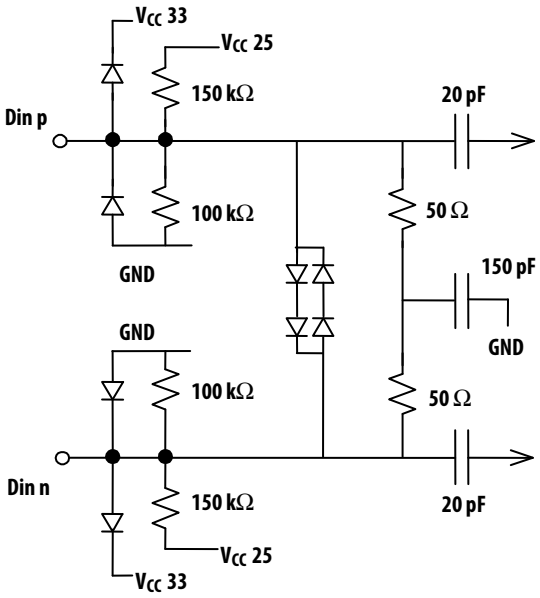


Figure 9. Transmitter Data Input Equivalent Circuit

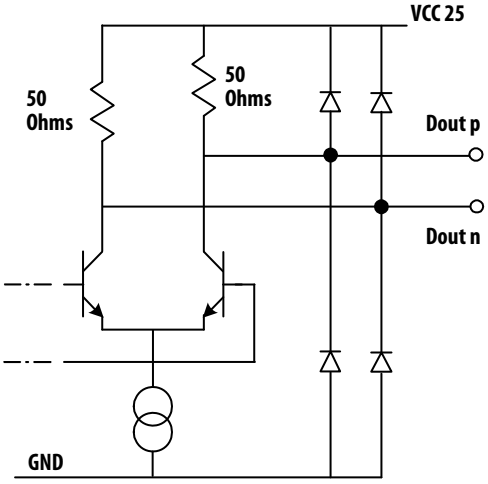


Figure 10. Receiver Data Output Equivalent Circuit

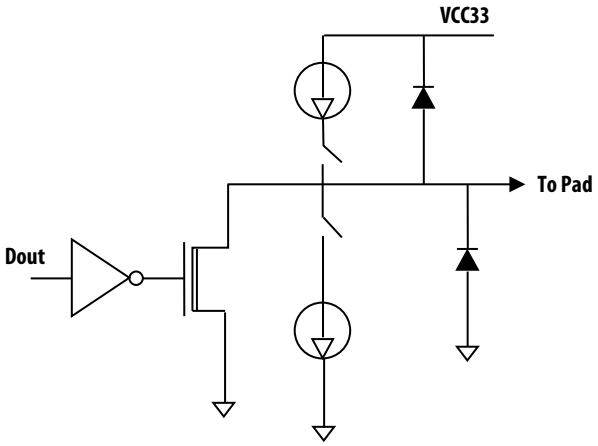


Figure 11. Low Speed IO Equivalent Circuit, INTL

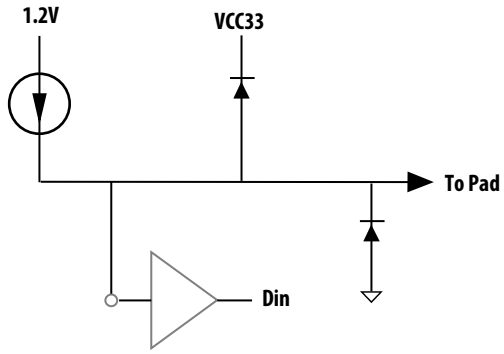


Figure 12. Low Speed IO Equivalent Circuit, RESETL

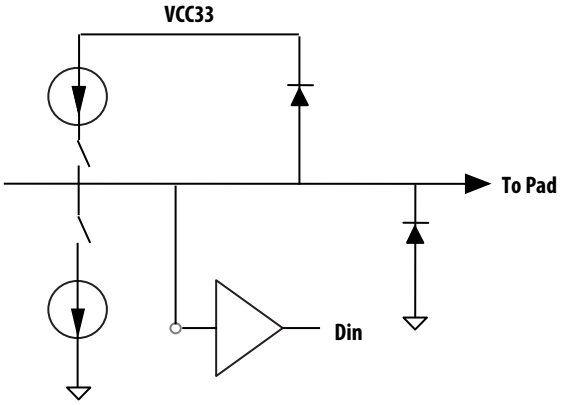


Figure 13. Low Speed IO Equivalent Circuit, ADR<2:0>

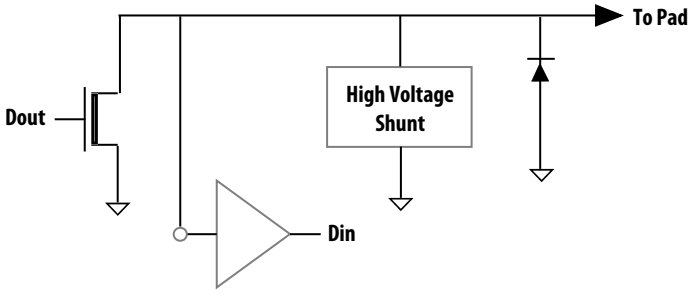


Figure 14. Low Speed IO Equivalent Circuit, SDA, SCL

Control Timing Diagrams

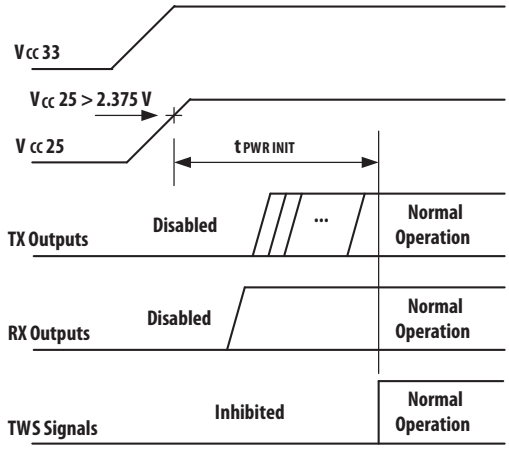


Figure 15. Power-Up Sequence

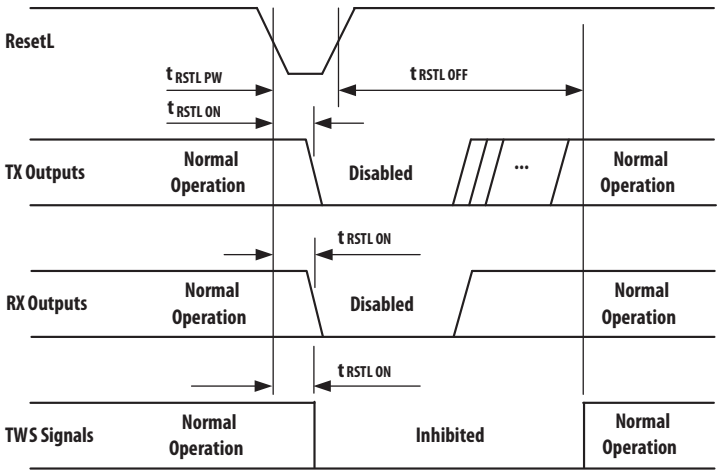


Figure 16. ResetL Sequence

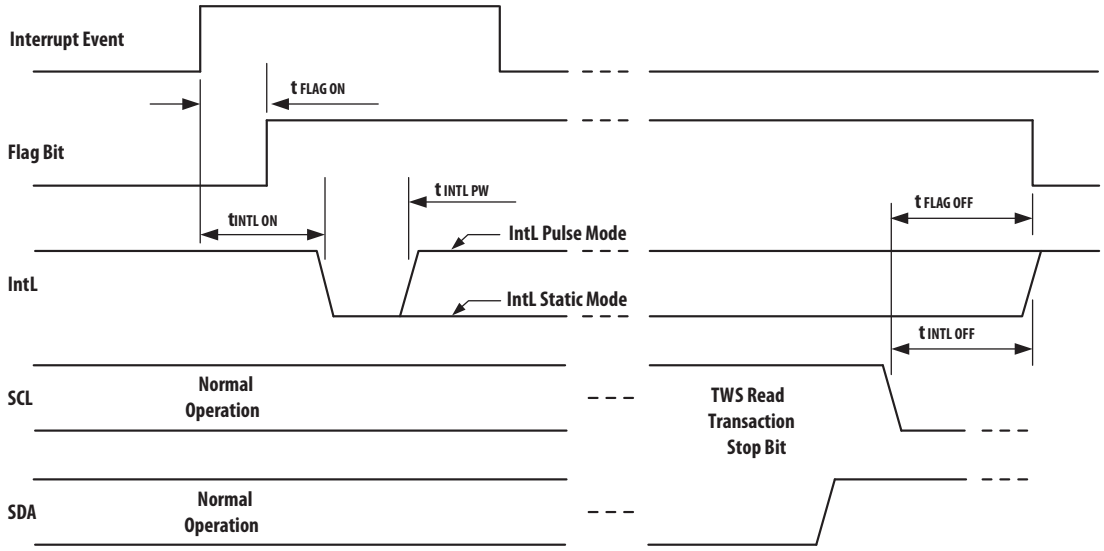


Figure 17. Interrupt Sequence

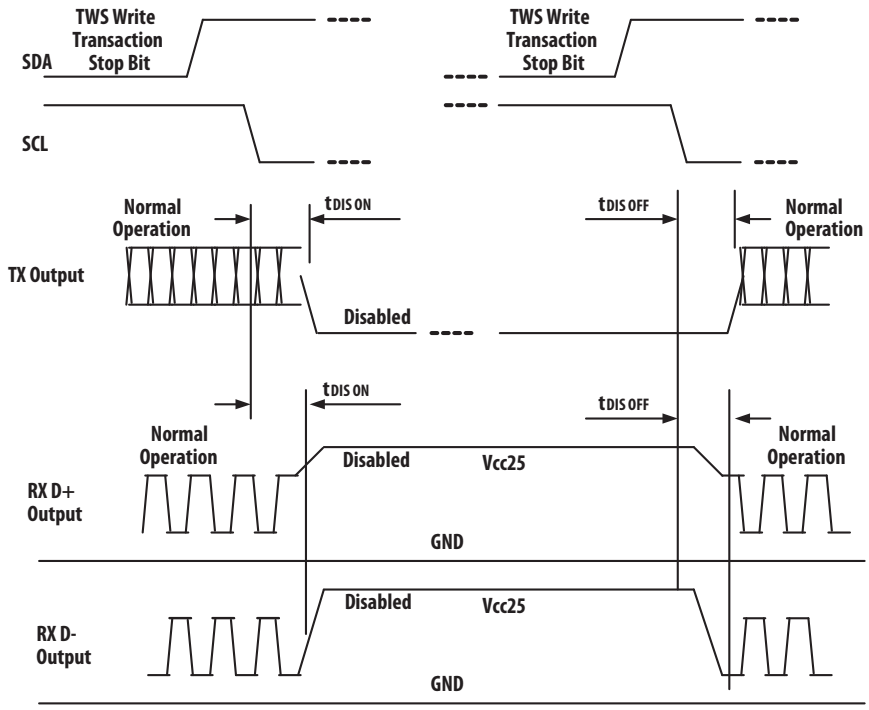


Figure 18. Channel Disable Sequence

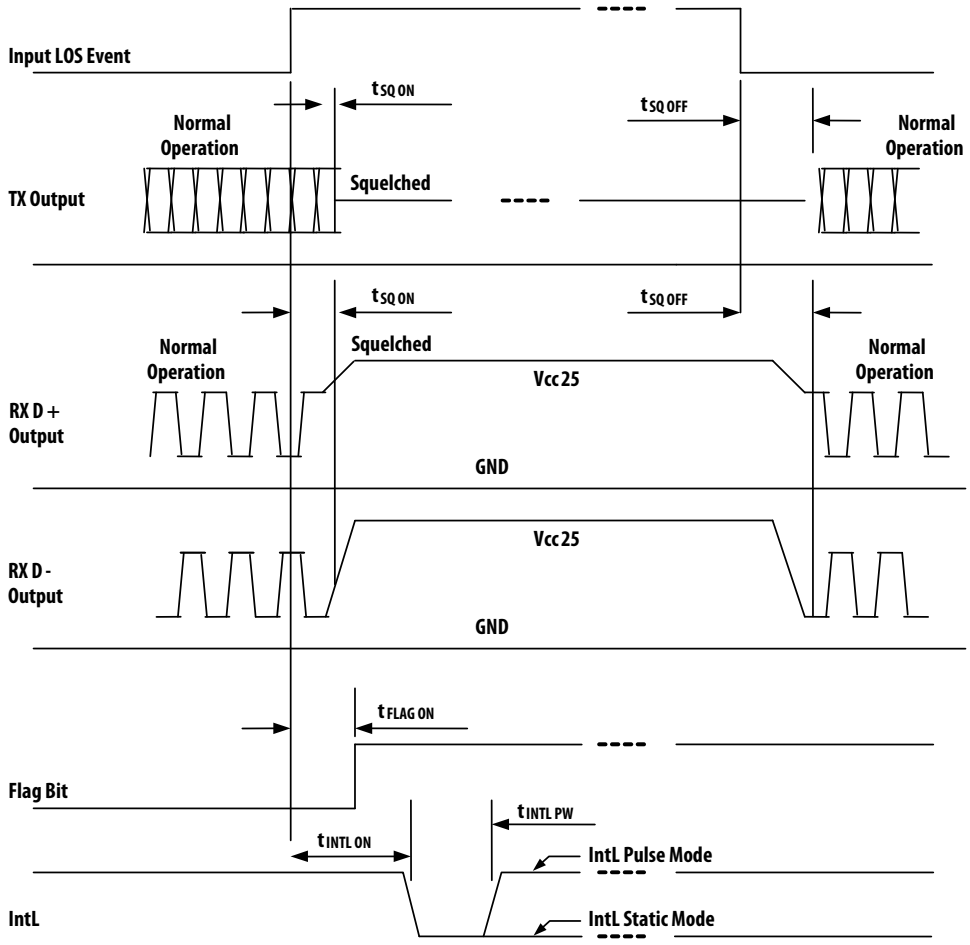
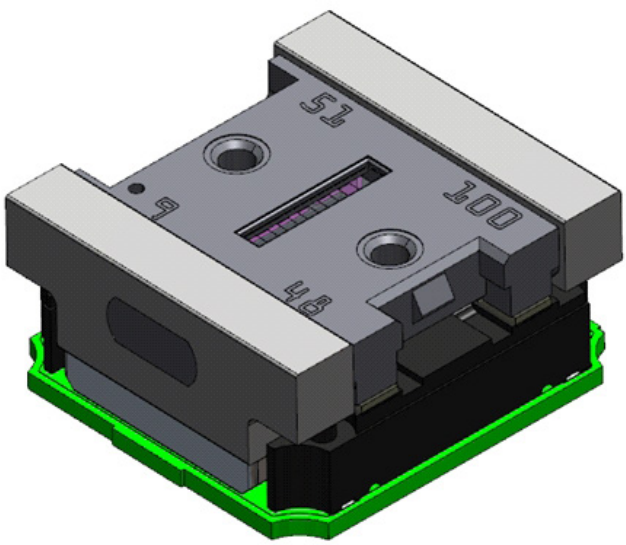


Figure 19. LOS Squelch Sequence

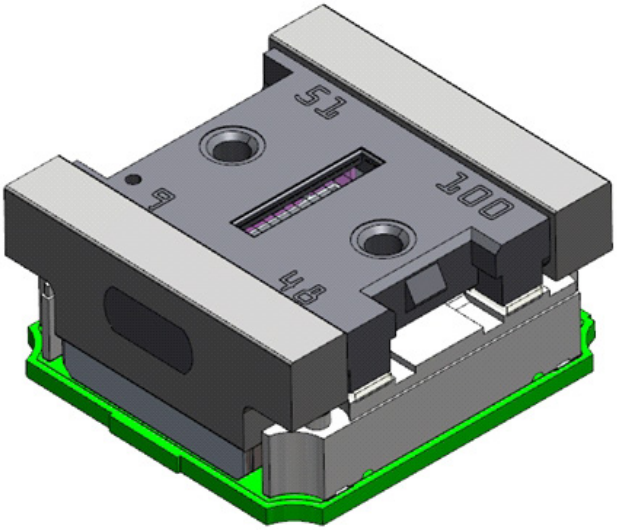
Module Outline

The mechanical outline of the TX and RX module are identical, shown as follows.

To differentiate TX from RX, the color of the TX WBP plastic is chosen to be white and for RX, black.



RX on the left



TX on the right

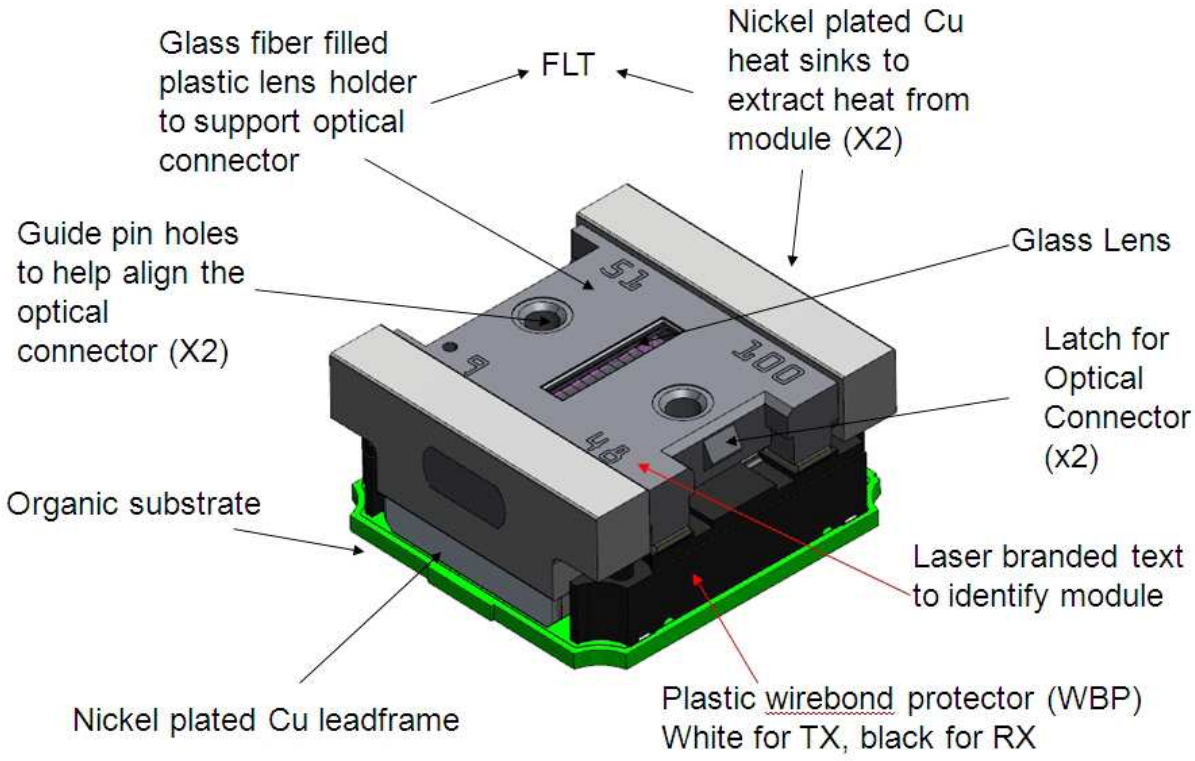


Figure 20. Module Outline

See "Appendix A: Module Mechanical Drawing" for the detailed mechanical dimensions.

LGA Interface

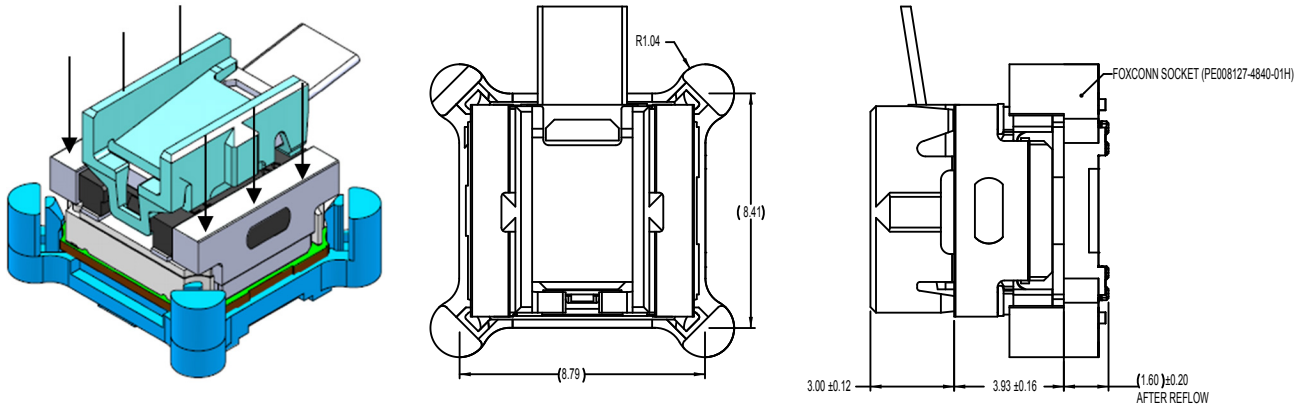


Figure 21. A Module and PRIZM in a Reference LGA Socket

The TX and RX modules shall be horizontally aligned to the LGA interposer through the module four corner. The LGA socket design shall be sufficient to guarantee the LGA contacts to the module corresponding substrate pads under the worst case tolerance. The corner feature of the LGA interposer can be spring loaded, but the horizontal force applied to the modules shall meet the requirements as in the Mechanical Forces section.

The TX and RX modules shall be pushed down against the LGA interposer on the Cu blocks as shown in Figure 1. The nominal force is 40 gram per LGA contact, which is 3.240 kg total. The force shall also meet the requirement as in the Mechanical Forces section. Under such force, the LGA socket shall have a vertical working range of a minimum of 150um.

The TX and RX LGA interface metallurgy over copper pads is electroless nickel, electroless palladium, and immersion gold (ENEPIG). The plating specification is as follows:

Supplier	Ni Plating Thickness (um)	Pd Plating Thickness (um)	Au Plating Thickness (um)
A	5 to 9	0.08 to 0.15	0.03 to 0.06
K	7 to 13	0.02 to 0.10	0.06 to 0.16

Host PCB Interface

Host PCB footprint depends on customer LGA solution, which shall meet the dimension and tolerance in order to work with the LGA interposer and the module substrate outline as in “Appendix A: Module Mechanical Drawing

Insertion and Removal Specifications

Parameter	Max. Cycles
MicroPOD Insertions into an LGA Socket	20
PRIZM Insertions into a MicroPOD	20

Mechanical Forces

The following tables specify the maximum forces that can be applied to the TX and RX modules during normal operation and handling.

Handling	Tooling	Forces	Spec	Comments
Module Removal from Tape and reel package	Pick and Place Machine	Tensile on Cu rails using vacuum during extraction from pocket	<0.5 kgf	vacuum head contacts and loads tops of Cu sidebars
Optical alignment of Module over uLGA socket posts	Pick and Place Machine	XYZ acceleration (+/-)	<0.25m/s^2	Compliant interfaces on vacuum head to minimize accelerations
Insertion of Module into uLGA	Pick and Place Machine	Vertical (compression) force on Cu blocks beyond uLGA post retention features	<0.5 kgf	
		XY shear (PCN contact to posts with a displacement of the module while holding the Cu blocks)	<0.4 kgf	
		Additional compression on Cu blocks to uLGA socket stops	<1 kgf	
Extraction of Module from uLGA (rework)	Manual Tweezers Extraction	Tensile on 1) optical connector and module interface and 2) TIM0	<0.45 kgf (4.4 N)	using special tweezers under a scope
Insertion of optical connector subassembly onto module	Manual Placement	Compression load on FLT plastic with loads transferred to Cu blocks	<0.45 kgf	
		Shear forces acting on optical connector and module FLT interface	<0.4 kgf	optical connector guide pin misaligned to FLT guidepin hole
Fiber connector assembly handling pre-Saddle Loading	Manual Manipulation	Shear forces acting on Cu block TIM0 adhesive	<0.5 kgf	Forces transferred from FO assembly without loading on Cu blocks to restrain Module in uLGA carrier
Fiber connector assembly handling post-Saddle Loading	Manual Manipulation	Shear forces acting on optical connector and module FLT interface	<0.1 kgf	Forces transferred from FO assembly with loading on Cu blocks to restrain Module in uLGA carrier
Fiber connector assembly handling post-Saddle Loading (full compression)	Manual Manipulation	Shear forces acting on optical connector and module FLT interface	<0.11 kgf	
Weight of FO assembly and overlaying FO stack	Manual Manipulation	Compressive load on FLT plastics	<0.45 kgf	
TIM3 Compression	Mechanical Press	Compressive on Cu Sidebars	< 12.3 kgf	< 24 hours
			< 3.6 kgf (8 lbf)	Subsequent Test/Card socket loads and system operation

Thermal Requirements

The module thermal interfaces are highlighted in blue in Figure 22, which represents two copper blocks as the system cooling interface. The user shall provide the thermal solution to these interfaces to meet the temperature range as in the recommended operating conditions.

The case temperature measurement point is highlighted, shown as follows.

The TX and RX modules are not intended for a normal solder reflowing process. Permanent damage can happen to the modules during the reflow process.

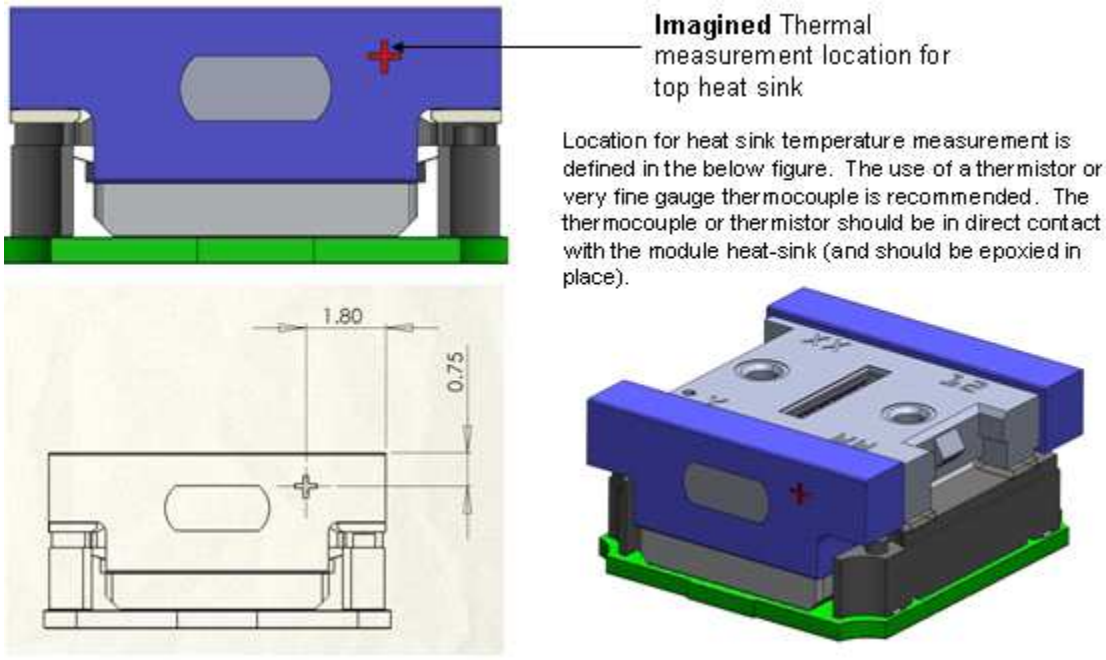
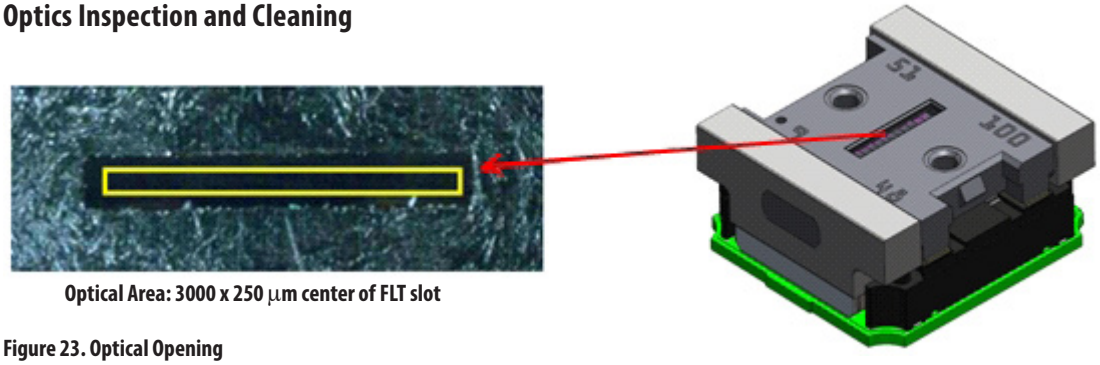


Figure 22. Module Thermal Interface (RX shown)

Optics Inspection and Cleaning



Optical Area: 3000 x 250 μm center of FLT slot

Figure 23. Optical Opening

Optical inspection shall be conducted at class 100k or better environment. ESD must be taken care during the operation.

Perform first pass inspection at 30× magnification under a low power scope (e.g., LEICA GZ6E scope with fluorescent ring white lighting) for optical opening with exposed glass substrate surface.

If the surface is contaminated with foreign debris or particles, use an air gun with clean ionized dry air or nitrogen supply (pressure at ~ 5kg/cm^2) to blow directly into the optical opening (no cotton swabs, no liquid solvents on the optics). Inspect under scope again. Repeat if necessary.

If the module requires further verification, perform second pass inspection at 80× or higher power. Set focus on the top surface ONLY of the glass substrate and complete inspection for the exposed area. If there is unacceptable contamination, the module may be routed back once for cleaning with ionized air.

The surface of the lenses should not be physically touched.

Control Interface and Memory Map

The control interface combines dedicated signal lines for address inputs, Adr[2:0], interrupt output, IntL, and reset input, ResetL, with two-wire serial, TWS, interface clock, SCL, and data, SDA, signals to provide users rich functionality over an efficient and easily used interface. The TWS interface is implemented as a slave device and compatible with industry standard two-wire serial protocol. In general, TWS bus timing and protocols follow the implementation popularized in Atmel Two-wire Serial EEPROMs. For additional details see, e.g., Atmel AT24C01A. Note the difference in write cycle time as described later.

Multi-byte writes are supported to allow up to 8 write transactions of up to 16 bytes each.without NACK. If the sequence of module actions is important, at least 100 ms wait between each functional change must be used. A functional change is a 1 or 2 byte write affecting one function. For example, if a channel is disabled and then enabled in the next write, a 100 ms wait period is needed after the disable to ensure it is effective and that the subsequent write or read is acknowledged. If insufficient wait time is allowed, the write or read following the initial write will receive a NACK (no-acknowledge). Reads to any location and writes to the page select registers x5i:127 and x6i:127 do not count as functional changes and do not require any wait time before the next read or write transaction.

The address signals, Adr2, Adr1 and Adr0, provide the ability to program the TWS bus address of the module.

The TX module address has the binary form 0101hjkx, where h, j and k correspond to Adr2, Adr1 and Adr0, respectively and x corresponds to the Read/Write command bit. Modules will respond to TWS bus addresses in the range of 50h to 5Fh (hereafter 5ih) depending upon the state of Adr2, Adr1 and Adr0.

The RX module address has the binary form 0110hjkx, where h, j and k correspond to Adr2, Adr1 and Adr0, respectively and x corresponds to the Read/Write command bit. Modules will respond to TWS bus addresses in the range of 60h to 6Fh (hereafter 6ih) depending upon the state of Adr2, Adr1 and Adr0.

An interrupt signal, IntL, is used to alert the host of a loss of input signal (LOS), transmitter fault conditions and/or assertion of any monitor flag. This reduces the need for dedicated status signal lines and polling the status and monitor registers while maintaining timely alerts to significant events. IntL can be programmed (page 01h byte 225 bit 0) to either pulse or static mode with static as the default mode.

A dedicated module reset signal, ResetL, is provided in case the TWS interface becomes dysfunctional. When ResetL is asserted, the outputs are disabled, TWS interface commands are inhibited and the module returns to factory default settings except Non-volatile Read-Write (RW) registers which retain the last write. A module register (memory map except the non-volatile registers) reset can also be initiated over the TWS interface (TX page 5ih or RX page 6ih byte 91, bit 0). A TWS reset can be initiated by nine SCL clock cycles with SDA high in each cycle and creating a start condition.

With the TWS interface the user can read a status register (byte 2 for TX page 5ih, RX page 6i) to see if data is available in the monitor registers, if the module has generated an IntL that has not been cleared and global status reports for loss of signal and fault conditions.

LOS, TX fault and/or monitor flag registers can be accessed to check the status of individual channels or which channel may have generated a recent IntL. LOS, TX fault and flag bits remain set (latched) after assertion even in the event the condition changes and operation resumes until cleared by the read operation of the associated registers or reset by ResetL or the TWS module reset function.

The user can read the present value of the various monitors. For transmitters and receivers, internal module temperature and supply voltages are reported. For transmitters, monitors provide for each channel laser bias current and laser light output power (LOP) information. For receivers, input power (Pave) is monitored for each channel. In addition, elapsed operating time is reported. All monitor items are two-byte fields and to maintain coherency, the host must access these with single two-byte read sequences. For each monitored item, alarm thresholds are established. If an item moves past a threshold, a flag is set, and, provided the item is not masked, IntL is asserted. The threshold settings are available in the upper memory page, 01h.

The user can select either a pulse or static mode for the interrupt signal IntL and initiate a module register reset. The user is provided the ability to disable individual channels. For transmitters, equalization levels can be independently set for individual channels. For receivers, output signal amplitude, de-emphasis levels and rate select can be independently set for individual channels. In the upper page, 01h, control field the user can invert the truth of the differential inputs for individual transmitter channel and for the differential outputs of individual receiver channels. In addition, the user can disable the output squelch function on an individual channel basis for both transmitters and receivers. For transmitters the user can, on an individual channel basis, activate a margin mode that reduces the output optical modulation amplitude for the channel.

Most non-volatile control registers are located in the upper page 01(h). Other non-volatile functions include the IntL mode selection bit, input and output polarity flip bits, transmitter equalization control bits, receiver output amplitude control and receiver output de-emphasis control. Entries into these registers will retain the last write for supply voltage cycles and for ResetL and module register resets.

Volatile functions include module register reset, channel disable, squelch disable and margin activation.

A mask bit that can be set to prevent assertion of IntL for the individual item exists for every LOS, TX fault and monitor flag. Mask fields for LOS, TX fault and module monitors are in the lower memory page, 5ih for TX and 6ih for RX, and the mask field for the channel monitors are in the upper page 01h. Entries in the mask fields are volatile.

Page 00h, based on the Serial ID pages of XFP and QSFP, provides module identity and information regarding the capabilities of the module.

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40˚C, V_{cc33} = 3.435 V and V_{cc25} = 2.625 V.

Parameter	Symbol	Min	Typ	Max	Units	Reference
LVTTL Input Voltage High Threshold	Vihttl	2			V	Note 1
LVTTL Input Voltage Low Threshold	Vilttl			0.8	V	Note 1
LVTTL Output Pull-up Current	Ioputtl	80		250	µA	Pull-up to 3.3 V
LVTTL Output Pull-down Current	Ioputtl	80		250	µA	Pull-down to 0.0V
Address Assert Time			6.6	100	ms	Note 2
Interrupt Assert Time	$t_{INTL\ ON}$			100	ms	Note 3
Interrupt Pulse Width	$t_{INTL\ PW}$	5	28	50	µs	Note 4
Interrupt De-assert Time	$t_{INTL\ OFF}$			100	ms	Note 5
Reset Assert Time	$t_{RSTL\ ON}$		0.2	100	µs	Note 6
Reset De-assert Time	$t_{RSTL\ OFF}$		350	2000	ms	Note 7
Initialization Time TWS Interfaces				2000	ms	
Data Ready Time	t_{data}			2000	ms	Note 8
Tx Fault Assert Time	$t_{Txfault,ON}$			100	ms	Note 9
Flag Assert Time	$t_{flag,ON}$			100	ms	Note 10
Mask Assert Time	$t_{mask,OFF}$			100	ms	Note 11
Mask Deassert Time	$t_{mask,ON}$			100	ms	Note 12
Select Change Time	$t_{ratesel}$			100	ms	Note 13
TWS Data In Set Up Time	$t_{SU:SDA}$	0.10			µs	Note 14
TWS Data In Hold Time	$t_{HD:SDA}$	0			µs	Note 15
TWS Clock Low to Data Out Valid	t_{AA}	0.10		0.90	µs	Note 16
TWS Data Out Hold Time	t_{DH}	100			ns	Note 17
TWS Data Output Rise Time	$t_{r\ SDA}$			0.30	µs	Measured between 0.8V and 2.0V
TWS Data Output Fall Time	$t_{f\ SDA}$			0.30	µs	
TWS Interface Timing						See Atmel Two-Wire Serial EEPROM, e.g. AT24C01A . Note difference in Write Cycle Time
TWS Write Cycle Time (up to 2 sequential bytes)	t_{WC}	100			ms	
Serial Interface Clock Holdoff - "Clock Stretching"	T_clock_hold			500	µs	Note 18
Endurance (Write cycles)		50,000			cycles	Note 19

Notes:
1. 3.3 V LVTTL compatible control inputs. This includes ADR[2:0] pins.
2. is the module response time from a change in module address, Adr[2:0], to response to TWS communication using the new address.
3. This is the module response time from occurrence of interrupt generating event to IntL assertion, Vout:IntL = Vol. IntL assert time of 100ms assumes the intL is derived from the logic states of (1) RX LOS status, (2) TX LOS status, or (3) TX FAULT status, or any combination thereof, AND all other status flags are masked.
4. Pulse or static level can be selected for IntL. Static mode is default. See Memory Map.
5. This is the module response time from clear on read operation, measured from falling SCL edge after stop bit of read transaction, until Vout:IntL = Voh where IntL is in static mode.
6. Assertion of ResetL activates a complete module reset, i.e. module returns to factory default and non-volatile control settings. While ResetL is Low, TX and RX outputs are disabled and the module does not respond to the TWS interface.
7. This is the response time from ResetL de-assertion to resumption of operation.
8. Time from power on to Data Not Ready (Byte 2, bit 0) deasserted and Int_L asserted.
9. Time from Tx Fault state to Tx Fault bit set (value = 1b) and Int_L asserted
10. Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and Int_L asserted. Flag assert/de-assert timings for all signals assumes the module temperature is stable. Flag assert/de-assert timings may be significantly longer if the module case temperature changes faster than 4C/min.
11. Time from mask bit set (value = 1b) until associated Int_L assertion is inhibited.
12. Time from mask bit cleared (value = 0b) until associated Int_L operation resumes.
13. Time from change of state of Application or Rate Select bit until transmitter or receiver bandwidth is in conformance with appropriate specification
14. Data In Set Up Time is measured from Vil(max)SDA or Vih(min)SDA to Vil(max)SCL.
15. Data In Hold Time is measured from Vil(max)SCL to Vil(max)SDA or Vih(min)SDA.
16. Clock Low to Data Out Time is measured from Vil(max)SCL to Vol(max)SDA or Voh(min)SDA.
17. Data Out Hold Time is measured from Vil(max)SCL to Vol(max)SDA or Voh(min)SDA.
18. Maximum time the modules may hold the SCL line low before continuing with a read or write operation.
19. 50K write cycles at 70C. Applies to non-volatile control registers in memory map.