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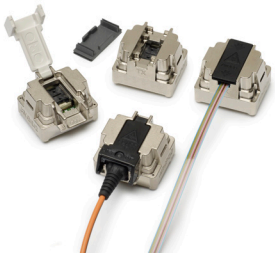
MiniPOD™
AFBR-811VxyZ, AFBR-821VxyZ

10 Gbps/Channel

Twelve Channel, Parallel Fiber Optics Modules

Data Sheet



Description

The AFBR-811VxyZ Twelve Channel, Pluggable, Parallel Fiber Optics Transmitter and AFBR-821VxyZ Twelve Channel, Pluggable, Parallel Fiber Optics Receiver are high performance fiber optics modules for short-range parallel multi-lane data communication and interconnect applications. The high density optical modules are designed to operate over multimode fiber systems using a nominal wavelength of 850 nm.

Avago's MiniPOD solution offers system designers two module package options to optimize their cable management and board layout. AFBR-811RxyZ Tx/AFBR-821RxyZ Rx is used with round multi-lane cable assemblies for applications requiring multiple turns of the jumper cable inside the chassis. AFBR-811FxyZ Tx/AFBR-821FxyZ Rx is used with flat ribbon cable assemblies, allowing dense tiling of the modules as the jumper cables can be thread under the dust-cap of the next module. This top mounted optical connection maximizes board layout density by eliminating board space lost to the optical connector and strain relief.

The electrical interface uses a 9×9 MEG-Array connector with 1.27 mm pitch

http://portal.fciconnect.com/Comergent//fci/drawing/55714.pdf

The optical interface requires the user to provide a custom designed optical turn 1×12 ribbon cable PRIZM® LightTurn® connector.

The thermal interface provided can require either a user provided heat sink or use of the Avago general purpose clip on heat sink, to maintain the module case temperature to be between 0 °C to 70 °C during continuous operation.

Applications

- 100 GbE and IB-QDR / IB-DDR / IB-SDR interconnects
- Data Aggregation, Backplane and Proprietary Protocol and Density Applications
- High Performance and High Productivity computer interconnects
- Switch Fabric interconnects

Patent - www.avagotech.com/patents

Features

- Compliant to IEEE 802.3ba 100GbE (100GBASE-SR10 and nPPI) per lane
- Compliant to 12×QDR Infiniband
- Operates at 10.3125 Gbps per channel with 64b/66b encoded data for 100GbE application and at 10 Gbps with 8b/10b encoded data for IB-QDR application
- High Aggregate bandwidth: 120 Gbps per module
- High density footprint: 21.95 mm × 18.62 mm size
- Two package options to optimize internal cable management and system layout
- Separate transmitter and receiver modules
- 850 nm VCSEL array in transmitter; PIN array in receiver
- Links up to 150 m at 10.3125 Gbps with OM4 4700 MHz•km 50 μm MMF
- Optical Interface: PRIZM™ LightTurn® optical turn 1×12 ribbon fiber connector
- Pluggable electrical interface: 9×9 MEG-Array for ease of design and manufacturability
- Low Power consumption: 3.0 W Max per Transmitter/Receiver pair (0 °C to 70 °C operating range)
- Dedicated signals for module address, module reset and host interrupt
- Two Wire Serial (TWS) interface with maskable interrupt for expanded functionality including:
  - Individual channel functions: disable, squelch disable, lane polarity inversion, TX eye margin enable
  - A/D read back: module temperature and supply voltages, per channel laser current and laser power, or received power
  - Status: per channel Tx fault, electrical (transmitter) or optical (receiver) LOS, and alarm flags
  - Programmable equalization integrated with DC blocking caps at transmitter data input
  - Programmable receiver output swing and de-emphasis level
  - Field Upgradable Firmware capability
- 0 °C to 70 °C case temperature continuous operating range. 85 °C supported for short durations

Part Number Ordering Options

Modules for use with Flat Ribbon Jumper Cable	Transmitter Base Part Number	AFBR-811FxyZ
	Receiver Base Part Number	AFBR-821FxyZ
Modules for use with Round Jumper Cable	Transmitter Base Part Number	AFBR-811RxyZ
	Receiver Base Part Number	AFBR-821RxyZ
MiniPOD Evaluation Board		AFBR-800EVB
MiniPOD Evaluation Kit		AFBR-800EVK
MiniPOD Round Module Dust Cover Opening Tool		AFBR-800RTL
MiniPOD Extraction Tool		AFBR-800ETL
MiniPOD PRIZM® LightTurn® Removal Tool		AFBR-800FTL

Where:

81 = Transmitter; 82 = Receiver

F/R: R = module package for use with round cable;
F = module package for use with Flat ribbon cable

x: N = No Heat Sink,
H = Pin Clip-on Heat Sink attached (see Figure 24)

y: 1 = 100 m

Warning

EN 60825-1:2007
COMPLIES WITH 21 CPR 1040.10 AND 1040.11
EXCEPT FOR DEVIATIONS PERSUANT TO LASER
NOTICE NO. 50, DATED JUNE 24, 2007

CAUTION! Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure

CAUTION! Laser Class 3R for laser module assembly without fiber optic cable attachment.

INVISIBLE LASER RADIATION, AVOID DIRECT EYE EXPO-SURE! CLASS 3R LASER PRODUCT WITHOUT OPTIC CABLE ASSEMBLY

CAUTION! Laser Class 1 Classification for laser module assembly including fiber optic cable attachment. Safe to view laser output with the naked eye or with the aid of typical magnifying optics (e.g. telescope or microscope)

CLASS 1 LASER PRODUCT

INVISIBLE LASER RADIATION, DO NOT VIEW DIRECTLY WITH OPTICAL INSTRUMENTS. CLASS 1 LASER PRODUCT WITH OPTIC CABLE ASSEMBLY.

Note: Standard used for classification: EN 60825-1:2007

Transmitter Module

The optical transmitter module (see Figure 1) incorporates a 12-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 12-channel input buffer and laser driver, diagnostic monitors, control and bias blocks. The transmitter is designed for EN-60825 and CDRH eye safety compliance; Class 3R out of the module. When fully assembled with the PRIZM LightTurn optical connector class 1M is achieved. The Tx Input Buffer provides CML compatible differential inputs (presenting a nominal differential input impedance of 100 Ω and a nominal common mode impedance to signal ground of 25 Ω) for the high speed electrical interface that can operate over a wide common mode range without requiring external DC blocking capacitors. For module control and interrogation, the control interface incorporates a Two Wire Serial (TWS) interface of clock and data signals and dedicated signals for host interrupt, module address setting and module reset. Diagnostic monitors for VCSEL bias, light output power (LOP), temperature, both supply voltages and elapsed operating time are implemented and results are available through the TWS interface.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential inputs, de-activate channels, place channels into margin mode (system level diagnostic mode where TX OMA is reduced by ~1dB), disable the squelch function and program input equalization levels to reduce the effect of long PCB traces. A reset for the control registers is available. Serial ID information and alarm thresholds are provided. To reduce the need for polling, the TWS interface is augmented with an interrupt signal for the host.

Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of input signal (LOS) and transmitter fault conditions. All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset by reading the appropriate flag register. The optical output will squelch for loss of input signal unless squelch is disabled. Fault detection or channel deactivation through the TWS interface will disable the channel. Status, alarm and fault information are available via the TWS interface. The interrupt signal (selectable via the TWS interface as a pulse or static level) is provided to inform hosts of an assertion of an alarm, LOS and/or Tx fault.

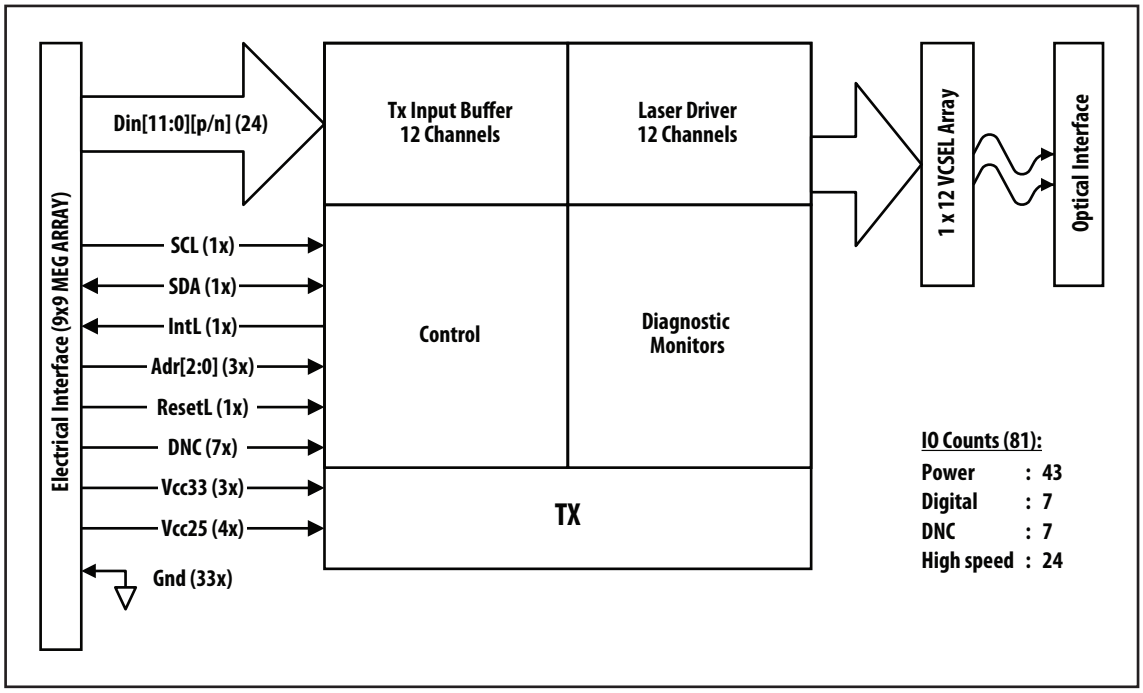


Figure 1. Transmitter Block Diagram

Receiver Module

The optical receiver module (see Figure 2) incorporates a 12-channel PIN photodiode array, a 12-channel pre-amplifier and output buffer, diagnostic monitors, control and bias blocks. The Rx Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 Ω to AC ground and 100 Ω differentially that should be differentially terminated with 100 Ω. External DC blocking capacitors are required. For module control and interrogation, the control interface incorporates a Two Wire Serial (TWS) interface of clock and data signals and dedicated signals for host interrupt, module address setting and module reset. Diagnostic monitors for optical input power, temperature, both supply voltages and elapsed operating time are implemented and results are available through the TWS interface.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential outputs, de-activate channels, disable the squelch function, program output signal amplitude and de-emphasis and change receiver bandwidth. A reset for the control registers is available. Serial ID information and alarm thresholds are provided. To reduce the need for polling, the TWS interface is augmented with an interrupt signal for the host.

Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of optical input signal (LOS). All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register. The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through TWS interface. Status and alarm information are available via the TWS interface. The interrupt signal (selectable via the TWS interface as a pulse or static level) is provided to inform hosts of an assertion of an alarm and/or LOS.

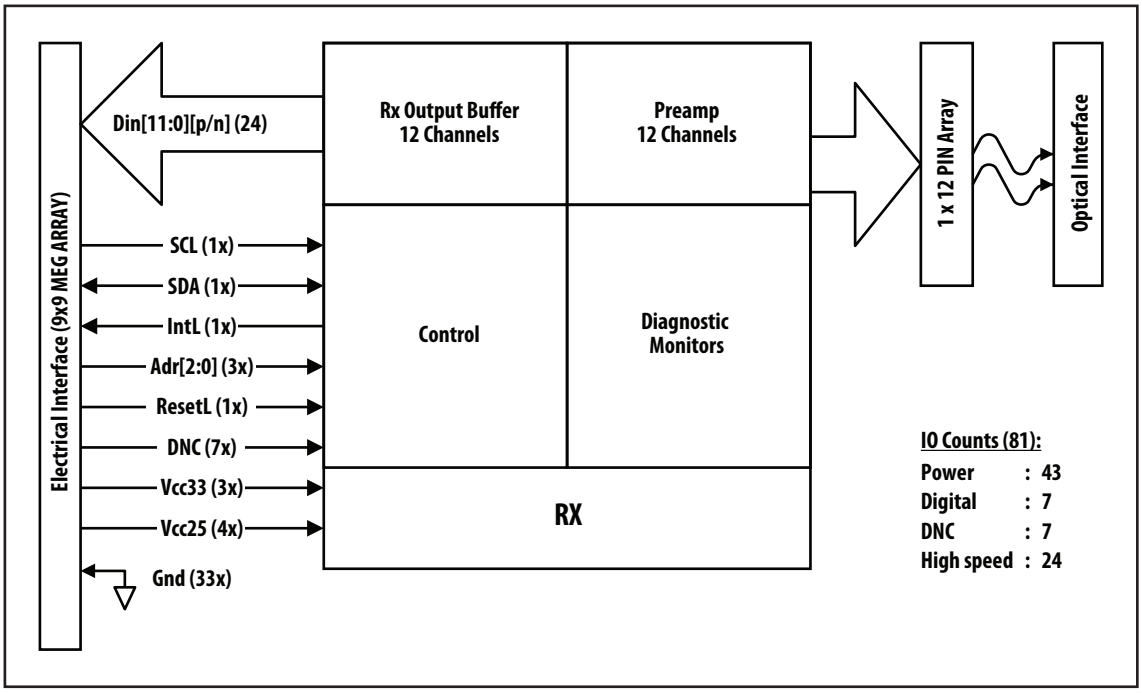


Figure 2. Receiver Block Diagram

High Speed Signal Interface

Figure 3 shows the interface between an ASIC/SerDes and the fiber optics modules. For simplicity, only one channel is shown. As shown in Figure 3, the compliance points are on the host board side of the electrical connectors. Sets of s-parameters are defined for the transmitter and receiver interfaces. The transmitter and receiver are designed, when operating within Recommended Operating Conditions, to provide a robust eye-opening at the receiver outputs. See the Recommended Operating Conditions and the Receiver Electrical Characteristics for details.

Unused inputs and outputs should be terminated with 100 Ω differential loads.

The transmitter inputs support a wide common mode range and DC blocking capacitors are not needed (internal capacitors are not shown in Figure 3). Depending on the common mode range tolerance of the ASIC/SerDes inputs, DC blocking capacitors may be required in series with the receiver; in this case 100 nF capacitors are recommended. Differential impedances are nominally 100 Ω. The common mode output impedance for the receiver is nominally 25 Ω while the nominal common mode input impedance of the transmitter is 25 Ω.

Transmitter Input Equalization

Transmitter inputs can be programmed for one of several levels of equalization. See Figure 4. The default case provides a flat gain-frequency response in the inputs. Different levels of compensation can be selected to equalize skin-effect losses across the host circuit board. See Tx Memory Map 01h Upper Page section addresses 228 – 233 for programming details.

Receiver Output Amplitude and De-emphasis

Receiver outputs can be programmed to provide several levels of amplitude and de-emphasis. See Figure 5 for de-emphasis definition. The user can program for peak-to-peak amplitude and then a de-emphasis level. If zero de-emphasis is selected, then the signal steady state equals the peak-to-peak level. For other levels of de-emphasis the selected de-emphasis reduces the steady-state from the peak-to-peak level. The change from peak-to-peak level to steady-state occurs within a bit time. See Rx Memory Map 01h Upper Page section addresses 228 – 233 for amplitude programming details and addresses 234 – 239 for de-emphasis programming details.

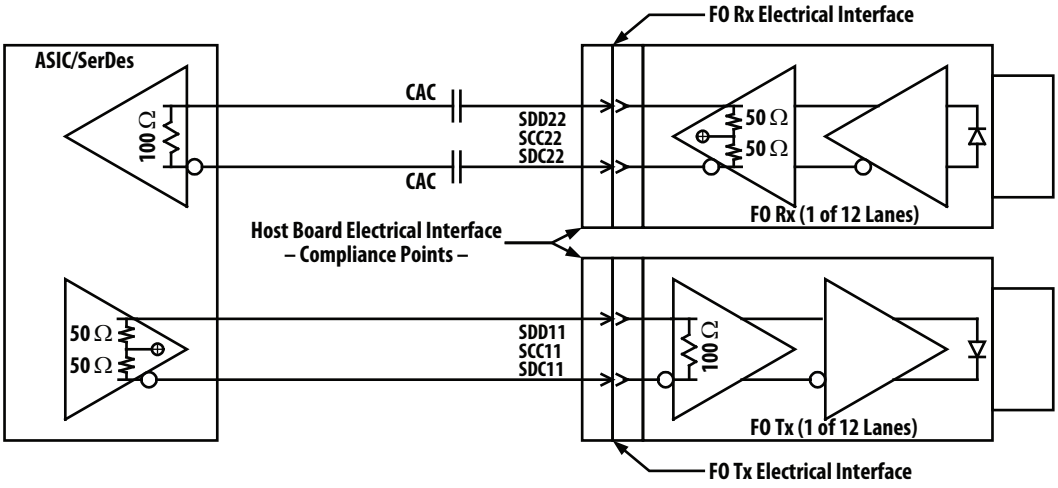


Figure 3. Application Reference Diagram

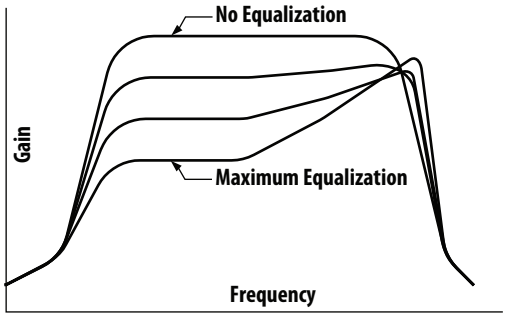


Figure 4. Transmitter Input Equalization

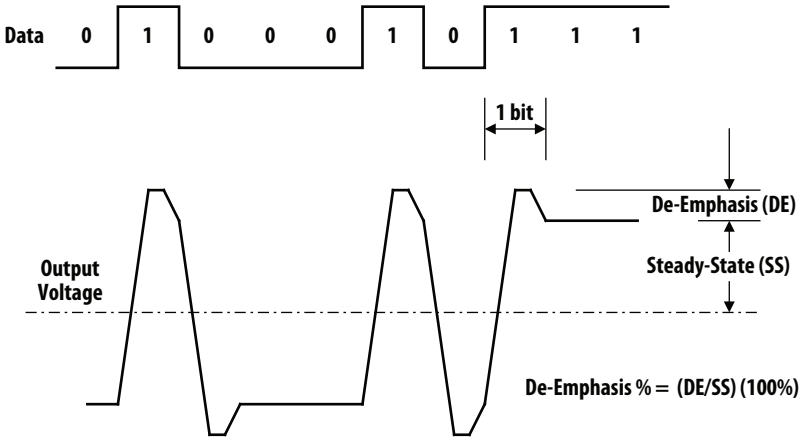


Figure 5. Definition of De-emphasis and Steady State

Control Signal Interface

The control interface includes dedicated signals for address inputs, interrupt output and reset input and bi-directional clock and data lines for a two-wire serial access (TWS interface) to control and status and information registers. The TWS interface is compatible with industry standard two-wire serial protocol. The MiniPOD module is implemented as a slave device. Signal and timing characteristics are further defined in the Control Characteristics and Control Interface and Memory Map sections.

The registers of the serial interface memory are defined in the Control Interface and Memory Map section.

Link Model and Reference Channel

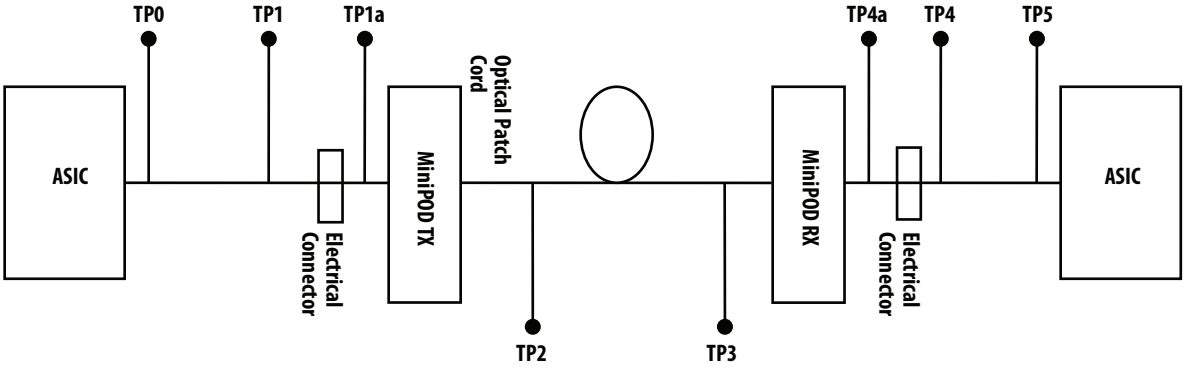


Figure 6. Link Model test point definitions

Performance specifications for the MiniPOD modules based on IEEE 802.3ba 100GBASE-SR10.

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operation Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_s	-40	85	°C	
Absolute Maximum Operating Temperature			85	°C	1
2.5 V Power Supply Voltage	V_{cc25}	-0.5	3.0	V	
3.3 V Power Supply Voltage	V_{cc33}	-0.5	4.0	V	
Data Input Voltage – Single Ended		-0.5	Vcc33+0.5, Vcc25+0.5, 4.0	V	
Data Input Voltage – Differential	$\|V_{Dip} - V_{Din}\|$		1.0	V	2
Control Input Voltage	V_i	-0.5	Vcc33+0.5, 4.0	V	3
Control Output Current	I_o	-20	20	mA	
Relative Humidity	RH	5	95	%	4
Receiver Damage Threshold	Rx_P_{MAX}		+4	dBm	

Notes:
1. Electro-optical specifications are not guaranteed outside the recommended operating temperature range. Operation above the Absolute Maximum Case Temperature for extended periods may adversely affect reliability.
2. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry.
3. The maximum limit is the lesser of V_{cc} + 0.5 V or 4.0 V.
4. Exposure to a condensing environment is not allowed.

Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Case Temperature	T_c	0		70	°C	Note 1
Case Temperature (short term)	T_{c_ext}	70		85	°C	Note 2
2.5 V Power Supply Voltage	V_{cc25}	2.375	2.5	2.625	V	Note 3
3.3 V Power Supply Voltage	V_{cc33}	3.135	3.3	3.465	V	
Signal Rate per Channel (rates < 3.125 Gb/s must be 8b/10b encoded)		1.25		10.3125	GBd	Note 4
Host Electrical Compliance		Per IEEE 802.3ba-2010 TP1a and TP4 nPPI specifications for host				
Control Input Voltage High	V_{ih}	2.3		3.6	V	
Control Input Voltage Low	V_{il}	-0.3		0.4	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Two Wire Serial Interface Write Cycle Time (up to 2 sequential bytes)	t_{WC}	100			ms	
Reset Pulse Width	$t_{RSTL\ PW}$	10			µs	
Power Supply Noise				100	mVpp	Note 5, 500 Hz to 5.4 GHz
Receiver Differential Data Output Load			100		Ω	Figure 3
AC Coupling Capacitors – Receiver Data Outputs	C_{ac}		0.1		µF	Note 6, Figure 3
Fiber Length: 4700 MHz•km 50 µm MMF (OM4)		0.5		150	m	Note 7
2000 MHz•km 50 µm MMF (OM3)		0.5		100	m	
Module Retention Screw Torque				0.06	N.m	Note 8
Module Top Surface Load Limit				100	N	Note 9
MEG-Array Mating Force (required)				70	N	
MEG-Array de-Mating Force (required)				35	N	
MEG-Array Side Load				50	N	See Figure 28
Fiber Pull Force (long duration**)				0.98	N	See Figure 29
Fiber Pull Force (short duration*)				2.2	N	See Figure 29
PRIZM Insertion Force (short duration*)				40	N	Note 10, See Figure 30
Number of Ribbons (Flat Cable Housing)				3		Note 11

Notes:

1. To prevent a degradation in reliability, avoid continuous operation above 70 °C. The case temperature is referenced to the Thermocouple measurement point, as shown in Figure 20; it is the same location for Tx and Rx, flat and round cable housing.
2. Short term is defined per section 4.1.2 of Telcordia GR-63-CORE Issue 3, March 2006 and corresponds to a period of not more than 96 consecutive hours and a total of not more than 15 days in 1 year (This refers to a total of 360 hours in any given year, but no more than 15 occurrences during that 1-year period).
3. There are no restrictions to the 2.5 V and 3.3 V power supply sequencing.
4. Higher data rates are possible. For further details, contact your Avago sales representative.
5. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 8 for recommended power supply filters.
6. For data pattern with restricted run lengths and disparity, e.g. 8b10b, smaller value capacitors may provide acceptable results.
7. Channel insertion loss includes 3.5 dB/km attenuation, 1.5 dB connector loss and 0.3 dB modal noise penalty allocations.
8. The PCB material should be evaluated to ensure that damage does not occur.
9. Load applied perpendicular to the module heat sink interface surface. See Figure 27.
10. Refer to the "PRIZM® LightTurn® Connector – to – Mini-POD™ Parallel Optic Module Assembly Recommendations" procedure available from Avago sales. 40 N max applies only when the PRIZM connector is being inserted/attached, per the PRIZM Connector Assembly Instructions. For all other objects being inserted inside the MiniPOD module, (i.e., not the PRIZM optical connector), the max force is 10 N. The 40 N can only be applied by a human finger tip. No tools or thumbs are to be used in the PRIZM connector attach process.
11. This is the number of ribbon fibers that can be accommodated beneath the dust-cap of a flat cable housing MiniPOD. Hence the maximum number of MiniPODs that can be tiled in a row is 3.

* Short duration is < 15 seconds.

** Long duration (> 5 minutes), exceeding this force long term could cause the optical light output power to drop or Rx sensitivity to diminish, which is not recoverable.

Transmitter Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_c = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V.

Parameter	Symbols	Min	Typ	Max	Units	Reference
Power Consumption (Max EQ)			1.2	1.6	W	Note 1
Power Supply Current – V_{cc25}			280	365	mA	Note 2
Power Supply Current – V_{cc33}			105	185	mA	Note 3
Differential Input Impedance		85	100	115	Ω	Informative
LOS Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	$\Delta V_{DI\ PP\ LOS}$	50			mVpp	Informative
LOS De-Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	$\Delta V_{DI\ PP\ LOS}$			210	mVpp	Note 4, Informative
LOS Hysteresis		0.5		4	dB	
Power On Initialization Time	$t_{PWR\ INIT}$		350	2000	ms	Note 5
Parameter	**Test Point**	**Min**	**Typ**	**Max**	**Units**	**Reference**
Single ended input voltage tolerance	TP1a	-0.3		4.0	V	Note 6
AC common mode input voltage tolerance	TP1a	15			mV	RMS
Differential input return loss	TP1				dB	Note 7, 10 MHz to 11.1 GHz
Differential to common-mode						
input return loss	TP1	10			dB	10 MHz to 11.1 GHz
J2 Jitter tolerance	TP1a	0.17			UI	Defined in 802.3ba
J9 Jitter tolerance	TP1a	0.29			UI	Defined in 802.3ba
Data Dependent Pulse Width Shrinkage (DDPWS) tolerance	TP1a	0.07			UI	Defined in 802.3ba
Eye Mask Coordinates: X1, X2, Y1, Y2	TP1a	SPECIFICATION VALUES 0.11, 0.31, 95, 350			UI mV	Note 8, Hit Ratio = $5x10^{-5}$

* For control signal timing including Adr[2:0], IntL, ResetL, SCL and SDA see Control Characteristics: Transmitter/Receiver.

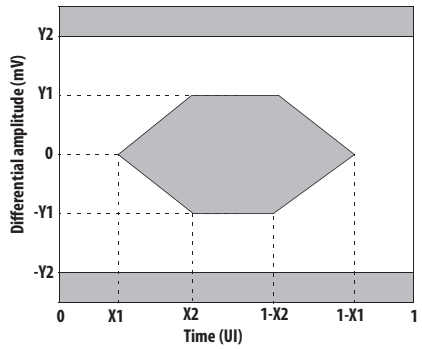
Notes:

1. Max power is 1.7 W above 70 °C, to 85 °C case temperature.
2. Supply current includes that of all V_{cc25} contacts.
3. Supply current includes that of all V_{cc33} contacts. Max current is 210 mA above 70 °C, to 85 °C case temperature.
4. Tx data input must conform to IEEE 802.3ba-2010 TP1a electrical host compliance specification.
5. Power On Initialization Time is the time from when the supply voltages reach and remain above the minimum Recommended Operating Conditions to the time when the module enables TWS access. The module at that point is fully functional.
6. Referred to TP1 signal common; The single-ended input voltage tolerance is the allowable range of the instantaneous input signals.
7. From 10 MHz to 11.1 GHz, the magnitude in decibels of the module differential input return loss at TP1 and the host differential output return loss at TP1a shall not exceed the limit given in Equation

   Return_loss (f) ≥ 12 – 2√(f) 0.01 ≤ f < 4.1 dB

   ≥ 6.3 – 13log10(f/5.5) 4.11 ≤ f < 11.1 dB

   Return_loss (f) is the return loss at frequency f

   f is the frequency in GHz
8. 

Tx Electrical Eye Mask Coordinates (TP1a) at Hit ratio 5 x 10^{-5} hits per sample

Receiver Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_c = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V.

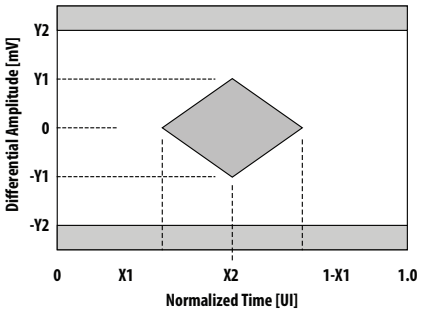
Parameter	Test Point	Min	Typ	Max	Units	Reference
Power Consumption			1.1	1.4	W	Note 1
Power Supply Current (V_{cc25}) – @ Default De-emphasis / Default output swing			350	425	mA	Note 2
Power Supply Current (V_{cc33}) – @ Default De-emphasis / Default output swing			48	90	mA	Note 3
Power Supply Current (V_{cc25}) – @ Max De-emphasis/Max output swing			430	525	mA	Note 2
Power Supply Current (V_{cc33}) – @ Max De-emphasis/Max output swing			48	90	mA	Note 3
Data Output Differential Peak-to-Peak Voltage Swing (Default De-emphasis)	TP4	400	500	600	mVpp	Note 4, 100 Ω Load (default setting)
Data Output Common Mode Voltage	TP4	2.0		2.540	V	Over Amplitude Range
AC common-mode output voltage (RMS)	TP4			7.5	mV	
Termination mismatch at 1 MHz	TP4			5	%	
Differential Output Impedance	TP4	85		115	Ω	Informative
Differential Output Return Loss, 10M – 11.1 GHz	TP4				dB	Note 5
CM to Differential Mode Conversion, 0.1G –11.1 GHz	TP4				dB	Note 6
Power On Initialization Time			288	2000	ms	
Output transition time (20% to 80%)	TP4	28			ps	
J2 Jitter Output	TP4			0.42	UI	Defined in 802.3ba
J9 Jitter Output	TP4			0.65	UI	Defined in 802.3ba
Data Dependent Pulse Width Shrinkage	TP4			0.34	UI	Defined in 802.3ba
Inter-channel Skew	TP4			11	ns	
Inter-channel Skew Variation	TP4		100		ps	Note 7
Eye Mask Coordinates: X1, X2, Y1, Y2	TP4	SPECIFICATION VALUES 0.29, 0.5, 150, 425			UI mV	Note 8, Hit Ratio = $5x10^{-5}$

Notes:

1. Max conditions include default output amplitude and de-emphasis programming.
2. Supply current includes that of all Vcc25 contacts.
3. Supply current includes that of all Vcc33 contacts.
4. See section on page 61 "Receiver Output Amplitude Control Code Description" for range of voltages defined in the receiver upper page 01h, address range 228 to 233. Data outputs are CML compatible. Data Output Differential Peak to Peak Voltage Swing is defined as follows: $\Delta V_{DO\ pp} = \Delta V_{DOH} - \Delta V_{DOL}$ where ΔV_{DOH} = High State Differential Data Output Voltage and ΔV_{DOL} = Low State Differential Data Output Voltage. Output voltage swing is adjustable via TWS interface.
5. From 10 MHz to 11.1 GHz. The magnitude in decibels of the module differential output return loss at TP4 and the host differential input return loss at TP4a shall not exceed the limit given in Equation

   Return_loss (*f*) ≥ 12 – 2√(f) 0.01 ≤ f < 4.1 dB
   ≥ 6.3 – 13log10(f/5.5) 4.11 ≤ f < 11.1 dB
6. From 10 MHz to 11.1 GHz. The magnitude in decibels of the host common mode output return loss at TP4 shall not exceed the limit given in Equation:

   Return_loss (*f*) ≥ 7 – 1.6f 0.01 ≤ f < 2.5 dB
   ≥ 3 2.5 ≤ f < 11.1 dB

   f is the frequency in GHz.
7. Inter-Channel Skew is defined for the condition of equal amplitude, zero ps skew input signals at TP1a.
8. 

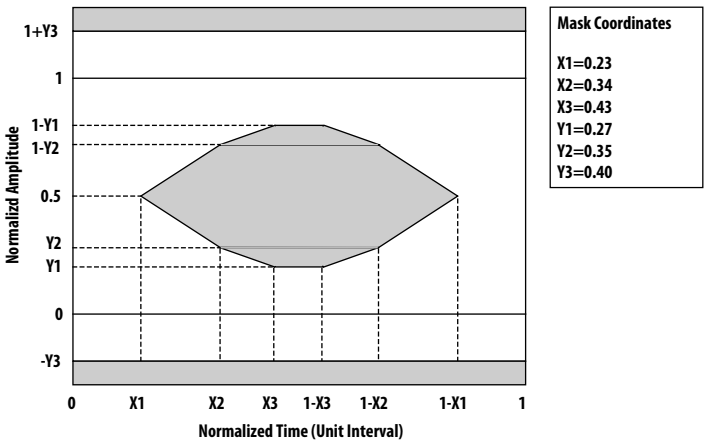
Rx Electrical Eye Mask Coordinates (TP4) at Hit ratio 5 x 10^{-5} hits per sample

Transmitter Optical Characteristics[1]

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_c = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V. Test point = TP2. Note: The TX output performance is only guaranteed with a differential input that meets the recommended operating conditions. A link driven with a single-ended signal will degrade the jitter performance.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Center Wavelength	λ_c	840	850	860	nm	
RMS spectral width			0.35	0.65	nm	2
Average launch Power, each lane	$P_{O\ AVE}$	-7.6		2.4	dBm	
Output Optical Power: Disabled	$P_{O\ OFF}$			-30	dBm	
Extinction Ratio	ER	3			dB	
Optical Modulation Amplitude, each lane	OMA	-5.6		3	dBm	3
Output Power (Squelched OMA)		-2.4			dBm	AC Squelch
Difference in launch power between any two lanes (OMA)				4	dB	
Peak power, each lane				4	dBm	
Launch Power in OMA minus TDP, each lane	Po - TDP	-6.5			dBm	
Transmitter and Dispersion Penalty, each lane	TDP			3.5	dB	
Optical return loss tolerance				12	dB	
Encircled flux			≥ 86% at 19 μm, ≤ 30% at 4.5 μm			
			Specification Values			
Eye mask coordinates: X1, X2, X3 Y1, Y2, Y3			0.23, 0.34, 0.43 0.27, 0.35, 0.4		UI	4, Hit ratio = $5x10^{-5}$ per sample
Power On Initialization Time Tx Outputs	$t_{PWR\ INIT}$		350	2000	ms	
Reset De-assert Re-initialization Time Tx Outputs	$t_{RSTL\ OFF}$		350	2000	ms	
Output Disable Assert Time for Fault	$t_{DIS\ ON}$		9	100	ms	
Output Squelch Assert Time for LOS	$t_{SQ\ ON}$		52	80	μs	
Output Squelch De-assert Time for LOS	$t_{SQ\ OFF}$		49	80	μs	

Notes:
1. These optical specifications are dependent upon the performance of the PRIZM LightTurn to cable assembly, which assumes a maximum of 2 dB insertion loss. More details are provided on the PRIZM LightTurn cable assembly specification. Please contact your Avago sales representative to receive this specification.
2. RMS spectral width is the standard deviation of the spectrum.
3. Output of user provided fiber connector. Even if the TDP < 0.9 dB, the OMA minimum must exceed this minimum value.
4. Compliance assured up to 10.3125 Gbps.



Transmitter eye mask definitions (TP2) at Hit ratio 5 x 10^{-5} hits per sample

Receiver Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_c = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V.

Parameter	Test Point	Min	Typ	Max	Units	Reference
Optical Modulation Amplitude (OMA), each lane	TP3			+3	dBm	1
Stressed Sensitivity (OMA), each lane	TP3			-5.4	dBm	2
Receiver Sensitivity (OMA)	TP3	-11.3			dBm	Informative
Operating Center Wavelength	TP3	840		860	nm	
Receiver Reflectance	TP3			-12	dB	
Peak Power, each lane	TP3			+4	dBm	
Output Rise/Fall time (20-80%)	TP3	25	40	50	ps	3
LOS to Data Output Squelch Assert Time	TP3		50	300	µs	4
Data Output Squelch De-assert Time	TP3		120	300	µs	5
LOS ASSERT Threshold (OMA)	TP3	-30	-14		dBm	
LOS De-ASSERT Threshold (OMA)	TP3		-12.4	-8	dBm	
LOS Hysteresis	TP3	0.5	1.6		dB	

Notes:

1. These optical specifications are dependent upon the performance of the PRIZM LIghtTurn cable assembly, which assumes a maximum of 2 dB insertion loss. More details are provided on the PRIZM LightTurn cable assembly specification. Please contact your Avago sales representative to receive this specification.
2. Measured with conformance test signal at TP3 for BER = 10e-12.
3. These are unfiltered rise and fall times without de-emphasis measured between the 20% and 80% levels using a 500 MHz square wave test pattern. Impairments in measurements due to the test system are removed. Specifications are for information only.
4. This is the module response time from fall of Rx input to less than Rx input LOS threshold to squelch of Rx outputs.
5. This is the module response time from rise of Rx input to greater than Rx input LOS threshold to resumption of Rx outputs.

100GBASE-SR10 Illustrative Link Power Budgets

Parameter	OM3	OM4	Units	Reference
Effective Modal Bandwidth at 850 nm	2000	4700	MHz•km	
Launch Power in OMA minus TDP, each lane	-6.5		dBm	
Transmitter and Dispersion Penalty, each lane	3.5		dB	
Receiver Sensitivity (OMA)	-11.3		dBm	
Power Budget (for maximum TDP)	8.3		dB	
Operating Distance	0.5 to 100	0.5 to 150	m	
Channel Insertion Loss	1.9	1.5	dB	
Allocation for Penalties (for max. TDP)	6.4	6.5	dB	
Unallocated Margin	0	0.3	dB	
Additional Insertion Loss Allowed	0		dB	

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	Transmitter and Receiver modules withstand minimum 1000 V on all pins.
	JEDEC Machine Model (MM) (JESD22-A115-A)	Transmitter and Receiver modules withstand minimum 50 V on all pins.
Immunity	Variation of EN 61000-4-3	Typically minimum effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing	EN 60825-1:2007 CFR21 section 1040	P_{out}: IEC AEL and US FDA CDRH Class 3R* without optical connector, Class 1 with optical connector. CDRH Accession Number: 1020008-001 TUV Certificate Number: R72131700
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File Number: E173874
RoHS Compliance (RoHS Directive 2002/95/EC issued January 27, 2003)	BS EN 1122:2001 Mtd B by ICP for Cadmium, EPA Method 3051A by ICP for Lead and Mercury, EPA Method 3060A and 7196A by UV/Vis Spectrophotometry for Hexavalent Chromium. EPA Method 3540C/3550B by GC/MS for PPB and PBDE BS EN method by ICP and EPA methods by ICP, UV/Vis Spectrophotometry and GC/MS.	Less than 100 ppm of cadmium, Less than 1000 ppm lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl esters.

Transmitter / Receiver Module Contact Assignment and Signal Description

Optical Fiber Exit Side

	1	2	3	4	5	6	7	8	9
A	GND	D2+	GND	D4+	GND	D6+	GND	D8+	GND
B	GND	D2–	GND	D4–	GND	D6–	GND	D8–	GND
C	GND	GND	ADR<2>	Vcc33	Vcc33	Vcc33	DNC	GND	GND
D	D0+	D0–	GND	SDA	DNC	INTL	GND	D10–	D10+
E	GND	GND	ADR<1>	RESET	DNC	SCL	DNC	GND	GND
F	D1+	D1–	GND	Vcc25	DNC	DNC	GND	D11–	D11+
G	GND	GND	ADR<0>	Vcc25	Vcc25	Vcc25	DNC	GND	GND
H	GND	D3–	GND	D5–	GND	D7–	GND	D9–	GND
J	GND	D3+	GND	D5+	GND	D7+	GND	D9+	GND

TX/RX Host Board Pattern – TOP VIEW

Figure 7. TX / RX Host Board Pattern

Signal Name	Signal Description	I/O	Type
Adr[2:0]	TWS Module Bus Address bits: Address has the form 0101hjkx where Adr2, Adr1 and Adr0 correspond to h, j and k respectively and x corresponds to the R/W command.	I	3.3 V LVTTL
D[11:0]p	Module Data Non-inverting Input / Output for channels 11 through 0	I	CML
D[11:0]n	Module Data Inverting Input/ Output for channels 11 through 0	I	CML
DNC	Reserved – Do Not Connect to any electrical potential on Host PCB		
GND	Signal Common: All module voltages are referenced to this potential unless otherwise stated. Connect these pins directly to the host board signal ground plane.		
IntL	Interrupt signal to Host, Asserted Low: An interrupt is generated in response to any Fault condition, loss of input signal or assertion of any monitor Flag. It may be programmed through the TWS interface to generate either a pulse or static level with static mode as default. This output presents a High-Z condition when IntL is de-asserted and requires a pull-up on the Host board. Pull-up to the Host 3.3 V supply is required.	O	3.3 V LVTTL, high-Z or driven to 0 level
ResetL	Reset signal to module, Asserted Low: When asserted the optical outputs are disabled, TWS interface commands are inhibited, and the module returns to default and non-volatile settings. An internal pull-up biases the input High if the input is open.	I	3.3 V LVTTL
SDA	TWS interface data signal: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is required.	I/O	3.3 V LVTTL, high-Z or driven to 0 level
SCL	TWS interface clock signal l: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is required.	I	3.3 V LVTTL
V_{cc25}	2.5 V Power supply, External common connection of pins required – not common internally		
V_{cc33}	3.3 V Power supply, External common connection of pins required – not common internally		
Case Common	Not accessible in connector. Case common incorporates exposed conductive surfaces including threaded bosses and is electrically isolated from signal common, i.e. GND. Connect as appropriate for EMI shield integrity		

Recommended Power Supply Filtering

It is recommended to use separate power supply filters for V_{cc33} and V_{cc25} as in Figure 8. This filter is similar to other module specifications, such as SFF-8431 Rev 3.0 section D17 Figure 56.

Separate power supply filters shall be used for TX and RX modules.

The host power supply noise level compliance point is at point X.

The host power supply voltage level compliance point is at point Y, and host must take into account of the possible power supply drop due to the MEG-Array interface.

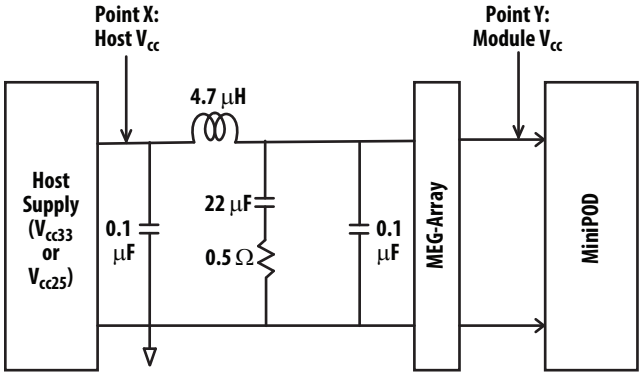


Figure 8. Recommended TX and RX Power Supply Filter

Power Supply Sequence

TX and RX Modules Power Supplies

There is no special requirement in the order of V_{cc33} and V_{cc25} power supply up/down sequence for TX or RX modules. However, it is recommended that

- Upon power down, the V_{cc33} and V_{cc25} shall be within 0 mV to +50 mV. If the residual voltage is larger than 50 mV, it can cause the TX or RX module to fail to start up.

Host ASIC Power Supplies

It is required that

- The maximum delay of power up/down between host ASIC and TX or RX module shall be shorter than 1 s to avoid any potential reliability damage to the modules.

It is recommended that: [1]

- The host ASIC power supply shall be turned on no later than TX or RX module power supplies (3.3 V and 2.5 V).
- The host ASIC power supply shall be turned off no earlier than module power supplies (3.3 V and 2.5 V).

If this condition cannot be met in the system design, the following shall be taken into account in the ASIC design. In the case when the RX module is powered on, host ASIC is power off, the host ASIC electrical input ESD diodes can be forward-biased through a 50 Ω resistor to the V_{cc25} supply (see Figure 10). The host ASIC ESD diodes shall be designed to tolerate such forward biasing.

High Speed and Low Speed IOs

The power supply sequence and the ramp rate shall be designed by the user to meet the absolute maximum specifications as in "Data Input Voltage – Single Ended" and "Control Input Voltage".

It is required that:

- Data signal shall NOT be presented at TX high speed inputs before both V_{cc33} and V_{cc25} are turned on for the TX module; and data signal shall be turned off at TX high speed inputs before both V_{cc33} and V_{cc25} are turned off for the TX module.

It is recommended that:

- The low speed inputs are pulled down when the TX and RX V_{cc33} or V_{cc25} are off.

Note:

1. In the case when host ASIC is turned on and the module power supply is off, the TX high speed input (if DC coupled to ASIC) and TX/RX low speed IO ESD diodes can be forward-biased by the ASIC. The following design shall take care of the potential latch up or reliability issues:
   - The TX high speed ESD diodes are designed to tolerate a minimum of 10 mA forward biasing current assuming ASIC is CML driver
   - The host system or ASIC low speed IO pull-ups shall be sufficient to limit the forward biasing current in the low speed IO ESD diodes.

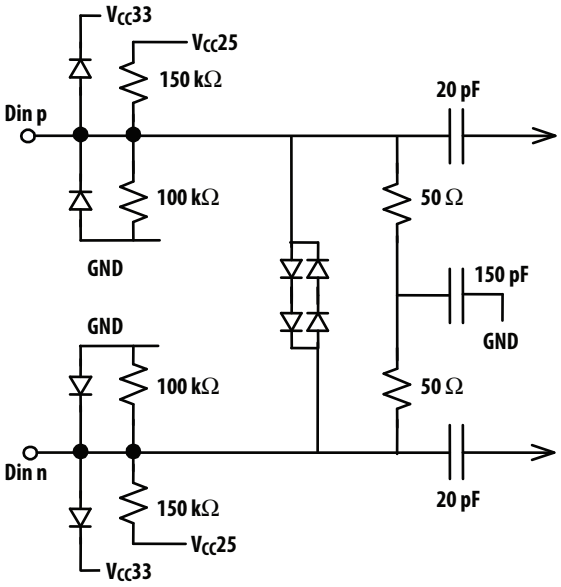


Figure 9. Transmitter Data Input Equivalent Circuit

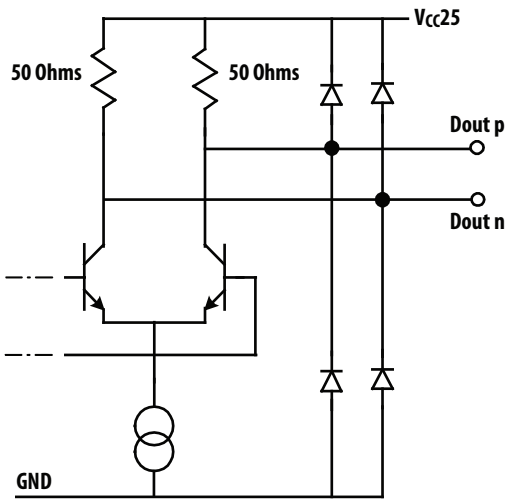


Figure 10. Receiver Data Output Equivalent Circuit

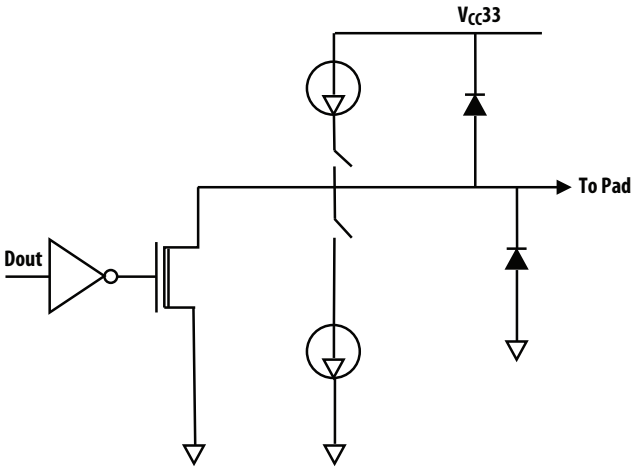


Figure 11. Low Speed IO Equivalent Circuit, INTL

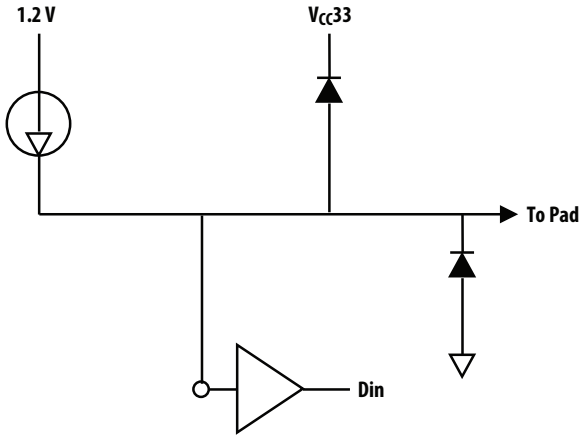


Figure 12. Low Speed IO Equivalent Circuit, RESETL

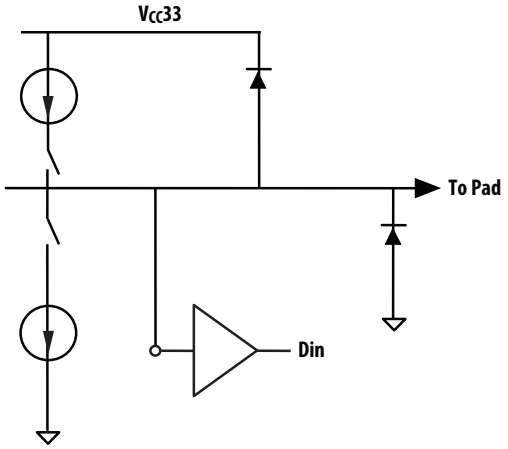


Figure 13. Low Speed IO Equivalent Circuit, ADR<2:0>

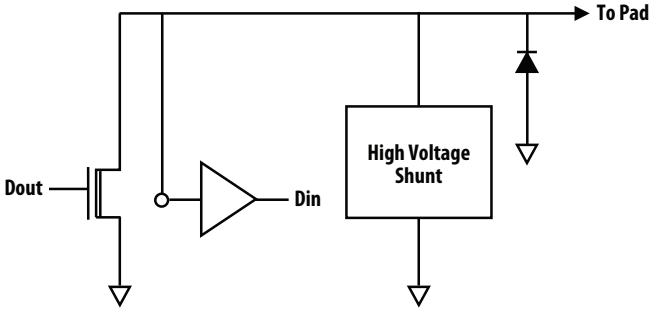


Figure 14. Low Speed IO Equivalent Circuit, SDA, SCL

Control Timing Diagrams

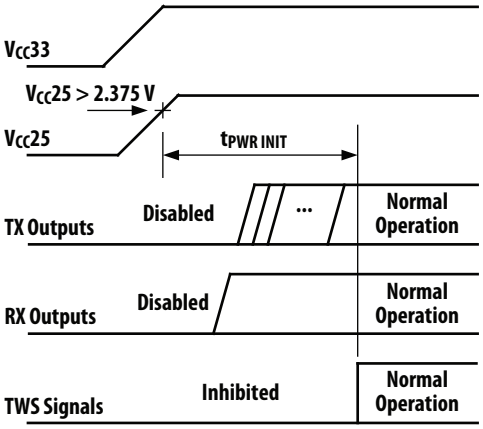


Figure 15. Power-Up Sequence

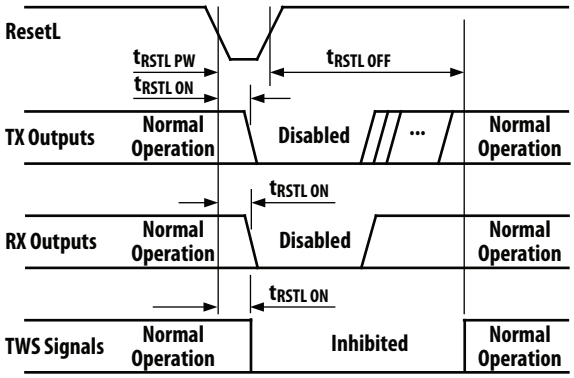


Figure 16. ResetL Sequence

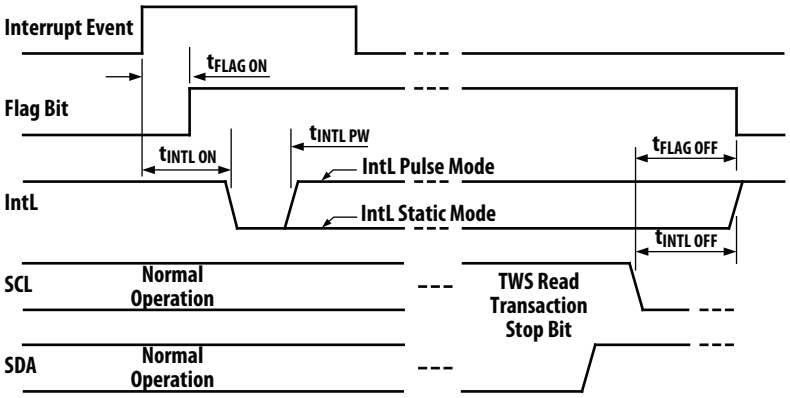


Figure 17. Interrupt Sequence

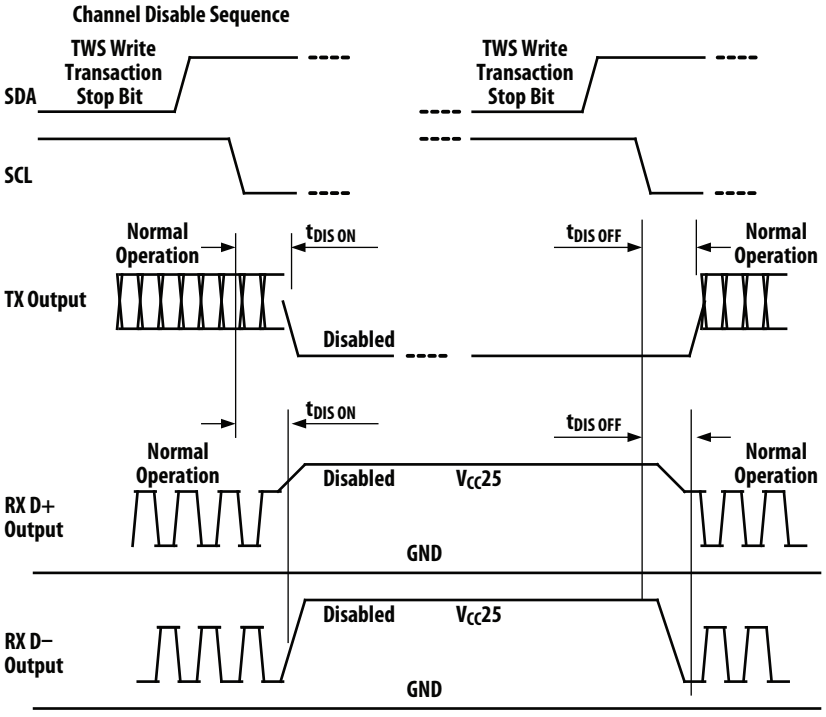


Figure 18. Channel Disable Sequence

LOS Squelch Sequence

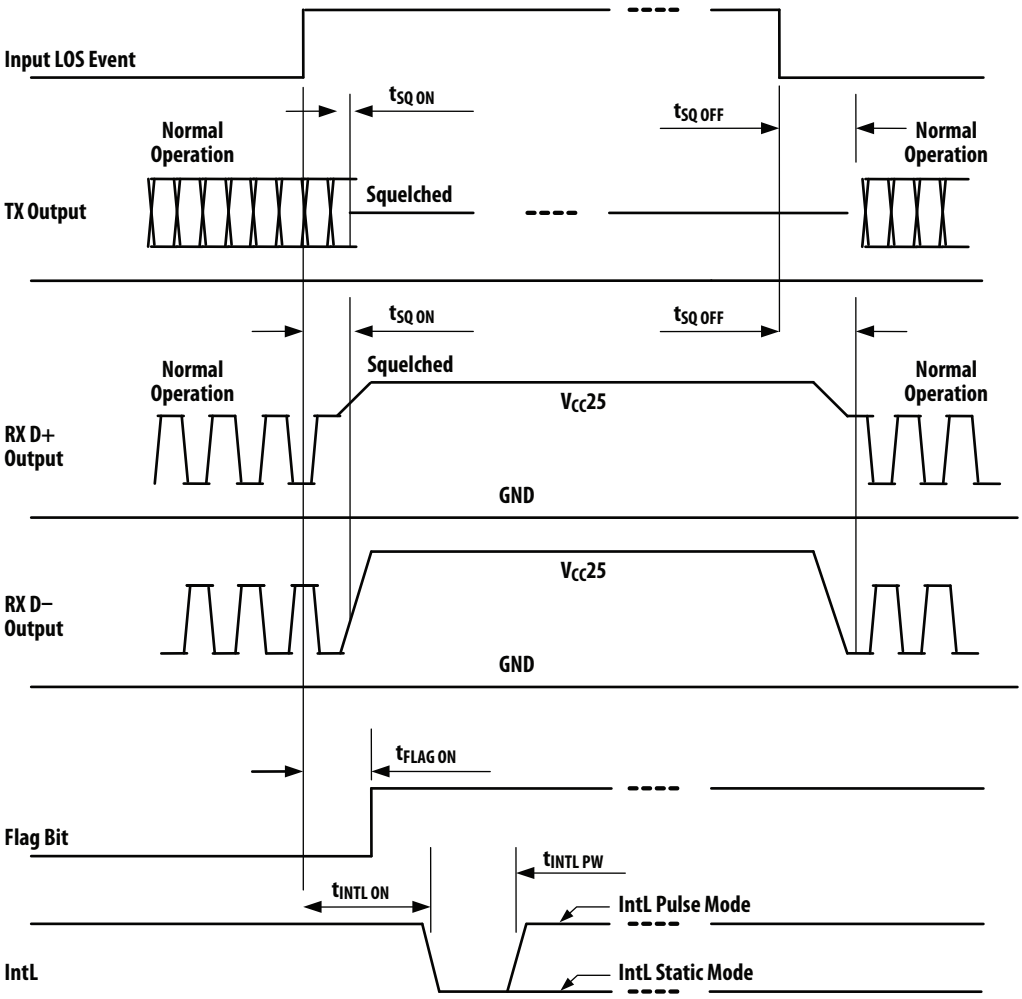
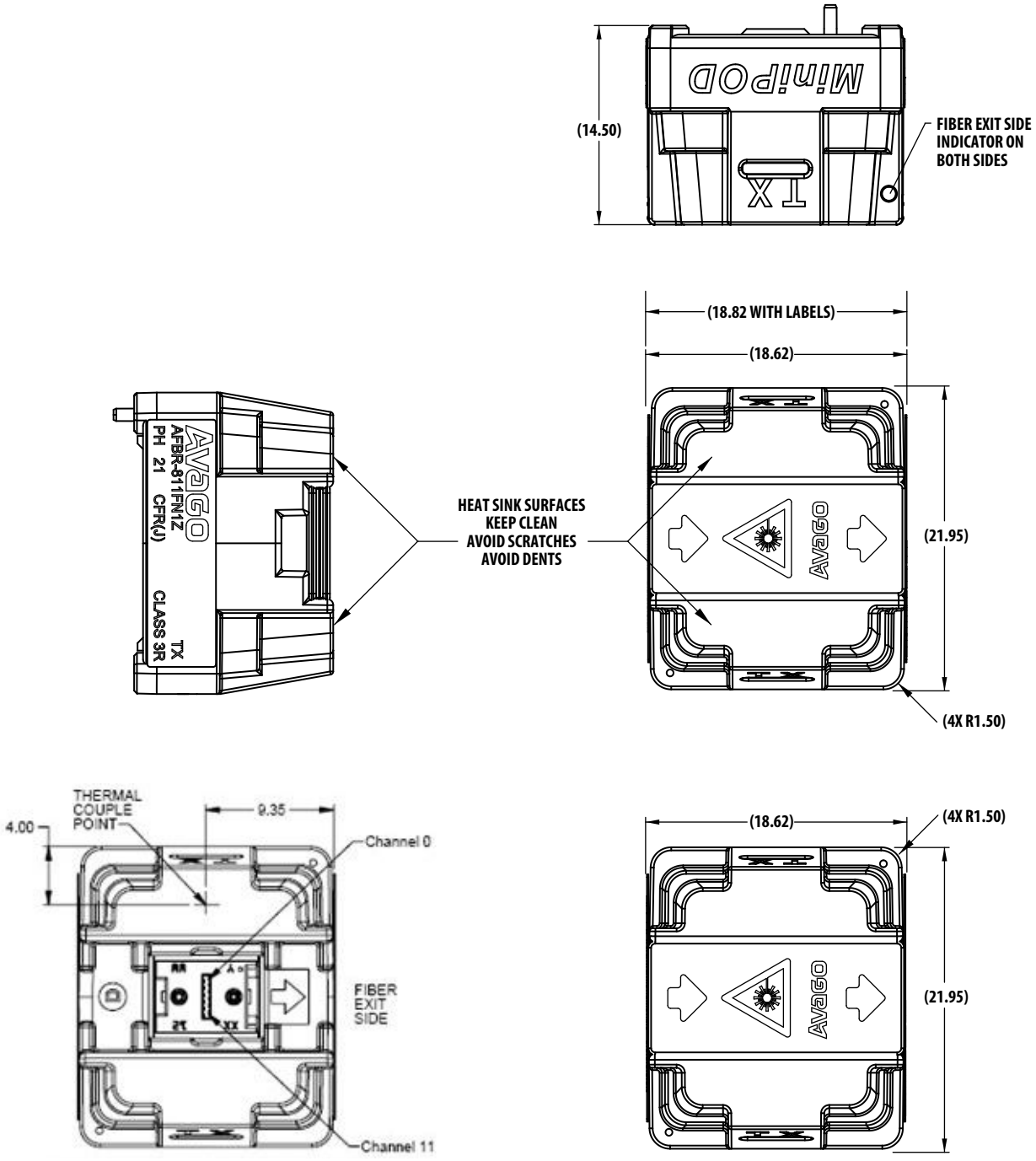


Figure 19. LOS Squelch Sequence

Package Mechanical Outline – Flat Ribbon Cable Housing



CHANNEL LOCATIONS ARE THE SAME FOR "TX" AND "RX"

Figure 20. Package Dimensions 1 (mm)

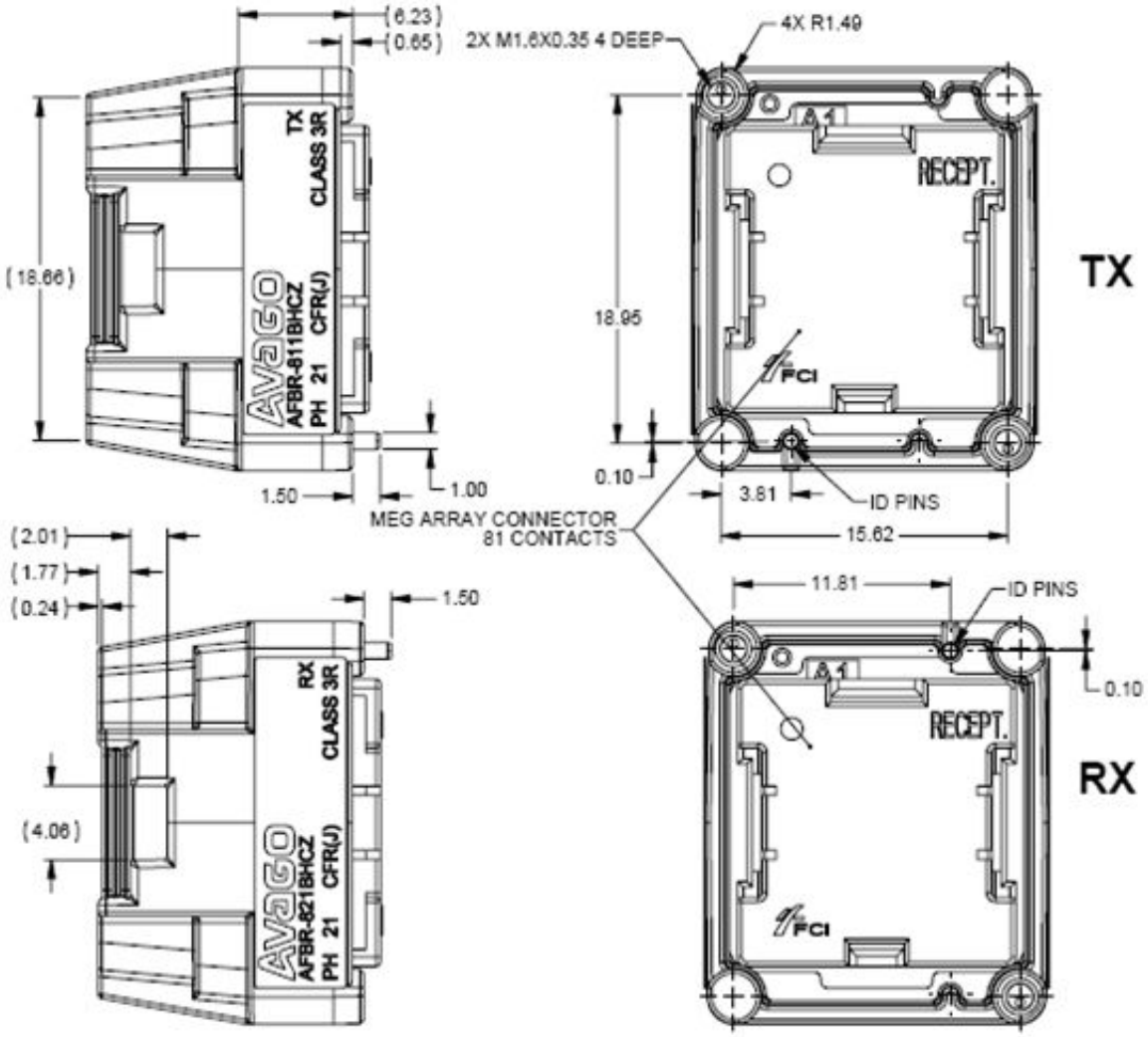


Figure 21. Package Dimensions 2 (mm)

Package Mechanical Outline – Round Cable Housing

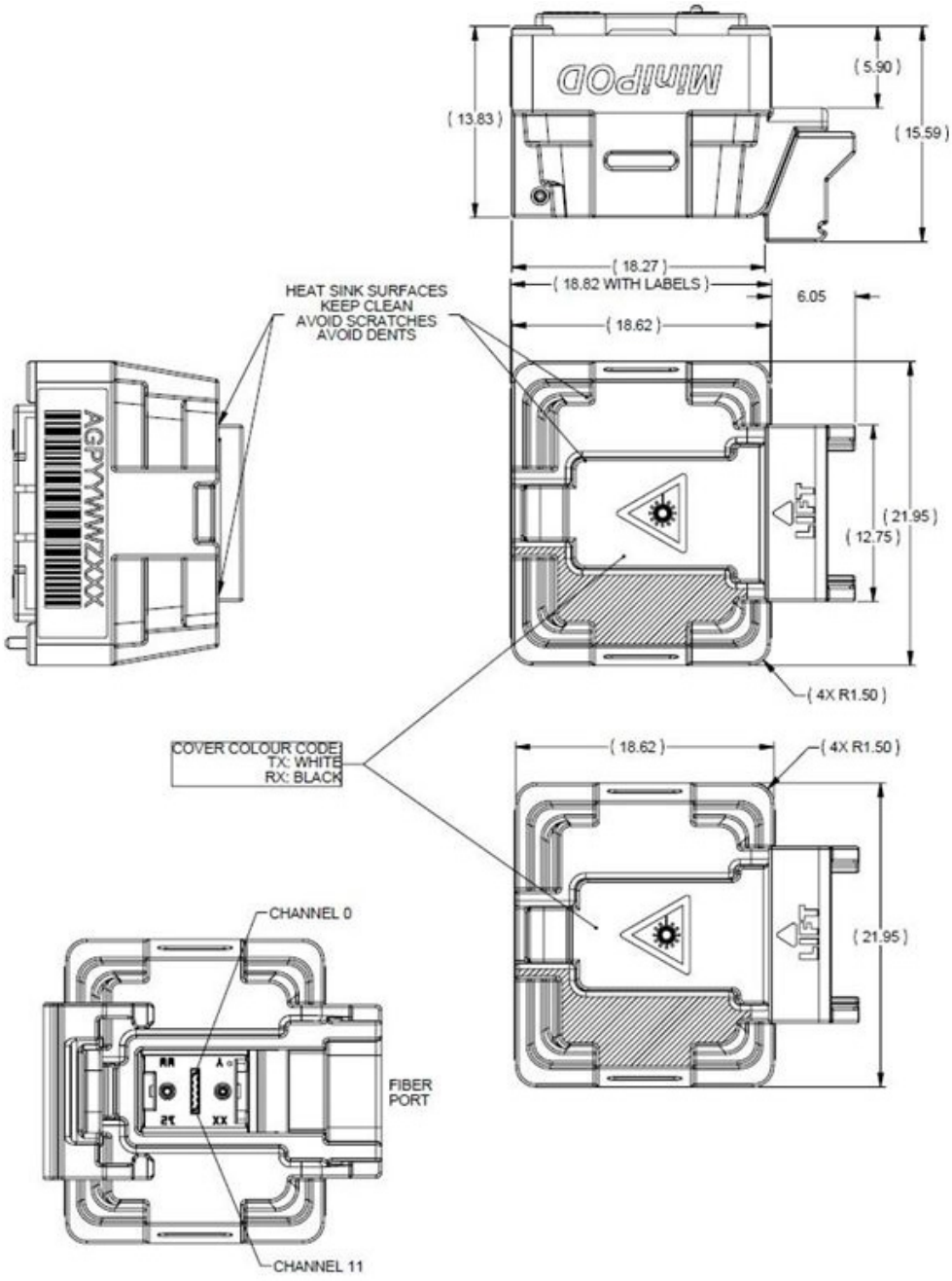


Figure 22. Package Dimensions 1 (in mm)

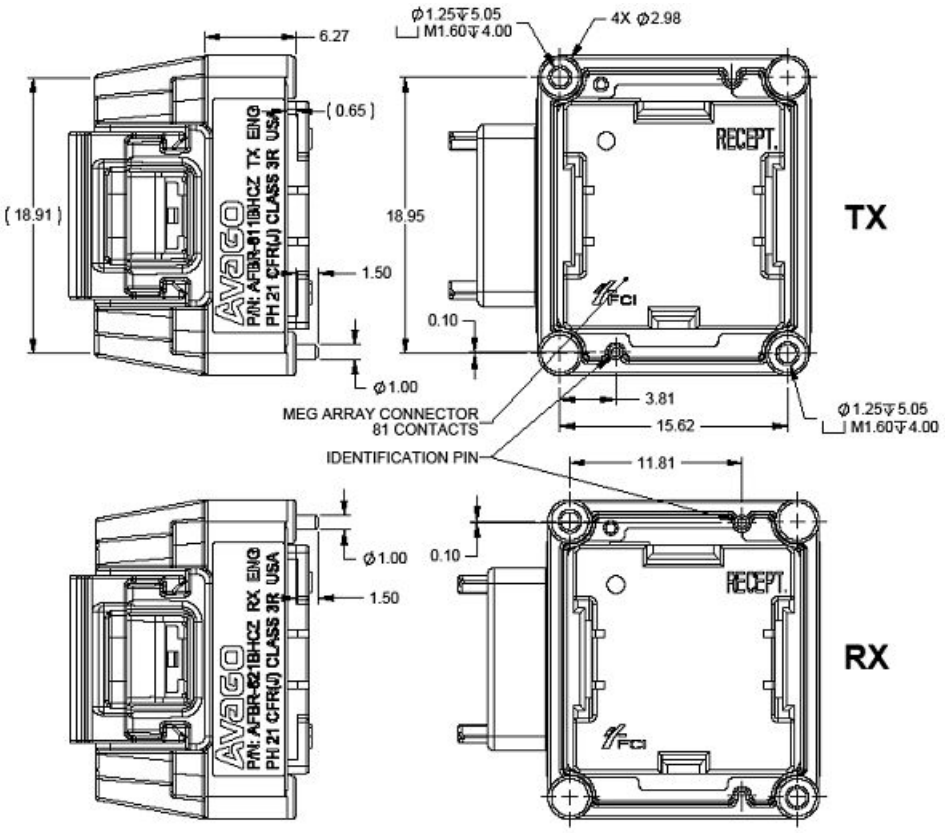


Figure 23. Package Dimensions 2 (in mm)

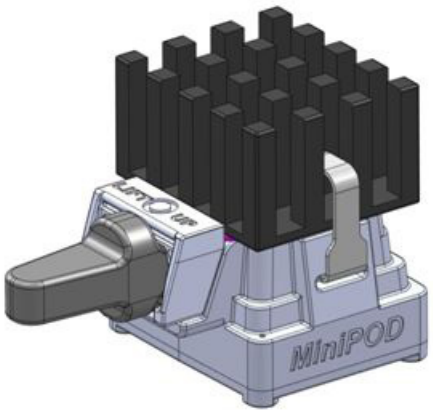


Figure 24. Heatsink Option (x = H in part number)

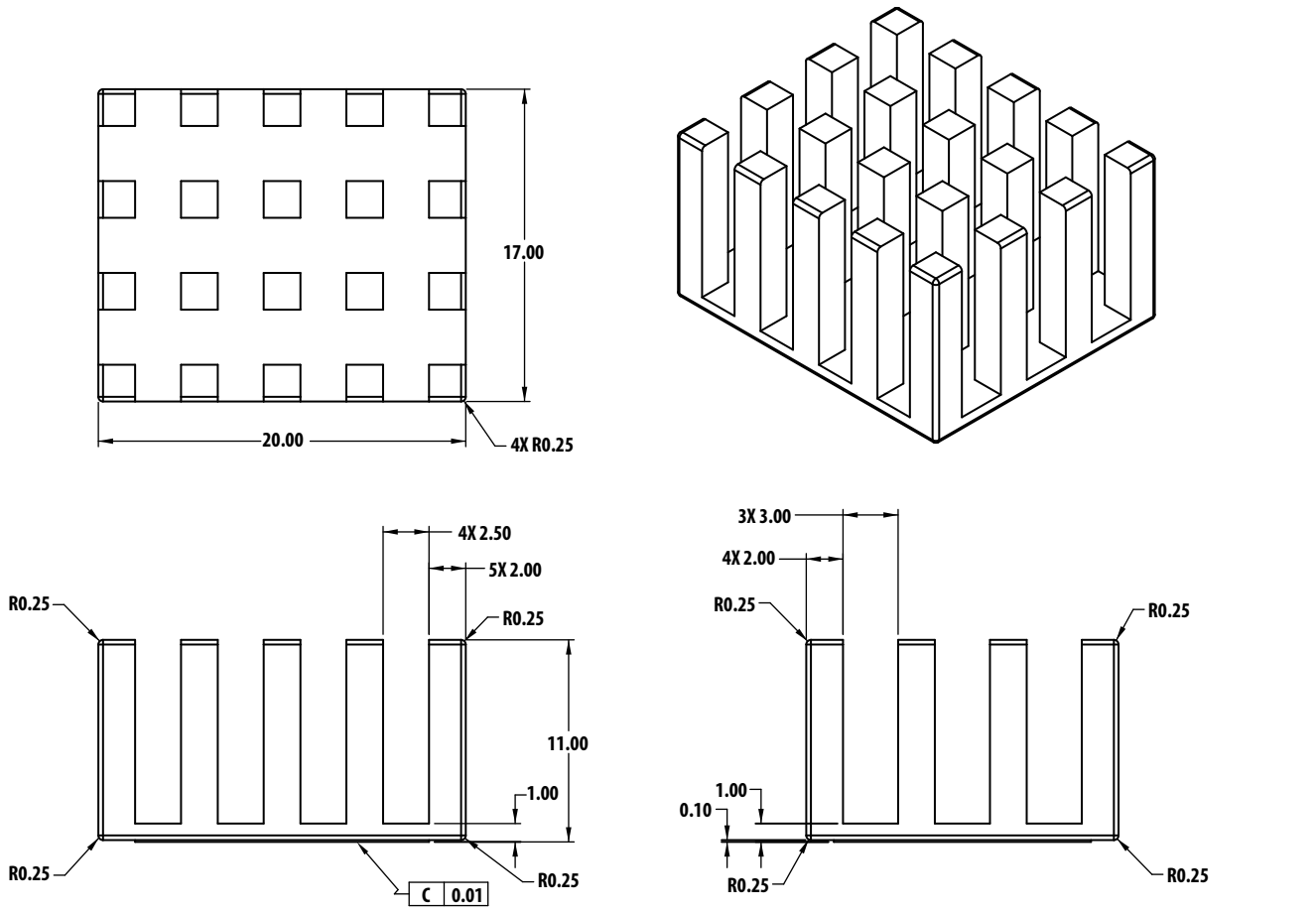


Figure 25. Heatsink Drawing (dimensions in mm)

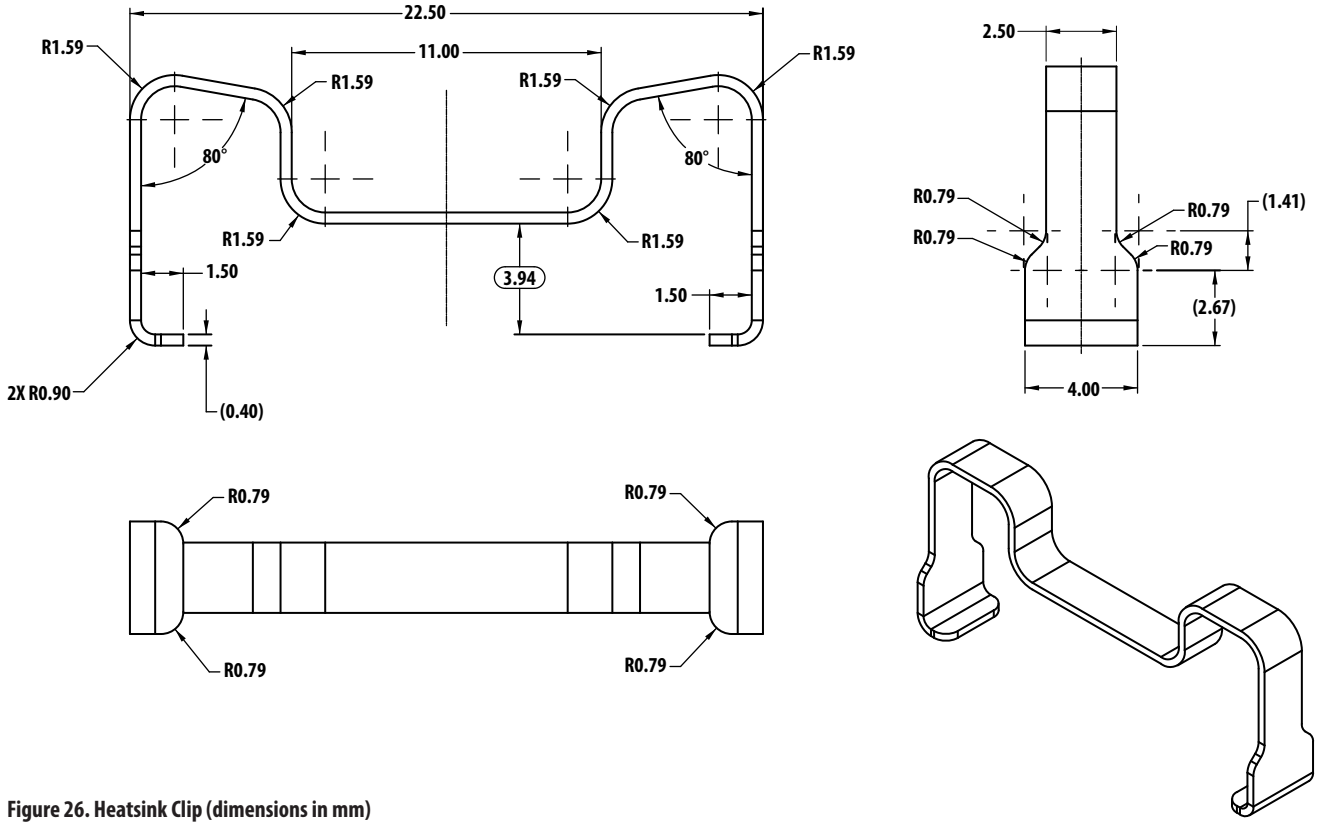


Figure 26. Heatsink Clip (dimensions in mm)

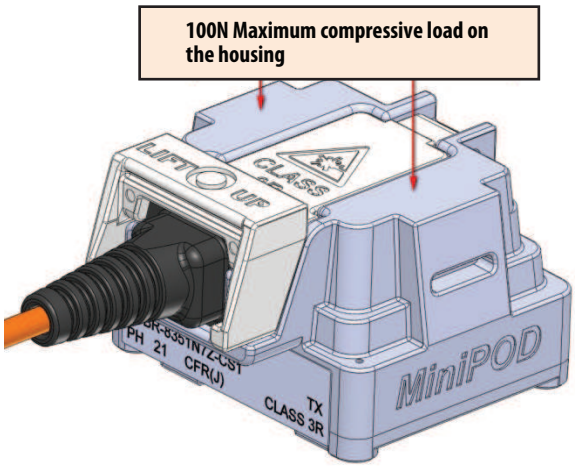


Figure 27. Module Compression Force

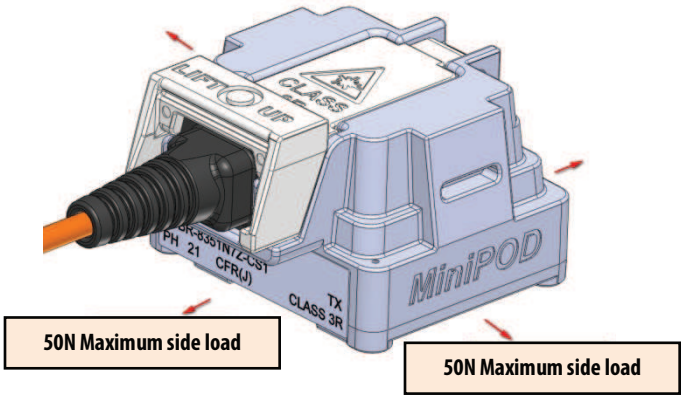


Figure 28. Module Side Force

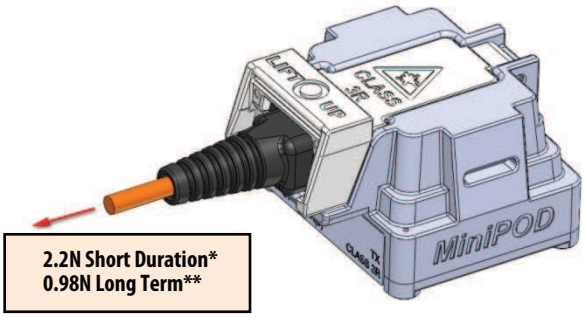


Figure 29. Fiber Pull Force

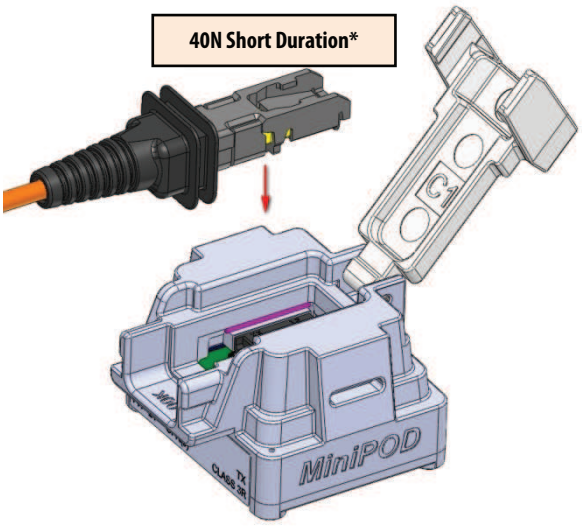


Figure 30. PRIZM Insertion Force

* Short duration is <15 seconds.

** Long term (>5 minutes), exceeding this force long term could cause the optical light output power to drop or Rx sensitivity to diminish, which is not recoverable.

Host PCB Layout

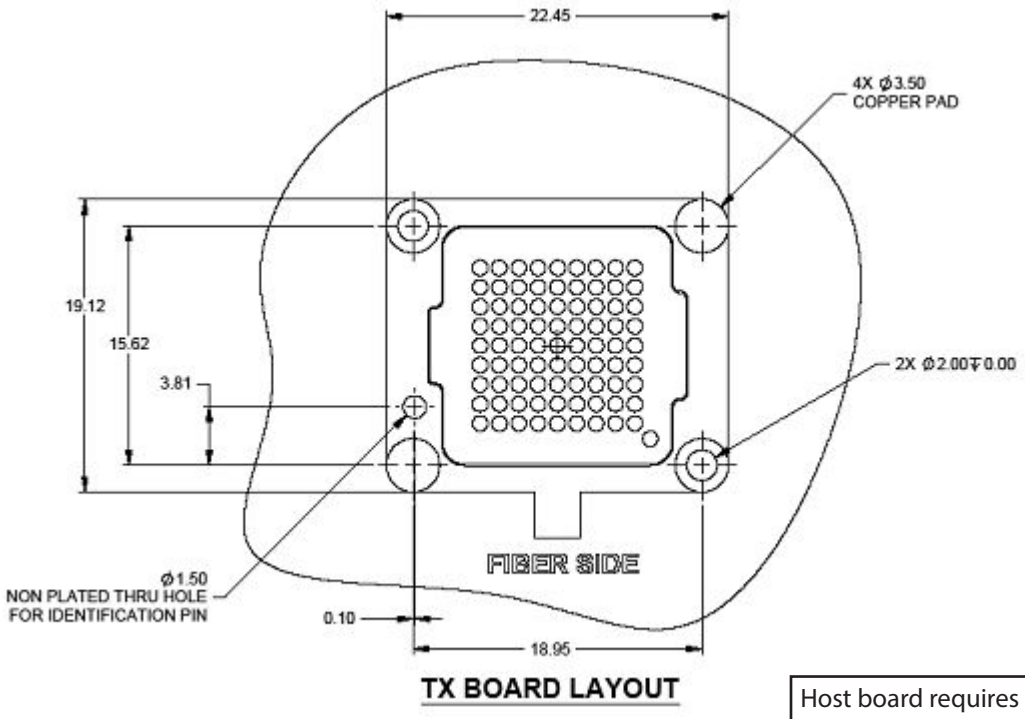


Figure 31. TX Host PCB Layout

Host board requires FCI P/N 55714
9×9 pin 4mm plug connector
(Recommend 55714-202LF)

http://portal.fciconnect.com/Comergent//fci/drawing/55714.pdf

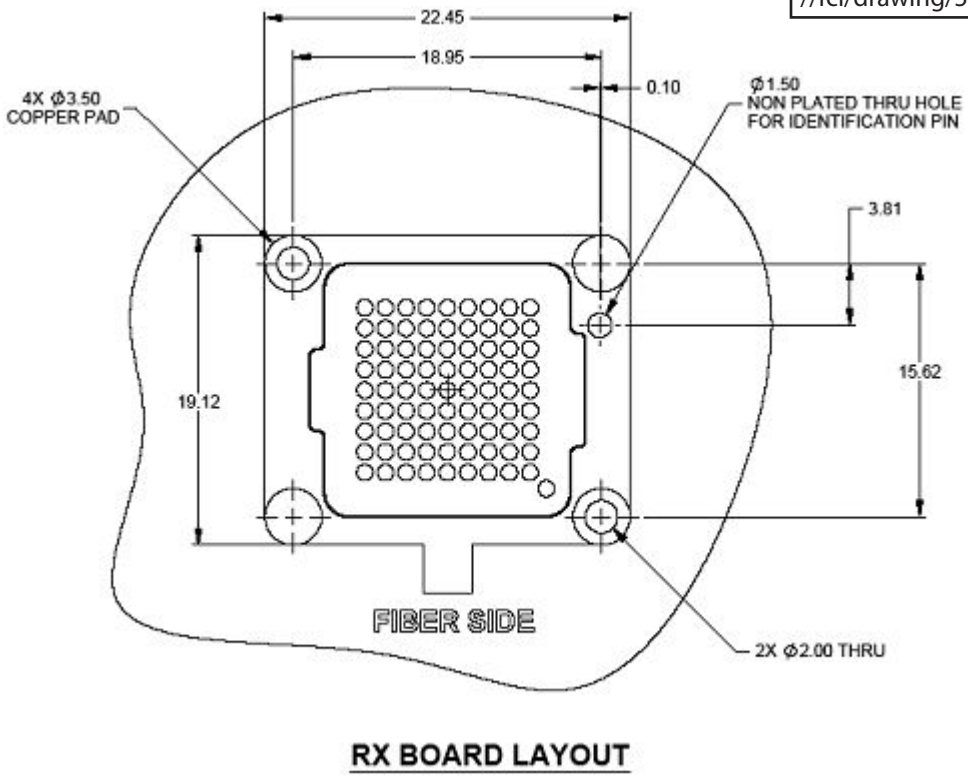


Figure 32. RX Host PCB Layout