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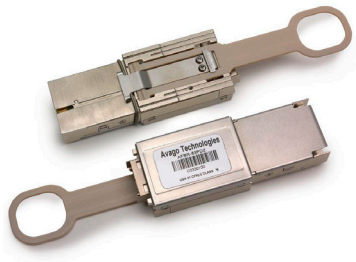
AFBR-83PDZ

12Channel x 10.3125Gbps Transceiver
CXP Pluggable, Parallel Fiber-Optics Module

Data Sheet



Description

The Avago Technologies AFBR-83PDZ is a Twelve-Channel, Pluggable, Parallel, Fiber-Optic CXP Transceiver for 100 Gigabit Ethernet (100GbE) and 12 x 10G InfiniBand (IB) quadruple data rate (IB-QDR) applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnect applications. It integrates twelve data lanes in each direction with greater than 120 Gbps aggregate bandwidth. Each lane can operate at 10.3125 Gbps up to 100 m using OM3 fiber and 150m using OM4 fiber. These modules are backward compatible to the 12 x 5G IB dual data rate (IB-DDR) and 12 x 2.5G IB single data rate (IB-SDR) applications.

These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850 nm. The electrical interface uses an 84-contact edge type connector. The optical interface uses a 24-fiber MTP® (MPO) connector. This module incorporates Avago Technologies proven integrated circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

Applications

- 100 GbE and IB-QDR / IB-DDR / IB-SDR interconnects
- Data Aggregation, Backplane and Proprietary Protocol and Density Applications
- Datacom/Telecom switch & router connections

Part Number Ordering Options

AFBR-83PDZ	12x 10.3125 Gbps (Ethernet) and IB-QDR/ IB-DDR/IB-SDR with Full Diagnostic Monitoring
AFBR-83EVB	CXP Evaluation Board
AFBR-83EVK*	CXP Evaluation Kit

* Includes GUI, User Guide, i-Port and Power Supply

Features

- Compliant to SFF-8642: Mini Multilane Series: Shielded Integrated Connector, and IBTA Annex A6 CXP Interface Specification
- Each of the twelve channels is compliant on a per lane electrical and optical specification basis with the IEEE 802.3ba 100GbE (100 GBASE-SR10 and CPPI) specifications, and supporting InfiniBand QDR/DDR/SDR application
- Multi-rate capable from 1 Gbps to 10.5 Gbps
- High Channel Capacity: >120 Gbps per module, bi-directional, with twelve independent Transmitters and Receivers each
- Operates at 10.3125 Gbps per channel with 64b/66b encoded data for 100GbE application and at 10 Gbps with 8b/10b encoded data for IB-QDR application
- Hot Pluggable
- Links up to 100 m using OM3 fiber and 150 m using OM4 fiber
- 0 to 70° C case temperature operating range
- 3.3 V power supply only
- Low power dissipation of < 3 W
- Proven High Reliability 850 nm technology: Avago VCSEL array transmitter and Avago PIN array receiver
- Two Wire Serial (TWS) interface with maskable interrupt for expanded functionality including:
  - Individual channel functions: channel/output disable, squelch disable, and lane polarity inversion
  - Diagnostic Monitoring functions: module temperature and supply voltages, per channel laser current and laser power, and input receiver power
  - Status per channel: Tx fault, electrical (transmitter) and optical (receiver) LOS, and alarm flags
- Utilizes a standard 24 lane optical fiber with MTP® (MPO) optical connector for high density and thin, light-weight cable management

Patent - www.avagotech.com/patents

WARNING

CAUTION! Viewing the laser output with certain optical instruments (for example, eye loupes, magnifiers and microscopes) within a distance of 100 mm may pose an eye hazard

CAUTION! Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure

Note: Standard used for classification: EN 60825-1:2007

CLASS 1M LASER PRODUCT: INVISIBLE LASER RADIATION, DO NOT VIEW DIRECTLY WITH OPTICAL INSTRUMENTS

Transmitter

The optical transmitter incorporates a 12-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 12-channel input buffer and laser driver, diagnostic monitors, and control and bias blocks. The transmitter is designed for EN 60825 and CDRH eye safety compliance. The Tx Input Buffer provides differential inputs presenting a nominal differential input impedance of 100 Ohms. AC coupling capacitors of 0.1uF value are located inside the CXP module and are not required on the host board. For module control and interrogation, the control interface incorporates a Two Wire Serial (TWS) interface of clock and data signals.

Modules have monitors for VCSEL bias, light output power (LOP), temperature, and power supply voltage implemented; real-time results are available through the TWS interface. Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential inputs, de-activate channels, disable the squelch function and program input equalization levels to reduce the effect of long PCB traces.

Flags are also set and interrupts generated for loss of input signal (LOS) and transmitter fault conditions. All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset by reading the appropriate flag register.

The optical output will squelch for loss of input signal unless squelch is disabled. The input thresholds for the Tx squelch are tied to Tx LOS thresholds which are informative only. See Tx LOS thresholds specification on page 6. Fault detection or channel deactivation through the TWS interface will disable the channel. Status, alarm and fault information are available via the TWS interface. To reduce the need for polling, the hardware interrupt signal is provided to inform hosts of an assertion of an alarm, LOS and/or Tx fault.

Receiver

The optical receiver incorporates a 12-channel PIN photodiode array, a 12-channel pre-amplifier and output buffer, diagnostic monitors, and control and bias blocks. The Rx Output Buffer provides differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 Ω to AC ground and 100 Ω differentially that should be differentially terminated with 100 Ω. AC coupling capacitors of 0.1uF value are located inside the CXP module and are not required on the host board.

Modules have a monitor for optical input power; results are available through the TWS interface. Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential outputs, de-activate channels, disable the squelch function, program output signal amplitude and deemphasis.

Flags are also set and interrupts generated for loss of optical input signal (LOS). All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register.

The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through TWS interface. Status and alarm information are available via the TWS interface. To reduce the need for polling, the hardware interrupt signal is provided to inform hosts of an assertion of an alarm and/or LOS.

High Speed Electrical Signal Interface

TX

TX[0-11]p/n are the CXP module transmitter electrical data inputs and are internally AC coupled (0.1 μF) differential lines with 100 Ω differential terminations. AC coupling capacitors exist inside the CXP module and are not required on the host board. All transmitter electrical input channels are compliant to module CPPI specifications per IEEE 802.3ba.

RX

Rx[0-11]p/n are the CXP module receiver electrical data outputs and are internally AC coupled (0.1 μF) differential lines that should be terminated with 100 Ω differential at the host side. AC coupling capacitors exist inside the CXP module and are not required on the host board. All receiver electrical output channels are compliant to module CPPI specifications per IEEE 802.3ba.

Tx Equalization Control

Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel.

- Codes 1xxxb are reserved.
- Writing 0111b calls for full-scale equalization.
- Writing 0000b calls for no equalization.

Intermediate code values call for intermediate levels of equalization.

Rx De-emphasis Control

Rx Output de-Emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel.

- Codes 1xxxb are reserved.
- Writing 0111b calls for full-scale de-emphasis.
- Writing 0000b calls for minimum de-emphasis.

Writing intermediate code values calls for intermediate levels of de-emphasis.

Regulatory & Compliance

Various standard and regulations apply to the modules. These include eye-safety, EMC, ESD and RoHS. See the Regulatory Section for details regarding these and component recognition.

Handling and Cleaning

The transceiver module can be damaged by exposure to current surges and over voltage events. Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Wave soldering, reflow soldering and/or aqueous wash process with the modules on board are not recommended. Normal handling precautions for electrostatic discharge sensitive devices should be observed.

Each module is supplied with an inserted port plug for protection of the optical ports. This plug should always be in place whenever a fiber cable is not inserted.

The optical connector includes recessed elements that are exposed whenever a cable or port plug is not inserted. Prior to insertion of a fiber optic cable, it is recommended that the cable end be cleaned to avoid contamination from the cable plug. The port plug ensures the optics remains clean and no additional cleaning should be needed. In the event of contamination, dry nitrogen or clean dry air at less than 20 psi can be used to dislodge the contamination. The optical port features (e.g. guide pins) preclude use of a solid instrument. Liquids are also not advised.

Link Model and Reference Channel

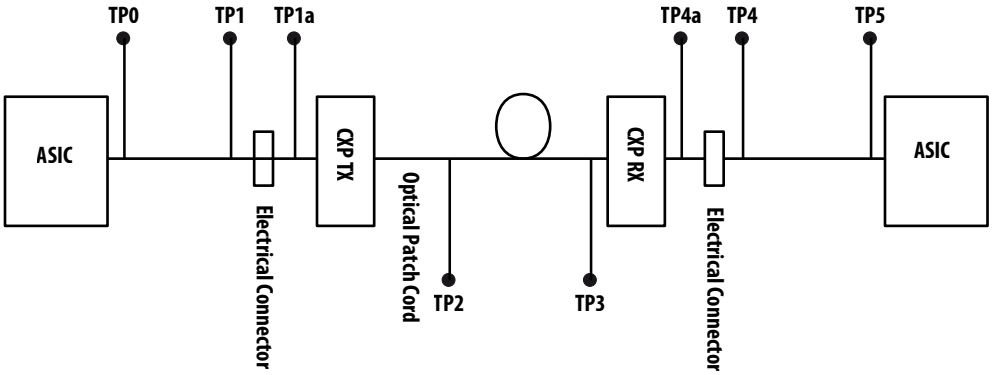


Figure 1. Link Model test point definitions

Performance specifications for the AFBR-83PDZ Transceiver are based on IEEE 802.3ba 100GBASE-SR10.

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operation Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	Ts	-40	85	°C	
Absolute Maximum Operating Temperature			85	°C	Note 1
3.3 V Power Supply Voltage	Vcc33	-0.5	4.0	V	
Data Input Voltage – Single Ended		-0.5	Vcc33+0.5, 4.0	V	
Data Input Voltage – Differential	$\|V_{dip} - V_{din}\|$		1.6	V	Note 2
Control Input Voltage	Vi	-0.5	Vcc33+0.5 4.0	V	Note 3
Control Output Current	Io	-20	20	mA	
Relative Humidity	RH	5	85	%	
Receiver Damage Threshold			4	dBm	Note 4

Notes:
1. Electro-optical specifications are not guaranteed outside the recommended operating temperature range. Operation at or above the maximum Absolute Maximum Case Temperature for extended periods may adversely affect reliability.
2. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry.
3. The maximum limit is the lesser of Vcc33 + 0.5 V or 4.0 V
4. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power

Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the electrical characteristics hold unless otherwise noted. Electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Case Temperature	Tc	0		70	°C	
3.3 V Power Supply Voltage	Vcc33	3.135	3.3	3.465	V	
Signal Rate per Channel			10.3125		GBd	Note 1
Control Input Voltage High	Vih	2.3		3.6	V	
Control Input Voltage Low	Vil	-0.3		0.4	V	
Host Electrical Compliance			Per IEEE 802.3ba-2010 TP1a and TP4 CPPI specifications for host			
Fiber Length: 4700 MHz•km 50 μm MMF (OM4)				150	m	Note 2
Fiber Length: 2000 MHz•km 50 μm MMF (OM3)				100	m	
Receiver Differential Data Output Load			100		Ω	

Note:
1. For applications beyond 10.3 Gbps per channel, please contact Avago Sales.
2. Channel insertion loss of 1.9 dB (OM3) / 1.5dB (OM4) included with 1.5dB (OM3) / 1dB (OM4) allocated for connection and splice loss.

Transceiver Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40° C, Vcc33 = 3.3 V

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transceiver Power Consumption				3.0	W	With module default settings
Transceiver Power Supply Current – Vcc33				1.0	A	With module default settings
Maximum inrush current				1.25	A	On any contact
Maximum current ramp rate				100	mA/μs	
Power Supply Noise including ripple				50	mVpp	Note 1
Power On Initialization Time	$t_{pwr\ init}$			2000	ms	
Two Wire Serial Interface Clock Rate				400	kHz	
TWS Write Cycle Time (4 byte write)				40	ms	

Note:
1. 1 kHz to frequency of operation at the host supply side of the recommended power supply filter with the module and recommended filter in place. See Figure 8 for recommended power supply filter.

Transmitter Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40° C, Vcc33 = 3.3 V

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential Input Impedance		80	100	120	Ω	
LOS Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	ΔVdi pp losA		110		mVpp	Note 1 Informative
LOS De-Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	ΔVdi pp losD		130	210	mVpp	Note 1 Informative
LOS Hysteresis		0.5		4	dB	

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Single ended input voltage tolerance	TP1a	-0.3		4.0	V	Note 2
AC common mode input voltage tolerance	TP1a	15			mV	RMS
Differential input return loss	TP1		footnote		dB	10 MHz to 11.1 GHz Note 3
Differential to common-mode input return loss	TP1	10			dB	10 MHz to 11.1 GHz
J2 Jitter tolerance	TP1a	0.17			UI	Defined in 802.3 ba spec
J9 Jitter tolerance	TP1a	0.29			UI	Defined in 802.3 ba spec
Data Dependent Pulse Width Shrinkage (DDPWS) tolerance	TP1a	0.07			UI	
Eye Mask Coordinates: X1, X2, Y1, Y2	TP1a	SPECIFICATION VALUES	0.11, 0.31 95, 350		UI mV	Hit Ratio = $5x10^{-5}$

Notes:

1. At default Tx EQ setting only. Informative only. Tx LOS thresholds also represent the Tx channel squelch thresholds when enabled. Behavior per IBTA Annex A6 CXP Interface Specification (Tx squelch disabled).
2. Referred to TP1 signal common; The single-ended input voltage tolerance is the allowable range of the instantaneous input signals
3. From 10 MHz to 11.1 GHz, the magnitude in decibels of the module differential input return loss at TP1 and the host differential output return loss at TP1a shall not exceed the limit given in Equation

$$\text{Return\_loss}(f) \geq 12 - 2\sqrt{f} \qquad 0.01 \leq f < 4.1 \text{ GHz}$$

$$\geq 6.3 - 13\log_{10}\left(\frac{f}{5.5}\right) \qquad 4.11 \leq f < 11.1 \text{ GHz}$$

Return_loss(f) is the return loss at frequency f
f is the frequency in GHz.

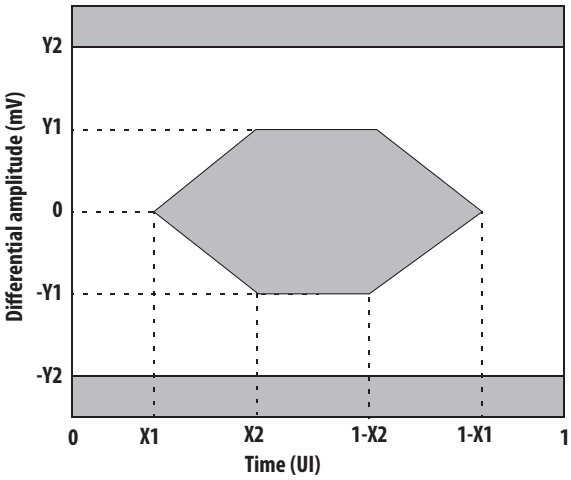


Figure 2. Tx Electrical Eye Mask Coordinates (TP1a) at Hit ratio 5 x 10^{-5} hits per sample

Receiver Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions, with module default settings, unless otherwise noted. Typical values are for Tc = 40° C, Vcc33 = 3.3 V

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Data Output Differential Peak-to-Peak Voltage Swing	TP4	300		850	mV	
AC common mode voltage (RMS)	TP4			7.5	mV	RMS
Termination mismatch at 1MHz	TP4			5	%	
Differential output return loss	TP4		footnote			10 MHz to 11.1 GHz Note 1
Common-mode output return loss	TP4		footnote			10 MHz to 11.1 GHz Note 2
Output transition time 20% to 80%	TP4	28			ps	
J2 Jitter output	TP4			0.42	UI	Defined in 802.3ba spec
J9 Jitter output	TP4			0.65	UI	Defined in 802.3ba spec
Data Dependent Pulse Width Shrinkage (DDPWS)	TP4			0.34	UI	
Eye Mask coordinates: X1, X2, Y1, Y2	TP4	SPECIFICATION VALUES 0.29, 0.5 150, 425			 UI mV	Hit Ratio = $5x10^{-5}$

Notes:

1. From 10 MHz to 11.1 GHz, the magnitude in decibels of the module differential output return loss at TP4 and the host differential input return loss at TP4a shall not exceed the limit given in Equation

$$\text{Return\_loss}(f) \geq 12 - 2\sqrt{f} \qquad 0.01 \leq f < 4.1 \text{ GHz}$$

$$\geq 6.3 - 13\log_{10}\left(\frac{f}{5.5}\right) \qquad 4.11 \leq f < 11.1 \text{ GHz}$$

2. From 10 MHz to 11.1 GHz, the magnitude in decibels of the module common-mode output return loss at TP4 shall not exceed the limit given in Equation

$$\text{Return\_loss}(f) \geq 7 - 1.6f \qquad 0.01 \leq f < 2.5 \text{ GHz}$$

$$\geq 3 \qquad 2.5 \leq f < 11.1 \text{ GHz}$$

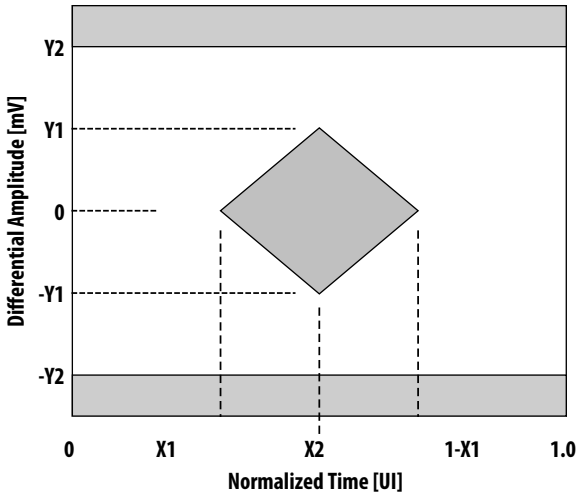


Figure 3. Rx Electrical Eye Mask Coordinates (TP4) at Hit ratio 5 x 10^{-5} hits per sample

Transmitter Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40° C, Vcc33 = 3.3 V

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Center wavelength	TP2	840	850	860	nm	
RMS spectral width	TP2			0.65	nm	RMS Spectral Width is the standard deviation of the spectrum
Average launch power, each lane	TP2	-7.6		2.4	dBm	
Optical Modulation Amplitude (OMA) each lane	TP2	-5.6		3	dBm	Even if the TDP<0.9 dB, the OMA minimum must exceed this minimum value
Difference in launch power between any two lanes (OMA)	TP2			4	dB	
Peak power, each lane	TP2			4	dBm	
Launch power in OMA minus TDP, each lane	TP2	-6.5			dBm	
Transmitter and dispersion penalty (TDP), each lane	TP2			3.5	dB	
Extinction ratio	TP2	3			dB	
Optical return loss tolerance	TP2			12	dB	
Encircled flux	TP2		≥ 86% at 19 μm, ≤ 30% at 4.5 μm			If measured into type A1a.2 50 μm fiber in accordance with EN 61280-1-4
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3	TP2		SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4		UI	Hit Ratio = $5x10^{-5}$
Average launch power of OFF transmitter, each lane	TP2			-30	dBm	

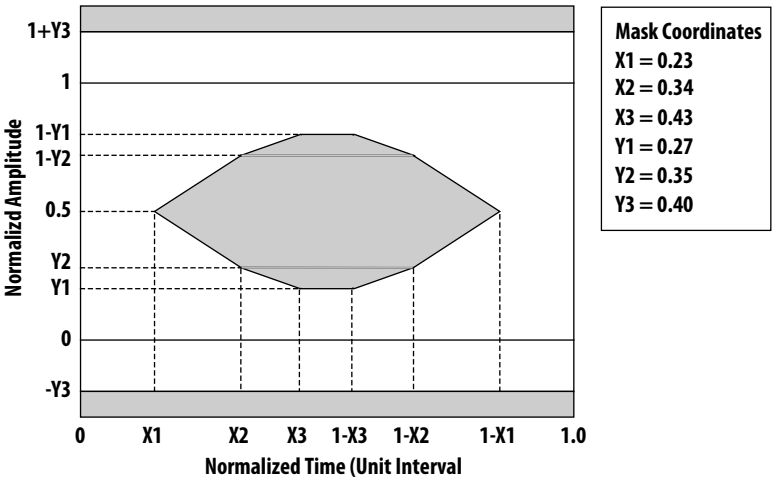


Figure 4. Transmitter eye mask definitions (TP2) at Hit ratio 5 x 10^{-5} hits per sample

Receiver Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40° C, Vcc33 = 3.3 V

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Center wavelength, each lane	TP3	840	850	860	nm	
Average power at receiver input, each lane	TP3	-9.5		2.4	dBm	
Receiver Reflectance	TP3			-12	dB	
Receiver Sensitivity (OMA)	TP3	-11.3		3	dBm	Informative
Stressed receiver sensitivity in OMA, each lane	TP3			-5.4	dBm	Measured with conformance test signal at TP3 for BER = 10e-12
Peak power, each lane	TP3			4	dBm	
Conditions of stressed receiver sensitivity:	TP3					Note 1
Vertical Eye Closure Penalty, each lane	TP3		1.9		dB	
Stressed eye J2, Jitter, each lane	TP3		0.30		UI	
Stressed eye J9, Jitter, each lane	TP3		0.47		UI	
OMA of each aggressor lane	TP3		-0.4		dBm	
Rx LOS Assert Threshold	TP3	-30			dBm OMA	
Rx LOS De-assert Threshold	TP3			-8	dBm OMA	
LOS Hysteresis	TP3	0.5			dB	

Notes:
1. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver. The apparent discrepancy between VECP and TDP is because VECP is defined at eye center while TDP is defined with ±0.15 UI offsets of the sampling instant

100GBASE-SR10 Illustrative Link Power Budgets

Parameter	OM3	OM4	Units	Reference
Effective Modal Bandwidth at 850 nm	2000	4700	MHz•km	
Launch Power in OMA minus TDP, each lane	-6.5		dBm	
Transmitter and Dispersion Penalty, each lane	3.5		dB	
Receiver Sensitivity (OMA)	-11.3		dBm	
Power Budget (for maximum TDP)	8.3		dB	
Operating Distance	0.5 to 100	0.5 to 150	m	
Channel Insertion Loss	1.9	1.5	dB	
Allocation for Penalties (for max. TDP)	6.4	6.5	dB	
Unallocated Margin	0	0.3	dB	
Additional Insertion Loss Allowed	0		dB	

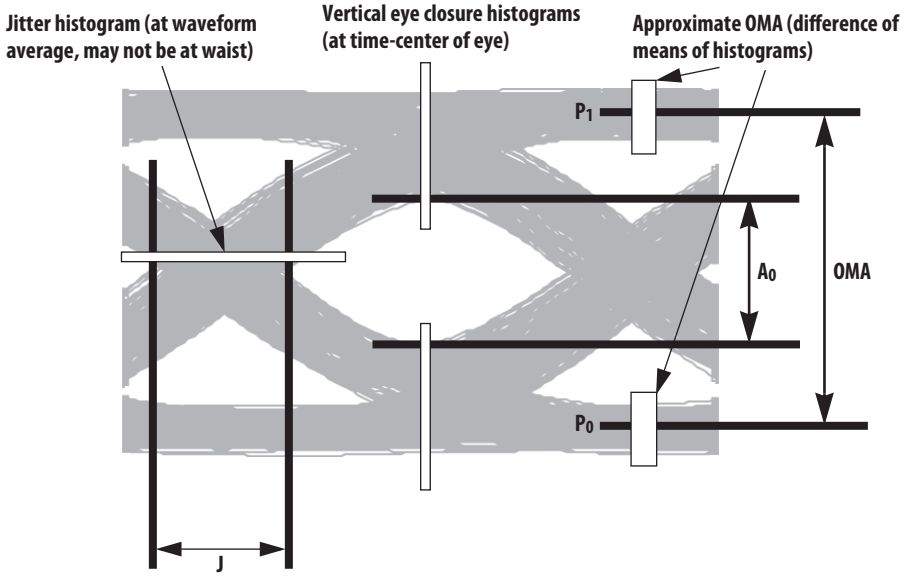


Figure 5. Required characteristics of the conformance test signal at TP3 – definitions of the conditions of stressed receiver sensitivity

Regulatory and Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	High speed signal contacts shall withstand 1000 V. All other contacts shall withstand 2000 V
Electrostatic Discharge (ESD) to Optical Connector Receptacle	EN 61000-4-2, criterion B	When installed in a properly grounded housing and chassis the units are subjected to 15 KV air discharges during operation and 8 KV direct contact discharges to the case
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	Typically passes with 10 dB margin. Actual performance dependent on enclosure design
Immunity	Variation of EN 61000-4-3	Typically minimum effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure
Laser Eye Safety and Equipment Type Testing	EN 60825-1:2007	Pout: EN AEL & US FDA CDRH Class 1M TUV File Number:R72102960
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File Number: E173874
RoHS Compliance	BS EN 1122:2001 Mtd B by ICP for Cadmium, EPA Method 3051A by ICP for Lead and Mercury, EPA Method 3060A & 7196A by UV/Vis Spectrophotometry for Hexavalent Chromium. EPA Method 3540C/3550B by GC/MS for PPB and PBDE BS EN method by ICP and EPA methods by ICP, UV/Vis Spectrophotometry and GC/MS.	Less than 100 ppm of cadmium, Less than 1000 ppm of lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl esters.

Transceiver Contact Assignment and Signal Description

There are 21 pads per level, for a total of 84, with 48 pads allocated for (12+12) differential pairs, 28 for Signal Common or Ground (GND), 4 for power connections, 4 for control/service.

Bottom side				Top Side		
I/O #	Name	Contact Length		Contact Length	Name	I/O #
Receiver -- Top Card						
C1	GND				GND	D1
C2	Rx1p				Rx0p	D2
C3	Rx1n				Rx0n	D3
C4	GND				GND	D4
C5	Rx3p				Rx2p	D5
C6	Rx3n				Rx2n	D6
C7	GND				GND	D7
C8	Rx5p				Rx4p	D8
C9	Rx5n				Rx4n	D9
C10	GND				GND	D10
C11	Rx7p				Rx6p	D11
C12	Rx7n				Rx6n	D12
C13	GND				GND	D13
C14	Rx9p				Rx8p	D14
C15	Rx9n				Rx8n	D15
C16	GND				GND	D16
C17	Rx11p				Rx10p	D17
C18	Rx11n				Rx10n	D18
C19	GND				GND	D19
C20	PRSNT_L				Vcc3.3-Rx	D20
C21	Int_L/Reset_L				Not used	D21
Transmitter -- Bottom Card						
A1	GND				GND	B1
A2	Tx1p				Tx0p	B2
A3	Tx1n				Tx0n	B3
A4	GND				GND	B4
A5	Tx3p				Tx2p	B5
A6	Tx3n				Tx2n	B6
A7	GND				GND	B7
A8	Tx5p				Tx4p	B8
A9	Tx5n				Tx4n	B9
A10	GND				GND	B10
A11	Tx7p				Tx6p	B11
A12	Tx7n				Tx6n	B12
A13	GND				GND	B13
A14	Tx9p				Tx8p	B14
A15	Tx9n				Tx8n	B15
A16	GND				GND	B16
A17	Tx11p				Tx10p	B17
A18	Tx11n				Tx10n	B18
A19	GND				GND	B19
A20	SCL				Vcc3.3-Tx	B20
A21	SDA				Not used	B21

Pin	Signal Name	Signal Description	Logic	Notes
A1	GND	Ground		
A2	TX1p	Transmitter Non-Inverted Data Input	CML-I	
A3	TX1n	Transmitter Inverted Data Input	CML-I	
A4	GND	Ground		
A5	TX3p	Transmitter Non-Inverted Data Input	CML-I	
A6	TX3n	Transmitter Inverted Data Input	CML-I	
A7	GND	Ground		
A8	TX5p	Transmitter Non-Inverted Data Input	CML-I	
A9	TX5n	Transmitter Inverted Data Input	CML-I	
A10	GND	Ground		
A11	TX7p	Transmitter Non-Inverted Data Input	CML-I	
A12	TX7n	Transmitter Inverted Data Input	CML-I	
A13	GND	Ground		
A14	TX9p	Transmitter Non-Inverted Data Input	CML-I	
A15	TX9n	Transmitter Inverted Data Input	CML-I	
A16	GND	Ground		
A17	TX11p	Transmitter Non-Inverted Data Input	CML-I	
A18	TX11n	Transmitter Inverted Data Input	CML-I	
A19	GND	Ground		
A20	SCL	Two-wire serial interface clock	LVCMOS-I/O	1
A21	SDA	Two-wire serial interface data	LVCMOS-I/O	1
B1	GND	Ground		
B2	TX0p	Transmitter Non-Inverted Data Input	CML-I	
B3	TX0n	Transmitter Inverted Data Input	CML-I	
B4	GND	Ground		
B5	TX2p	Transmitter Non-Inverted Data Input	CML-I	
B6	TX2n	Transmitter Inverted Data Input	CML-I	
B7	GND	Ground		
B8	TX4p	Transmitter Non-Inverted Data Input	CML-I	
B9	TX4n	Transmitter Inverted Data Input	CML-I	
B10	GND	Ground		
B11	TX6p	Transmitter Non-Inverted Data Input	CML-I	
B12	TX6n	Transmitter Inverted Data Input	CML-I	
B13	GND	Ground		
B14	TX8p	Transmitter Non-Inverted Data Input	CML-I	
B15	TX8n	Transmitter Inverted Data Input	CML-I	
B16	GND	Ground		
B17	TX10p	Transmitter Non-Inverted Data Input	CML-I	
B18	TX10n	Transmitter Inverted Data Input	CML-I	
B19	GND	Ground		
B20	VCC3.3-TX	+3.3 V Power supply Transmitter		
B21	Not used	Not used , 3.3 V only		

Note:
1. Host shall use a pull up of 1.5 kOhm – 10 kOhm to Vcc3.3.

Pin	Signal Name	Signal Description	Logic	Notes
C1	GND	Ground		
C2	RX1p	Receiver Non-Inverted Data Output	CML-O	
C3	RX1n	Receiver Inverted Data Output	CML-O	
C4	GND	Ground		
C5	RX3p	Receiver Non-Inverted Data Output	CML-O	
C6	RX3n	Receiver Inverted Data Output	CML-O	
C7	GND	Ground		
C8	RX5p	Receiver Non-Inverted Data Output	CML-O	
C9	RX5n	Receiver Inverted Data Output	CML-O	
C10	GND	Ground		
C11	RX7p	Receiver Non-Inverted Data Output	CML-O	
C12	RX7n	Receiver Inverted Data Output	CML-O	
C13	GND	Ground		
C14	RX9p	Receiver Non-Inverted Data Output	CML-O	
C15	RX9n	Receiver Inverted Data Output	CML-O	
C16	GND	Ground		
C17	RX11p	Receiver Non-Inverted Data Output	CML-O	
C18	RX11n	Receiver Inverted Data Output	CML-O	
C19	GND	Ground		
C20	PRSNT_L	Module Present	O	1
C21	Int_L/Reset_L	Interrupt / Reset	I/O	2
D1	GND	Ground		
D2	RX0p	Receiver Non-Inverted Data Output	CML-O	
D3	RX0n	Receiver Inverted Data Output	CML-O	
D4	GND	Ground		
D5	RX2p	Receiver Non-Inverted Data Output	CML-O	
D6	RX2n	Receiver Inverted Data Output	CML-O	
D7	GND	Ground		
D8	RX4p	Receiver Non-Inverted Data Output	CML-O	
D9	RX4n	Receiver Inverted Data Output	CML-O	
D10	GND	Ground		
D11	RX6p	Receiver Non-Inverted Data Output	CML-O	
D12	RX6n	Receiver Inverted Data Output	CML-O	
D13	GND	Ground		
D14	RX8p	Receiver Non-Inverted Data Output	CML-O	
D15	RX8n	Receiver Inverted Data Output	CML-O	
D16	GND	Ground		
D17	RX10p	Receiver Non-Inverted Data Output	CML-O	
D18	RX10n	Receiver Inverted Data Output	CML-O	
D19	GND	Ground		
D20	VCC3.3-RX	+3.3 V Power supply receiver		
D21	Not used	Not used , 3.3 V only		

Notes:

1. Shorted directly to GND inside the module.
2. Int_L/Reset_L is a bidirectional contact. When driven from the host, it operates logically as a Reset signal (input). When driven from the module, it operates logically as an Interrupt signal (output). Signal levels are per specified in Low Speed Logic section. Host shall use a pull up of 1.5 kOhm – 10 kOhm to Vcc3.3 for this pin.

Control Interface

The control interface includes a bi-directional Int_L/Reset_L interrupt/reset signal and two-wire serial – SCL (clock) and SDA (data) signals to provide users rich functionality over an efficient and easily used interface. The TWS interface is implemented as a slave device and compatible with industry standard two-wire serial protocol. Signal and timing characteristics are further defined in this section. In general, TWS bus timing and protocols follow the implementation popularized in Atmel Two-wire Serial EEPROMs.

Low-Speed Electrical Contact Definitions

SDA, SCL

SCL is the clock of the two-wire serial interface, and SDA is the data for the two-wire interface. SCL and SDA must be pulled up in the host through a pull-up resistor of value appropriate to the overall bus capacitance and the rise and fall time requirements as per "CXP two-wire Serial Interface Timing Specifications" table.

The host supplied SCL input to the CXP transceiver is used to positive-edge clock data into each CXP device and negative-edge clock data out of each device. CXP transceivers operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Since all CXP transceivers use the same two base addresses, each CXP port requires its own SCL/SDA bus. Support of multiple ports in a host requires multiple SCL/SDA buses, or multiplexing circuitry such as a multiplexer chip or a switch chip.

INT_L/RESET_L

Int_L/Reset_L is a bidirectional contact. When driven from the host, it operates logically as a Reset signal. When driven from the module, it operates logically as an Interrupt signal. In both cases, the signal is asserted low, as indicated by the '_L' suffix. The Int_L/Reset_L signal requires open collector outputs in both the host and the module, and must be pulled up on the host board with 1.5 kOhm – 10 kOhm resistor. The two uses are distinguished by timing – a shorter assertion, driven by the module indicates an interrupt and a longer assertion of the signal driven by the host indicates a reset as per "I/O Timing for Control and Status Functions" Table below.

Int_L operation:

When Int_L/Reset_L is pulled "Low" by the module for longer than the minimum pulse width ($t_{Int\_L,\ PW\text{-}min}$) and shorter than the maximum pulse width ($t_{Int\_L,\ PW\text{-}max}$) the signal signifies an interrupt. When asserted "Low", Int_L indicates a possible module operational fault or a status critical to the host system. The host identifies the cause of the interrupt using the two-wire serial interface. Int_L must operate in Pulse mode (as opposed to Static mode), in order to distinguish a short Int_L signal from a longer Reset_L signal, so the module must de-assert Int_L/Reset_L after the interrupt has been signaled.

Reset_L operation:

When the Int_L/Reset_L signal is pulled "Low" by the host for longer than the minimum reset pulse length ($t_{Reset\_L,PW\text{-}min}$), it initiates a complete module reset, returning all user module settings to their default state. There is no maximum reset pulse length. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the Reset_L signal is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an Int_L signal with the Data_Not_Ready bit (Memory Map, Byte 2, bit 0) negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset from the host.

PRSNT_L

PRSNT_L is used to indicate when the module it plugged into the host receptacle. PRSNT_L is pulled up to Vcc3.3 on the host board through > 50 kΩ and pulled down directly to signal common (no resistor) in the module. The PRSNT_L is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

I/O Timing for Control and Status Functions

Parameter	Symbol	Min	Max	Unit	Condition, and Notes
Initialization Time	t_{init}		2000	ms	Note 1 2, 3
Reset Pulse Width - Min.	$t_{reset\_L,PW\text{-}min}$	25		ms	Note 4
Monitor Data Ready Time	t_{data}		2000	ms	Note 5
Reset Assert Time	$t_{RSTL,OFF}$		2000	ms	Note 6
Int_L Assert Time	$t_{Int\_L,ON}$		200	ms	Note 7
Interrupt Pulse Width - Min	$t_{Int\_L,PW\text{-}min}$	5		µs	Note 8
Interrupt Pulse Width - Max	$t_{Int\_L,PW\text{-}max}$		50	µs	Note 9
Int_L Deassert Time	$t_{Int\_L,OFF}$		100	ms	Note 10
Rx LOS Assert Time	$t_{LOS,ON}$		100	ms	Note 11
Tx Fault Assert Time	$t_{Txfault,ON}$		200	ms	Note 12
Flag Assert Time	$t_{flag,ON}$		200	ms	Note 13
Mask Assert Time	$t_{mask,OFF}$		100	ms	Note 14
Mask Deassert Time	$t_{mask,ON}$		100	ms	Note 15
Select Change Time	$t_{ratesel}$		100	ms	Note 16

Notes:
1. Time from power on, hot plug or rising edge of reset until the module is fully functional.
2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level as specified in the power supply specifications.
3. Fully functional is defined as Int_L asserted due to Data Not Ready (Byte 2, bit 0) deasserted. The module should meet the optical and electrical specifications.
4. This is the minimum Reset_L pulse width required to reset a module. Assertion of Reset_L activates a complete module reset, i.e. module returns to the factory default control settings. While Reset_L is low, the Tx and Rx outputs are disabled and the module does not response to the 2WS serial interface.
5. Time from power on to Data Not Ready (Byte 2, bit 0) deasserted and Int_L asserted.
6. Time from rising edge on the Reset_L contact until the module is fully functional. During the Reset Time module will not respond to a "low" on the Int_L/Reset_L signal.
7. Time from occurrence of condition triggering Int_L until Vout:Int_L = Vol.
8. Int_L operates in pulse mode. Static mode (Int_L stays low until reset by host) is not supported for Int_L.
9. Int_L pulse width must not exceed $t_{Int\_L,PW\text{-}max}$ to distinguish Int_L from a Reset for other devices on bus.
10. Time from clear on read operation of associated flag until Int_L Status (Lower page, byte 2, bit 1) is cleared. This includes deassert times for Rx LOS, Tx Fault and other flag bit. Measured from falling clock edge after stop bit of read transaction.
11. Time from Rx LOS state to Rx LOS bit set (value = 1b) and Int_L asserted.
12. Time from Tx Fault state to Tx Fault bit set (value = 1b) and Int_L asserted.
13. Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and Int_L asserted.
14. Time from mask bit set (value = 1b) until associated Int_L assertion is inhibited.
15. Time from mask bit cleared (value = 0b) until associated Int_L operation resumes.
16. Time from change of state of Application or Rate Select bit until transmitter or receiver bandwidth is in conformance with appropriate specification.

Low Speed Logic

Management signaling logic levels are based on Low Voltage CMOS operating at 3.3V Vcc. Host shall use a pull-up (1.5 kOhm – 10 kOhm) to Vcc3.3 for the Two-wire interface SCL (clock), SDA (address & data), and Int_L/Reset_L signals.

Low Speed Control and Sense Signal Specifications

Parameter	Symbol	Min	Max	Units	Condition
Module Input Voltage Low	Vil	-0.3	0.4	V	Pull-up to 3.3V. Min Vih = 0.7*3.3V.
Module Input Voltage High	Vih	2.3	3.6	V	
Module Output Voltage Low	Vol	-0.3	0.3	V	Condition I_{OL}=3.0 mA. Pull-up to 3.3V.
Module Output Voltage High	Voh	2.8	3.6	V	Min Voh = 3.3V - 0.5V.
Module Output Current High	Ioh	-10	10	µA	-0.3 V < Voutput < 3.6 V
Capacitance of module on SCL, SDA and Int_L/Reset_L I/O contacts	$C_{i,SCLSDA}$		36	pF	Allocate 28 pF for IC, 8 pF for module PCB
Capacitance of module on Int_L/Reset_L I/O contact	C_{i,INT_L}		36	pF	Allocate 28 pF for IC, 8 pF for module PCB
Total bus capacitive load, SCL, SDA and Int_L/Reset_L I/O pin	Cb		100	pF	3.0 kΩ Pullup resistor, max
			200	pF	1.6 kΩ Pullup resistor, max

Management Interface Timing Specification

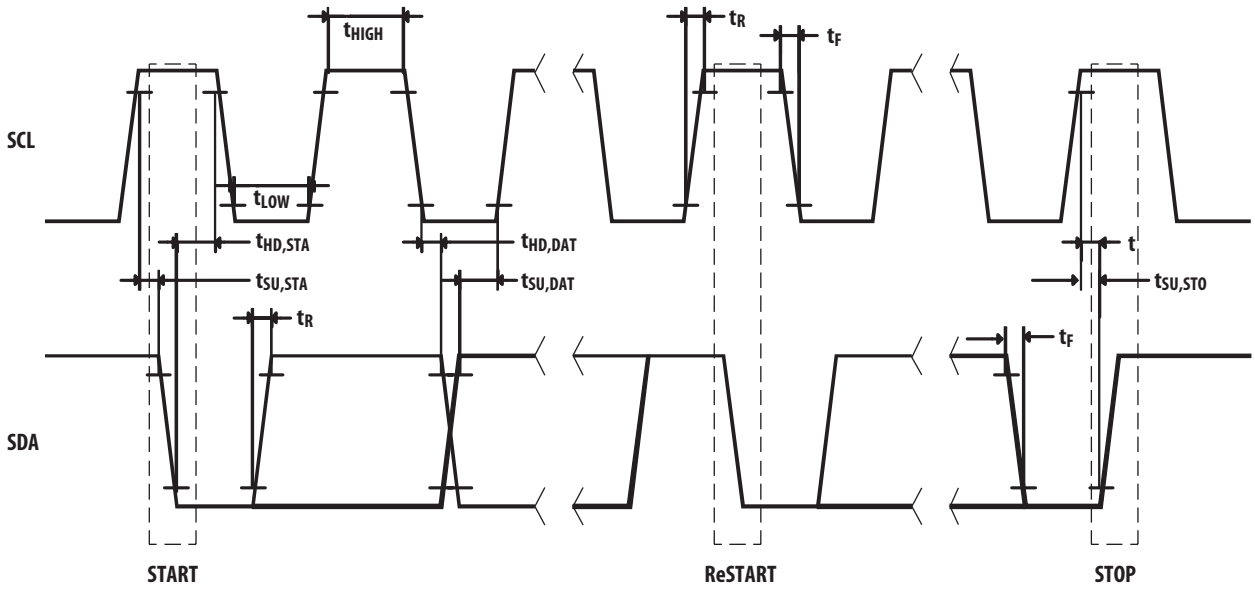


Figure 6. Two-wire Serial Interface Timing Diagram

CXP Two-Wire Serial Interface Timing Specifications

Parameter	Symbol	Min	Max	Unit	Condition
Clock Frequency	f_{SCL}	0	400	kHz	
Clock Pulse Width Low	t_{LOW}	1.3		µs	
Clock Pulse Width High	t_{HIGH}	0.6		µs	
Time bus free before new transmission can start	t_{BUF}	20		µs	Note 1
START Set-up Time	$t_{SU,STA}$	0.6		µs	
START Hold Time	$t_{HD,STA}$	0.6		µs	
Data Set-up Time	$t_{SU,DAT}$	0.1		µs	Note 2
Data Hold Time	$t_{HD,DAT}$	0		µs	Note 3
SDA and SCL rise time	$t_{R,400}$		0.3	µs	Note 4
SDA and SCL fall time	$t_{F,400}$		0.3	µs	Note 5
STOP Set-up Time	$t_{SU,STO}$	0.6		µs	

Notes:
1. Between STOP & START and between ACK & ReSTART.
2. Data In Set Up Time is measured from Vil(max)SDA or Vih(min)SDA to Vil(max)SCL.
3. Data In Hold Time is measured from Vil(max)SCL to Vil(max)SDA or Vih(min)SDA.
4. Rise Time is measured from Vol(max)SDA to Voh(min)SDA.
5. Fall Time is measured from Voh(min)SDA to Vol(max)SDA.

Memory Specifications

Memory may be accessed in single-byte or multi-byte (up to 4 bytes) memory blocks. The largest multiple-byte contiguous write operation that a module shall handle is 4 bytes. The minimum size write block is 1 byte.

Memory Transaction Timing Specification

Parameter	Symbol	Min	Max	Unit	Condition
Serial Interface Clock Holdoff - "Clock Stretching"	T_clock_hold		500	µs	Note 1
Complete Single or Sequential Write	t_{WR}		40	ms	Note 2
Endurance (Write cycles)		50,000	75,000	cycles	Note 3

Notes:
1. Maximum time the CXP module may hold the SCL line low before continuing with a read or write operation.
2. Complete up to 4 Byte write. Timing should start from Stop bit at the end of the sequential write operation and continue until the module responds to another operation.
3. 50 K write cycles at 70° C.

I/O Timing for Squelch and Disable

Parameter	Symbol	Min	Max	Unit	Condition and Notes
Rx Squelch Assert Time	$t_{Rxsq,ON}$		0.080	ms	Note 1
Rx Squelch Deassert Time	$t_{Rxsq,OFF}$		0.080	ms	Note 2
Tx Squelch Assert Time	$t_{Txsq,ON}$		400	ms	Note 3
Tx Squelch Deassert Time	$t_{Txsq,OFF}$		400	ms	Note 4
Tx Disable Assert Time	$t_{Txdis,ON}$		100	ms	Note 5
Tx Disable Deassert Time	$t_{Txdis,OFF}$		400	ms	Note 6
Rx Output Disable Assert Time	$t_{Rxdis,ON}$		100	ms	Note 7
Rx Output Disable Deassert Time	$t_{Rxdis,OFF}$		100	ms	Note 8
Squelch Disable Assert Time	$t_{Sqdis,ON}$		100	ms	Note 9
Squelch Disable Deassert Time	$t_{Sqdis,OFF}$		100	ms	Note 10

Notes:
1. Time from loss of Rx input signal until the squelched output condition is reached.
2. Time from resumption of Rx input signals until normal Rx output condition is reached.
3. Time from loss of Tx input signal until the squelched output condition is reached.
4. Time from resumption of Tx input signals until normal Tx output condition is reached.
5. Time from Tx Disable bit set (value = 1b) until optical output falls below 10% of nominal.
6. Time from Tx Disable bit cleared (value = 0b) until optical output rises above 90% of nominal. Measured from Stop bit low-to-high SDA transition.
7. Time from Rx Output Disable bit set (value = 1b) until Rx output falls below 10% of nominal.
8. Time from Rx Output Disable bit cleared (value = 0b) until Rx output rises above 90% of nominal.
9. This applies to Rx and Tx Squelch and is the time from bit set (value = 1b) until squelch functionality is disabled.
10. This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b) until squelch functionality is enabled.

Memory Map

Tx Lower Page (1010 000x) – Required		
Byte	**Type**	**Functions**
0-6	RO	Tx Status: 0xA8 Presence, Flat/ Paging Memory Presence, Interrupt, Data Not Ready, Loss of Signal, Fault, Summary of Alarms
7-18	RO	Latched Tx Alarms: Loss of Signal, Fault, Per-channel Alarms (Power or Current High/Low), Device Alarms (Temp, Vcc3.3 or Vcc12)
22-27	RO	Module Monitors: Temp, Voltage
38-39	RO	Module Monitors: Elapsed Operating Time
40-41	RW	Module Control: Rate/Application Select
51	RW	Module Control: Tx Reset
52-67	RW	Tx Channel Control: Disables, Squelch, Polarity Flip, Margin, Equalization Control
95-106	RW	Masks for Alarms: Channel (LOS, Fault), Channel Internal (Power or Current High/Low) and Module (Temp, Voltage)
110-118	RW	Vendor Specific Area – Read/Write
119-126	RW	Password
127	RW	Upper Page Select Byte (00h or 01h)

Rx Lower Page (1010 100x) – Optional		
Byte	**Type**	**Functions**
0-6	RO	Rx Status: Flat/ Paging Memory, Interrupt, Data Not Ready, Loss of Signal, Fault, Summary of Alarms
7-18	RO	Latched Rx Alarms: Loss of Signal, Fault, Per-channel Alarms (Power or Current High/Low), Device Alarms (Temp, Vcc3.3 or Vcc12)
22-27	RO	Module Monitors: Temp, Voltage
38-39	RO	Module Monitors: Elapsed Operating Time
40-41	RW	Module Control: Rate/Application Select
51	RW	Module Control: Rx Reset
52-73	RW	Rx Channel Control: Disables, Squelch, Polarity Flip, Margin, Amplitude, Pre-emphasis Control
95-106	RW	Masks for Alarms: Channel (LOS, Fault), Channel Internal (Power High/Low) and Module (Temp, Voltage)
110-118	RW	Vendor Specific Area – Read/Write
119-126	RW	Password
127	RW	Upper Page Select Byte (00h or 01h)

Tx Upper Page 01h (Optional)		
Byte	**Type**	**Functions**
128-167	RO	Module Alarm Threshold Settings
168-179	RO	Channel Alarm Threshold Settings
180-181	RO	Checksum
182-229	RO	Per-Channel Monitors: Tx Bias Current and Light Output
230-255		Reserved – Vendor-Specific Tx Functions

Upper Page 00h (identical for Tx & Rx) Required		
Byte	**Type**	**Functions**
128-129	RO	Identifiers
130-146	RO	Device Description: Cable & Connector, Power Supplies, Max Case Temp, Min-Max Signal Rate, Laser Wavelength or Copper Attenuation, and Supported Functions
147	RO	Description: Device Technology
152-222	RO	Vendor Information: Name & OUI, PN & PN rev, Serial Number, Data Code, & Customer-specific Information
223	RO	Checksum on 128-222
224-255	RO	Vendor Specific Area – Read-only

Rx Upper Page 01h (Optional)		
Byte	**Type**	**Functions**
128-167	RO	Module Alarm Threshold Settings
168-179	RO	Channel Alarm Threshold Settings
180-181	RO	Checksum
206-229	RO	Per-Channel Monitors: Rx Input Power
230-255		Reserved – Vendor-Specific Rx Functions

Digital Monitoring Interface

Through TWS interface, the host can fetch the monitoring data as summarized in the previous section. The following table summarizes the function and the specifications.

Digital Monitoring Specifications

Monitor		Tolerance		DMI Range*		Alarm Setting		
Parameter	Unit	min	max	min	max	min	max	Comment
V_{cc33}	volt	-0.1	+0.1	3.135	3.465	2.94	3.63	Test point at module connector
Temperature	C	-5	+5	0	70	-5	75	Case temperature
TX Bias current	mA	-1	+1	0	11	0.5	10	Note 1
TX Light Output Power	dB/dBm	- 3	+3	-9	+2.4	-11.6	+5.4	at TP2
RX Light Input Power	dB/dBm	- 3	+3	-10	+2.4	-13.5	+3.4	at TP3
DMI on-time	%	-10	+10					

* Within DMI range, the tolerance is guaranteed. The modules still reports data if the operating condition is out of the DMI range, but the tolerance is not guaranteed.

Note
1. TX bias DMI report accuracy not guaranteed when TX squelch is disabled, and LOS is asserted, i.e. no valid electrical inputs into TX.

Connector Orientation for 24 fiber MTP/MPO connector

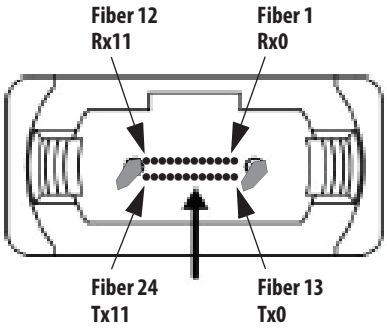


Figure 7. 24-fiber MPO Receptacle

Optical cables with 24-fiber MPO-style connectors on each end shall be built "Key up/Key down" so that the helix half-twist incurred when the cable is lugged into transceivers will correctly connect transmitter lanes to receiver lanes: lanes 0 to 0 and 11 to 11. MPO-style 'male" alignment pins are used in the receptacle and a "female" MPO-style connector shall be used on the cable connector.

Recommended Power Supply Filter

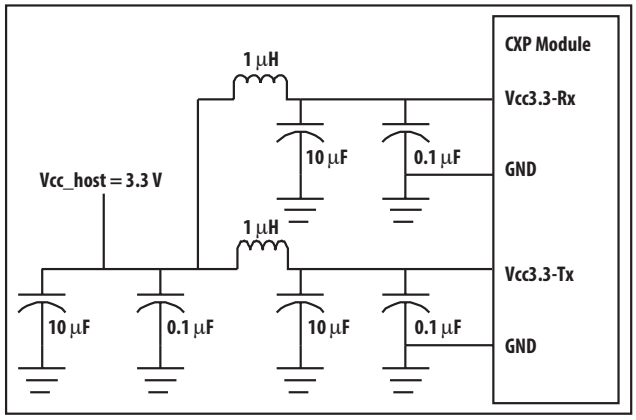
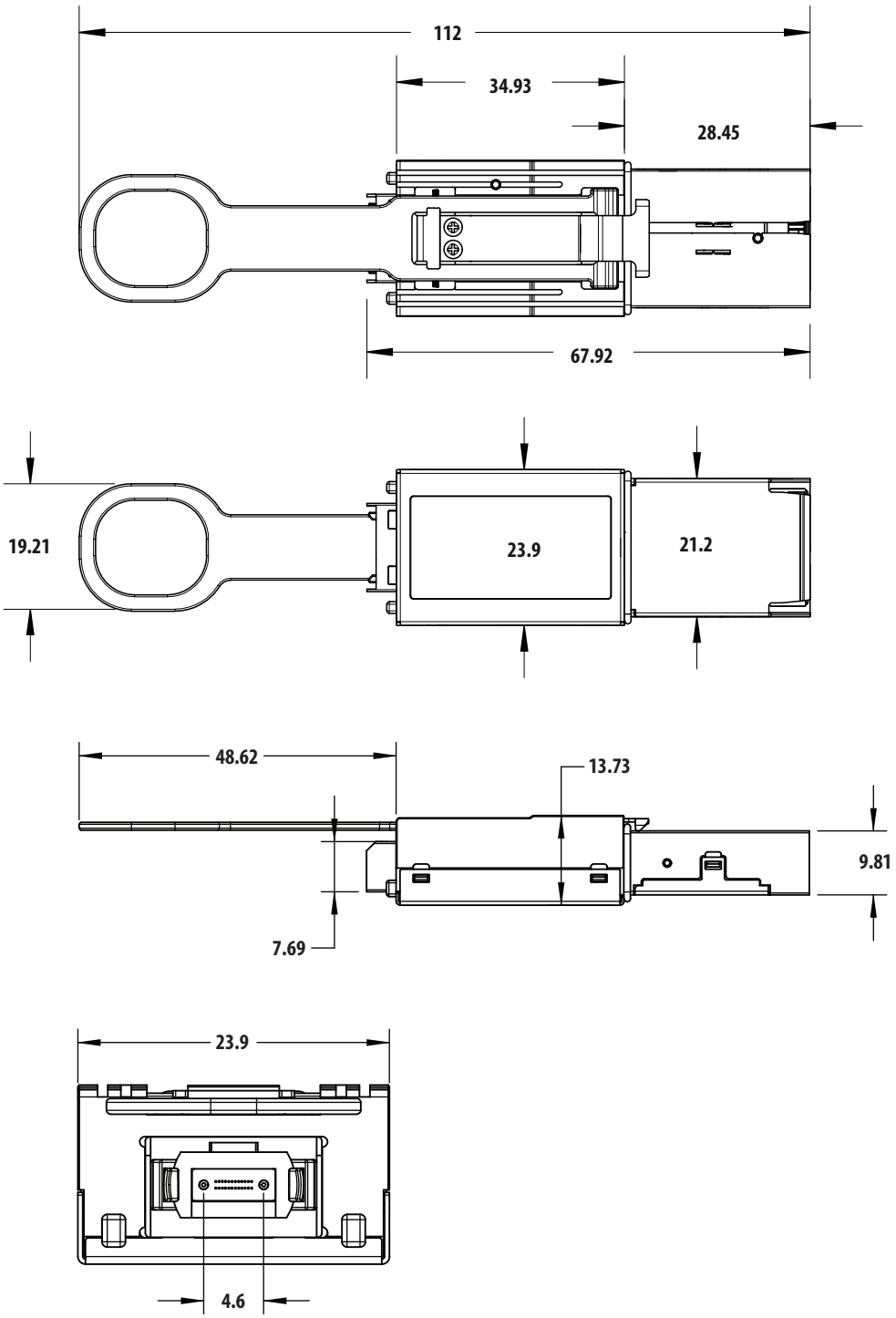


Figure 8. Recommended Power Supply Filter

Mechanical Dimensions, Package Outline



All dimensions in millimeters:

Figure 9. Transceiver package dimensions

Fixed Receptacle Connector

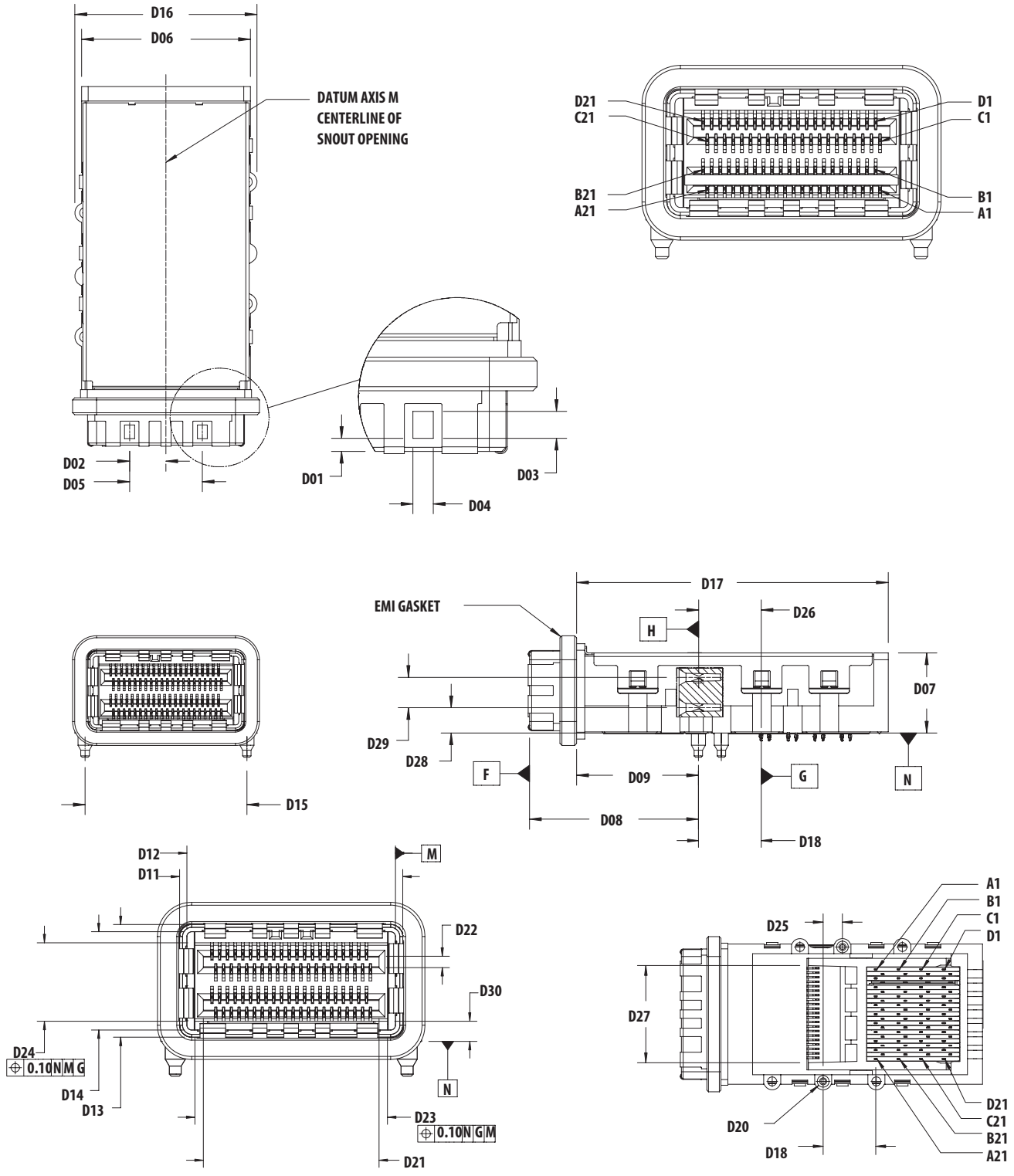


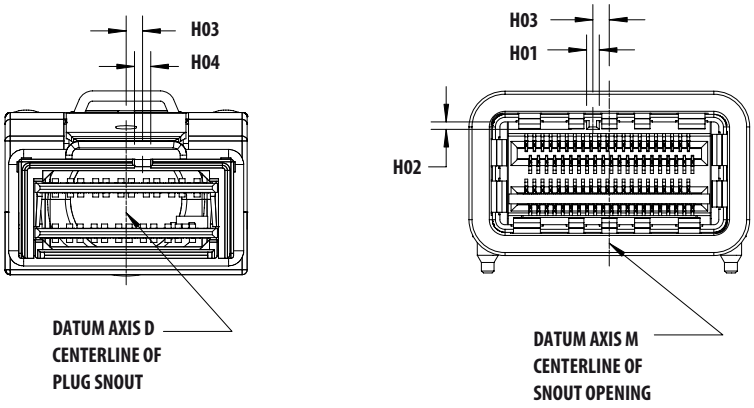
Figure 10. Receptacle connector dimensions (on host board)

Fixed Receptacle Connector Dimensions (see Figure 10)

	Description	Dim.	Tol.
D01	Latch Hole from Face	0.97	0.05
D02	Latch Hole from Datum M	5.40	Basic
D03	Latch Hole Length	2.00	0.10
D04	Latch Hole Width	1.50	0.10
D05	Latch Hole to Hole	10.80	Basic
D06	Shell Width	25.05	0.25
D07	Shell Height	11.88	0.13
D08	Locating Post to Face	25.06	0.08
D09	Locating Post to EMI Shell Base	18.06	0.13
D10	Not used		
D11	Snout Width	23.10	0.08
D12	Snout Opening Width	21.60	0.05
D13	Snout Height	11.70	0.08
D14	Snout Opening Height	10.20	0.05
D16	Shell Width Base	27.00	0.25

	Description	Dim.	Tol.
D17	EMI Shell Base to Back	46.22	0.25
D18	Connector Contact to Locating Post	9.30	0.05
D19	Not used		
D20	Peg Diameter	2.08	0.05
D21	Card Slot Width	18.20	0.08
D22	Card Slot Height	1.18	0.05
D23	Receptacle Body Width	19.94	0.08
D24	Receptacle Body Height	8.15	0.08
D25	Peg to Peg	3.41	0.05
D26	Contact Centerline to 1st Row of Compliant Contacts	9.25	0.05
D27	Housing, Leg to Leg	17.35	0.05
D28	PCB to Lower Card Slot	3.75	0.10
D29	Lower Card Slot to Upper Card Slot	4.50	0.10
D30	Datum N to Bottom of Receptacle Housing	2.10	0.10

Connector Orientation Key



	Description	Dim.	Tol.
H01	Orientation Key Width	1.25	0.13
H02	Orientation Key Height	0.75	0.13
H03	Orientation Key Location	1.625	0.13
H04	Orientation Key Slot	1.60	0.13

Figure 11. Connector Orientation Key

Host PCB Footprint

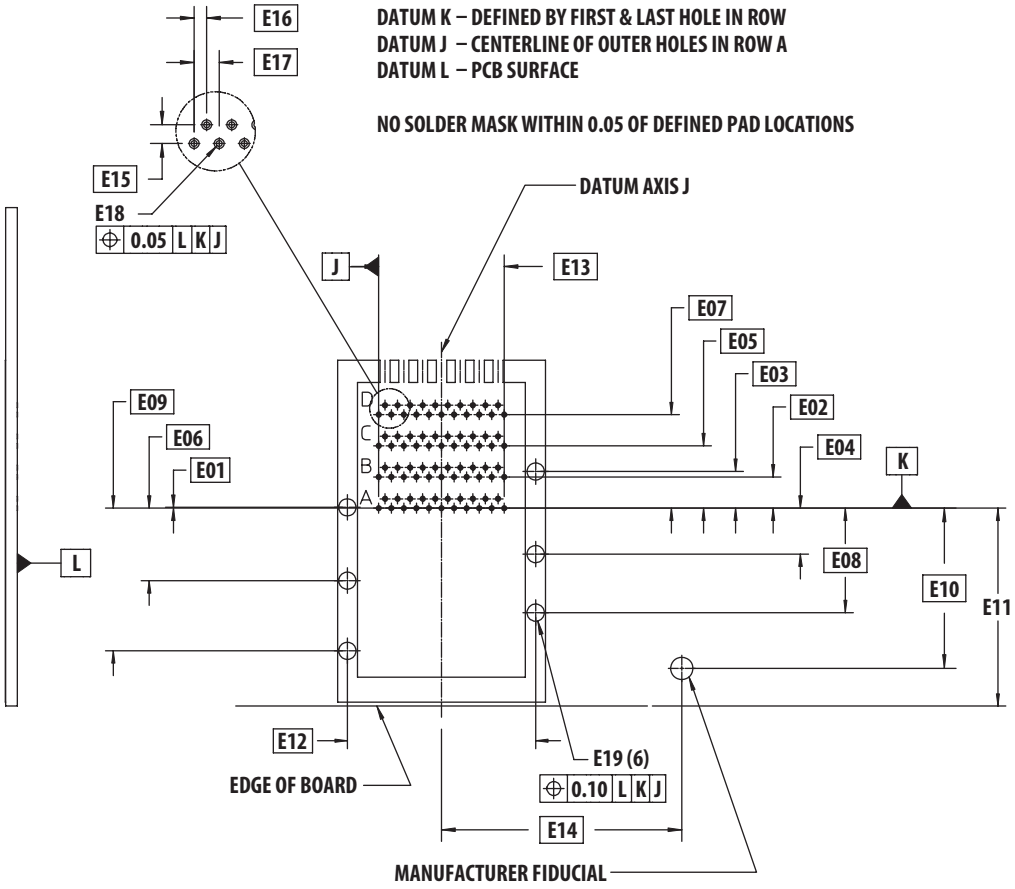


Figure 12. Host board PCB footprint dimensions

	Description	Dim.	
E01	Shield Screw Hole to Datum K	0.10	Basic
E02	Row A (Datum K) to Row B	4.00	Basic
E03	Shield Screw Hole to Datum K	4.70	Basic
E04	Shield Screw Hole to Datum K	5.89	Basic
E05	Row A (Datum K) to Row C	8.00	Basic
E06	Shield Screw Hole to Datum K	9.30	Basic
E07	Row A (Datum K) to Row D	12.00	Basic
E08	Shield Screw Hole to Datum K	13.40	Basic
E09	Shield Screw Hole to Datum K	18.30	Basic
E10	Connector Datum to Manufacturer Fiducial	Basic	N/A

	Description	Dim.	
E11	Connector Datum to Card Edge	25.38	Ref
E12	Shield Mounting Hole to Mounting Hole	24.00	Basic
E13	Shield Contact Center to Center	16.00	Basic
E14	Connector Datum to Manufacturer Fiducial	Basic	N/A
E15	Within row pitch – Front to Back	1.20	Basic
E16	Within row Horizontal Offset	0.80	Basic
E17	Within row pitch – Horizontal	1.60	Basic
E18	Contact Hole Finished Diameter	0.37	0.05
E19	Shield Mounting Hole Diameter	2.20	0.05

Ground Pad

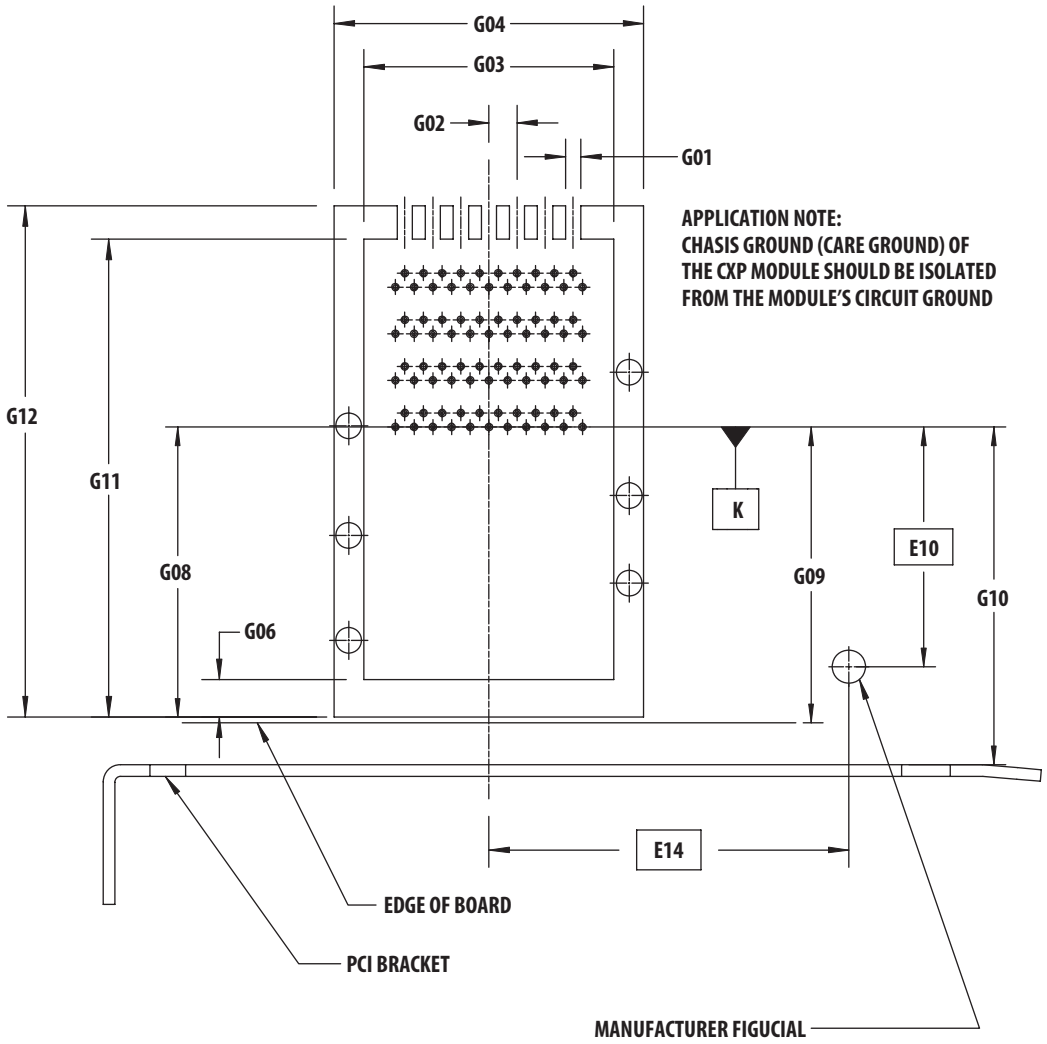


Figure 13. Ground pad dimensions (host board)

	Description	Dim.	Tol.
G01	Ground Pad Alley Width	1.30	0.10
G02	Ground Pad Alley Spacing	2.40	0.10
G03	Ground Pad Inner Width	21.40	0.10
G04	Ground Pad Width	26.49	0.10
G05	Pad Center to Manufacturer Fiducial	Basic	N/A
G06	Ground Pad Width	3.21	0.10
G07	Connector Datum to Manufacturer Fiducial	Basic	N/A
G08	Connector Datum to Front Pad Edge	24.88	0.10
G09	Connector Datum to Card Edge	25.38	0.10
G10	Connector Datum to Bezel	28.96	0.10
G11	Ground Pad Edge to Inside Pad Edge	40.99	0.10
G12	Ground Pad Length	43.84	0.10