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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# IGLOO nano Low Power Flash FPGAs with Flash\*Freeze Technology

## Features and Benefits

### Low Power

- nanoPower Consumption—Industry's Lowest Power
- 1.2 V to 1.5 V Core Voltage Support for Low Power
- Supports Single-Voltage System Operation
- Low Power Active FPGA Operation
- Flash\*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
- Easy Entry to / Exit from Ultra-Low Power Flash\*Freeze Mode

### Small Footprint Packages

- As Small as 3x3 mm in Size

### Wide Range of Features

- 10,000 to 250,000 System Gates
- Up to 36 kbits of True Dual-Port SRAM
- Up to 71 User I/Os

### Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Instant On Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off
- 250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance

### In-System Programming (ISP) and Security

- ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532-compliant)
- FlashLock<sup>®</sup> Designed to Secure FPGA Contents
- 1.2 V Programming

### High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure

### Advanced I/Os

- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7 V to 3.6 V
- Wide Range Power Supply Voltage Support per JESD8-12, Allowing I/Os to Operate from 1.14 V to 1.575 V
- I/O Registers on Input, Output, and Enable Paths
- Selectable Schmitt Trigger Inputs
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Weak Pull-Up/Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the IGLOO<sup>®</sup> Family

### Clock Conditioning Circuit (CCC) and PLL<sup>†</sup>

- Up to Six CCC Blocks, One with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 250 MHz)

### Embedded Memory

- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations)<sup>†</sup>
- True Dual-Port SRAM (except × 18 organization)<sup>†</sup>

### Enhanced Commercial Temperature Range

- T<sub>j</sub> = -20°C to +85°C

IGLOO nano Devices	AGLN010	AGLN015 <sup>†</sup>	AGLN020		AGLN060	AGLN125	AGLN250
IGLOO nano-Z Devices <sup>1</sup>				AGLN030Z <sup>1</sup>	AGLN060Z <sup>1</sup>	AGLN125Z <sup>1</sup>	AGLN250Z <sup>1</sup>
System Gates	10,000	15,000	20,000	30,000	60,000	125,000	250,000
Typical Equivalent Macrocells	86	128	172	256	512	1,024	2,048
VersaTiles (D-flip-flops)	260	384	520	768	1,536	3,072	6,144
Flash*Freeze Mode (typical, μW)	2	4	4	5	10	16	24
RAM Kbits (1,024 bits) <sup>2</sup>	–	–	–	–	18	36	36
4,608-Bit Blocks <sup>2</sup>	–	–	–	–	4	8	8
FlashROM Kbits (1,024 bits)	1	1	1	1	1	1	1
Secure (AES) ISP <sup>2</sup>	–	–	–	–	Yes	Yes	Yes
Integrated PLL in CCCs <sup>2,3</sup>	–	–	–	–	1	1	1
VersaNet Globals	4	4	4	6	18	18	18
I/O Banks	2	3	3	2	2	2	4
Maximum User I/Os (packaged device)	34	49	52	77	71	71	68
Maximum User I/Os (Known Good Die)	34	–	52	83	71	71	68

<sup>†</sup> AGLN030 and smaller devices do not support this feature.

IGLOO nano Devices	AGLN010	AGLN015 <sup>1</sup>	AGLN020		AGLN060	AGLN125	AGLN250
IGLOO nano-Z Devices <sup>1</sup>				AGLN030Z <sup>1</sup>	AGLN060Z <sup>1</sup>	AGLN125Z <sup>1</sup>	AGLN250Z <sup>1</sup>
Package Pins							
UC/CS	UC36		UC81,	UC81, CS81	CS81	CS81	CS81
QFN	QN48	QN68	CS81	QN48, QN68			
VQFP			QN68	VQ100	VQ100	VQ100	VQ100

**Notes:**

1. Not recommended for new designs. Few devices/packages are obsoleted. For more information on obsoleted devices/packages, refer to the [PDN 1503 - IGLOO nano Z and ProASIC3 nano Z Families](#).
2. AGLN030 and smaller devices do not support this feature.
3. AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs.
4. For higher densities and support of additional features, refer to the [DS0095: IGLOO Low Power Flash FPGAs Datasheet and IGLOOe Low-Power Flash FPGAs Datasheet](#).

## I/Os Per Package

IGLOO nano Devices	AGLN010	AGLN015 <sup>1</sup>	AGLN020		AGLN060	AGLN125	AGLN250
IGLOO nano-Z Devices <sup>1</sup>				AGLN030Z <sup>1</sup>	AGLN060Z <sup>1</sup>	AGLN125Z <sup>1</sup>	AGLN250Z <sup>1</sup>
Known Good Die	34	–	52	83	71	71	68
UC36	23	–	–	–	–	–	–
QN48	34	–	–	34	–	–	–
QN68	–	49	49	49	–	–	–
UC81	–	–	52	66	–	–	–
CS81	–	–	52	66	60	60	60
VQ100	–	–	–	77	71	71	68

**Notes:**

1. Not recommended for new designs.
2. When considering migrating your design to a lower- or higher-density device, refer to the [DS0095: IGLOO Low Power Flash FPGAs Datasheet](#) and [IGLOO FPGA Fabric User's Guide](#) to ensure compliance with design and board migration requirements.
3. When the Flash\*Freeze pin is used to directly enable Flash\*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.
4. "G" indicates RoHS-compliant packages. Refer to "[IGLOO nano Ordering Information](#)" on page IV for the location of the "G" in the part number. For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only.

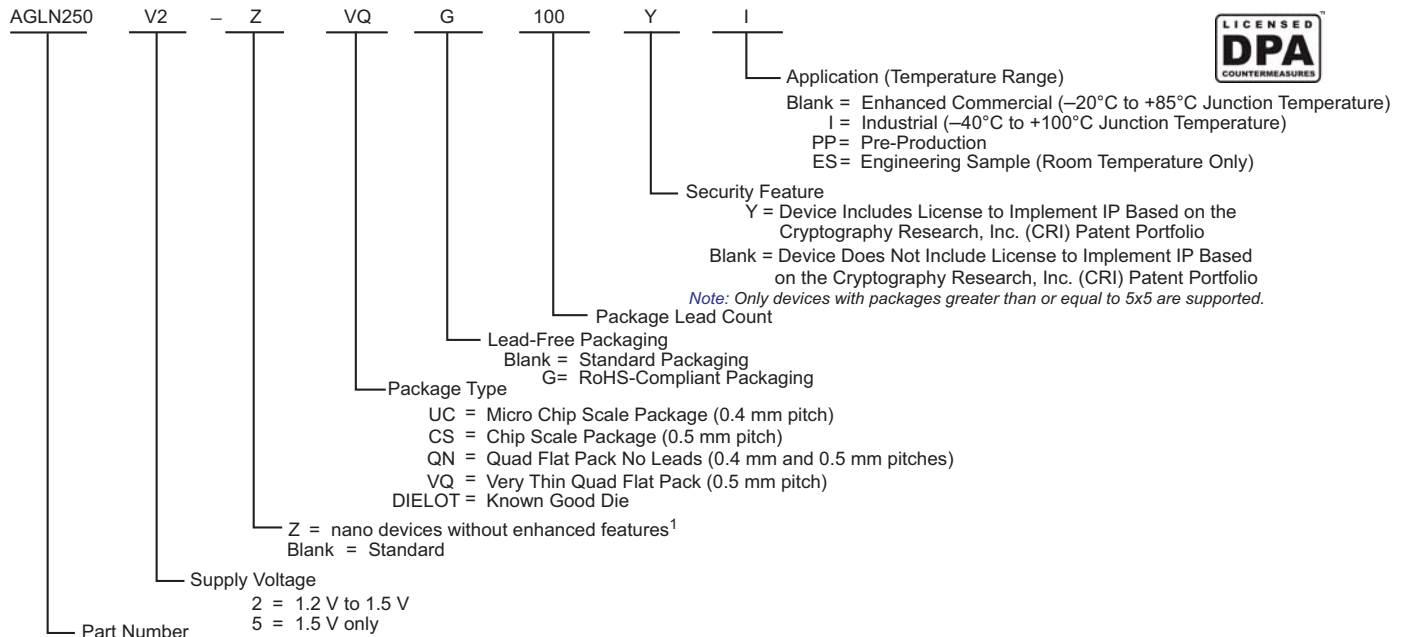
**Table 1 • IGLOO nano FPGAs Package Sizes Dimensions**

Packages	UC36	UC81	CS81	QN48	QN68	VQ100
Length × Width (mm\mm)	3 x 3	4 x 4	5 x 5	6 x 6	8 x 8	14 x 14
Nominal Area (mm <sup>2</sup> )	9	16	25	36	64	196
Pitch (mm)	0.4	0.4	0.5	0.4	0.4	0.5
Height (mm)	0.80	0.80	0.80	0.90	0.90	1.20

## IGLOO nano Device Status

IGLOO nano Devices	Status	IGLOO nano-Z Devices	Status
AGLN010	Production		
AGLN015	Not recommended for new designs.		
AGLN020	Production		
		AGLN030Z	Not recommended for new designs.
AGLN060	Production	AGLN060Z	Not recommended for new designs.
AGLN125	Production	AGLN125Z	Not recommended for new designs.
AGLN250	Production	AGLN250Z	Not recommended for new designs.

## IGLOO nano Ordering Information



### IGLOO nano Devices

- AGLN010 = 10,000 System Gates
- AGLN015 = 15,000 System Gates (AGLN015 is not recommended for new designs)
- AGLN020 = 20,000 System Gates
- AGLN030 = 30,000 System Gates
- AGLN060 = 60,000 System Gates
- AGLN125 = 125,000 System Gates
- AGLN250 = 250,000 System Gates

### Notes:

- Z-feature grade devices AGLN060Z, AGLN125Z, and AGLN250Z do not support the enhanced nano features of Schmitt Trigger input, bus hold (hold previous I/O state in Flash\*Freeze mode), cold-sparing, hot-swap I/O capability and 1.2 V programming. The AGLN030 Z feature grade does not support Schmitt trigger input, bus hold and 1.2 V programming. For the VQ100, CS81, UC81, QN68, and QN48 packages, the Z feature grade and the N part number are not marked on the device. Z feature grade devices are not recommended for new designs.
- AGLN030 is available in the Z feature grade only.
- Marking Information: IGLOO nano V2 devices do not have a V2 marking, but IGLOO nano V5 devices are marked with a V5 designator.

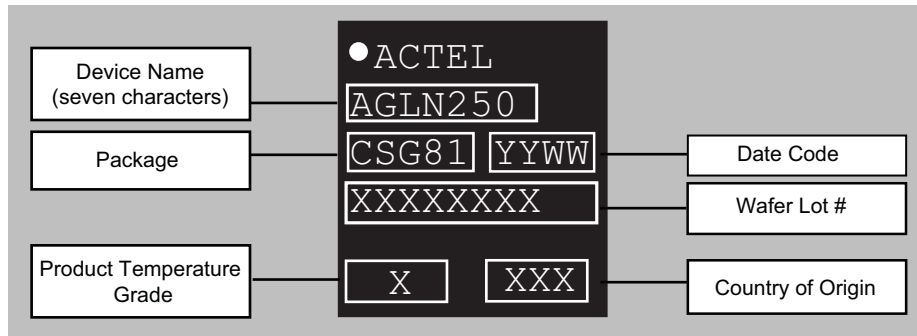
## Devices Not Recommended For New Designs

AGLN015, AGLN030Z, AGLN060Z, AGLN125Z, and AGLN250Z are not recommended for new designs. For more information on obsoleted devices/packages, refer to the [PDN1503 - IGLOO nano Z and ProASIC3 nano Z Families](#).

## Device Marking

Microsemi normally topside marks the full ordering part number on each device. There are some exceptions to this, such as some of the Z feature grade nano devices, the V2 designator for IGLOO devices, and packages where space is physically limited. Packages that have limited characters available are UC36, UC81, CS81, QN48, QN68, and QFN132. On these specific packages, a subset of the device marking will be used that includes the required legal information and as much of the part number as allowed by character limitation of the device. In this case, devices will have a truncated device marking and may exclude the applications markings, such as the I designator for Industrial Devices or the ES designator for Engineering Samples.

Figure 1 shows an example of device marking based on the AGLN250V2-CSG81. The actual mark will vary by the device/package combination ordered.



**Figure 1 • Example of Device Marking for Small Form Factor Packages**

## IGLOO nano Products Available in the Z Feature Grade

IGLOO nano-Z Devices	AGLN030Z*	AGLN060Z*	AGLN125Z*	AGLN250Z*
	QN48	–	–	–
	QN68	–	–	–
	UC81	–	–	–
	CS81	CS81	CS81	CS81
<b>Packages</b>	VQ100	VQ100	VQ100	VQ100

Note: \*Not recommended for new designs.

## Temperature Grade Offerings

Package	AGLN010	AGLN015*	AGLN020		AGLN060	AGLN125	AGLN250
				AGLN030Z*	AGLN060Z*	AGLN125Z*	AGLN250Z*
UC36	C, I	–	–	–	–	–	–
QN48	C, I	–	–	C, I	–	–	–
QN68	–	C, I	C, I	C, I	–	–	–
UC81	–	–	C, I	C, I	–	–	–
CS81	–	–	C, I	C, I	C, I	C, I	C, I
VQ100	–	–	–	C, I	C, I	C, I	C, I

Note: \* Not recommended for new designs.

C = Enhanced Commercial temperature range: –20°C to +85°C junction temperature

I = Industrial temperature range: –40°C to +100°C junction temperature

Contact your local Microsemi representative for device availability: <http://www.microsemi.com/soc/contact/default.aspx>.

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# 1 – IGLOO nano Device Overview

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## General Description

The IGLOO family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash\*Freeze technology used in IGLOO nano devices enables entering and exiting an ultra-low power mode that consumes nanoPower while retaining SRAM and register data. Flash\*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO nano device is completely functional in the system. This allows the IGLOO nano device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO nano devices the advantage of being a secure, low power, single-chip solution that is Instant On. The IGLOO nano device is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO nano devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGLN030 and smaller devices have no PLL or RAM support. IGLOO nano devices have up to 250 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 71 user I/Os.

IGLOO nano devices increase the breadth of the IGLOO product line by adding new features and packages for greater customer value in high volume consumer, portable, and battery-backed markets. Features such as smaller footprint packages designed with two-layer PCBs in mind, power consumption measured in nanoPower, Schmitt trigger, and bus hold (hold previous I/O state in Flash\*Freeze mode) functionality make these devices ideal for deployment in applications that require high levels of flexibility and low cost.

## Flash\*Freeze Technology

The IGLOO nano device offers unique Flash\*Freeze technology, allowing the device to enter and exit ultra-low power Flash\*Freeze mode. IGLOO nano devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash\*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO nano V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash\*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, HIGH, or LOW.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and small-footprint packages make IGLOO nano devices the best fit for portable electronics.

## Flash Advantages

### **Low Power**

Flash-based IGLOO nano devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO nano devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO nano devices also have low dynamic power consumption to further maximize power savings; power is reduced even further by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash\*Freeze technology, gives the IGLOO nano device the lowest total system power offered by any FPGA.

### **Security**

Nonvolatile, flash-based IGLOO nano devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO nano devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO nano devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of security in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO nano devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO nano devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO nano devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of IGLOO nano devices. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. IGLOO nano devices, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO nano device provides the best available security for programmable logic designs.

### **Single Chip**

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO nano FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

### **Instant On**

Microsemi flash-based IGLOO nano devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO nano devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO nano device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO nano devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO nano flash FPGAs enable the user to quickly enter and exit Flash\*Freeze mode. This is done almost instantly (within 1  $\mu$ s) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.

## **Reduced Cost of Ownership**

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based IGLOO nano devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic.

Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO nano device architecture mitigates the need for ASIC migration at higher user volumes. This makes IGLOO nano devices cost-effective ASIC replacement solutions, especially for applications in the consumer, networking/communications, computing, and avionics markets.

With a variety of devices under \$1, IGLOO nano FPGAs enable cost-effective implementation of programmable logic and quick time to market.

## **Firm-Error Immunity**

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO nano flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO nano FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

## **Advanced Flash Technology**

The IGLOO nano device offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO nano FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

## **Advanced Architecture**

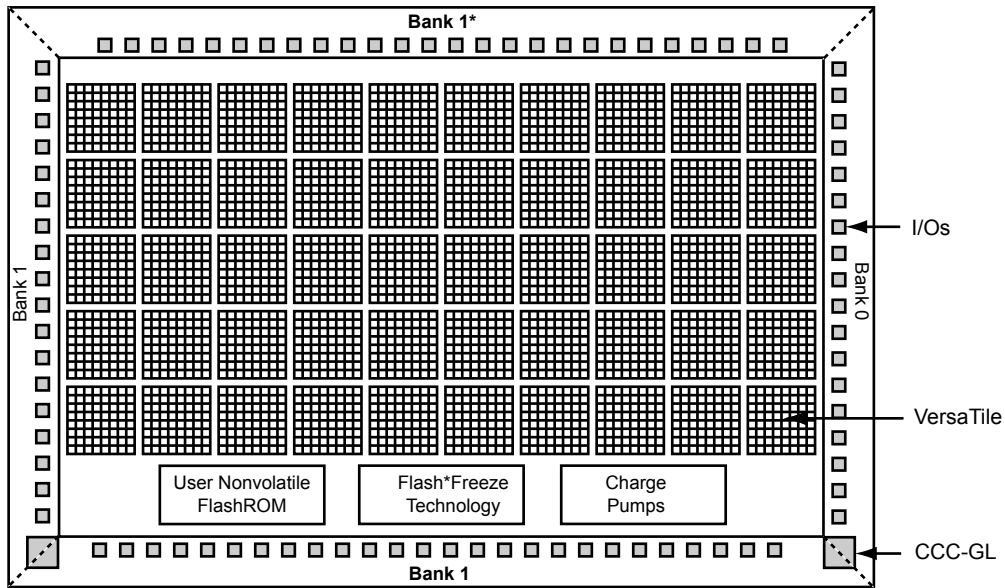
The proprietary IGLOO nano architecture provides granularity comparable to standard-cell ASICs. The IGLOO nano device consists of five distinct and programmable architectural features ([Figure 1-3 on page 1-5](#) to [Figure 1-4 on page 1-5](#)):

- Flash\*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory<sup>†</sup>
- Extensive CCCs and PLLs<sup>†</sup>
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO nano core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC<sup>®</sup> family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

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<sup>†</sup> The AGLN030 and smaller devices do not support PLL or SRAM.



Note: \*Bank 0 for the AGLN030 device

Figure 1-1 • IGLOO Device Architecture Overview with Two I/O Banks and No RAM (AGLN010 and AGLN030)

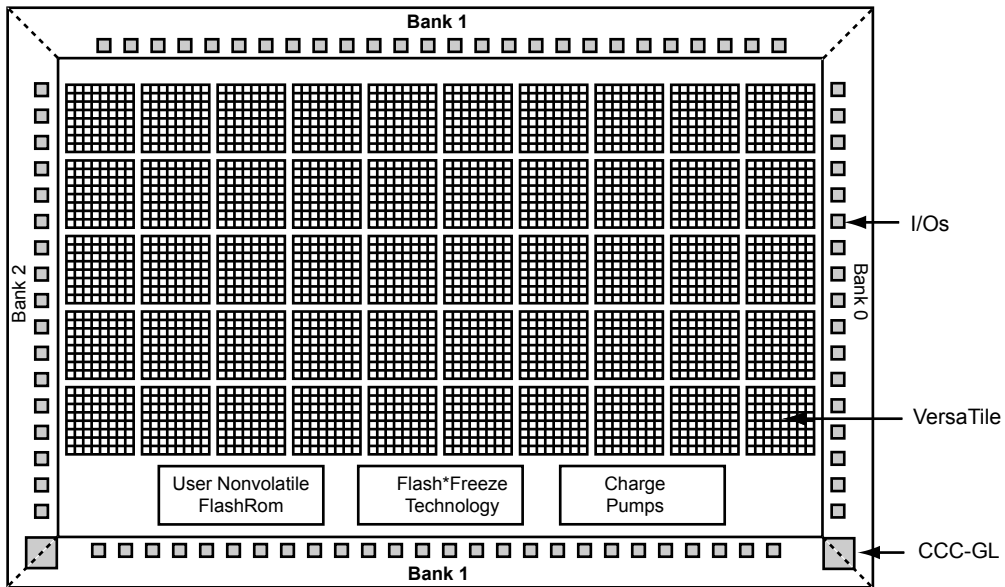


Figure 1-2 • IGLOO Device Architecture Overview with Three I/O Banks and No RAM (AGLN015 and AGLN020)

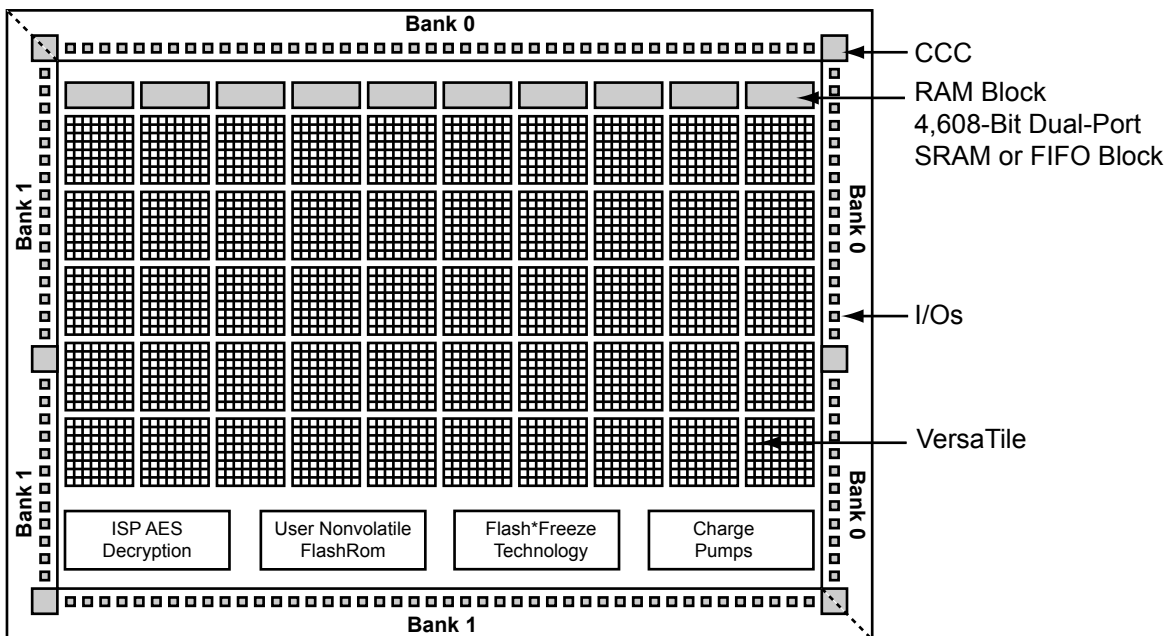


Figure 1-3 • IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125)

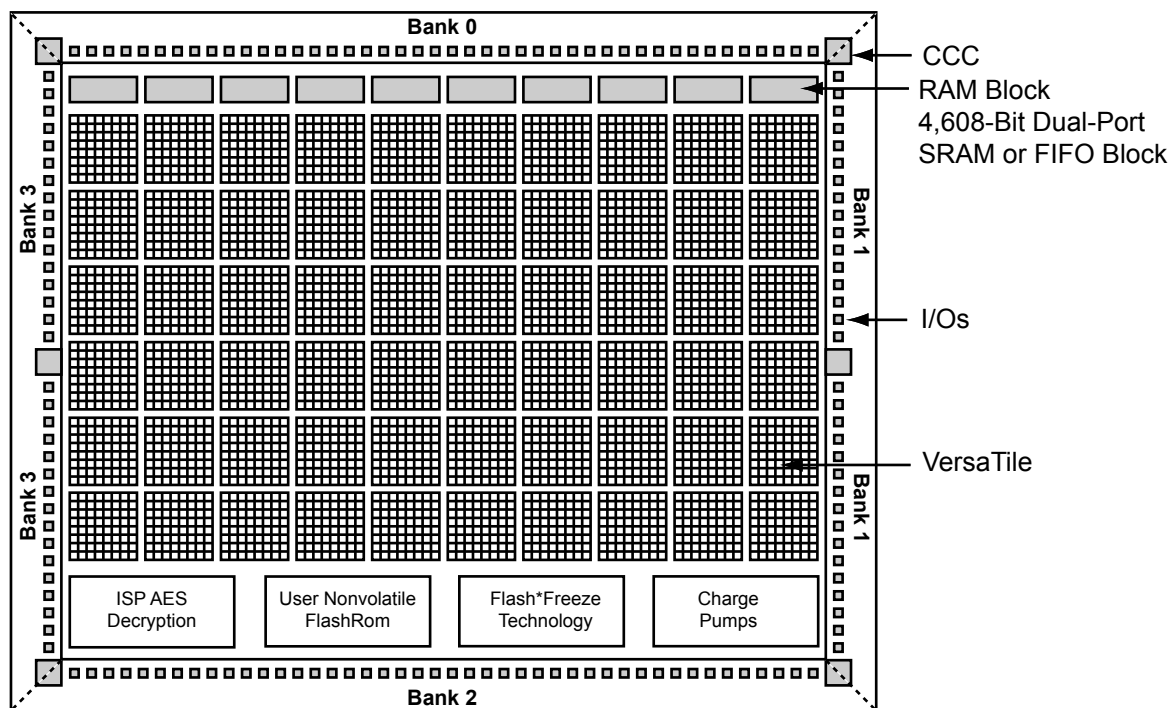


Figure 1-4 • IGLOO Device Architecture Overview with Four I/O Banks (AGLN250)

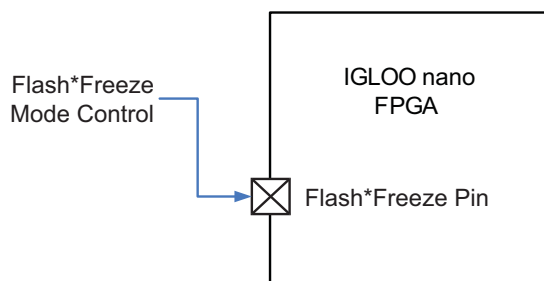
## Flash\*Freeze Technology

The IGLOO nano device has an ultra-low power static mode, called Flash\*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash\*Freeze technology enables the user to quickly (within 1  $\mu$ s) enter and exit Flash\*Freeze mode by activating the Flash\*Freeze pin while all power supplies are kept at their original values. I/Os, global I/Os, and clocks can still be driven and can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash\*Freeze mode.

Alternatively, I/Os can be set to a specific state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 2  $\mu$ W in this mode.

Flash\*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash\*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to [Figure 1-5](#) for an illustration of entering/exiting Flash\*Freeze mode. It is also possible to use the Flash\*Freeze pin as a regular I/O if Flash\*Freeze mode usage is not planned.



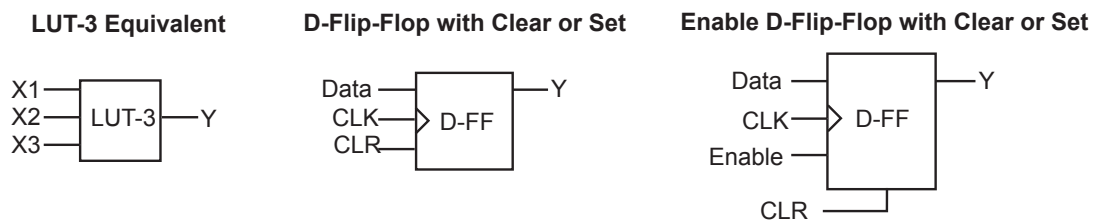
**Figure 1-5 • IGLOO nano Flash\*Freeze Mode**

## VersaTiles

The IGLOO nano core consists of VersaTiles, which have been enhanced beyond the ProASIC<sup>PLUS</sup>® core tiles. The IGLOO nano VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 1-6](#) for VersaTile configurations.



**Figure 1-6 • VersaTile Configurations**

## **User Nonvolatile FlashROM**

IGLOO nano devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO nano IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGLN030 and smaller devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The IGLOO nano development software solutions, Libero<sup>®</sup> System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature enables the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Microsemi Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

## **SRAM and FIFO**

IGLOO nano devices (except the AGLN030 and smaller devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGLN030 and smaller devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## **PLL and CCC**

Higher density IGLOO nano devices using either the two I/O bank or four I/O bank architectures provide designers with very flexible clock conditioning capabilities. AGLN060, AGLN125, and AGLN250 contain six CCCs. One CCC (center west side) has a PLL. The AGLN030 and smaller devices use different CCCs in their architecture (CCC-GL). These CCC-GLs contain a global MUX but do not have any PLLs or programmable delays.

For devices using the six CCC block architecture, these are located at the four corners and the centers of the east and west sides. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from dedicated connections to the CCC block, which are located near the CCC.

The CCC block has these key features:

- Wide input frequency range ( $f_{IN\_CCC}$ ) = 1.5 MHz up to 250 MHz
- Output frequency range ( $f_{OUT\_CCC}$ ) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 μs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz /  $f_{OUT\_CCC}$  (for PLL only)

### **Global Clocking**

IGLOO nano devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

### **I/Os with Advanced I/O Standards**

IGLOO nano FPGAs feature a flexible I/O structure, supporting a range of voltages (1.2 V, 1.2 V wide range, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V).

The I/Os are organized into banks with two, three, or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of various single-data-rate applications for all versions of nano devices and double-data-rate applications for the AGLN060, AGLN125, and AGLN250 devices.

IGLOO nano devices support LVTTTL and LVCMOS I/O standards, are hot-swappable, and support cold-sparing and Schmitt trigger.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

### **Wide Range I/O Support**

IGLOO nano devices support JEDEC-defined wide range I/O operation. IGLOO nano devices support both the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.



## Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

**Note:** PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-7 on page 1-9).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
  - 1 – I/O is set to drive out logic High
  - 0 – I/O is set to drive out logic Low
  - Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming
  - Z -Tri-State: I/O is tristated

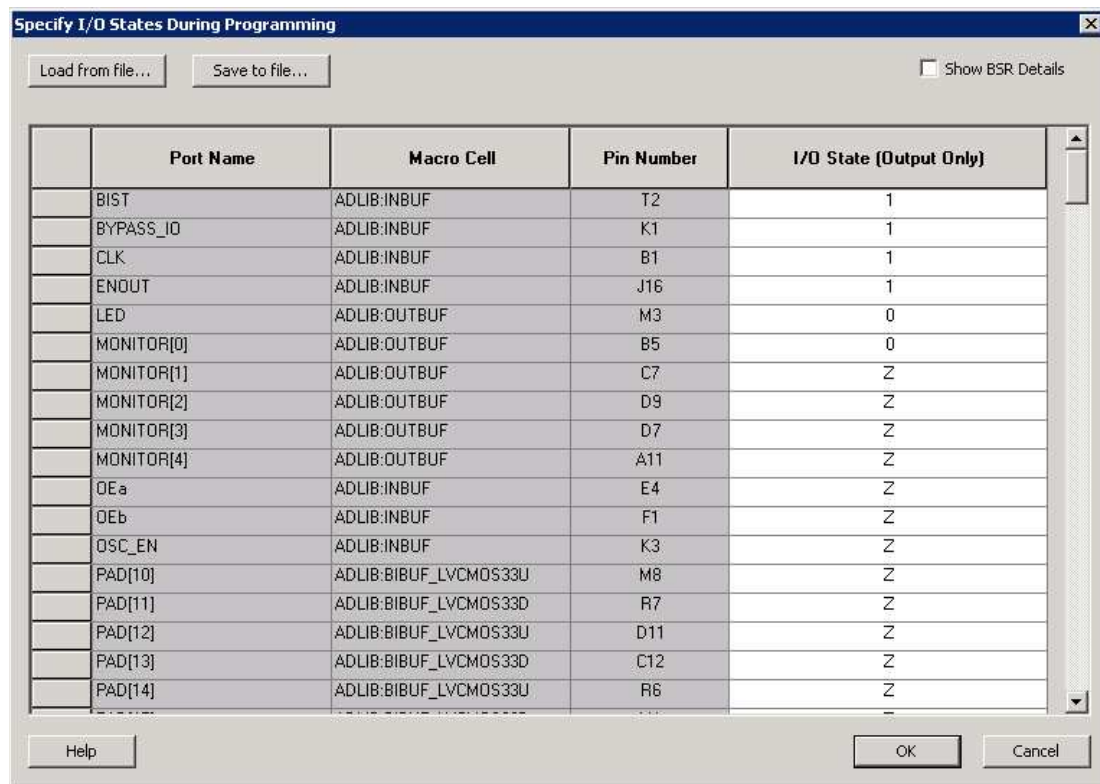


Figure 1-7 • I/O States During Programming Window

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

**Note:** I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

## 2 – IGLOO nano DC and Switching Characteristics

### General Specifications

The Z feature grade does not support the enhanced nano features of Schmitt trigger input, Flash\*Freeze bus hold (hold previous I/O state in Flash\*Freeze mode), cold-sparing, and hot-swap I/O capability. Refer to "IGLOO nano Ordering Information" on page IV for more information.

### Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2](#) on [page 2-2](#) is not implied.

**Table 2-1 • Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	-0.3 to 1.65	V
VJTAG	JTAG DC voltage	-0.3 to 3.75	V
VPUMP	Programming voltage	-0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	-0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage	-0.3 to 3.75	V
VI <sup>1</sup>	I/O input voltage	-0.3 V to 3.6 V	V
T <sub>STG</sub> <sup>2</sup>	Storage temperature	-65 to +150	°C
T <sub>J</sub> <sup>2</sup>	Junction temperature	+125	°C

**Notes:**

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-4](#) on [page 2-3](#).
2. For flash programming and retention maximum limits, refer to [Table 2-3](#) on [page 2-2](#), and for recommended operating limits, refer to [Table 2-2](#) on [page 2-2](#).

**Table 2-2 • Recommended Operating Conditions <sup>1</sup>**

Symbol	Parameter		Extended Commercial	Industrial	Units
T <sub>J</sub>	Junction temperature		-20 to +85 <sup>2</sup>	-40 to +100 <sup>2</sup>	°C
VCC	1.5 V DC core supply voltage <sup>3</sup>		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range core voltage <sup>4,5</sup>		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP <sup>6</sup>	Programming voltage	Programming mode	3.15 to 3.45	3.15 to 3.45	V
		Operation	0 to 3.6	0 to 3.6	V
VCCPLL <sup>7</sup>	Analog power supply (PLL)	1.5 V DC core supply voltage <sup>3</sup>	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V wide range core supply voltage <sup>4</sup>	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV <sup>8,9</sup>	1.2 V DC supply voltage <sup>4</sup>		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range supply voltage <sup>4</sup>		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.3 V DC wide range supply voltage <sup>10</sup>		2.7 to 3.6	2.7 to 3.6	V

**Notes:**

- All parameters representing voltages are measured with respect to GND unless otherwise specified.
- Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero Online Help.
- For IGLOO<sup>®</sup> nano V5 devices
- For IGLOO nano V2 devices only, operating at VCCI ≥ VCC
- IGLOO nano V5 devices can be programmed with the VCC core voltage at 1.5 V only. IGLOO nano V2 devices can be programmed with the VCC core voltage at 1.2 V (with FlashPro4 only) or 1.5 V. If you are using FlashPro3 and want to do in-system programming using 1.2 V, please contact the factory.
- V<sub>PUMP</sub> can be left floating during operation (not programming mode).
- VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter for further information.
- VMV pins must be connected to the corresponding VCCI pins. See the Pin Descriptions chapter of the *IGLOO nano FPGA Fabric User's Guide* for further information.
- The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-21 on page 2-19](#). VCCI should be at the same voltage within a given I/O bank.
- 3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.

**Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature<sup>1</sup>**

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T <sub>STG</sub> (°C) <sup>2</sup>	Maximum Operating Junction Temperature T <sub>J</sub> (°C) <sup>2</sup>
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

**Notes:**

- This is a stress rating only; functional operation at any condition other than those indicated is not implied.
- These limits apply for program/data retention only. Refer to [Table 2-1 on page 2-1](#) and [Table 2-2](#) for device operating conditions and absolute limits.

**Table 2-4 • Overshoot and Undershoot Limits <sup>1</sup>**

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle <sup>2</sup>	Maximum Overshoot/Undershoot <sup>2</sup>
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

**Notes:**

1. Based on reliability requirements at 85°C.
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.

## I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO nano device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-1 on page 2-4](#).

There are five regions to consider during power-up.

IGLOO nano I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 2-1](#) and [Figure 2-2 on page 2-5](#)).
2.  $VCCI > VCC - 0.75\text{ V}$  (typical)
3. Chip is in the operating mode.

### VCCI Trip Point:

Ramping up (V5 devices):  $0.6\text{ V} < \text{trip\_point\_up} < 1.2\text{ V}$

Ramping down (V5 devices):  $0.5\text{ V} < \text{trip\_point\_down} < 1.1\text{ V}$

Ramping up (V2 devices):  $0.75\text{ V} < \text{trip\_point\_up} < 1.05\text{ V}$

Ramping down (V2 devices):  $0.65\text{ V} < \text{trip\_point\_down} < 0.95\text{ V}$

### VCC Trip Point:

Ramping up (V5 devices):  $0.6\text{ V} < \text{trip\_point\_up} < 1.1\text{ V}$

Ramping down (V5 devices):  $0.5\text{ V} < \text{trip\_point\_down} < 1.0\text{ V}$

Ramping up (V2 devices):  $0.65\text{ V} < \text{trip\_point\_up} < 1.05\text{ V}$

Ramping down (V2 devices):  $0.55\text{ V} < \text{trip\_point\_down} < 0.95\text{ V}$

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

### PLL Behavior at Brownout Condition

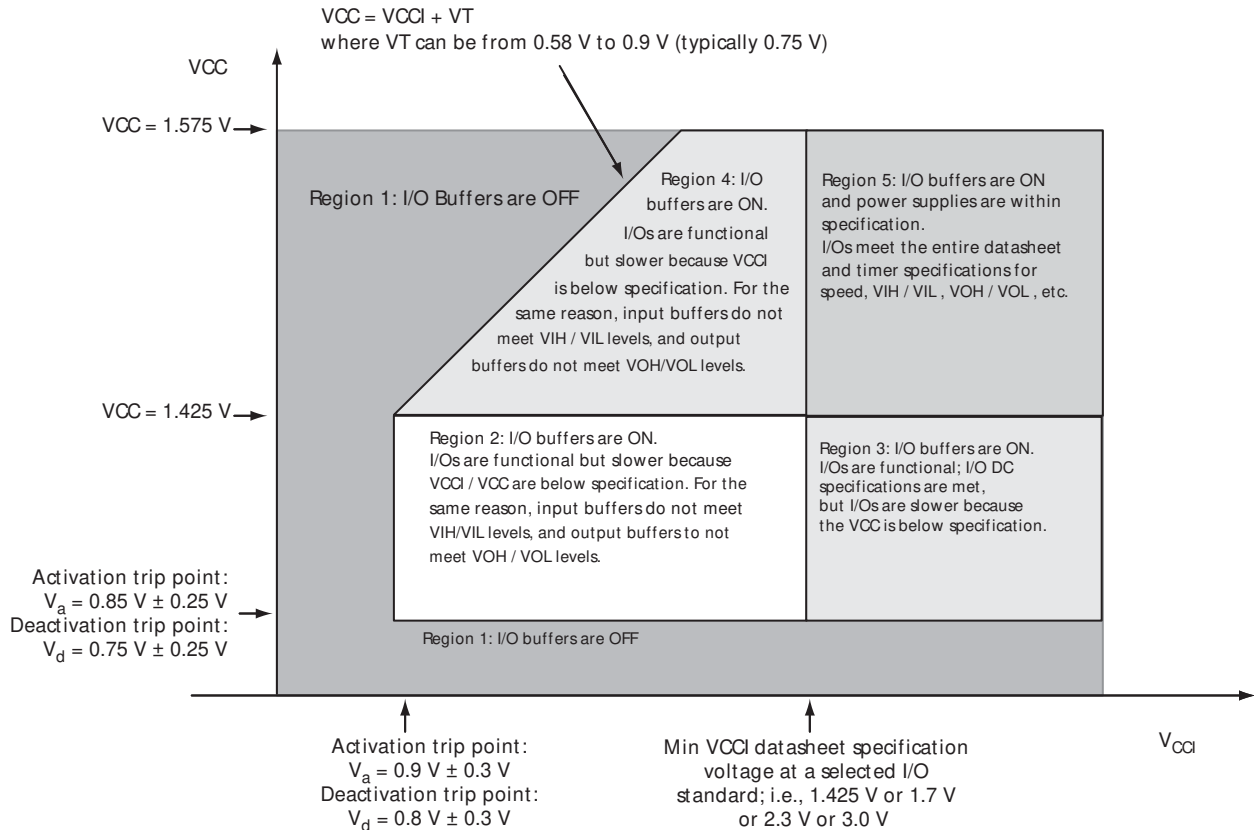
Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ( $0.75\text{ V} \pm 0.25\text{ V}$  for V5 devices, and  $0.75\text{ V} \pm 0.2\text{ V}$  for V2 devices), the PLL output lock signal goes LOW and/or the output clock is lost. Refer to the "Brownout Voltage" section in the "Power-Up/Down Behavior of Low Power Flash Devices" chapter of the *IGLOO nano FPGA Fabric User's Guide* for information on clock and lock recovery.

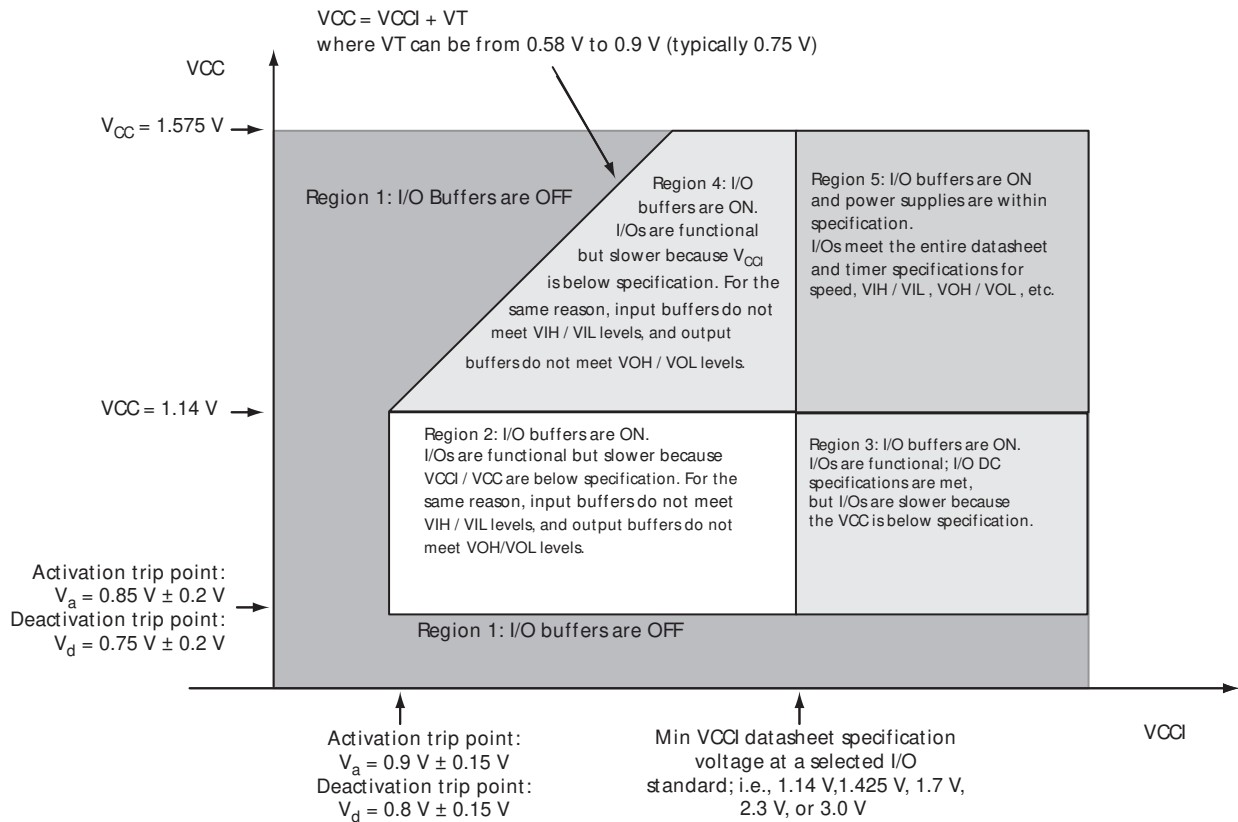
### Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.



**Figure 2-1 • V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**



**Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

## Thermal Characteristics

### Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

$T_A$  = Ambient temperature

$\Delta T$  = Temperature gradient between junction (silicon) and ambient  $\Delta T = \theta_{ja} * P$

$\theta_{ja}$  = Junction-to-ambient of the package.  $\theta_{ja}$  numbers are located in Figure 2-5.

P = Power dissipation

### Package Thermal Characteristics

The device junction-to-case thermal resistivity is  $\theta_{jc}$  and the junction-to-ambient air thermal resistivity is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown for two air flow rates. The maximum operating junction temperature is 100°C. EQ 2 shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja}(\text{}^\circ\text{C/W)}} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{20.5^\circ\text{C/W}} = 1.46 \text{ W}$$

EQ 2

**Table 2-5 • Package Thermal Resistivities**

Package Type	Pin Count	$\theta_{jc}$	$\theta_{ja}$			Units
			Still Air	200 ft./min.	500 ft./min.	
Chip Scale Package (CSP)	36	TBD	TBD	TBD	TBD	C/W
	81	TBD	TBD	TBD	TBD	C/W
Quad Flat No Lead (QFN)	48	TBD	TBD	TBD	TBD	C/W
	68	TBD	TBD	TBD	TBD	C/W
	100	TBD	TBD	TBD	TBD	C/W
Very Thin Quad Flat Pack (VQFP)	100	10.0	35.3	29.4	27.1	C/W

### Temperature and Voltage Derating Factors

**Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425 \text{ V}$ )**  
For IGLOO nano V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ( $^\circ\text{C}$ )						
	$-40^\circ\text{C}$	$-20^\circ\text{C}$	$0^\circ\text{C}$	$25^\circ\text{C}$	$70^\circ\text{C}$	$85^\circ\text{C}$	$100^\circ\text{C}$
1.425	0.947	0.956	0.965	0.978	1.000	1.009	1.013
1.5	0.875	0.883	0.892	0.904	0.925	0.932	0.937
1.575	0.821	0.829	0.837	0.848	0.868	0.875	0.879



**Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$ )**  
 For IGLOO nano V2, 1.2 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ( $^\circ\text{C}$ )						
	$-40^\circ\text{C}$	$-20^\circ\text{C}$	$0^\circ\text{C}$	$25^\circ\text{C}$	$70^\circ\text{C}$	$85^\circ\text{C}$	$100^\circ\text{C}$
1.14	0.968	0.974	0.979	0.991	1.000	1.006	1.009
1.2	0.863	0.868	0.873	0.884	0.892	0.898	0.901
1.26	0.792	0.797	0.801	0.811	0.819	0.824	0.827

## Calculating Power Dissipation

### Quiescent Supply Current

Quiescent supply current ( $I_{DD}$ ) calculation depends on multiple factors, including operating voltages ( $V_{CC}$ ,  $V_{CCI}$ , and  $V_{JTAG}$ ), operating temperature, system clock frequency, and power mode usage. Microsemi recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

**Table 2-8 • Power Supply State per Mode**

Modes/Power Supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

*Note:* Off: Power Supply level = 0 V

**Table 2-9 • Quiescent Supply Current ( $I_{DD}$ ) Characteristics, IGLOO nano Flash\*Freeze Mode\***

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
Typical ( $25^\circ\text{C}$ )	1.2 V	1.9	3.3	3.3	8	13	20	$\mu\text{A}$
	1.5 V	5.8	6	6	10	18	34	$\mu\text{A}$

*Note:* \* $I_{DD}$  includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-9 through Table 2-14 on page 2-9 and Table 2-15 on page 2-10 through Table 2-18 on page 2-11 (PDC6 and PDC7).

**Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Sleep Mode\***

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
VCCI = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	μA

Note:  $*I_{DD} = N_{BANKS} * I_{CCI}$

**Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Shutdown Mode**

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	0	0	0	0	μA

**Table 2-12 • Quiescent Supply Current (IDD), No IGLOO nano Flash\*Freeze Mode<sup>1</sup>**

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
<b>ICCA Current<sup>2</sup></b>								
Typical (25°C)	1.2 V	3.7	5	5	10	13	18	μA
	1.5 V	8	14	14	20	28	44	μA
<b>ICCI or JTAG Current</b>								
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	μA

**Notes:**

1.  $IDD = N_{BANKS} * ICCI + ICCA$ . JTAG counts as one bank when powered.
2. Includes VCC, VCCPLL, and VPUMP currents.