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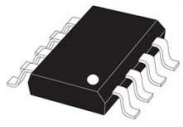
AIS1120SX
AIS2120SX

MEMS automotive acceleration sensor: single/dual-axis with SPI interface

Datasheet - production data



SOIC8

Features

- AEC-Q100 qualified
- 3.3 V single supply operation
- 14-bit data output
- ±120 *g* full scale
- Slow and fast offset cancellation
- Embedded self-test
- Selectable low-pass filter
- SPI interface
- ECOPACK® compliant
- Extended temperature range -40 °C to +105 °C

Applications

- Airbag systems
- Vibrations, impact monitoring

Description

The AIS1120SX / AIS2120SX is a central acceleration sensor with a single or dual axis sensing element and an IC interface able to provide acceleration information to a master control unit via an SPI protocol.

The sensing element, capable of detecting the acceleration, is manufactured using a dedicated process developed by ST to produce inertial sensors and actuators in silicon.

The IC interface is manufactured using a BCD process that allows a high level of integration. The device is factory trimmed to better tune the characteristics of the sensing element with the acceleration information to be supplied.

The AIS1120SX / AIS2120SX has a full scale of ±120 *g*. The acquisition chain consists of a C/V converter, a full-differential charge amplifier, a 2nd order ΣΔ analog-to-digital converter and a digital core, which includes filtering, compensation and interpolation, control logic and SPI protocol generation.

The differential capacitance of the sensor is proportional to the proof mass displacement; thus, by sensing the differential capacitance, the position of the sensor is determined. Then, since the mass position is known, and the position is related to the input acceleration, the input acceleration can be easily deduced.

The device is available in a plastic SOIC8 package and is guaranteed to operate over a temperature range extending from -40 °C to +105 °C.

Table 1. Device summary

Order code	*g*-range	Sensitivity axes	Operating temperature range [°C]	Package	Packing
AIS1120SXTR	120 *g*	x	-40 to +105	SOIC8N	Tape and reel
AIS2120SXTR	120 *g*	xy	-40 to +105	SOIC8N	Tape and reel

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List of figures

1 Block diagrams and pin description

1.1 Block diagrams

Figure 1. AIS1120SX block diagram

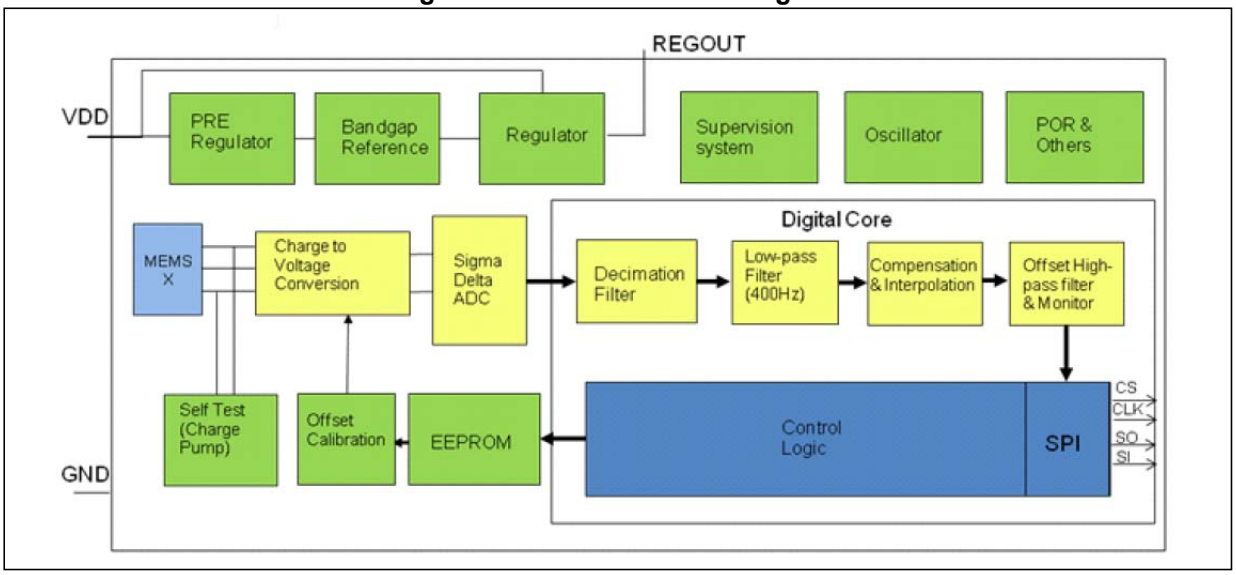
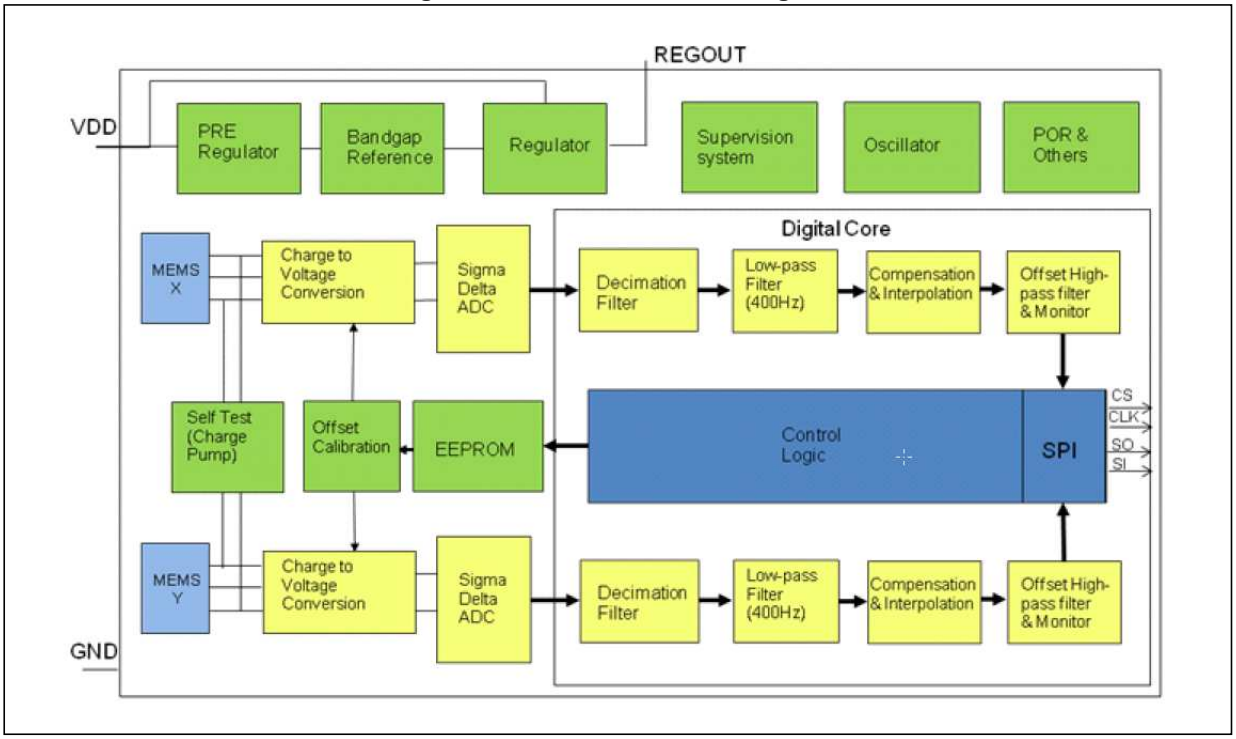


Figure 2. AIS2120SX block diagram

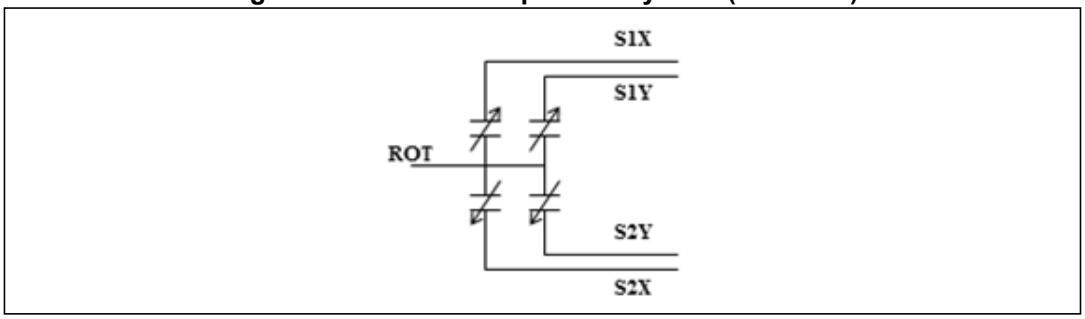


1.1.1 Mechanical element

A proprietary process is used to create a surface micromachined accelerometer. This technology allows processing suspended silicon structures which are attached to the substrate in few points called anchors and are free to move in the direction of the sensed acceleration thanks to flexible springs. In order to be compatible with standard packaging techniques, a cap is placed at wafer level on the top of the sensing element.

From an electrical point of view, the sensor can be represented as a differential capacitive system (see below for a dual-axis element). When the acceleration is applied to the sensor, the proof mass displaces from its nominal position, causing an unbalance in the capacitive half-bridge. This unbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor:

Figure 3. Differential capacitive system (dual axis)



The differential capacitive change towards acceleration can be expressed, in small displacements approximation, as:

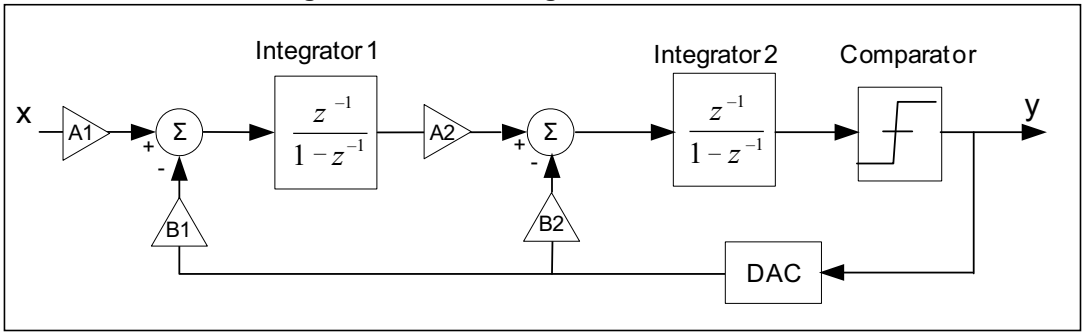
$$\Delta C = \frac{2C_0 ma}{gk}$$

Where C_0 is the at-rest capacitance, m is the inertial mass, a the acceleration, k stiffness of the springs and g the distance between capacitor electrodes.

1.1.2 Sigma-Delta converter

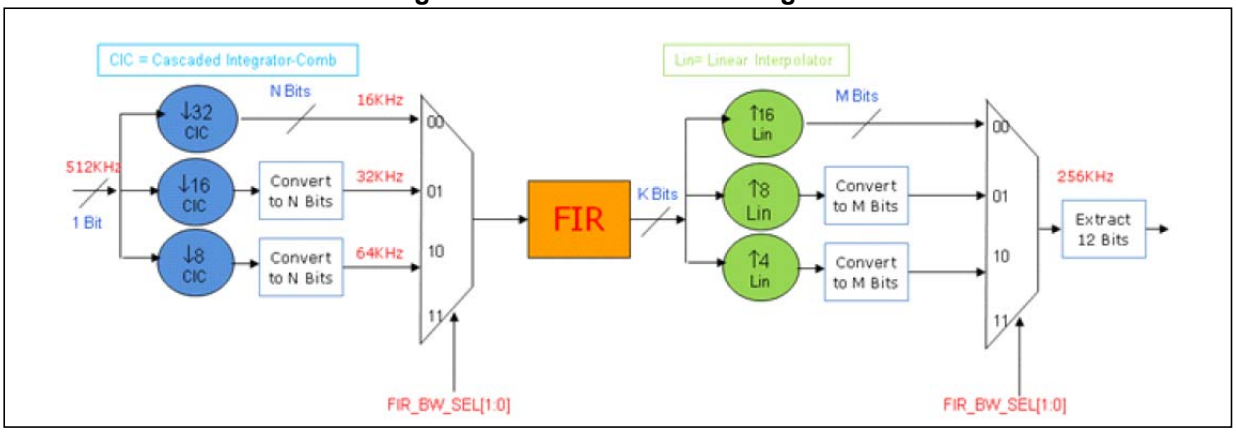
A 2nd order sigma-delta modulator is used to convert the differential voltage that comes from the charge-to-voltage converter to a pulse-density modulated (PDM) data stream. The data stream will be further processed through on-chip digital filters.

Figure 4. 2nd order sigma-delta modulator



1.1.3 Filter architecture

Figure 5. Filter architecture diagram



The architecture of the digital filters allows selecting 3 different cut-off frequencies based on 2 bits in the register map: FIR_BW_SEL[1:0].

The cut-off frequencies are 400 Hz, 800 Hz, and 1600 Hz. For the 1600 Hz filter, the noise level is higher and the ENOB is 10/11 bits, and not 12 bits.

The cut-off frequency has to be selected for each axis during the initialization phase. Once the initialization phase is finished and the end of the initialization bit is set, the cut-off frequency is locked and any attempt to change it during normal mode will generate an SPI error.

The cut-off frequencies can be selected as described below:

FIR_BW_SEL[1:0]:

= "00" FIR with F3DB = 400 Hz is selected (default);

= "01" FIR with F3DB = 800 Hz is selected;

= "10" FIR with F3DB = 1600 Hz is selected (ENOB is 10/11bits in this mode);

= "11" FIR with F3DB = 400 Hz is selected.

1.1.4 Decimation filter

$$H_D(z) = \left[\frac{1 - z^{-D \times M}}{1 - z^{-1}}\right]^N$$

Differential delay: D=1

Number of sections: N=3

Decimation factor:

- M = 32 if FIR_BW_SEL[1:0] = "00" (400 Hz)
- M = 16 if FIR_BW_SEL[1:0] = "01" (800 Hz)
- M = 8 if FIR_BW_SEL[1:0] = "10" (1600 Hz)

1.1.5 Low-pass filter

H_LPF (Z) is a FIR digital filter with 26 coefficients (K = 25):

$$H_{LPF}(Z) = \sum_{i=0}^{K} a_i Z^{-i}$$

Figure 6 and *Figure 7* shows the comparison between the FIR filter and an analog Bessel filter when the cut-off frequency is 400 Hz.

Figure 6. FIR vs. 4th and 6th order Bessel filter for amplitude frequency response

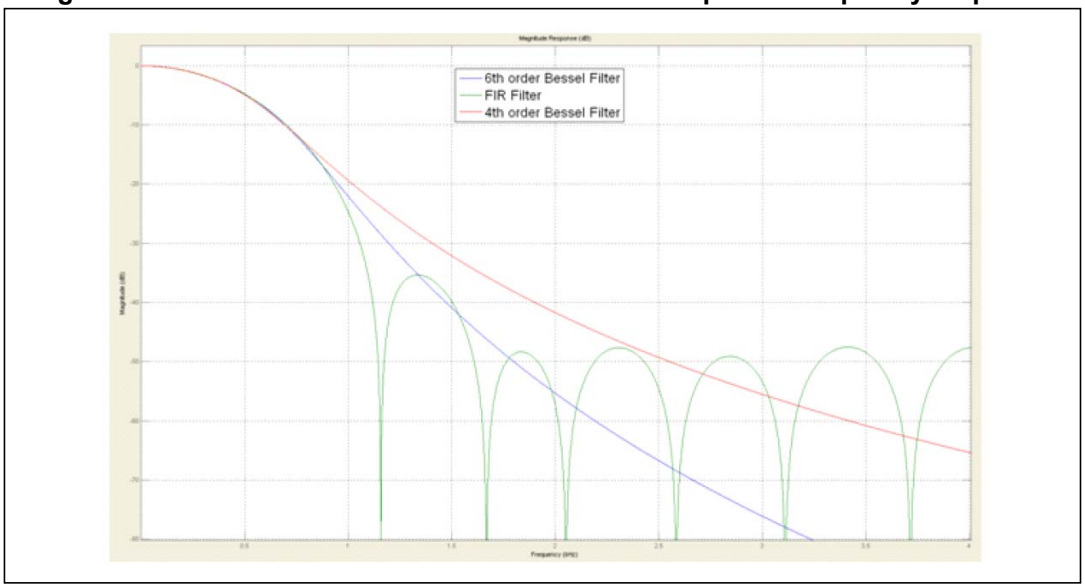
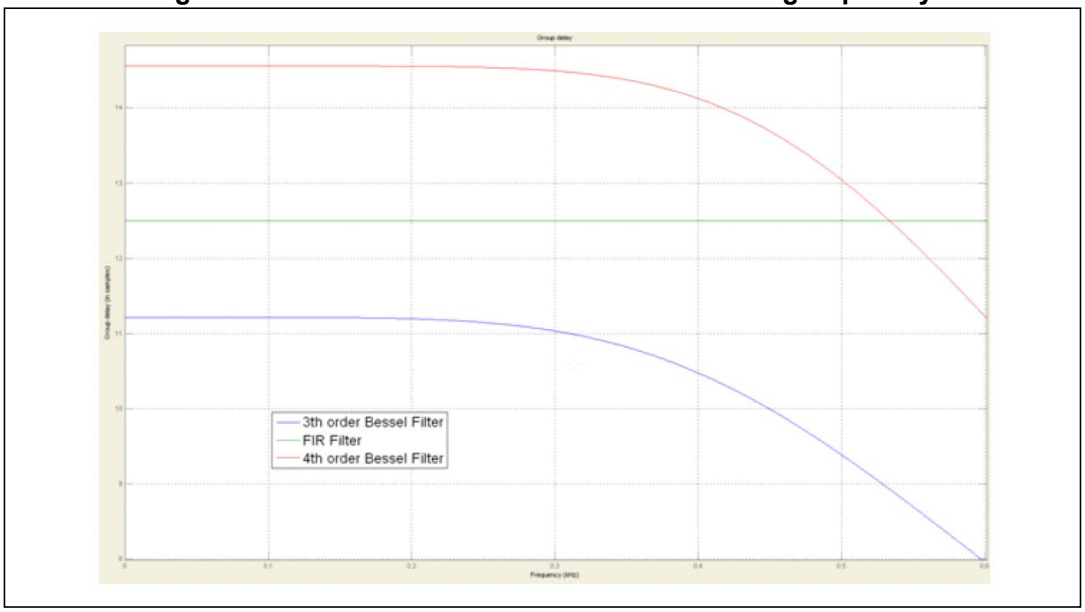


Figure 7. FIR vs. 3rd and 4th order Bessel filter for group delay



1.1.6 Signal compensation

On-chip EEPROM bits are used to compensate sensitivity error and offset error.

1.1.7 Linear interpolation

The device features an L-to-1 linear data interpolation computed from the present and the previous samples. L depends on the cut-off frequency selected:

Interpolation factor:

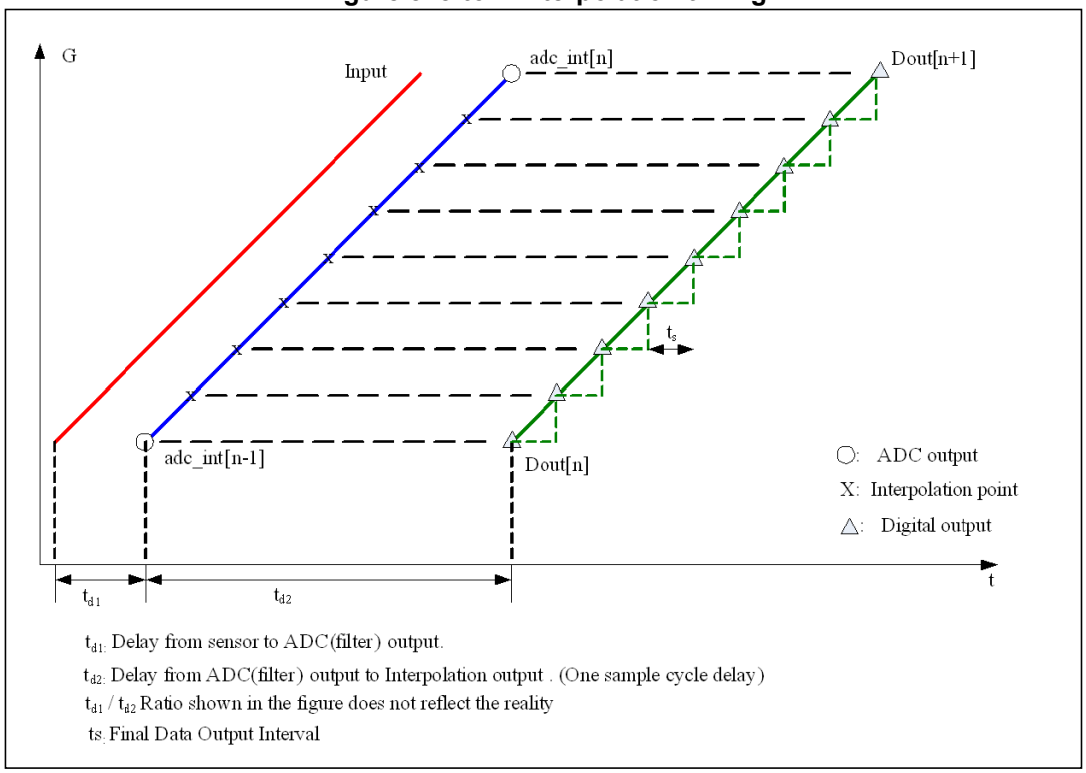
- L = 16 if FIR_BW_SEL[1:0] = "00" or “11”
- L = 8 if FIR_BW_SEL[1:0] = "01"
- L = 4 if FIR_BW_SEL[1:0] = "10"

The data interpolation helps reduce sample jitter. The digital result will have a latency of one sample time before being sent to the SPI bus.

The maximum jitter will be 62.5 µs/16 = 3.9 µs.

Figure 8 shows an interpolation example.

Figure 8. 8-to-1 interpolation timing



1.1.8 Signal delays

Figure 9. Signal delay of reading-chain blocks with 400 Hz filter

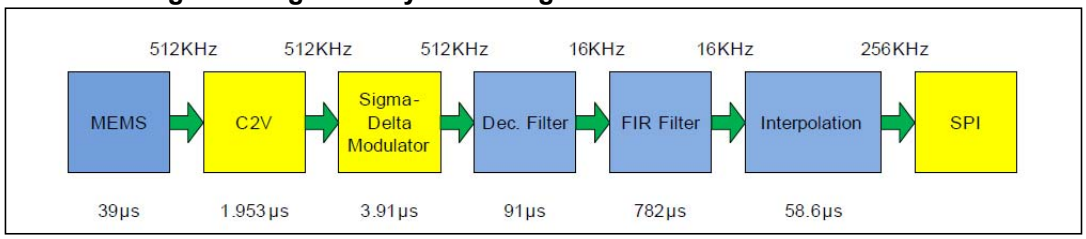


Figure 10. Signal delay of reading-chain blocks with 800 Hz filter

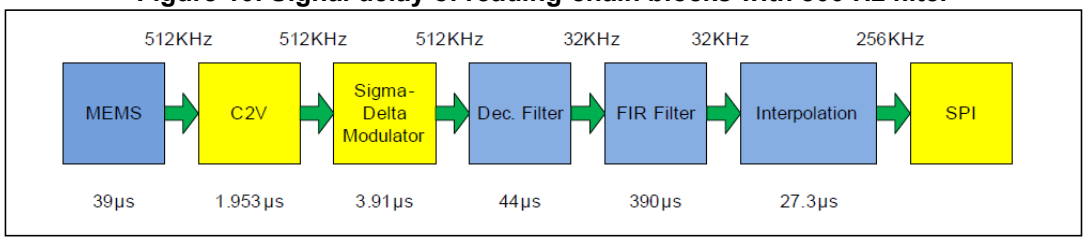
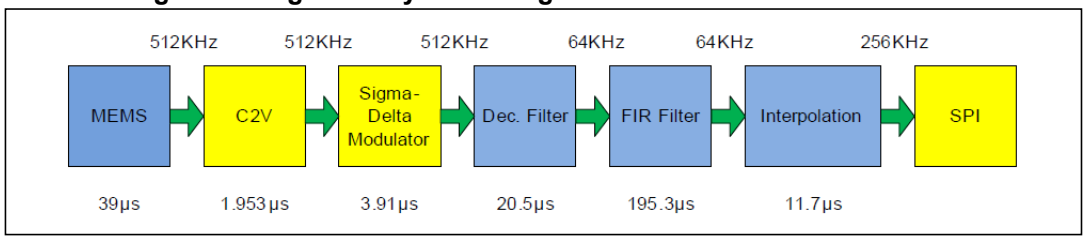


Figure 11. Signal delay of reading-chain blocks with 1600 Hz filter



1.1.9 Offset cancellation

The offset cancellation is performed in the last step of the digital signal processing and includes two modes:

1. Slow offset cancellation

2. Fast offset cancellation

The digital low-pass filter with selectable bandwidth (fast, slow cancellation) is controlled by a state machine. Fast offset cancellation is used after power-on. Slow offset cancellation, for continuously running offset cancellation, operates in normal mode.

Offset cancellation uses a moving average filter with a fixed update limit. Fast offset cancellation occurs after power up while EOI = 0. Slow offset cancellation occurs after EOI is set to 1.

The Offset Cancellation Error Flag is set when the offset is outside the offset correction range (±1020 LSB) during slow offset cancellation. A hardware error is indicated based on this flag being set for the affected axis. The flow chart for the offset cancellation block is shown in the following figure.

Figure 12. Offset cancellation block diagram

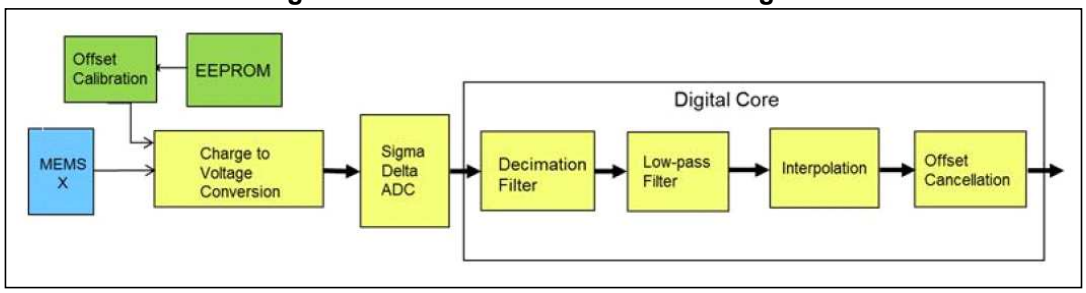
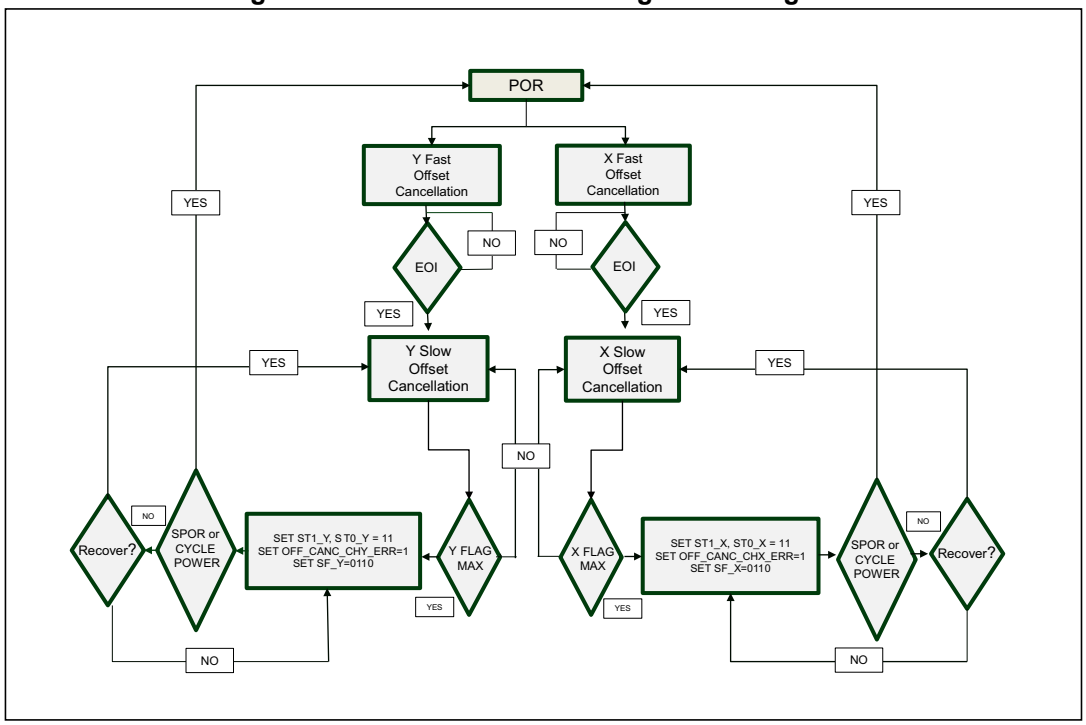


Figure 13. Offset cancellation flag monitoring flow



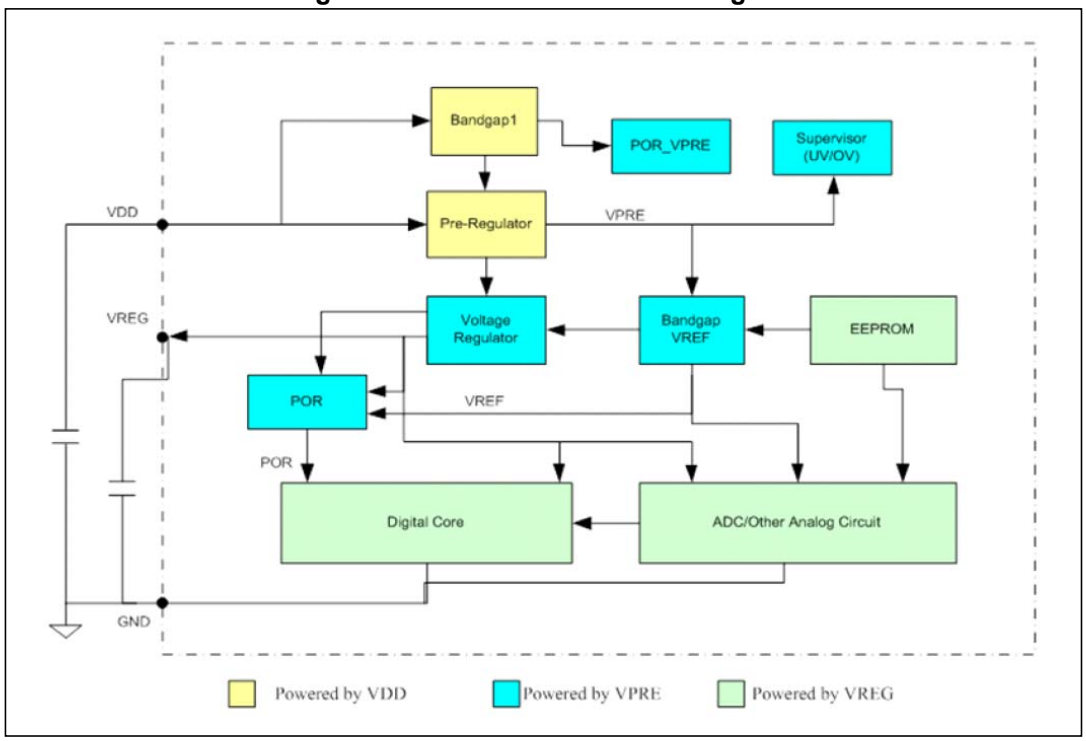
1.1.10 State machine and on-chip-oscillator

There is an on-chip oscillator implemented. The clock frequency is trimmed to 16.384 MHz at room temp. This clock is used for the digital core. One 1024 KHz clock divided from this main clock is used for the sigma-delta convertor and digital signal processing module (DSP).

1.1.11 Power domain block diagram

Figure 14 shows the power domain of the device. A pre-regulator is implemented to improve power supply sensitivity and PSRR of the device. The pre-regulator provides power to an on-chip bandgap reference and the EEPROM.

Figure 14. Power domain block diagram

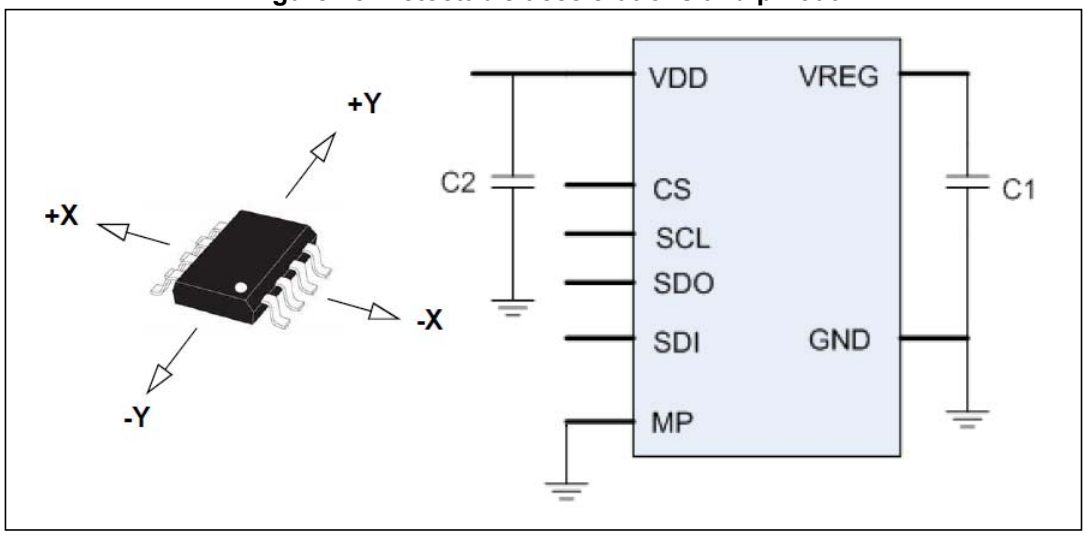


Key blocks of the power section are:

1. **Pre-regulator**: based on a self-biased supply-thermal independent structure, which is able to produce an internal stable voltage of 2.8 V ±15%, with a maximum output current of 3 mA. The architecture is based on a bandgap cell, which produces a thermal-independent reference, which is used in turn to produce the voltage pre-regulator output; the pre-regulator is powered by VDD, and is designed to supply only some internal low-power blocks.
2. **Regulator**: an on-chip 2.8 V regulator supplies internal power for the device; it should not be used to power other devices via the VREG terminal. A bypass capacitor is required on the VREG pin to keep the regulator stable.
3. **Bandgap reference**: the voltage bandgap is powered by the voltage pre-regulator and is used as voltage reference for all other circuits including the front-end, supervision circuits and A/D converter.
4. **Charge-to-voltage converter**: the C/V converter consists of a fully differential charge integrator with a continuous time ICMFB (Input Common Mode Feedback) control loop, discrete time ICMFB, and a Switched Capacitor OCMFB (Output Common Mode Feedback) control loop. Furthermore the C/V converter has one 9-bit DAC in order to trim the offset of the measurement chain and mechanical element.
5. **Self-test charge pump**: the self-test charge pump internally generates a voltage higher than the 2.8 V regulated supply voltage. The charge pump is activated when the self-test mode is enabled and provides an excitation voltage of 6.6 V. During the self-test the voltage is applied and disconnected to the sensor according to a duty cycle which allows simulating a well-known force on the sensor.

1.2 Pin description

Figure 15. Detectable accelerations and pinout



C1 = 1 µF ± 10%, 10 V (ceramic, VREG capacitor)

C2 = 0.1 µF ± 10%, 10 V (ceramic, power supply decoupling capacitor)

Note: An acceleration of the device in the "+X" or "+Y" directions results in a positive output change, a deceleration in this direction (or acceleration to the opposite side) results in a negative output signal.

Table 2. Pin description

Pin#	Name	Function
1	SCL	SPI clock
2	SDI	SPI data in
3	SDO	SPI data out
4	CS	SPI chip select
5	GND	Power supply return pin (ground level)
6	VREG	Voltage regulator output. A ceramic capacitor of 1.0 µF ± 10% 10 V must be connected to this pin, which should not be used to power other devices.
7	VDD	This pin provides power to the device. A ceramic capacitor of 0.1 µF ± 10% 10 V must be connected to this pin.
8	MP	Connect to GND

2 Customer accessible data arrays (registers)

Figure 16. Accessible registers

Address	Name	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]
0x00	REG_CTRL_0	0	0	0	0	0	0	0	END_OF_INIT
0x01	REG_CTRL_1	0	0	0	0	0	SELF_TEST_CMD[2:0]		
0x02	REG_CONFIG	FIR_BW_SEL_CHY[1:0]		FIR_BW_SEL_CHX[1:0]		DIS_OFF_MON_CHY	DIS_OFF_MON_CHX	DIS_OFF_CANC_CHY	DIS_OFF_CANC_CHX
0x03	REG_STATUS_0	STATUS[1:0]		TESTMODE_ENABLED	REG_CTRL_0_WR_ERR_LATCH	0	LOSSCAP_ERR_LATCH	END_OF_PWRUP_LATCH	RST_ACTIVE_LATCH
0x04	REG_STATUS_1	SPI_ERR	EEPROM_ERR_LATCH	0	0	OFF_CANC_CHY_ERR	OFF_CANC_CHX_ERR	REG_CONFIG_WR_ERR_LATCH	REG_CTRL_1_WR_ERR_LATCH
0x05	REG_STATUS_2	A2D_SAT_CHY_ERR	A2D_SAT_CHX_ERR	0	CHARGE_PUMP_ERR_LATCH	VREG_LOW_ERR	VREG_HIGH_ERR	VDD_LOW_ERR	VDD_HIGH_ERR
0x06	REG_CHID_REVID	0	0	CHY_ACTIVE	CHX_ACTIVE	0	REVID[2:0]		
0x07	REG_ACC_CHX_LOW	REG_ACC_CHX[7:0]							
0x08	REG_ACC_CHX_HIGH	AccelDataXLatch	0	REG_ACC_CHX[13:8]					
0x09	REG_ACC_CHY_LOW	REG_ACC_CHY[7:0]							
0x0A	REG_ACC_CHY_HIGH	AccelDataYLatch	0	REG_ACC_CHY[13:8]					
0x0B	REG_OSC_COUNTER	OSC_COUNTER[7:0]							
0x0C	REG_ID_SENSOR_TYPE	ID_SENSOR_TYPE[7:0]							
0x0D	REG_ID_VEH_MANUF	0	0	0	0	ID_VEH_MANUF[3:0]			
0x0E	REG_ID_SENSOR_MANUF	ID_SENSOR_MANUF[7:0]							
0x0F	REG_ID_LOT_0	ID_LOT[7:0]							
0x10	REG_ID_LOT_1	ID_LOT[15:8]							
0x11	REG_ID_LOT_2	ID_LOT[23:16]							
0x12	REG_ID_LOT_3	0	0	ID_LOT[29:24]					
0x13	REG_ID_WAFER	0	0	0	ID_WAFER[4:0]				
0x14	REG_ID_COOR_X	ID_COOR_X[7:0]							
0x15	REG_ID_COOR_Y	ID_COOR_Y[7:0]							
0x16	REG_RESET	0	0	0	0	0	0	SOFT_RST[1:0]	
0x17	OFF_CHX_HIGH	OFF_CHX[10:3]							
0x18	OFF_CHX_LOW	OffDataXLatch	0	0	0	0	OFF_CHX[2:0]		
0x19	OFF_CHY_HIGH	OFF_CHY[10:3]							
0x1A	OFF_CHY_LOW	OffDataYLatch	0	0	0	0	OFF_CHY[2:0]		
0x1B	Not used	0	0	0	0	0	0	0	0
0x1C	Not used	0	0	0	0	0	0	0	0
0x1D	Not used	0	0	0	0	0	0	0	0
0x1E	Reserved	-							
0x1F	Reserved	-							

2.1 REG_CTRL_0

Table 3. REG_CTRL_0

REG_CTRL_0 (address: 0x00)				
Name	**Bit#**	**R/W**	**Reset state**	**Description**
0	[7:1]	R	0	
END_OF_INIT	0	R/W	0	End of initialization: Initialization is the time interval from reset to Self-test end: =”0” then device is in Initialization Phase = “1” then the device is in end of initialization phase (device is in normal mode) Rules : -When END_OF_BIT="1" then writing operations of REG_CTRL_1 and REG_CONFIG bits do not have effect and generate error flags CTRL_REG_1_WR_ERR="1"/CONFIG_REG_WR_ERR="1". -Cannot write EOI='1' if there is EE or HE error. -Cannot write EOI='1' if device is in +ve or -ve self-test (either CHX or CHY). Doing so, RE error (and CONFIG_REG_0_WR_ERR='1') will be produced

2.2 REG_CTRL_1

Table 4. REG_CTRL_1

REG_CTRL_1 (address: 0x01)				
Name	**Bit#**	**R/W**	**Reset state**	**Description**
0	[7:3]	R	0	
SELF_TEST_CMD	[2:0]	R/W	0	Self-test commands: = "000" then device is in 0 *g* self-test if EOI='0'; = "001" then device starts self-test on channel X with positive voltage; = "010" then device starts self-test on channel X with negative voltage; = "011" then device is in 0 *g* self-test if EOI='0' = "100" then device is in 0 *g* self-test if EOI='0' = "101" then device starts self-test on channel Y with positive voltage; = "110" then device starts self-test on channel Y with negative voltage; = "111" then device is in 0 *g* self-test if EOI='0' Rules : -Cannot write if EOI='1' -Cannot start a self-test on CHX/CHY if the channel is not enabled -Cannot switch from non-0g(-ve/+ve) self_test to another non-0g self_test(-ve/+ve) without going to 0g self-test Note: When starting channel X self-test: Channel X acceleration command will read channel X self-test value Channel Y acceleration command will read temperature sensor value for self-test temperature compensation algorithm. When starting channel Y self-test: Channel X acceleration command will read temperature sensor value for self-test temperature compensation algorithm. Channel Y acceleration command will read channel Y self-test value

2.3 REG_CONFIG

Table 5. REG_CONFIG

REG_CONFIG (address: 0x02)				
Name	**Bit#**	**R/W**	**Reset state**	**Description**

FIR_BW_SEL_CHY[1:0]	[7:6]	R/W	00	Channel Y FIR bandwidth selection bits:
				if = "00" FIR with F3DB = 400 Hz is selected;
				if = "01" FIR with F3DB = 800 Hz is selected;
				if = "10" FIR with F3DB = 1600 Hz is selected (resolution is 10/11bits in this mode);
				if = "11" FIR with F3DB = 400 Hz is selected.
				FIR_BW_SEL_CHY[1:0] is writable if END_OF_INIT="0".
				Writing FIR_BW_SEL_CHY[1:0] when END_OF_INIT="1" or when Channel Y self-test is activated, does not have effect and generates an error:
				CONFIG_REG_WR_ERR="1".

FIR_BW_SEL_CHX[1:0]	[5:4]	R/W	00	Channel X FIR bandwith selection bits:
				if = "00" FIR with F3DB = 400 Hz is selected;
				if = "01" FIR with F3DB = 800 Hz is selected;
				if = "10" FIR with F3DB = 1600 Hz is selected (resolution is 10/11bits in this mode);
				if = "11" FIR with F3DB = 400 Hz is selected.
				FIR_BW_SEL_CHX[1:0] is writable if END_OF_INIT="0".
				Writing FIR_BW_SEL_CHX[1:0] when END_OF_INIT="1" or when Channel X self-test is activated does not have effect and generates an error:
				CONFIG_REG_WR_ERR="1".

DIS_OFF_MON_CHY	3	R/W	0	Offset monitor channel Y disable bit. if = "0" then channel Y offset monitor is on; if = "1" then channel Y offset monitor is off. DIS_OFF_MON_CHY is writable if END_OF_INIT="0". Writing DIS_OFF_MON_CHY when END_OF_INIT="1" does not have effect and generates an error: CONFIG_REG_WR_ERR="1"

Table 5. REG_CONFIG (continued)

REG_CONFIG (address: 0x02)				
Name	**Bit#**	**R/W**	**Reset state**	**Description**
DIS_OFF_MON_CHX	2	R/W	0	Offset monitor channel X disable bit. = "0" then channel X offset monitor is on; = "1" then channel X offset monitor is off. DIS_OFF_MON_CHX is writable if END_OF_INIT="0". Writing DIS_OFF_MON_CHX when END_OF_INIT="1" does not have effect and generates an error: CONFIG_REG_WR_ERR="1"
DIS_OFF_CANC_CHY	1	R/W	0	Offset cancellation channel Y disable bit. = "0" then channel Y offset cancellation circuit is on; = "1" then channel Y offset cancellation circuit is off. DIS_OFF_CANC_CHY is writable if END_OF_INIT="0". Writing DIS_OFF_CANC_CHY when END_OF_INIT="1" does not have effect and generates an error: CONFIG_REG_WR_ERR="1"
DIS_OFF_CANC_CHX	0	R/W	0	Offset cancellation channel X disable bit. = "0" then channel X offset cancellation circuit is on; = "1" then channel X offset cancellation circuit is off. DIS_OFF_CANC_CHX is writable if END_OF_INIT="0". Writing DIS_OFF_CANC_CHX when END_OF_INIT="1" does not have effect and generates an error: CONFIG_REG_WR_ERR="1"

2.4 REG_STATUS

Table 6. REG_STATUS_0

REG_STATUS_0 (address: 0x03)				
Name	**Bit#**	**R/W**	**Reset state**	**Description**
STATUS [1:0]	[7:6]	R	00	Status Error bits: if = "00" device is in initialization phase (power-up, configuration, fast offset cancellation); if = "01" device is in normal mode (EOI = 1); if = "10" device is test phase (0 *g* test or active self test); EOI = 0; if = "11" device is in initialization phase or normal mode and some errors are detected: acceleration data are disregarded due to errors in device.
TESTMODE_ENABLED	5	R	0	“0”: normal mode; “1”: test mode
REG_CTRL_0_WR_ERR(1)	4	R	0	Will be set to '1' if write EOI = '1' attempt is made with the device in +ve or -ve self-test (either CHX or CHY).
Not used	3	R	0	“0” always
LOSS_CAP	2	R	0	Loss of capacitor: if = "0" then loss of capacitor is not detected (correct behavior); if = "1" then loss of capacitor is detected (wrong behavior). Note: 1.LOSS_CAP check is done during the power-up stage (~400 µs after POR) only. 2.Recommended VDD ramp rate >1 V/ms 3.It is recommended that LOSS_CAP flag (and all other hardware flags) be reconfirmed with soft POR after power up (END_OF_PWRUP='1').
END_OF_PWRUP	1	R	0	="1": end of power-up sequence; ready for self-test.
RST_ACTIVE	0	R	0	Reset Active bit: if = "0" then device is out of reset; if = "1" then device has undergone a soft reset sequence. Cleared by a read.

1. Bit not latched (cleared by any read command).

Table 7. REG_STATUS_1

REG_STATUS_1 (address: 0x04)				
Name	**Bit#**	**R/W**	**Reset state**	**Description**
SPI_ERR(1)	7	R	0	SPI error: if = "0" then SPI format data is compliant with specifications (correct behavior); if = "1" then SPI format data is not complaint with specifications (wrong behavior).
EEPROM_ERR	6	R	0	EEPROM Error: CRC error reading EEPROM. if = "0" EEPROM reading is correct. if = "1" EEPROM reading is wrong. The bit can be cleared by a READ if NVM bit ErrFlgCfg='1'. If ErrFlgCfg='0', then this bit can't be cleared.
Not used	5:4	R	0	"0" always
OFF_CANC_CHY_ERR	3	R	0	The sensor sets this flag when the offset is outside the offset monitoring threshold (±1020 LSB) during slow offset cancellation for channel Y; this also creates hardware failure. When the offset is within the threshold, the flag will be '0' (not latched)
OFF_CANC_CHX_ERR	2	R	0	The sensor sets this flag when the offset is outside the offset monitoring threshold (±1020 LSB) during slow offset cancellation for channel X; this also creates hardware failure. When the offset is within the threshold, the flag will be '0' (not latched)
REG_CONFIG_WR_ERR(1)	1	R	0	Configuration register writing operation error: if = "0" then a writing operation is not addressed by the SPI on REG_CONFIG register when END_OF_INIT=1 (correct behavior); if = "1" then a writing operation is addressed by the SPI on REG_CONFIG register when END_OF_INIT=1 (wrong behavior).
REG_CTRL_1_WR_ERR(1)	0	R	0	Control register 1 writing operation error: if = "0" then a writing operation is not addressed by the SPI on REG_CNTR_1 register when END_OF_INIT=1 (correct behavior); if = "1" then a writing operation is addressed by the SPI on REG_CNTR_1 register when END_OF_INIT=1 (wrong behavior).

1. Bit not latched (cleared by any read command).

Table 8. REG_STATUS_2

REG_STATUS_2 (address: 0x05)				
Name	**Bit#**	**R/W**	**Reset state**	**Description**
A2D_SAT_CHY	7	R	0	if = "1" then CHY ADC saturation detected (wrong behavior).
A2D_SAT_CHX	6	R	0	if = "1" then CHY ADC saturation detected (wrong behavior).
Not used	5	R	0	
CHARGE_PUMP_ERR	4	R	0	Charge pump error: if = "0" then charge pump error is not detected (correct behavior); if = "1" charge pump error is detected (wrong behavior).
VREG_LOW_VOLT_DET	3	R	0	VREG low-voltage detection: if = "0" then regulated voltage VREG is over the minimum supply voltage (correct behavior); = "1" then regulated voltage VREG is under the minimum supply voltage (wrong behavior). This also creates hardware failure (not latched).
VREG_HIGH_VOLT_DET	2	R	0	VREG high-voltage detection: if = "0" then regulated voltage VREG is under the maximum supply voltage (correct behavior); if = "1" then regulated voltage VREG is over the maximum supply voltage (wrong behavior). This also creates hardware failure (not latched).
VDD_LOW_VOLT_DET	1	R	0	VDD low-voltage detection: if = "0" then supply voltage VDD is over the minimum supply voltage (correct behavior); if = "1" then supply voltage VDD is under the minimum supply voltage (wrong behavior). This also creates hardware failure (not latched).
VDD_HIGH_VOLT_DET	0	R	0	VDD high-voltage detection: if = "0" then supply voltage VDD is under the maximum supply voltage (correct behavior); if = "1" then supply voltage VDD is over the maximum supply voltage (wrong behavior). This also creates hardware failure (not latched).

2.5 REG_CHID_REVID

Table 9. REG_CHID_REVID

REG_CHID_REVID (address: 0x06)				
Name	**Bit#**	**R/W**	**Reset state**	**Description**
Not used	7	R	0	
Not used	6	R	0	
CHY_ACTIVE	5	R	0	= “1”: CHY reading chain enabled (copied NVM bit)
CHX_ACTIVE	4	R	0	= “1”: CHX reading chain enabled (copied NVM bit)
Not used	3	R	0	
REVID	[2:0]	R	0	Copied NVM bits 0x7C: bit 7 to bit 5 011 for A3 100 for A4

2.6 REG_ACC_CHX_LOW

Table 10. REG_ACC_CHX_LOW

REG_ACC_CHX_LOW (address: 0x07)				
Name	**Bit#**	**R/W**	**Reset state**	**Description**
REG_ACC_CHX	[7:0]	R	0x00	Channel X acceleration data LSBs register

2.7 REG_ACC_CHX_HIGH

Table 11. REG_ACC_CHX_HIGH

REG_ACC_CHX_HIGH (address: 0x08)				
Name	**Bit#**	**R/W**	**Reset state**	**Description**
AccelDataXLatch	7	R	0	Reading REG_ACC_CHX_LOW register sets the bit to '1' and REG_ACC_CHX_HIGH is locked to its corresponding LOW byte i.e REG_ACC_CHX_LOW; Cleared when it is read.
Not used	6	R	0	
REG_ACC_CHX	[5:0]	R	0	Channel X acceleration data MSBs register