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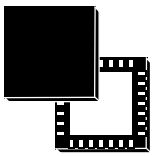
AIS326DQ

MEMS inertial sensor
3-axis, low g accelerometer with digital output

Features

- 3.3 V single supply operation
- 1.8 V compatible IOs
- SPI digital output interface
- 12 bit resolution
- Interrupt activated by motion
- Programmable interrupt threshold
- Embedded self-test
- High shock survivability
- ECOPACK® compliant
- Extended temperature range -40 °C to +105 °C



QFPN-28

Applications

- Anti-theft systems and inertial navigation
- Motion activated functions
- Vibration monitoring and compensation
- Tilt measurements
- Black boxes, event recorders

Description

The AIS326DQ is a three axes digital output accelerometer that includes a sensing element and an IC interface able to take the information from the sensing element and to provide the measured acceleration signals to the external world through an SPI serial interface. I^2C compatible interface is also available.

The sensing element, capable of detecting the acceleration, is manufactured using a dedicated process developed by ST to produce inertial sensors and actuators in silicon.

The IC interface instead is manufactured using a CMOS process that allows high level of integration to design a dedicated circuit which is factory trimmed to better match the sensing element characteristics.

The AIS326DQ has a user selectable full scale of ±2 *g*, ±6 *g* and it is capable of measuring acceleration over a bandwidth of 640 Hz for all axes. The device bandwidth may be selected accordingly to the application requirements. The self-test capability allows the user to check the functioning of the system.

The device is available in plastic quad flat package no lead surface mount (QFPN) and it is specified over a temperature range extending from -40 °C to +105 °C.

Table 1. Device summary

Order code	Operating temperature range [° C]	Package	Packing
AIS326DQ	-40 to +105	QFPN-28	Tray
AIS326DQTR	-40 to +105	QFPN-28	Tape and reel

Contents

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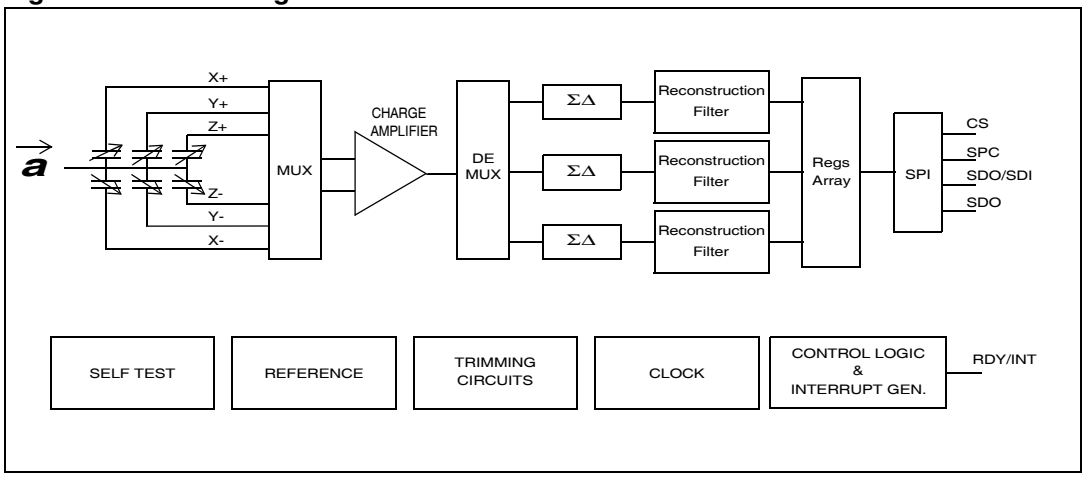
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 QFPN-28 pin description

Figure 2. Pin connection

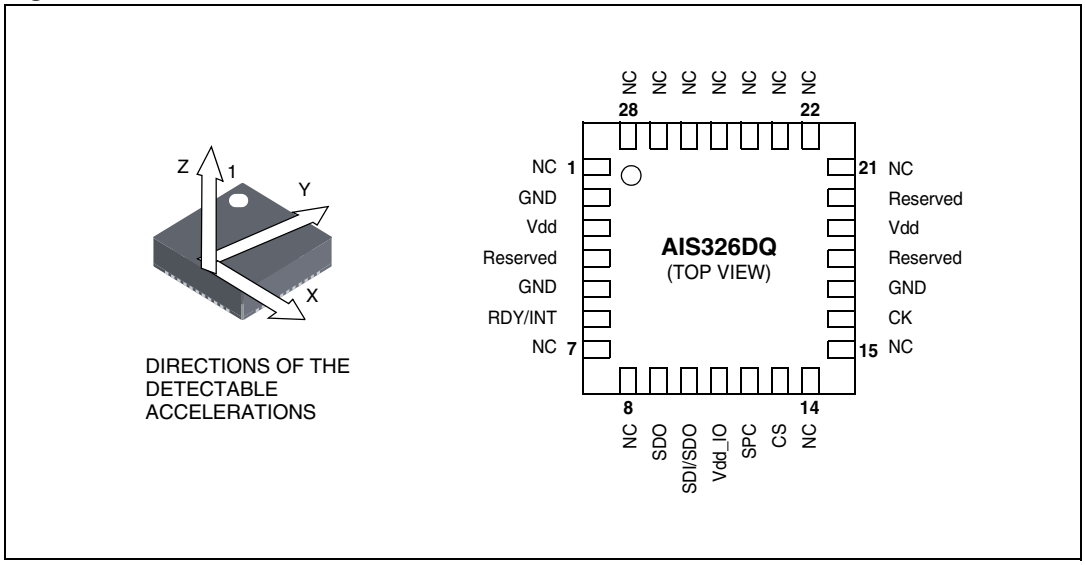


Table 2. Pin description

Pin#	Name	Function
1	NC	Internally not connected
2	GND	0 V supply
3	Vdd	Power supply
4	Reserved	Either leave unconnected or connect to GND
5	GND	0 V supply
6	RDY/INT	Data ready/inertial wake-up and free-fall interrupt
7, 8	NC	Internally not connected
9	SDO	SPI serial data output
10	SDI/ SDO	SPI serial data input (SDI) 3-wire interface serial data output (SDO)
11	Vdd_IO	Power supply for I/O pads
12	SPC	SPI serial port clock
13	CS	Chip select (logic 0: SPI enabled, logic 1: SPI disabled)
14, 15	NC	Internally not connected
16	CK	Optional external clock, if not used either leave unconnected or connect to GND
17	GND	0 V supply
18	Reserved	Either leave unconnected or connect to Vdd_IO
19	Vdd	Power supply
20	Reserved	Connect to Vdd
21 - 28	NC	Internally not connected

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

Table 3. Mechanical characteristics @ Vdd = 3.3 V, T = -40 °C to 105 °C unless otherwise noted(1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
FS	Measurement range(3)	FS bit set to 0	±1.7	±2.0		g
		FS bit set to 1	±5.3	±6.0		
Dres	Device resolution	Full-scale = ±2 *g* T = 25 °C, ODR1=40 Hz		1.0		mg
		Full-scale = ±2 *g* T = 25 °C, ODR2=160 Hz		2.0		
		Full-scale = ±2 *g* T = 25 °C, ODR3 = 640 Hz		3.9		
		Full-scale = ±2 *g* T = 25 °C, ODR4 = 2560 Hz		15.6		
So	Sensitivity	Full-scale = ±2 *g* 12 bit representation	952	1024	1096	LSb/g
		Full-scale = ±6 *g* 12 bit representation(4)	316	340	364	
TCSo	Sensitivity change vs temperature	Full-scale = ±2 *g* 12 bit representation		0.025		%/°C
Off	Zero-g level offset accuracy(5),(6)	Full-scale = ±2 *g* X, Y axis	-100		100	mg
		Full-scale = ±2 *g* Z axis	-200		200	
		Full-scale = ±6 *g* X, Y axis(4)	-100		100	
		Full-scale = ±6 *g* Z axis(4)	-200		200	
TCOff	Zero-g level change vs temperature	Max delta from 25 °C		0.2		mg/°C
NL	Non linearity(4)	Best fit straight line X, Y axis Full-scale = ±2 *g* ODR = 40 Hz		±2		% FS
		Best fit straight line Z axis Full-scale = ±2 *g* ODR = 40 Hz		±3		
CrAx	Cross axis(4)		-5		5	%

Table 3. Mechanical characteristics @ Vdd = 3.3 V, T = -40 °C to 105 °C unless otherwise noted(1) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
V_{st}	Self-test output change(7),(8)	Full-scale= ±2 *g* X axis	200	460	750	LSb
		Full-scale= ±2 *g* Y axis	200	460	750	
		Full-scale= ±2 *g* Z axis	140	360	580	
		Full-scale= ±6 *g* X axis	60	160	260	LSb
		Full-scale= ±6 *g* Y axis	60	160	260	
		Full-scale= ±6 *g* Z axis	45	120	200	
BW	System bandwidth(9)			ODRx/4		Hz
T_{OP}	Operating temperature range		-40		+105	°C
Wh	Product weight			0.2		gram

1. The product is factory calibrated at 3.3 V. Operation over 3.6 V is not recommended
2. Typical specifications are not guaranteed
3. Verified by wafer level test and specification of initial offset and sensitivity
4. Guaranteed by design
5. Zero-g level offset value after MSL3 preconditioning
6. Offset can be eliminated by enabling the built-in high pass filter (HPF)
7. Self test output changes with the power supply. “Self-test output change” is defined as $OUTPUT[LSb]_{(Self\text{-}test\ bit\ on\ CTRL\_REG1=1)} - OUTPUT[LSb]_{(Self\text{-}test\ bit\ on\ CTRL\_REG1=0)}$. 1LSb = 1g/1024 at 12 bit representation, 2 g Full-scale
8. Output data reach 99% of final value after 5/ODR when enabling Self-test mode due to device filtering
9. ODRx is output data rate. Refer to *Table 4* for specifications

2.2 Electrical characteristics

Table 4. Electrical characteristics @ Vdd=3.3 V, T = -40 °C to 105 °C unless otherwise noted(1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		3.0	3.3	3.6	V
Vdd_IO	I/O pads supply voltage(3)		1.71		Vdd	V
Idd	Supply current	Vdd = 3.3 V		0.67	0.80	mA
IddPdn	Current consumption in power-down mode			2	20	µA
VIH	Digital high level Input voltage(3)		0.8*Vdd_IO			V
VIL	Digital low level Input voltage(3)				0.2*Vdd_IO	
VOH	High level output voltage(3)		0.9*Vdd_IO			V
VOL	Low level output voltage(3)				0.1*Vdd_IO	
ODR1	Output data rate 1	Dec factor = 512		40		Hz
ODR2	Output data rate 2	Dec factor = 128		160		
ODR3	Output data rate 3	Dec factor = 32		640		
ODR4	Output data rate 4	Dec factor = 8		2560		
BW	System bandwidth(4)			ODRx/4		Hz
Ton	Turn-on time(5)			5/ODRx		s
T_{OP}	Operating temperature range		-40		+105	°C

1. The product is factory calibrated at 3.3 V. Operation over 3.6 V is not recommended
2. Typical specifications are not guaranteed
3. Guaranteed by design
4. Digital filter -3 dB frequency
5. Time to obtain valid data after exiting power-down mode

2.3 Communication interface characteristics

2.3.1 SPI - serial peripheral interface

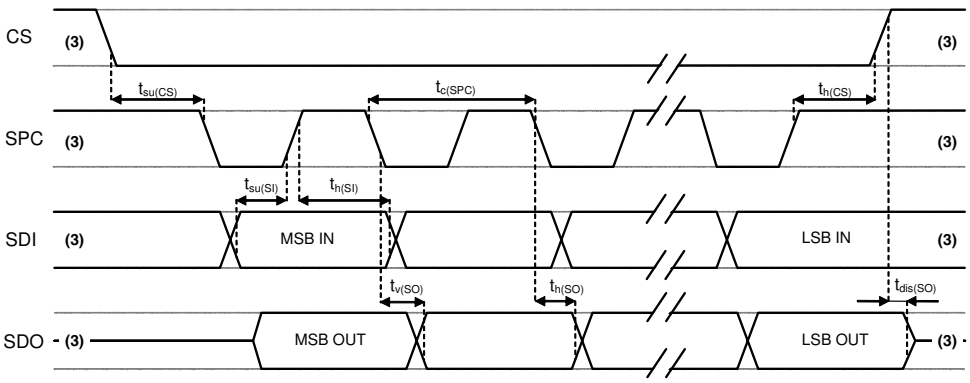
Subject to general operating conditions for Vdd and T_{OP}

Table 5. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
tc(SPC)	SPI clock cycle	125		ns
fc(SPC)	SPI clock frequency		8	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	10		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		55	
th(SO)	SDO output hold time	7		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 8 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 3. SPI slave timing diagram (2)



2. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output port
3. When no communication is on-going, data on CS, SPC, SDI and SDO are driven by internal pull-up resistors

2.4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage(1)	-0.3 to 6.0	V
Vdd_IO	I/O pins supply voltage(1)	-0.3 to Vdd +0.1	V
Vin	Input voltage on any control pin(1) (CS, SPC, SDI/SDO, SDO, CK)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 3.3 V)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
A_{UNP}	Acceleration (any axis, unpowered)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
T_{OP}	Operating temperature range	-40 to +105	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	4.0 (HBM)	kV
		200 (MM)	V
		1.5 (CDM)	kV

1. Supply voltage on any pin should never exceed 6.0 V.

This is a mechanical shock sensitive device, improper handling can cause permanent damages to the part.

This is an ESD sensitive device, improper handling can cause permanent damages to the part.

2.5 Terminology

2.5.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (point to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also very little over time. The Sensitivity tolerance describes the range of sensitivities of a large population of sensors.

2.5.2 Zero-g level

Zero-*g* level offset (Off) describes the deviation of an actual output signal from the ideal output signal if there is no acceleration present. A sensor in a steady state on a horizontal surface will measure 0 *g* in X axis and 0 g in Y axis whereas the Z axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, 00h with 16 bit representation, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to a precise MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level of an individual sensor is stable over lifetime. The Zero-*g* level tolerance describes the range of Zero-*g* levels of a population of sensors.

2.5.3 Self test

Self test allows to test the mechanical and electric part of the sensor, allowing the seismic mass to be moved by means of an electrostatic test-force. The self-test function is off when the self-test bit of CTRL_REG1 (control register 1) is programmed to '0'. When the self-test bit of CTRL_REG1 is programmed to '1'an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which is related to the selected full scale and depending on the Supply Voltage through the device sensitivity. When Self Test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Table 3* or *4* then the sensor is working properly and the parameters of the interface chip are within the defined specification.

3 Functionality

The AIS326DQ is a high performance, low-power, digital output 3-axes linear accelerometer packaged in a QFN package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and to provide a signal to the external world through an SPI serial interface.

3.1 Sensing element

A proprietary process is used to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the moulding phase of the plastic encapsulation.

When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor.

At steady state the nominal value of the capacitors are few pF and when an acceleration is applied the maximum variation of the capacitive load is up to 100 pF.

3.2 IC interface

The complete measurement chain is composed by a low-noise capacitive amplifier which converts into an analog voltage the capacitive unbalancing of the MEMS sensor and by three $\Sigma\Delta$ analog-to-digital converters, one for each axis, that translate the produced signal into a digital bitstream.

The $\Sigma\Delta$ converters are coupled with dedicated reconstruction filters which remove the high frequency components of the quantization noise and provide low rate and high resolution digital words.

The charge amplifier and the $\Sigma\Delta$ converters are operated respectively at 61.5 kHz and 20.5 kHz.

The data rate at the output of the reconstruction depends on the user selected decimation factor (DF) and spans from 40 Hz to 2560 Hz.

The acceleration data may be accessed through an SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The AIS326DQ features a data-ready signal (RDY) which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in digital system employing the device itself.

The AIS326DQ may also be configured to generate an inertial wake-up, direction detection and free-fall interrupt signal accordingly to a programmed acceleration event along the enabled axes.

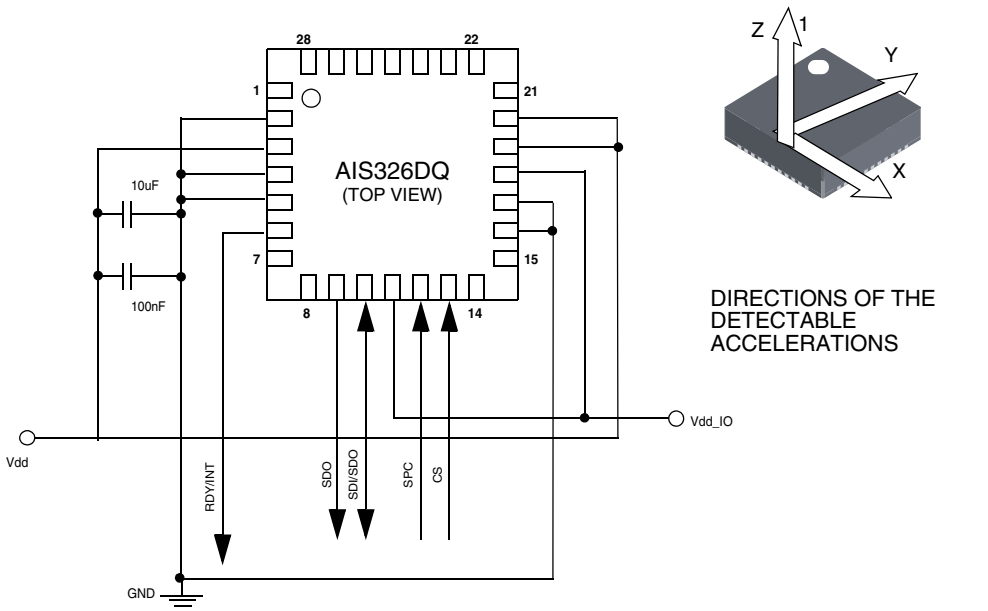
3.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-*g* level (Off).

The trimming values are stored inside the device by a non volatile structure. Any time the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation. This allows the user to employ the device without further calibration.

4 Application hints

Figure 4. AIS326DQ electrical connection



The device core is supplied through Vdd line while the I/O pads are supplied through Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF Al) should be placed as near as possible to the pin 3 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 4*). It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses. In this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data is selectable and accessible through the SPI interface. The design of the application board should take in consideration that the AIS326DQ is equipped also with an I2C compatible interface that it is activated when the signal on CS pin is high (logic:1).

The functions, the thresholds and the timing of the interrupt pin (INT) can be completely programmed by the user through the SPI interface.

5 Digital interface

The registers embedded inside the AIS326DQ may be accessed through SPI serial interface. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

Table 7. Serial interface pin description

Pin name	Pin description
CS	Chip select (logic 0: SPI enabled, logic 1: SPI disabled)
SPC	SPI serial port clock
SDI/SDO	SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO	SPI serial data output (SDO)

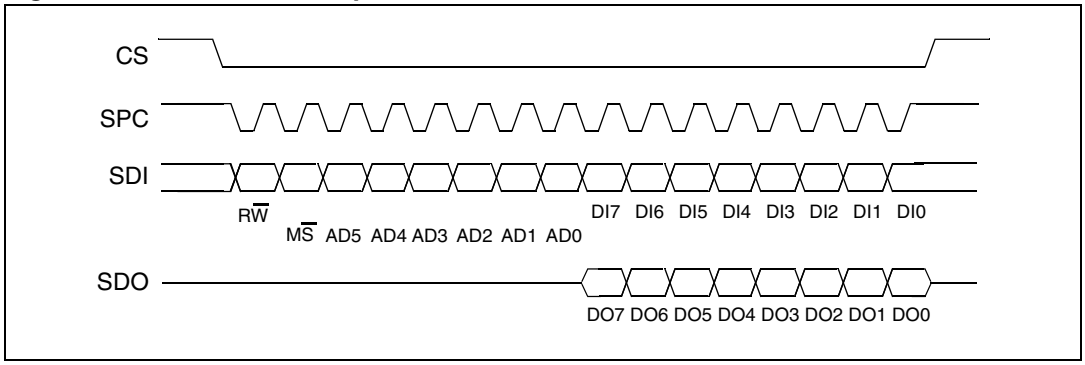
The embedded registers may be accessed also through an I^2C interface. For I^2C operation refer to LIS3LV02DQ datasheet or contact ST technical support.

5.1 SPI bus interface

The AIS326DQ SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 5. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end.

SPC is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission).

SDI and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple byte read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge

of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto increased in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written into the device (MSb first).

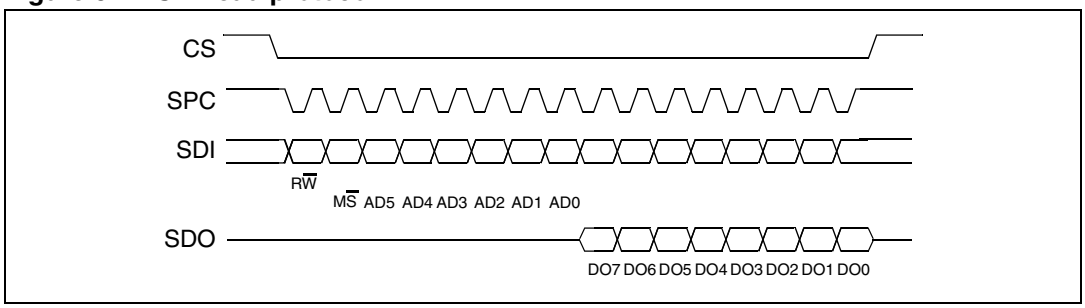
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When M$\overline{S}$ bit is 0 the address used to read/write data remains the same for every block. When M$\overline{S}$ bit is '1' the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.1.1 SPI Read

Figure 6. SPI read protocol



The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

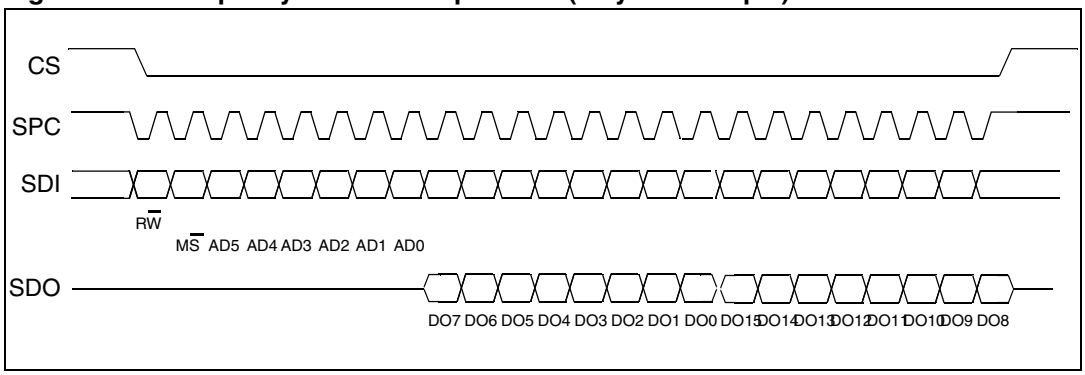
bit 1: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

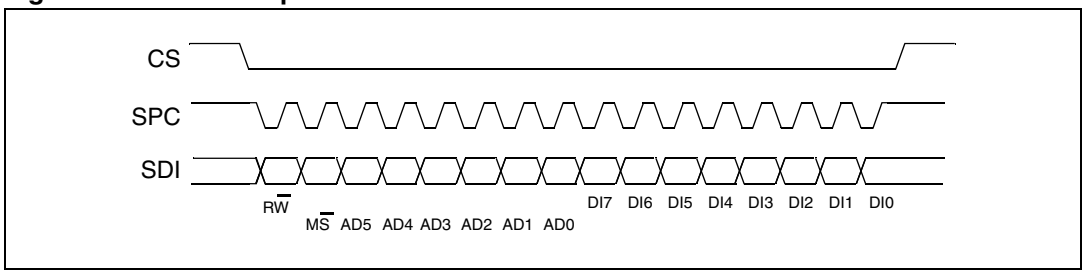
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 7. Multiple bytes SPI read protocol (2 bytes example)



5.1.2 SPI Write

Figure 8. SPI Write protocol



The SPI Write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

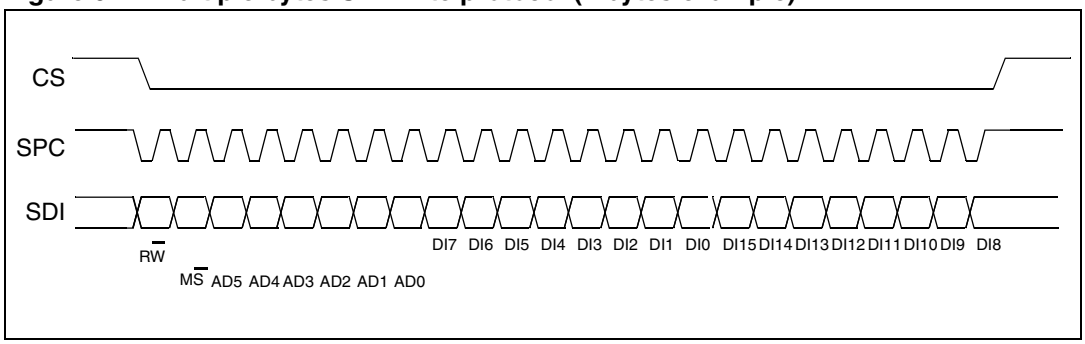
bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writing.

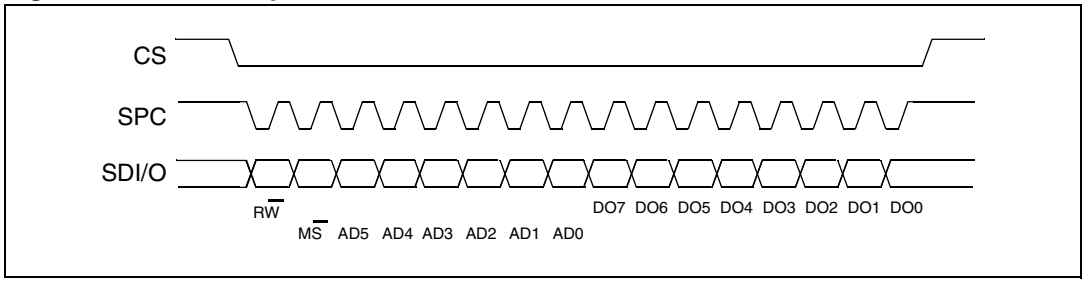
Figure 9. Multiple bytes SPI write protocol (2 bytes example)



5.1.3 SPI Read in 3-wires mode

3-wires mode is entered by setting to '1' bit SIM (SPI serial interface mode selection) in CTRL_REG2.

Figure 10. SPI read protocol in 3-wires mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

6 Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related address.

Table 8. Registers address map

Register name	Type	Register address		Default	Comment
		Binary	Hex		
	rw	0000000 - 0001110	00 - 0E		Reserved
WHO_AM_I	r	0001111	0F	00111010	Dummy register
	rw	0010000 - 0010101	10 - 15		Reserved
OFFSET_X	rw	0010110	16	Calibration	Loaded at boot
OFFSET_Y	rw	0010111	17	Calibration	Loaded at boot
OFFSET_Z	rw	0011000	18	Calibration	Loaded at boot
GAIN_X	rw	0011001	19	Calibration	Loaded at boot
GAIN_Y	rw	0011010	1A	Calibration	Loaded at boot
GAIN_Z	rw	0011011	1B	Calibration	Loaded at boot
		0011100 -0011111	1C-1F		Reserved
CTRL_REG1	rw	0100000	20	00000111	
CTRL_REG2	rw	0100001	21	00000000	
CTRL_REG3	rw	0100010	22	00001000	
HP_FILTER RESET	r	0100011	23	dummy	Dummy register
		0100100-0100110	24-26		Not used
STATUS_REG	rw	0100111	27	00000000	
OUTX_L	r	0101000	28	output	
OUTX_H	r	0101001	29	output	
OUTY_L	r	0101010	2A	output	
OUTY_H	r	0101011	2B	output	
OUTZ_L	r	0101100	2C	output	
OUTZ_H	r	0101101	2D	output	
	r	0101110	2E		Reserved
		0101111	2F		Not used
FF_WU_CFG	rw	0110000	30	00000000	
FF_WU_SRC	rw	0110001	31	00000000	
FF_WU_ACK	r	0110010	32	dummy	Dummy register
		0110011	33		Not used
FF_WU_THS_L	rw	0110100	34	00000000	

Table 8. Registers address map (continued)

Register name	Type	Register address		Default	Comment
		Binary	Hex		
FF_WU_THS_H	rw	0110101	35	00000000	
FF_WU_DURATION	rw	0110110	36	00000000	
		0110111	37		Not used
DD_CFG	rw	0111000	38	00000000	
DD_SRC	rw	0111001	39	00000000	
DD_ACK	r	0111010	3A	dummy	Dummy register
		0111011	3B		Not used
DD_THSI_L	rw	0111100	3C	00000000	
DD_THSI_H	rw	0111101	3D	00000000	
DD_THSE_L	rw	0111110	3E	00000000	
DD_THSE_H	rw	0111111	3F	00000000	
		1000000-1111111	40-7F		Reserved

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The registers *7.2* to *7.7* contain the factory calibration values, it is not necessary to change their value for normal device operation.

7.1 WHO_AM_I (0Fh)

Table 9. Register

W7	W6	W5	W4	W3	W2	W1	W0

Table 10. Register description

W7, W0	AIS326DQ physical address equal to 3Ah

Addressing this register the physical address of the device is returned. For AIS326DQ the physical address assigned in factory is 3Ah.

7.2 OFFSET_X (16h)

Table 11. OFFSET_X register

OX7	OX6	OX5	OX4	OX3	OX2	OX1	OX0

Table 12. OFFSET_X register description

OX7, OX0	Digital offset trimming for X-Axis

7.3 OFFSET_Y (17h)

Table 13. OFFSET_Y register

OY7	OY6	OY5	OY4	OY3	OY2	OY1	OY0

Table 14. OFFSET_Y register description

OY7, OY0	Digital offset trimming for Y-Axis