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AIS328DQ

High-performance ultra low-power 3-axis accelerometer with digital output for automotive applications

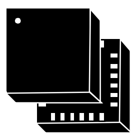
Datasheet — production data

Features

- Wide supply voltage range: 2.4 V to 3.6 V
- Low voltage compatible IOs: 1.8 V
- Ultra low-power mode consumption: down to 10 μA
- ±2*g*/±4*g*/±8*g* dynamically selectable full-scale
- SPI / I²C digital output interface
- 16-bit data output
- 2 independent programmable interrupt generators
- System sleep/wakeup function
- Extended temperature range: -40 °C to 105 °C
- Embedded self-test
- High shock survivability: up to 10000 *g*
- ECOPACK® RoHS and "Green" compliant
- AEC-Q100 qualification

Applications

- Telematics and black boxes
- In-dash car navigation
- Tilt / inclination measurement
- Anti-theft devices
- Intelligent power saving
- Impact recognition and logging
- Vibration monitoring and compensation
- Motion-activated functions



QFN 24 (4 x 4 x 1.8 mm^3)

Description

The AIS328DQ is an ultra low-power high performance 3-axis linear accelerometer with a digital serial interface SPI standard output. An I²C compatible interface is also available. The device features ultra low-power operational modes that allow advanced power saving and smart sleep-to-wakeup functions. The AIS328DQ has dynamic user-selectable full-scales of ±2*g*/±4*g*/±8*g* and is capable of measuring accelerations with output data rates from 0.5 Hz to 1 kHz. The self-test capability allows the user to check the functioning of the sensor in the final application. The device may be configured to generate an interrupt signal through inertial wakeup events, or by the position of the device itself. Thresholds and the timing of interrupt generators are programmable by the end user on-the-fly. Available in a small quad flat pack no-lead package (QFPN) with a 4x4 mm footprint, the AIS328DQ is able to respond to the trend towards application miniaturization, and is guaranteed to operate over a temperature range from -40 °C to +105 °C.

Table 1. Device summary

Order codes	Temperature range [° C]	Package	Packaging
AIS328DQ	-40 to +105	QFPN 4x4x1.8 24L	Tray
AIS328DQTR	-40 to +105	QFPN 4x4x1.8 24L	Tape and reel

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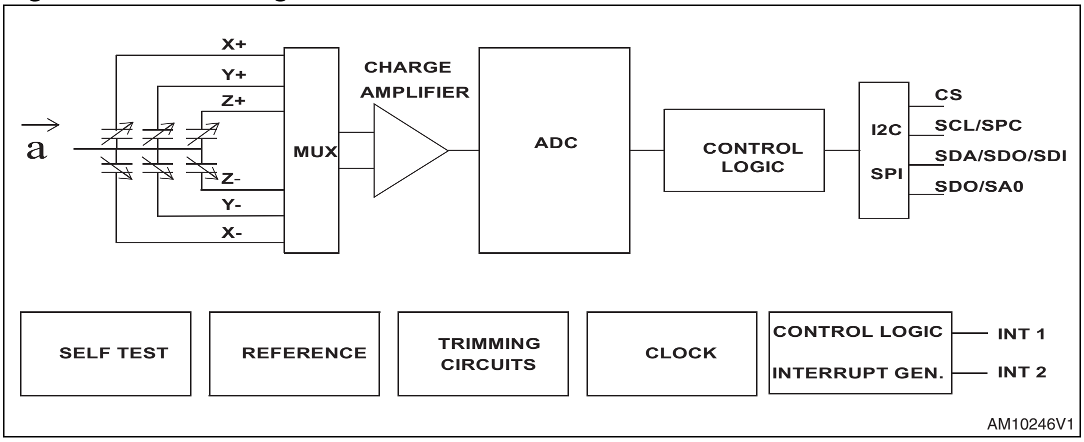
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Detectable accelerations and pin indicator

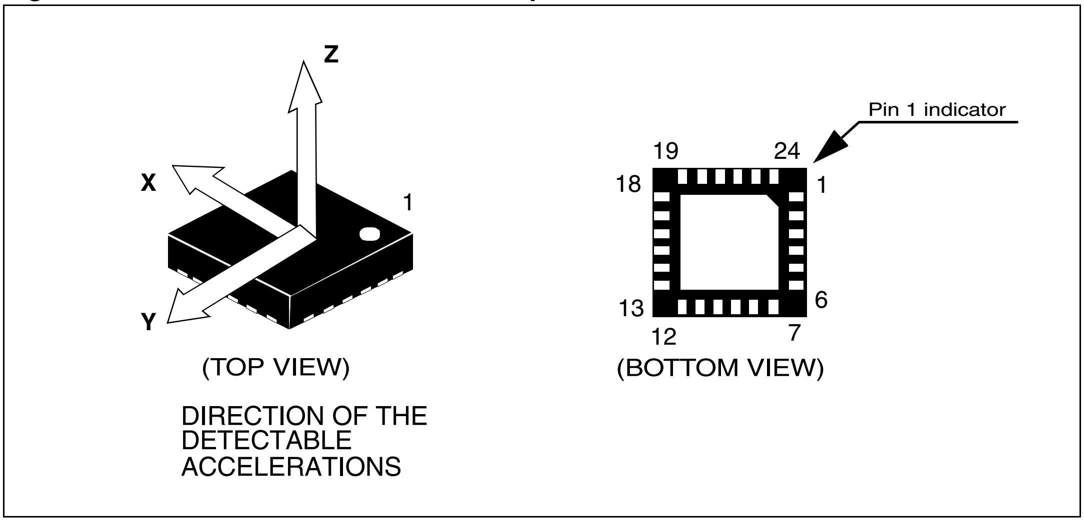


Table 2. Pin description

Pin#	Name	Function
1,2	NC	Not connected
3	INT_2	Inertial interrupt 2
4	Reserved	Connect to GND
5	VDD	Power supply
6	GND	0 V supply
7	INT_1	Inertial interrupt 1
8	GND	0 V supply
9	GND	0 V supply
10	GND	0 V supply
11	SPC SCL	SPI serial port clock (SPC) I²C serial clock (SCL) Internal active pull-up
12	CS	SPI enable I²C/SPI mode selection (0: SPI enabled; 1: I²C mode) Internal active pull-up
13	Reserved	Connect to Vdd
14	VDD_IO	Power supply for I/O pins
15	SDO SA0	SPI serial data output (SDO) I²C less significant bit of the device address (SA0) Internal active pull-up
16	SDI SDO SDA	SPI serial data input (SDI) 3-wire interface serial data output (SDO) I²C serial data (SDA) Internal active pull-up
17-24	NC	Not internally connected

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd=3.3 V, T=-40 °C to +105 °C unless otherwise noted[a].

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
FS	Measurement range[2]	FS bit set to 00		±2.0		*g*
		FS bit set to 01		±4.0		
		FS bit set to 11		±8.0		
So	Sensitivity	FS bit set to 00 12-bit representation	0.90	0.98	1.06	m*g*/digit
		FS bit set to 01 12-bit representation	1.81	1.95	2.12	
		FS bit set to 11 12-bit representation	3.62	3.91	4.25	
Off	Zero-*g* level offset accuracy[3],[4],[5]	X,Y axes	-200		200	m*g*
		Z-axis	-300		300	
TyOff	Typical zero-*g* level offset accuracy[5],[6]	FS bit set to 00	-30	±20	30	m*g*
TCOff	Zero-*g* level change vs. temperature	Excursion from 25 °C (X, Y axes)	-2	±0.2	2	m*g*/°C
		Excursion from 25 °C (Z-axis)	-3	±0.8	3	
An	Acceleration noise density	FS bit set to 00	100	218	600	μ*g*/√Hz
CrAx	Cross-axis[7]		-5		+5	%
Vst	Self-test output change[8],[9],[10]	FS bit set to 00 X-axis	-500	-800	-1100	LSb
		FS bit set to 00 Y-axis	500	800	1100	LSb
		FS bit set to 00 Z-axis	400	600	800	LSb
Wh	Product weight			60		mgram
Top	Operating temperature range		-40		+105	°C

1. Typical values are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Zero-*g* level offset value after MSL3 preconditioning.
4. Zero-*g* level offset at the FS bit set to 01 and 11 is guaranteed by design.

a. The product is factory calibrated at 3.3 V. Operational power supply (Vdd) over 3.6 V is not recommended.

5. Offset can be eliminated by enabling the built-in high-pass filter.
6. Typical zero-*g* level offset as per factory calibration @ T = 25 °C.
7. Guaranteed by design.
8. The sign of "Self-test output change" is defined by a sign bit, for all axes. Values in *Table 3* are defined with the STsign bit in the CTRL_REG4 register equal to logic "0" (positive self-test), at T = 25 °C.
9. Self-test output changes with the power supply. "Self-test output change" is defined as $OUTPUT[LSb]_{(CTRL\_REG4\ ST\ bit=1)}$ - $OUTPUT[LSb]_{(CTRL\_REG4\ ST\ bit=0)}$. 1LSb=4*g*/4096 at 12-bit representation, ±2 *g* full-scale.
10. Output data reaches 99% of final value after 3/ODR when enabling self-test mode, due to device filtering.

2.2 Electrical characteristics

@ Vdd = 3.3 V, T = -40 °C to +105 °C unless otherwise noted[b].

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ[1].	Max.	Unit
Vdd	Supply voltage		2.4	3.3	3.6	V
Vdd_IO	I/O pins supply voltage[2]		1.8		Vdd+0.1	V
Idd	Current consumption in normal mode	2.4 V to 3.6 V	200		450	µA
IddLP	Current consumption in low-power mode	ODR=1 Hz, BW=500 Hz, T=25 °C	8	10	12	µA
IddPdn	Current consumption in power-down mode		0.1	1	2	µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
VOH	High level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
ODR	Output data rate in normal mode	DR bit set to 00		50		Hz
		DR bit set to 01		100		
		DR bit set to 10		400		
		DR bit set to 11		1000		
ODR_{LP}	Output data rate in low-power mode	PM bit set to 010		0.5		Hz
		PM bit set to 011		1		
		PM bit set to 100		2		
		PM bit set to 101		5		
		PM bit set to 110		10		

b. The product is factory calibrated at 3.3 V. Operational power supply (Vdd) over 3.6 V is not recommended.

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ[(1)].	Max.	Unit
BW	System bandwidth			ODR/2		Hz
Ton	Turn-on time[(3)]	ODR = 100 Hz	0.9/ODR +1 ms	1/ODR+1 ms	1.1/ODR +1 ms	s
Top	Operating temperature range		-40		+105	°C

1. Typical values are not guaranteed.
2. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses; in this condition the measurement chain is powered off.
3. Time to obtain valid data after exiting power-down mode.

2.3 Communication interface characteristics

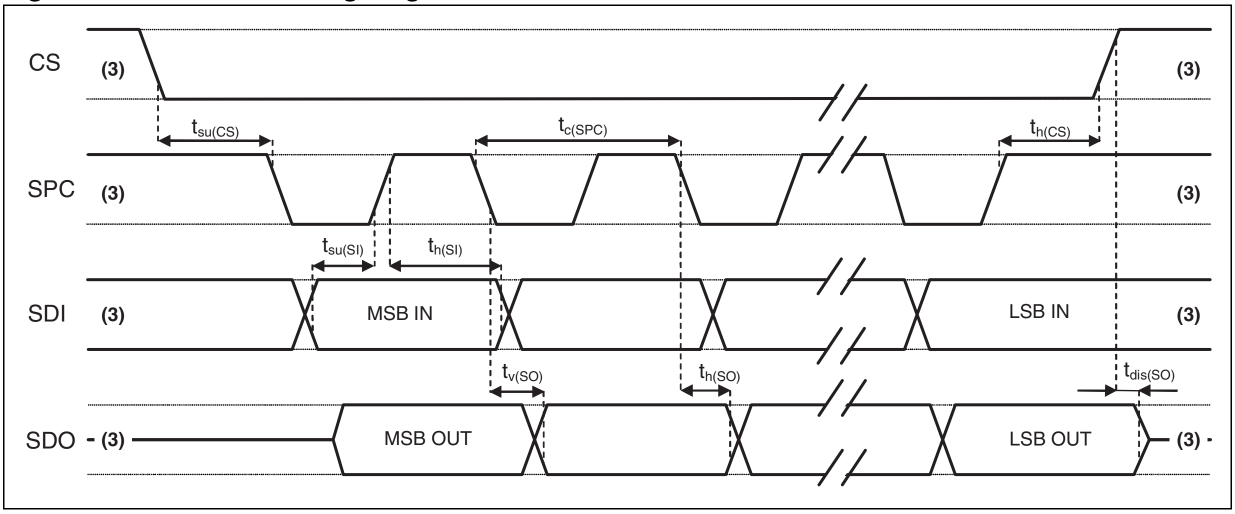
2.3.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top.

Table 5. SPI slave timing values

Symbol	Parameter	Value [(1)]		Unit
		Min.	Max.	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	6		ns
th(CS)	CS hold time	8		ns
tsu(SI)	SDI input setup time	5		ns
th(SI)	SDI input hold time	15		ns
tv(SO)	SDO valid output time		50	ns
th(SO)	SDO output hold time	9		ns
tdis(SO)	SDO output disable time		50	ns

Figure 3. SPI slave timing diagram (2)



1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.
2. Measurement points are made at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.
3. When no communication is ongoing, data on CS, SPC, SDI and SDO are driven by internal pull-up resistors.

2.3.2 I²C - inter IC control interface

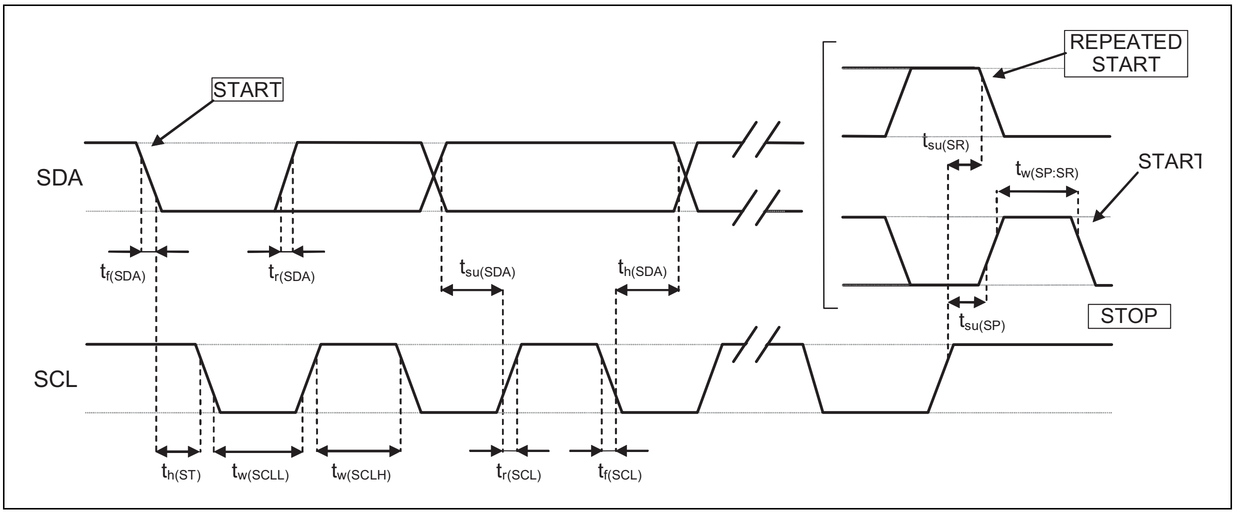
Subject to general operating conditions for Vdd and top.

Table 6. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	KHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	μs
$t_{h(ST)}$	START condition hold time	4		0.6		μs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram [c]



2.4 Absolute maximum ratings

Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4	V
Vdd_IO	I/O pin supply voltage	-0.3 to 4	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)(1)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
A_{UNP}	Acceleration (any axis, unpowered)(1)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
T_{OP}	Operating temperature range	-40 to +105	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	4 (HBM)	kV
		1.5 (CDM)	kV
		200 (MM)	V

c. Measurement points are made at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

1. Design guarantee; characterization done at 1500 *g*/0.5 ms, 3000 *g*/0.3 ms, 10000 *g*/0.1 ms; tests under these conditions have passed successfully.

Note: Supply voltage on any pin should never exceed 4.0 V.

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.

This is an ESD sensitive device, improper handling can cause permanent damage to the part.

2.5 Terminology

2.5.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying a 1 *g* acceleration to it. As the sensor can measure DC accelerations, this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, a ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also over time. The sensitivity tolerance describes the range of sensitivity of a large population of sensors.

2.5.2 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* on the X-axis and 0 *g* on the Y-axis, whereas the Z-axis measures 1 *g*. The output is ideally in the center of the dynamic range of the sensor (the content of the OUT registers is 00h, data expressed as 2’s complement number). A deviation from the ideal value in this case is called zero-*g* offset. Offset is, to some extent, a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see “Zero-*g* level change vs. temperature” in *Table 3*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a population of sensors.

2.5.3 Self-test

Self-test allows the sensor functionality to be tested without moving it. The self-test function is off when the self-test bit (ST) of CTRL_REG4 (control register 4) is programmed to ‘0‘. When the self-test bit of CTRL_REG4 is programmed to ‘1’ an actuation force is applied to the sensor, simulating a definite input acceleration. In this case, the sensor outputs exhibit a change in their DC levels which are related to the selected full-scale through the device sensitivity.

When self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

2.5.4 Sleep-to-wakeup

The “sleep-to-wakeup” function, in conjunction with low-power mode, allows further reduction of system power consumption and development of new smart applications. The AIS328DQ may be set to a low-power operating mode, characterized by lower data rate refreshments. In this way the device, even if sleeping, continues to sense acceleration and to generate interrupt requests.

When the “sleep-to-wakeup” function is activated, the AIS328DQ is able to automatically wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature, the system may be efficiently switched from low-power mode to full-performance depending on user-selectable positioning and acceleration events, therefore ensuring power saving and flexibility.

3 Functionality

The AIS328DQ is a “nano”, low-power, digital output 3-axis linear accelerometer packaged in a QFPN package. The device includes a sensing element and an IC interface capable of taking information from the sensing element and providing a signal to external applications through an I^2C/SPI serial interface.

3.1 Sensing element

A proprietary process is used to create a surface micro-machined accelerometer. The technology makes it possible to construct suspended silicon structures which are attached to the substrate at several points called “anchors”, and are free to move in the direction of the sensed acceleration. To be compatible with traditional packaging techniques, a cap is placed on top of the sensing element to prevent blocking of moving parts during the moulding phase of the plastic encapsulation.

When an acceleration is applied to the sensor, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state, the nominal value of the capacitors are a few pF, and when an acceleration is applied the maximum variation of the capacitive load is in the fF range.

3.2 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage that is made available to the user through an analog-to-digital converter.

The acceleration data may be accessed through an I^2C/SPI interface, therefore making the device particularly suitable for direct interfacing with a microcontroller.

The AIS328DQ features a data-ready signal (RDY) which indicates when a new set of measured acceleration data is available, therefore simplifying data synchronization in the digital system that uses the device.

The AIS328DQ may also be configured to generate an inertial wakeup and free-fall interrupt signal based on a programmed acceleration event along the enabled axes. Both free-fall and wakeup can be available simultaneously on two different pins.

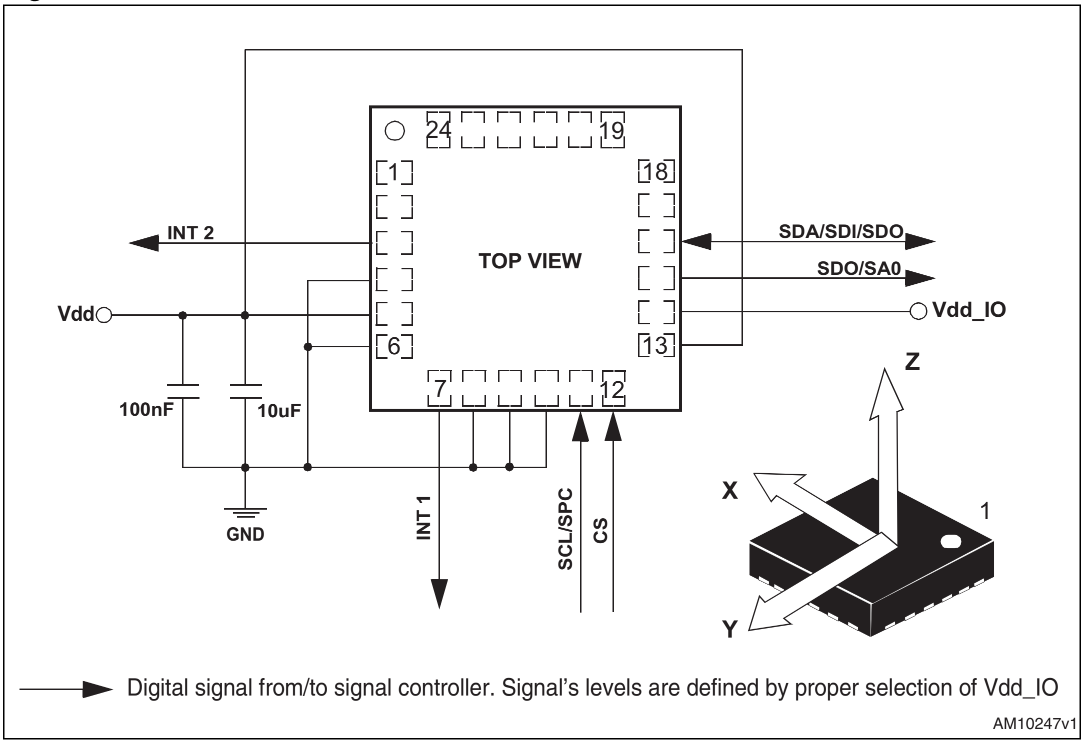
3.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and zero-*g* level (TyOff).

The trimming values are stored inside the device in non-volatile memory. When the device is turned on, the trimming parameters are downloaded into the registers to be used during active operation. This allows the device to be used without further calibration.

4 Application hints

Figure 5. AIS328DQ electrical connections



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 5 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to obtain proper behavior of the IC (refer to *Figure 5*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus; in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data is selectable and accessible through the I²C or SPI interfaces. When using the I²C, CS must be tied high.

The functions, the threshold, and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user through the I²C/SPI interface.

5 Digital interfaces

The registers embedded in the AIS328DQ may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I²C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 8. Serial interface pin description

Pin name	Pin description
CS	SPI enable I²C/SPI mode selection (1: I²C mode; 0: SPI enabled)
SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0 SDO	I²C less significant bit of the device address (SA0) SPI serial data output (SDO)

5.1 I²C serial interface

The AIS328DQ I²C is a bus slave. The I²C is employed to write data into registers, the content of which can also be read back.

The relevant I²C terminology is provided in *Table 9* below.

Table 9. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines are connected to Vdd_IO through a pull-up resistor embedded in the AIS328DQ. When the bus is free, both lines are high.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the AIS328DQ is 001100xb. The **SDO**/**SA0** pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is '1' (address 0011001b), otherwise if the SA0 pad is connected to ground, the LSb value is '0' (address 0011000b). This solution permits the connection and addressing of two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the AIS328DQ behaves like a slave device, and the following protocol must be adhered to. After the start condition (ST) a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSb enables address auto-increment. If the MSb of the SUB field is '1', the SUB (register address) is automatically increased to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit is '1' (read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (write) the master transmits to the slave with direction unchanged. *Table 10* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 10. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. **Transfer when master is receiving (reading) one byte of data from slave**

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. **Transfer when master is receiving (reading) multiple bytes of data from slave**

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

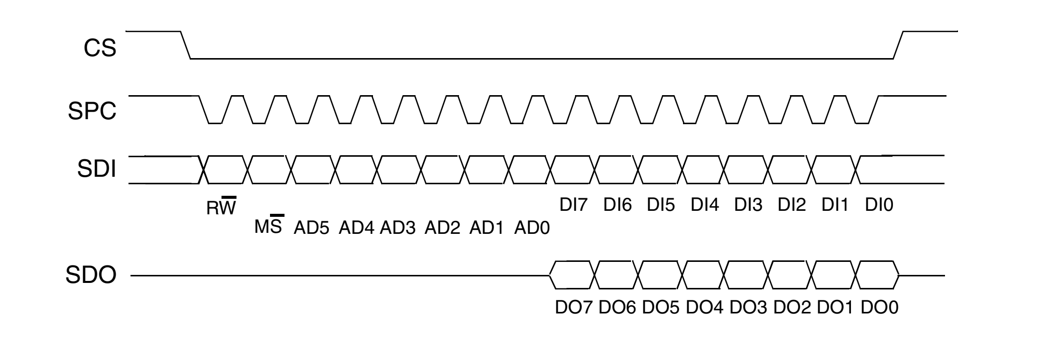
In the presented communication format, MAK is master acknowledge and NMAK is no master acknowledge.

5.2 SPI bus interface

The AIS328DQ SPI is a bus slave. The SPI allows the writing and reading of the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 6. Read and write protocol



CS is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and returns high at the end. **SPC** is the serial port clock and is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in cases of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC**, after the falling edge of **CS,** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC, just before the rising edge of **CS**.

bit 0: $R\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1: $M\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

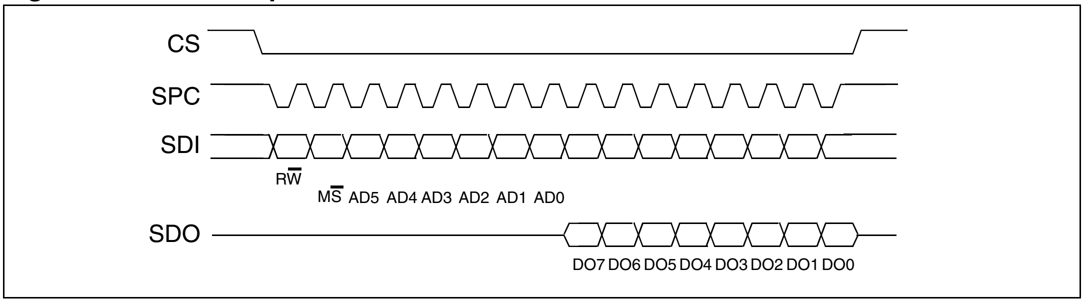
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When $M\overline{S}$ bit is ‘0’ the address used to read/write data remains the same for every block. When $M\overline{S}$ bit is ‘1’ the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 7. SPI read protocol



The SPI read command is performed with 16 clock pulses. Multiple byte read commands are performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

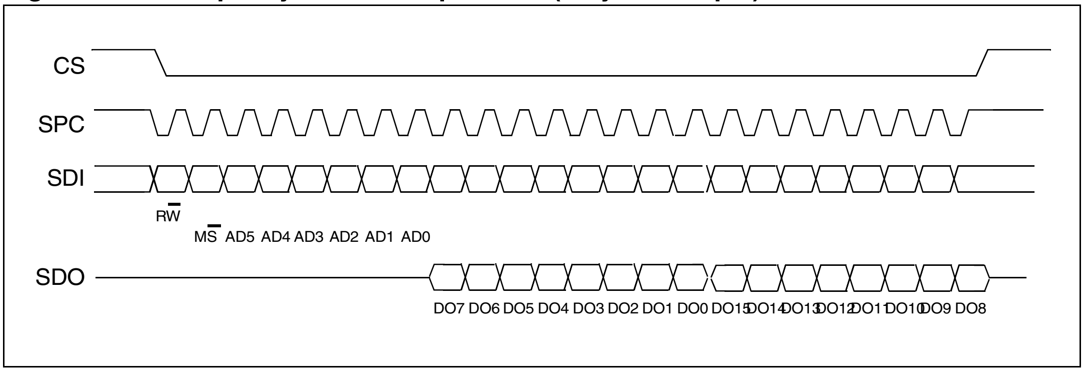
bit 1: $M\overline{S}$ bit. When 0, do not increment address; when 1, increment address in multiple readings.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

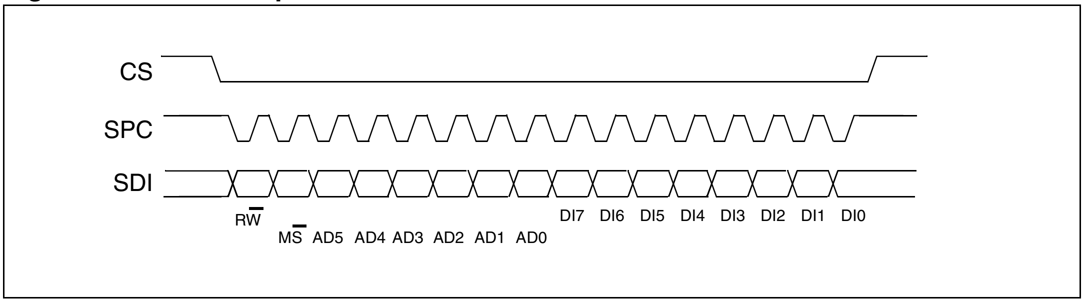
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 8. Multiple byte SPI read protocol (2-byte example)



5.2.2 SPI write

Figure 9. SPI write protocol



The SPI write command is performed with 16 clock pulses. Multiple byte write commands are performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

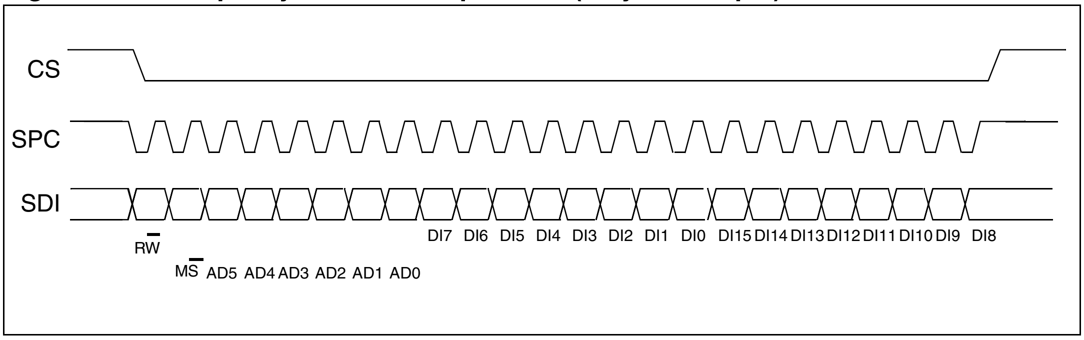
bit 1: MS bit. When 0, do not increment address; when 1, increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writing.

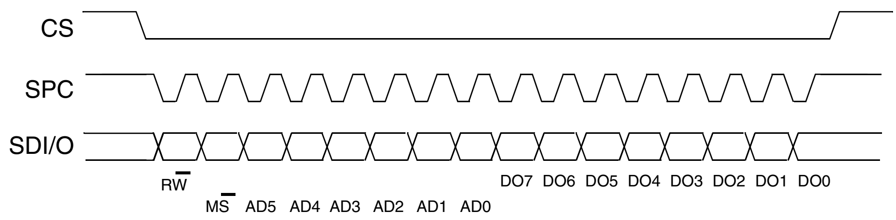
Figure 10. Multiple bytes SPI write protocol (2-byte example)



5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting to '1' the bit SIM (SPI serial interface mode selection) in CTRL_REG4.

Figure 11. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: $M\overline{S}$ bit. When 0, do not increment address; when 1, increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

Multiple read command is also available in 3-wire mode.

Note: If AIS328DQ is used in a multi-SPI slave environment (several devices sharing the same SPI bus), the accelerometer can be forced by software to remain in SPI mode. This objective can be achieved by sending at the beginning of the SPI communication the following sequence to the device:

a = read(0x17)

write(0x17, (0x80 OR a))

The programming of this register is a possibility to enhance the robustness of the SPI system.

6 Register mapping

Table 15 below provides a list of the 8-bit registers embedded in the device, and the related addresses.

Table 15. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (do not modify)		00 - 0E			Reserved
WHO_AM_I	r	0F	000 1111	00110010	Dummy register
Reserved (do not modify)		10 - 1F			Reserved
CTRL_REG1	rw	20	010 0000	00000111	
CTRL_REG2	rw	21	010 0001	00000000	
CTRL_REG3	rw	22	010 0010	00000000	
CTRL_REG4	rw	23	010 0011	00000000	
CTRL_REG5	rw	24	010 0100	00000000	
HP_FILTER_RESET	r	25	010 0101		Dummy register
REFERENCE	rw	26	010 0110	00000000	
STATUS_REG	r	27	010 0111	00000000	
OUT_X_L	r	28	010 1000	output	
OUT_X_H	r	29	010 1001	output	
OUT_Y_L	r	2A	010 1010	output	
OUT_Y_H	r	2B	010 1011	output	
OUT_Z_L	r	2C	010 1100	output	
OUT_Z_H	r	2D	010 1101	output	
Reserved (do not modify)		2E - 2F			Reserved
INT1_CFG	rw	30	011 0000	00000000	
INT1_SOURCE	r	31	011 0001	00000000	
INT1_THS	rw	32	011 0010	00000000	
INT1_DURATION	rw	33	011 0011	00000000	
INT2_CFG	rw	34	011 0100	00000000	
INT2_SOURCE	r	35	011 0101	00000000	
INT2_THS	rw	36	011 0110	00000000	
INT2_DURATION	rw	37	011 0111	00000000	
Reserved (do not modify)		38 - 3F			Reserved

Registers marked as *Reserved* must not be changed. Writing to those registers may change calibration data and therefore lead to a non-proper working device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibrated values. Their content is automatically restored when the device is powered up.