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AK09911

3-axis Electronic Compass

1. Features

- A 3-axis electronic compass IC with high sensitive Hall sensor technology.
- Best adapted to pedestrian city navigation use for cell phone and other portable appliance.

- Functions:
  - 3-axis magnetometer device suitable for compass application
  - Built-in A to D Converter for magnetometer data out
  - 14-bit data out for each 3-axis magnetic component
    - Sensitivity: 0.6 μT/LSB (typ.)
  - Serial interface
    - I^2C bus interface
      Standard, Fast and High-speed mode (up to 2.5 MHz) compliant with Philips I2C specification Ver.2.1
  - Operation mode
    - Power-down, Single measurement, Continuous measurement, Self-test and Fuse ROM access
  - DRDY function for measurement data ready
  - Magnetic sensor overflow monitor function
  - Built-in oscillator for internal clock source
  - Power on Reset circuit
  - Self test function with internal magnetic source

- Operating temperatures:
  - -30˚C to +85˚C
- Operating supply voltage:
  - Analog power supply +2.4V to +3.6V
  - Digital Interface supply +1.65V to analog power supply voltage
- Current consumption:
  - Power-down: 3 μA (typ.)
  - Measurement:
    - Average current consumption at 100 Hz repetition rate: 2.4 mA (typ.)

- Package:
  - AK09911C 8-pin WL-CSP (BGA): 1.2 mm × 1.2 mm × 0.5 mm (typ.)

2. Overview

AK09911 is 3-axis electronic compass IC with high sensitive Hall sensor technology.
Small package of AK09911 incorporates magnetic sensors for detecting terrestrial magnetism in the X-axis, Y-axis, and Z-axis, a sensor driving circuit, signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Self test function is also incorporated. From its compact foot print and thin package feature, it is suitable for map heading up purpose in GPS-equipped cell phone to realize pedestrian navigation function.

AK09911 has the following features:

(1) Silicon monolithic Hall-effect magnetic sensor with magnetic concentrator realizes 3-axis magnetometer on a silicon chip. Analog circuit, digital logic, power block and interface block are also integrated on a chip.

(2) Wide dynamic measurement range and high resolution with lower current consumption.
- Output data resolution: 14-bit (0.6 μT/LSB)
- Measurement range: ±4900 μT
- Average current at 100 Hz repetition rate: 2.4 mA (typ.)

(3) Digital serial interface
- I^2C bus interface to control AK09911 functions and to read out the measured data by external CPU. A dedicated power supply for I^2C bus interface can work in low-voltage apply as low as 1.65V.

(4) DRDY register informs to system that measurement is end and set of data in registers are ready to be read.

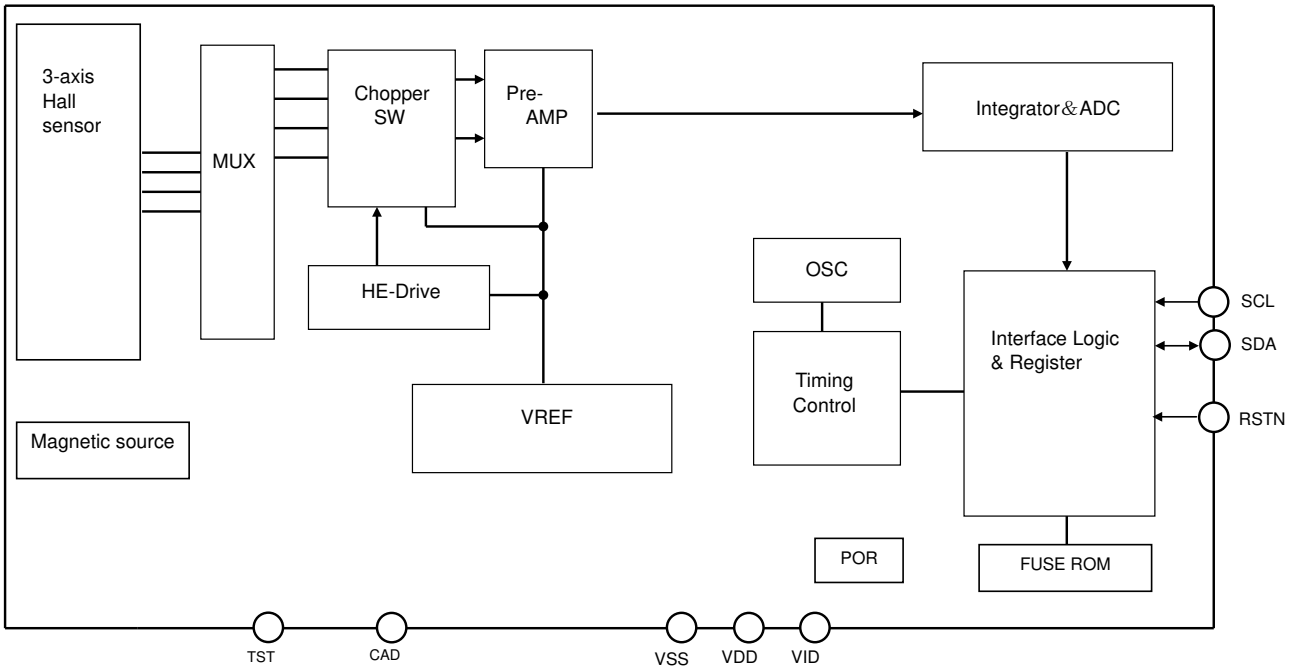
(5) Device is worked by on-chip oscillator so no external clock source is necessary.

(6) Self test function with internal magnetic source to confirm magnetic sensor operation on end products.

3. Table of Contents

4. Circuit Configration

4.1. Block Diagram



4.2. Block Function

Block	Function
3-axis Hall sensor	Monolithic Hall elements.
MUX	Multiplexer for selecting Hall elements.
Chopper SW	Performs chopping.
HE-Drive	Magnetic sensor drive circuit for constant-current driving of sensor.
Pre-AMP	Fixed-gain differential amplifier used to amplify the magnetic sensor signal.
Intergrator & ADC	Integrates and amplifies pre-AMP output and performs analog-to-digital conversion.
OSC	Generates an operating clock for sensor measurement.
POR	Power On Reset circuit. Generates reset signal on rising edge of VDD.
VREF	Generates reference voltage and current.
Interface Logic & Register	Exchanges data with an external CPU. I2C bus interface using two pins, namely, SCL and SDA. Standard, Fast and High-speed modes are supported. The low-voltage specification can be supported by applying 1.65V to the VID pin.
Timing Control	Generates a timing signal required for internal operation from a clock generated by the OSC.
Magnetic Source	Generates magnetic field for self test of magnetic sensor.
FUSE ROM	Fuse for adjustment.

4.3. Pin Function

Pin No.	Pin name	I/O	Power supply	Type	Function
A1	VDD	-	-	Power	Positive power supply pin.
A2	CAD	I	VDD	CMOS	Slave address input pin. Connect to VSS or VDD,
A3	TST	I/O	VDD	CMOS	Test pin. Pulled down by 100kΩ internal resister. Keep this pin electrically non-connected.
B1	VSS	-	-	Power	Ground pin.
B3	SCL	I	VID	CMOS	Control data clock input pin Input: Schmidt trigger
C1	VID	-	-	Power	Digital interface positive power supply pin.
C2	RSTN	I	VID	CMOS	Reset pin. Resets registers by setting to “L”.
C3	SDA	I/O	VID	CMOS	Control data input/output pin Input: Schmidt trigger, Output: Open drain

5. Overall Characteristics

5.1. Absolute Maximum Ratings

Vss=0V

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage (Vdd, Vid)	V+	-0.3	+4.3	V
Input voltage	VIN	-0.3	(V+)+0.3	V
Input current	IIN	-	±10	mA
Storage temperature	Tst	-40	+125	˚C

(Note 1) If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such exceeding conditions.

5.2. Recommended Operating Conditions

Vss=0V

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Operating temperature		Ta	-30		+85	˚C
Power supply voltage	VDD pin voltage	Vdd	2.4	3.0	3.6	V
	VID pin voltage	Vid	1.65		Vdd	V

5.3. Electrical Characteristics

The following conditions apply unless otherwise noted:
Vdd=2.4V to 3.6V, Vid=1.65V to Vdd, Temperature range=-30˚C to 85˚C

5.3.1. DC Characteristics

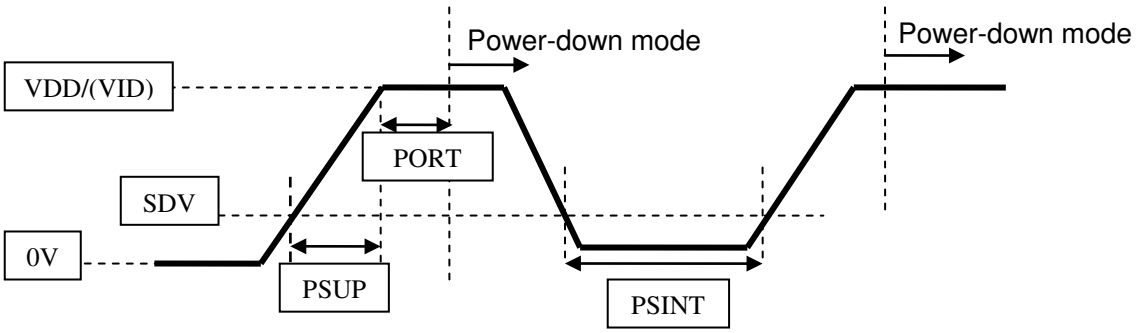
Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage 1	VIH1	RSTN		70%Vid		Vid+0.3	V
		SCL SDA		70%Vid			
Low level input voltage 1	VIL1	RSTN SCL SDA		-0.3		30%Vid	V
High level input voltage 2	VIH2	TST CAD		70%Vdd		Vdd+0.3	V
Low level input voltage 2	VIL2			-0.3		30%Vdd	V
Input current 1	IIN1	RSTN SCL SDA	Vin=Vss or Vid	-10		+10	µA
		CAD	Vin=Vss or Vdd	-10		+10	
Input current 2	IIN2	TST	Vin=Vdd			100	µA
Hysteresis input voltage (Note 2)	VHS	SCL SDA	Vid≥2V	5%Vid			V
			Vid<2V	10%Vid			
Low level output voltage (Note 3)	VOL	SDA	IOL≤+3mA Vid≥2V			0.4	V
			IOL≤+3mA Vid<2V			20%Vid	
Current consumption (Note 4)	IDD1	VDD VID	Power-down mode Vdd=Vid=3.0V		3	6	µA
	IDD2		When magnetic sensor is driven		3	6	mA
	IDD3		Self-test mode		5	8	mA
	IDD4		(Note 5)		0.1	5	µA

(Note 2) Schmitt trigger input (reference value for design)
(Note 3) Output is open-drain. Connect a pull-up resistor externally. Maximum capacitive load: 400pF (Capacitive load of each bus line for I2C bus interface).
(Note 4) Without any resistance load. It does not include the current consumed by external loads (pull-down resister, etc.). RSTN, SDA, SCL = Vid or 0V. CAD = Vdd or 0V.
(Note 5) (case 1) Vdd=ON, Vid=ON, RSTN pin = "L". (case 2) Vdd=ON, Vid=OFF (0V), RSTN pin = "L". (case 3) Vdd=OFF (0V), Vid=ON.

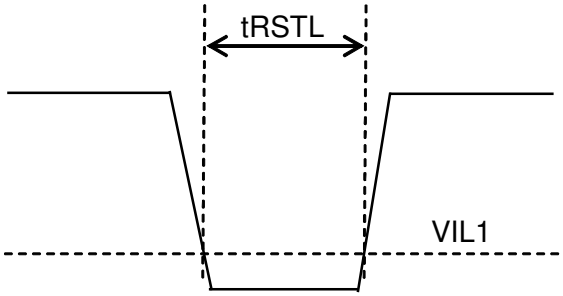
5.3.2. AC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply rise time (Note 6)	PSUP	VDD VID	Period of time that VDD (VID) changes from 0.2V to Vdd (Vid).			50	ms
POR completion time (Note 6)	PORT		Period of time after PSUP to Power-down mode (Note 7)			100	µs
Power supply turn off voltage (Note 6)	SDV	VDD VID	Turn off voltage to enable POR to restart (Note 7)			0.2	V
Power supply turn on interval (Note 6)	PSINT	VDD VID	Period of time that voltage lower than SDV needed to be kept to enable POR to restart (Note 7)	100			µs
Wait time before mode setting	Twat			100			µs

(Note 6) Reference value for design.
(Note 7) When POR circuit detects the rise of VDD/VID voltage, it resets internal circuits and initializes the registers. After reset, AK09911 transits to Power-down mode.



Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Reset input effective pulse width ("L")	tRSTL	RSTN		5			µs



5.3.3. Analog Circuit Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT		-	14	-	bit
Time for measurement	TSM	Single measurement mode		7.2	8.5	ms
Magnetic sensor sensitivity (Note 8)	BSE	Tc = 25 ˚C	0.57	0.6	0.63	μT/LSB
Magnetic sensor measurement range (Note 9)	BRG	Tc = 25 ˚C	±4912			μT
Magnetic sensor initial offset (Note 10)		Tc = 25 ˚C	-500		+500	LSB

(Note 8) Value after sensitivity is adjusted using sensitivity fine adjustment data stored in Fuse ROM.
(Note 9) Reference value for design
(Note 10) Value of measurement data register on shipment without applying magnetic field on purpose.

5.3.4. I²C Bus Interface

I²C bus interface is compliant with Standard mode, Fast mode and High-speed mode. Standard/Fast mode is selected automatically by fSCL.

☐ Standard mode

fSCL≤100kHz

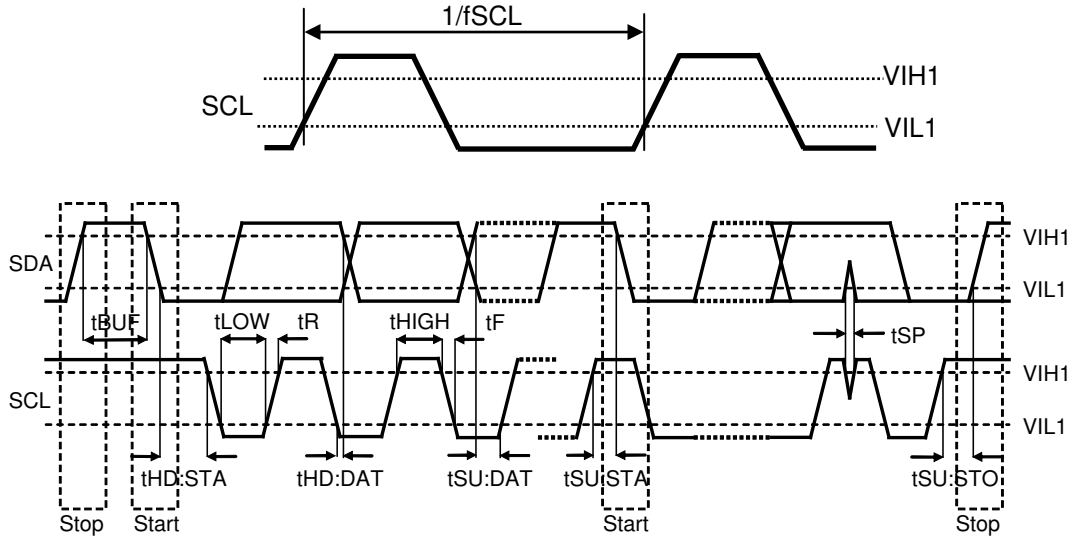
Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			100	kHz
tHIGH	SCL clock "High" time	4.0			μs
tLOW	SCL clock "Low" time	4.7			μs
tR	SDA and SCL rise time			1.0	μs
tF	SDA and SCL fall time			0.3	μs
tHD:STA	Start Condition hold time	4.0			μs
tSU:STA	Start Condition setup time	4.7			μs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μs
tSU:DAT	SDA setup time (vs. SCL rising edge)	250			ns
tSU:STO	Stop Condition setup time	4.0			μs
tBUF	Bus free time	4.7			μs

☐ Fast mode

100Hz≤fSCL≤400kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			400	kHz
tHIGH	SCL clock "High" time	0.6			μs
tLOW	SCL clock "Low" time	1.3			μs
tR	SDA and SCL rise time			0.3	μs
tF	SDA and SCL fall time			0.3	μs
tHD:STA	Start Condition hold time	0.6			μs
tSU:STA	Start Condition setup time	0.6			μs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μs
tSU:DAT	SDA setup time (vs. SCL rising edge)	100			ns
tSU:STO	Stop Condition setup time	0.6			μs
tBUF	Bus free time	1.3			μs
tSP	Noise suppression pulse width			50	ns

[I²C bus interface timing]



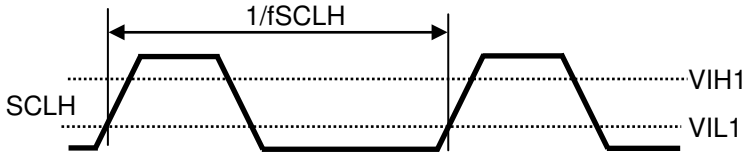
- High-speed mode (Hs-mode)
  - C_b≤100pF (C_b: load capacitance)
    fSCLH≤2.5MHz

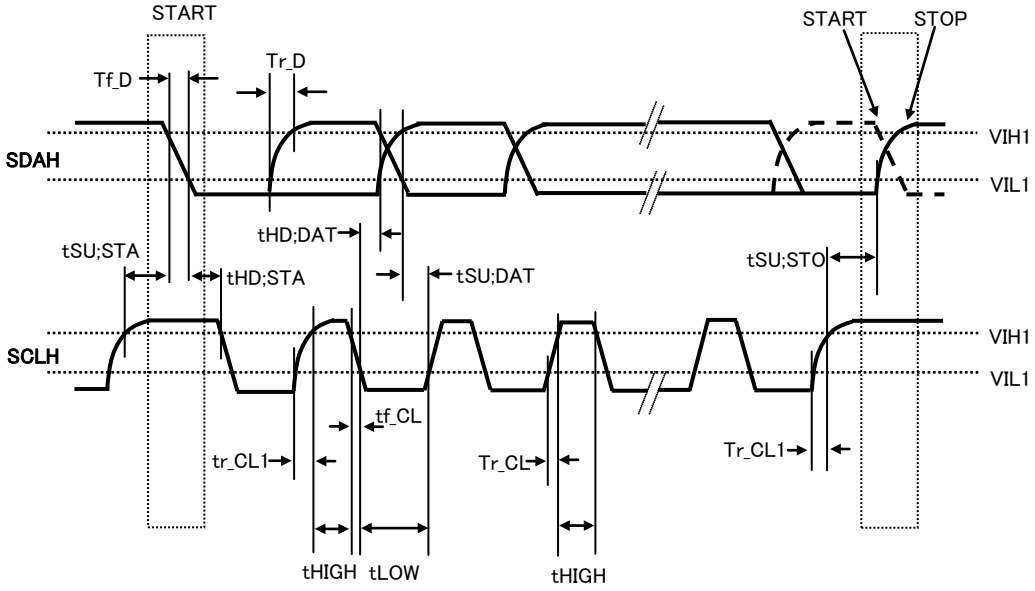
Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCLH	SCLH clock frequency			2.5	MHz
tHIGH	SCLH clock “High” time	110			ns
tLOW	SCLH clock “Low” time	220			ns
tR_CL	SCLH rise time	10		40	ns
tR_CL1	SCLH rise time after a repeated START condition and after an acknowledge bit	10		80	ns
tR_DA	SDAH rise time	10		80	ns
tF_CL	SCLH fall time	-		40	ns
tF_DA	SDAH fall time	-		80	ns
tHD:STA	Start Condition hold time	160			ns
tSU:STA	Start Condition setup time	160			ns
tHD:DAT	SDAH hold time (vs. SCLH falling edge)	0			ns
tSU:DAT	SDAH setup time (vs. SCLH rising edge)	10			ns
tSU:STO	Stop Condition setup time	160			ns
tSP	Noise suppression pulse width			10	ns

  - C_b≤400pF
    fSCLH≤1.7MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCLH	SCLH clock frequency			1.7	MHz
tHIGH	SCLH clock “High” time	120			ns
tLOW	SCLH clock “Low” time	320			ns
tR_CL	SCLH rise time	20		80	ns
tR_CL1	SCLH rise time after a repeated START condition and after an acknowledge bit	20		160	ns
tR_DA	SDAH rise time	20		160	ns
tF_CL	SCLH fall time	-		80	ns
tF_DA	SDAH fall time	-		160	ns
tHD:STA	Start Condition hold time	160			ns
tSU:STA	Start Condition setup time	160			ns
tHD:DAT	SDAH hold time (vs. SCLH falling edge)	0			ns
tSU:DAT	SDAH setup time (vs. SCLH rising edge)	10			ns
tSU:STO	Stop Condition setup time	160			ns
tSP	Noise suppression pulse width			10	ns

[I^2C bus interface timing of Hs-mode]





6. Function Explanation

6.1. Power States

When VDD and VID are turned on from Vdd=OFF (0V) and Vid=OFF (0V), all registers in AK09911 are initialized by POR circuit and AK09911 transits to Power-down mode.

All the states in the table below can be set, although the transition from state 2 to state 3 and the transition from state 3 to state 2 are prohibited.

Table 6.1. Power state

State	VDD	VID	Power state
1	OFF (0V)	OFF (0V)	OFF (0V). It doesn't affect external interface.Digital input pins other than SCL and SDA pin should be fixed to "L"(0V).
2	OFF (0V)	1.65V to 3.6V	OFF (0V) It doesn't affect external interface.
3	2.4V to 3.6V	OFF (0V)	OFF(0V) It doesn't affect external interface. Digital input pins other than SCL and SDA pin should be fixed to "L"(0V).
4	2.4V to 3.6V	1.65V to Vdd	ON

6.2. Reset Functions

When the power state is ON, always keep Vid≤Vdd.
Power-on reset (POR) works until Vdd reaches to the operation effective voltage (about 1.1V: reference value for design) on power-on sequence. After POR is deactivated, all registers are initialized and transits to Power-down mode.

When Vdd=2.4 to 3.6V, POR circuit and VID monitor circuit are active. When Vid=0V, AK09911 is in reset status and it consumes the current of reset state (IDD4).

AK09911 has four types of reset;

(1) Power on reset (POR)
When Vdd rise is detected, POR circuit operates, and AK09911 is reset.

(2) VID monitor
When VID is turned OFF, AK09911 is reset.

(3) Reset pin (RSTN)
AK09911 is reset by Reset pin. When Reset pin is not used, connect to VID.

(4) Soft reset
AK09911 is reset by setting SRST bit. When AK09911 is reset, all registers are initialized and AK09911 transits to Power-down mode.

6.3. Operation Mode

AK09911 has following nine operation modes:

(1) Power-down mode
(2) Single measurement mode
(3) Continuous measurement mode 1
(4) Continuous measurement mode 2
(5) Continuous measurement mode 3
(6) Continuous measurement mode 4
(7) Self-test mode
(8) Fuse ROM access mode

By setting CNTL2 register MODE[4:0] bits, the operation set for each mode is started.
A transition from one mode to another is shown below.

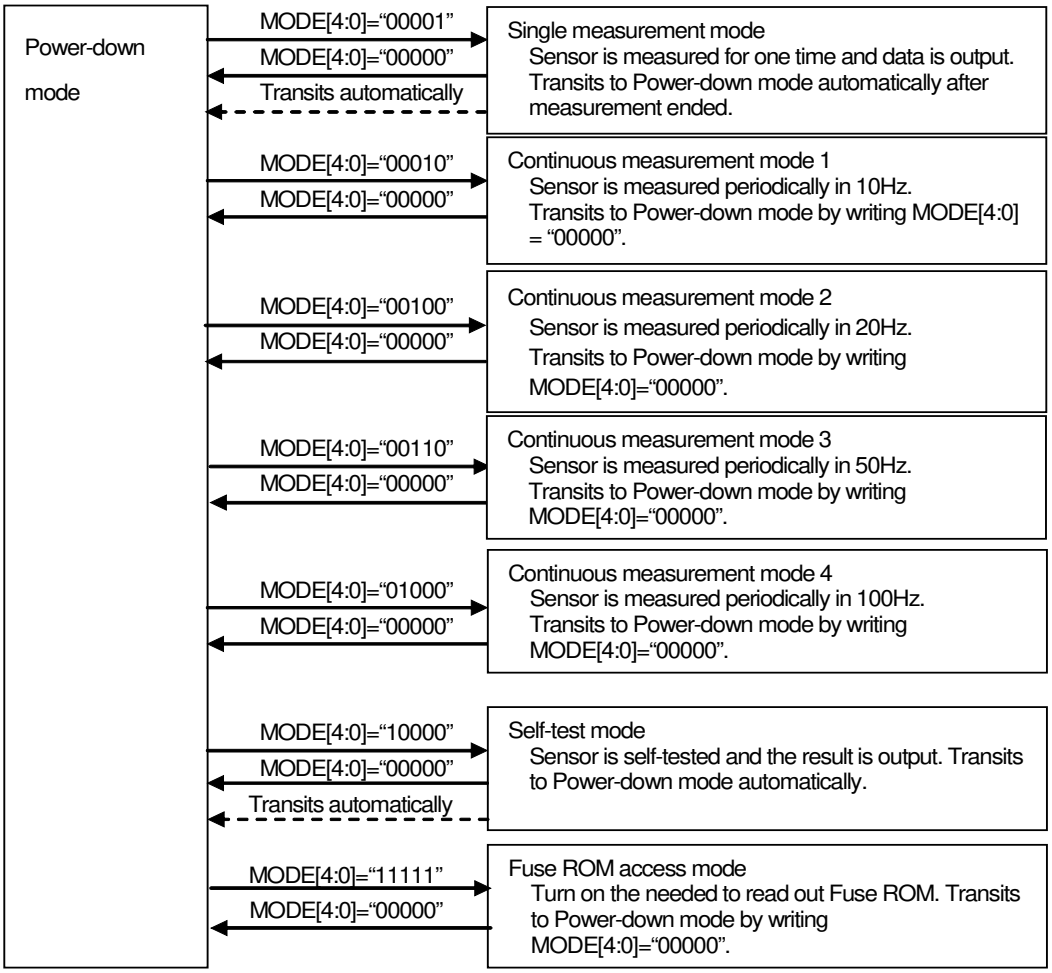


Figure 6.1. Operation mode

When power is turned ON, AK09911 is in Power-down mode. When a specified value is set to MODE[4:0], AK09911 transits to the specified mode and starts operation. When user wants to change operation mode, transit to Power-down mode first and then transit to other modes. After Power-down mode is set, at least 100 μs (Twat) is needed before setting another mode

6.4. Description of Each Operation Mode

6.4.1. Power-down Mode

Power to almost all internal circuits is turned off. All registers are accessible in Power-down mode. Data stored in read/write registers are remained. They can be reset by soft reset.

6.4.2. Single Measurement Mode

When Single measurement mode (MODE[4:0]="00001") is set, magnetic sensor measurement is started. After magnetic sensor measurement and signal processing is finished, measurement magnetic data is stored to measurement data registers (HXL to HZH), then AK09911 transits to Power-down mode automatically. On transition to Power-down mode, MODE[4:0] turns to "00000". At the same time, DRDY bit in ST1 register turnes to "1". This is called "Data Ready". When any of measurement data register (HXL to TMPS) or ST2 register is read, DRDY bit turnes to "0". It remains "1" on transition from Power-down mode to another mode. (Figure 6.2.)
When sensor is measuring (Measurement period), measurement data registers (HXL to TMPS) keep the previous data. Therefore, it is possible to read out data even in measurement period. Data read out in measurement period are previous data.(Figure 6.3.)

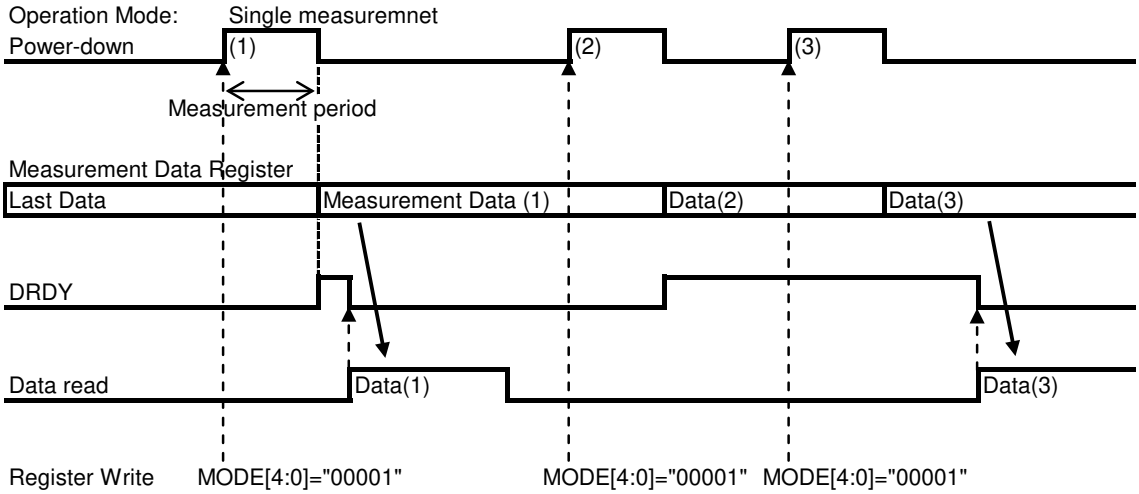


Figure 6.2. Single measurement mode when data is read out of measurement period

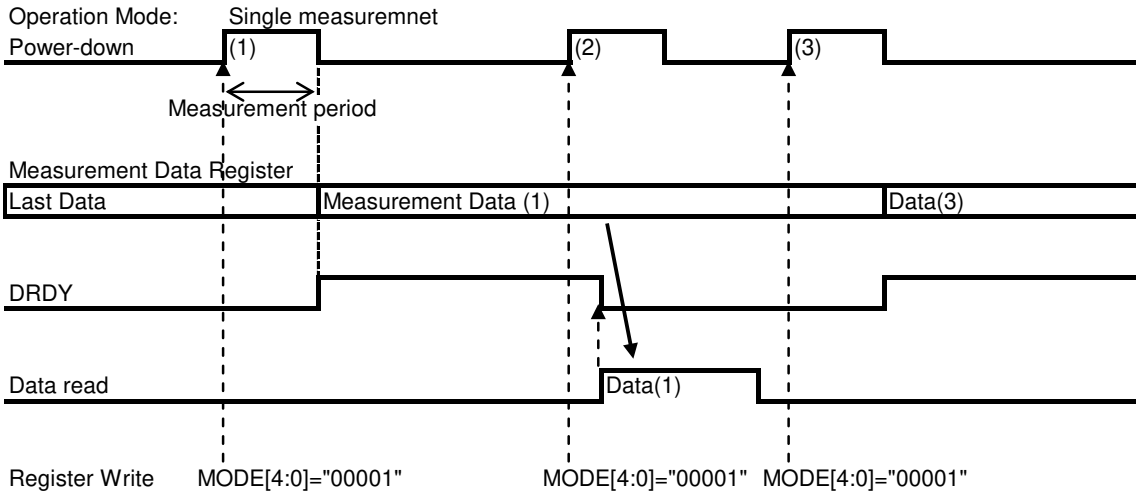


Figure 6.3. Single measurement mode when data read started during measurement period

6.4.3. Continuous Measurement Mode 1, 2, 3 and 4

When Continuous measurement mode 1 (MODE[4:0]="00010"), 2 (MODE[4:0]="00100"), 3 (MODE[4:0]="00110") or 4 (MODE[4:0]="01000") is set, magnetic sensor measurement is started periodically at 10 Hz, 20 Hz, 50 Hz or 100 Hz respectively. After magnetic sensor measurement and signal processing is finished, measurement magnetic data is stored to measurement data registers (HXL to HZH) and all circuits except for the minimum circuit required for counting cycle length are turned off (PD). When the next measurement timing comes, AK09911 wakes up automatically from PD and starts measurement again.
Continuous measurement mode ends when Power-down mode (MODE[4:0]="00000") is set. It repeats measurement until Power-down mode is set.
When Continuous measurement mode 1 (MODE[4:0]="00010"), 2 (MODE[4:0]="00100"), 3 (MODE[4:0]="00110") or 4 (MODE[4:0]="01000") is set again while AK09911 is already in Continuous measurement mode, a new measurement starts. ST1, ST2 and measurement data registers (HXL to TMPS) will not be initialized by this.

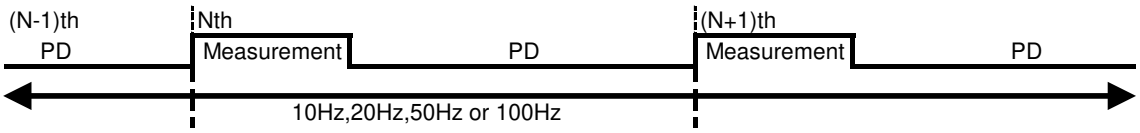


Figure 6.4. Continuous measurement mode

6.4.3.2. Data Ready

When measurement data is stored and ready to be read, DRDY bit in ST1 register turnes to "1". This is called "Data Ready". When measurement is performed correctly, AK09911 becomes Data Ready on transition to PD after measurement.

6.4.3.3. Normal Read Sequence

(1) Check Data Ready or not by polling DRDY bit of ST1 register
- DRDY: Shows Data Ready or not. Not when "0", Data Ready when "1".
- DOR: Shows if any data has been skipped before the current data or not. There are no skipped data when "0", there are skipped data when "1".

(2) Read measurement data
When any of measurement data register (HXL to TMPS) or ST2 register is read, AK09911 judges that data reading is started. When data reading is started, DRDY bit and DOR bit turnes to "0".

(3) Read ST2 register (required)
- HOFL: Shows if magnetic sensor is overflowed or not. "0" means not overflowed, "1" means overflowed.

When ST2 register is read, AK09911 judges that data reading is finished. Stored measurement data is protected during data reading and data is not updated. By reading ST2 register, this protection is released. It is required to read ST2 register after data reading.

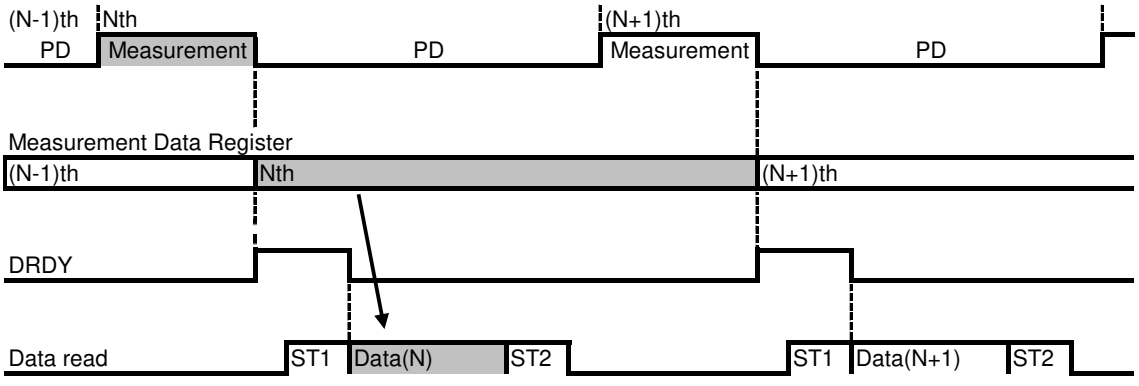


Figure 6.5. Normal read sequence

6.4.3.4. Data Read Start during Measurement

When sensor is measuring (Measurement period), measurement data registers (HXL to TMPS) keep the previous data. Therefore, it is possible to read out data even in measurement period. If data is started to be read during measurement period, previous data is read.

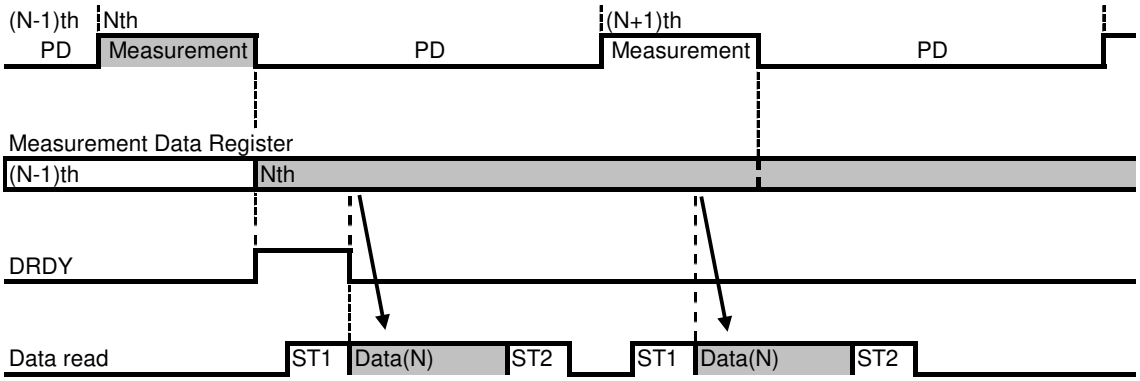


Figure 6.6. Data read start during measurement

6.4.3.5. Data Skip

When Nth data was not read before (N+1)th measurement ends, Data Ready remains until data is read. In this case, a set of measurement data is skipped so that DOR bit turnes to "1".
When data reading started after Nth measurement ended and did not finish reading before (N+1)th measurement ended, Nth measurement data is protected to keep correct data. In this case, a set of measurement data is skipped and not stored so that DOR bit turnes to "1".
In both case, DOR bit turnes to "0" at the next start of data reading.

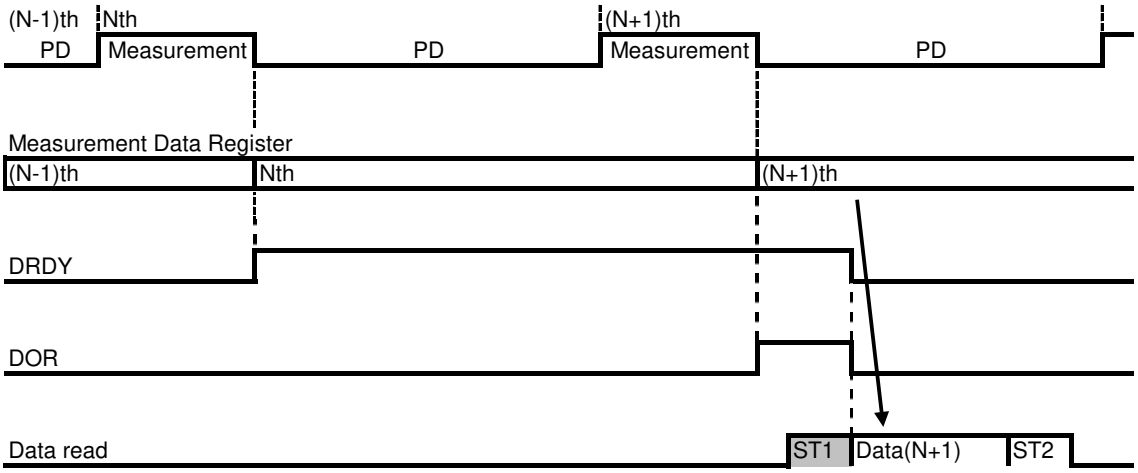


Figure 6.7. Data Skip: When data is not read

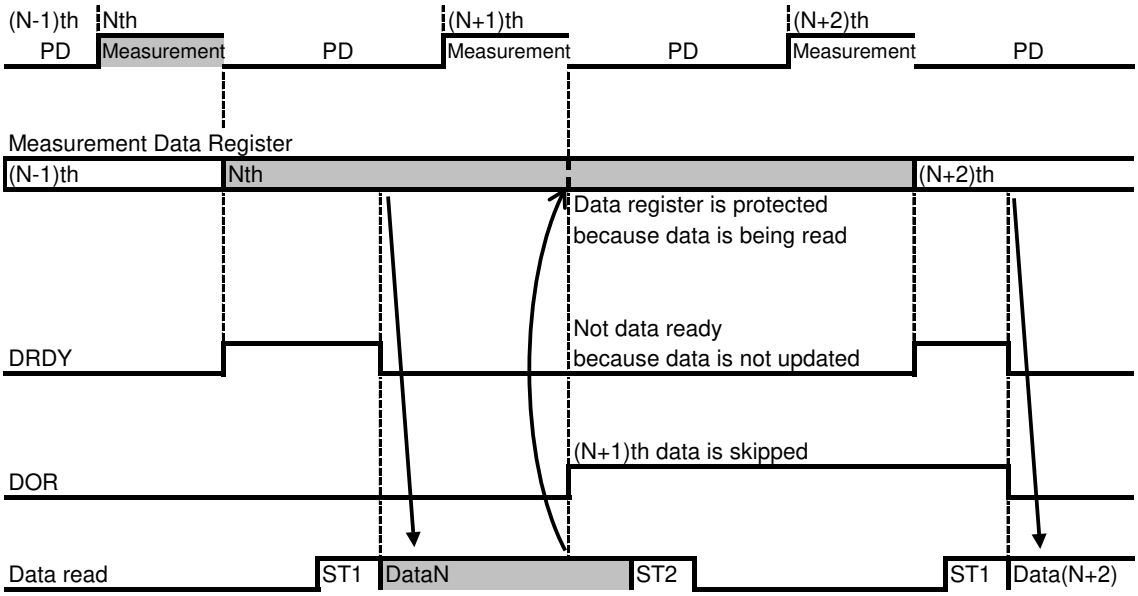


Figure 6.8. Data Skip: When data read has not been finished before the next measurement end

6.4.3.6. End Operation

Set Power-down mode (MODE[4:0]="00000") to end Continuous measurement mode.

6.4.3.7. Magnetic Sensor Overflow

AK09911 has the limitation for measurement range that the sum of absolute values of each axis should be smaller than 4912 μT.

$|X|+|Y|+|Z| < 4912\ \mu T$

When the magnetic field exceeded this limitation, data stored at measurement data are not correct. This is called Magnetic Sensor Overflow.
When magnetic sensor overlow occurs, HOFL bit turns to "1". When the next measurement starts, it returns to "0".

6.4.4. Self-test Mode

Self-test mode is used to check if the magnetic sensor is working normally.
When Self-test mode (MODE[4:0]="10000") is set, magnetic field is generated by the internal magnetic source and magnetic sensor is measured. Measurement data is stored to measurement data registers (HXL to HZH), then AK09911 transits to Power-down mode automatically.
Data read sequence and functions of read-only registers in Self-test mode is the same as Single measurement mode.

6.4.4.1. Self-test Sequence

(1) Set Power-down mode. (MODE[4:0]="00000")
(2) Set Self-test mode. (MODE[4:0]="10000")
(3) Check Data Ready or not by polling DRDY bit of ST1 register
When Data Ready, proceed to the next step.
(4) Read measurement data (HXL to HZH)

6.4.4.2. Self-test Judgment

When measurement data read by the above sequence is in the range of following table after sensitivity adjustment (refer to 8.3.11), AK09911 is working normally.

	HX[15:0]	**HY[15:0]**	**HZ[15:0]**
Criteria	$-30 \leq HX \leq +30$	$-30 \leq HY \leq +30$	$-400 \leq HZ \leq -50$

6.4.5. Fuse ROM Access Mode

Fuse ROM access mode is used to read Fuse ROM data. Sensitivity adjustment data for each axis is stored in fuse ROM.
Set Fuse ROM Access mode (MODE[4:0]="11111") before reading Fuse ROM data. When Fuse ROM Access mode is set, circuits required for reading fuse ROM are turned on.
After reading fuse ROM data, set Power-down mode (MODE[4:0]="00000") before the transition to another mode.

7. Serial Interface

The I^2C bus interface of AK09911 supports the Standard mode (100 kHz max.), the Fast mode (400 kHz max.) and the High-speed mode (Hs-mode, 2.5 MHz max.).

7.1. Data Transfer

To access AK09911 on the bus, generate a start condition first.
Next, transmit a one-byte slave address including a device address. At this time, AK09911 compares the slave address with its own address. If these addresses match, AK09911 generates an acknowledgement, and then executes READ or WRITE instruction. At the end of instruction execution, generate a stop condition.

7.1.1. Change of Data

A change of data on the SDA line must be made during "Low" period of the clock on the SCL line. When the clock signal on the SCL line is "High", the state of the SDA line must be stable. (Data on the SDA line can be changed only when the clock signal on the SCL line is "Low".)
During the SCL line is "High", the state of data on the SDA line is changed only when a start condition or a stop condition is generated.

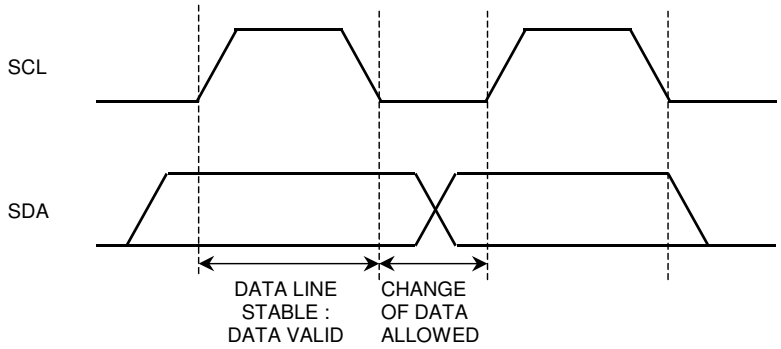


Figure 7.1. Data Change

7.1.2. Start/Stop Condition

If the SDA line is driven to "Low" from "High" when the SCL line is "High", a start condition is generated. Every instruction starts with a start condition.
If the SDA line is driven to "High" from "Low" when the SCL line is "High", a stop condition is generated. Every instruction stops with a stop condition.

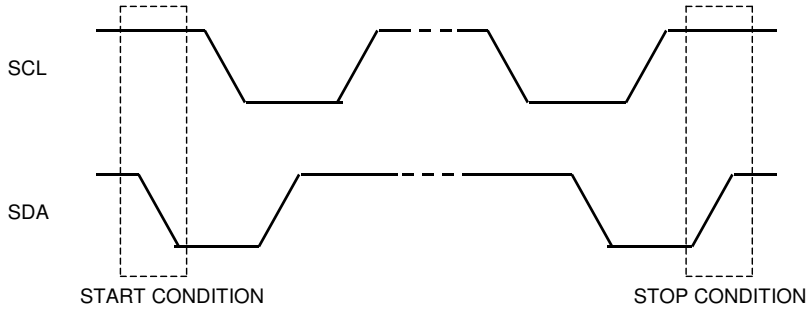


Figure 7.2. Start and Stop Condition

7.1.3. Acknowledge

The IC that is transmitting data releases the SDA line (in the "High" state) after sending 1-byte data.
The IC that receives the data drives the SDA line to "Low" on the next clock pulse. This operation is referred as acknowledge. With this operation, whether data has been transferred successfully can be checked.
AK09911 generates an acknowledge after reception of a start condition and slave address.
When a WRITE instruction is executed, AK09911 generates an acknowledge after every byte is received.
When a READ instruction is executed, AK09911 generates an acknowledge then transfers the data stored at the specified address. Next, AK09911 releases the SDA line then monitors the SDA line. If a master IC generates an acknowledge instead of a stop condition, AK09911 transmits the 8bit data stored at the next address. If no acknowledge is generated, AK09911 stops data transmission.

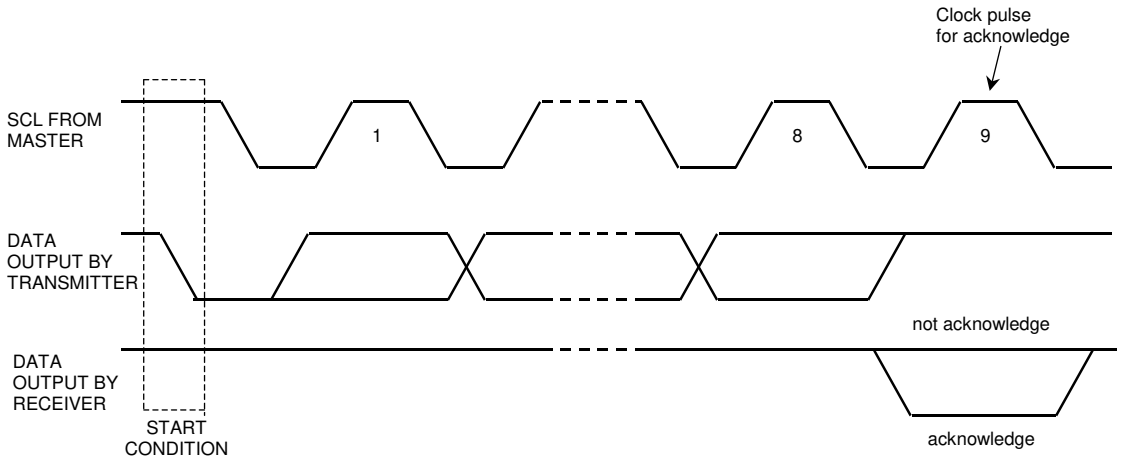


Figure 7.3. Generation of Acknowledge

7.1.4. Slave Address

The slave address of AK09911 can be selected from the following list by setting CAD pin. When CAD pin is fixed to VSS, the corresponding slave address bit is "0". When CAD pin is fixed to VDD, the corresponding slave address bit is "1".

Table 7.1. Slave Address and CAD pin

CAD	Slave Address
0	0CH
1	0DH

MSB LSB

0	**0**	**0**	**1**	**1**	**0**	**CAD**	**R/W**

Figure 7.4. Slave Address

The first byte including a slave address is transmitted after a start condition, and an IC to be accessed is selected from the ICs on the bus according to the slave address.
When a slave address is transferred, the IC whose device address matches the transferred slave address generates an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit.
When the R/W bit is set to "1", READ instruction is executed. When the R/W bit is set to "0", WRITE instruction is executed.

7.2. WRITE Instruction

When the R/W bit is set to "0", AK09911 performs write operation.
In write operation, AK09911 generates an acknowledge after receiving a start condition and the first byte (slave address) then receives the second byte. The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.

MSB							LSB
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**

Figure 7.5. Register Address

After receiving the second byte (register address), AK09911 generates an acknowledge then receives the third byte.
The third and the following bytes represent control data. Control data consists of 8 bits and is based on the MSB-first configuration. AK09911 generates an acknowledge after every byte is received. Data transfer always stops with a stop condition generated by the master.

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Figure 7.6. Control Data

AK09911 can write multiple bytes of data at a time.
After reception of the third byte (control data), AK09911 generates an acknowledge then receives the next data. If additional data is received instead of a stop condition after receiving one byte of data, the address counter inside the LSI chip is automatically incremented and the data is written at the next address.
The address is incremented from 00H to 18H, from 30H to 32H, or from 60H to 62H. When the address is 00H to 18H, the address is incremented 00H → 01H → 02H → 03H → 10H → 11H →... → 18H,and the address goes back to 00H after 18H. When the address is 30H to 32H, the address goes back to 30H after 32H. When the address is 60H to 62H, the address goes back to 60H after 62H.
Actual data is written only to Read/Write registers (refer to Table 8.2.).

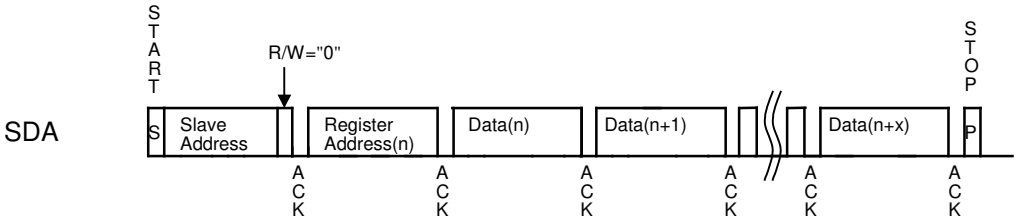


Figure 7.7. WRITE Instruction

7.3. READ Instruction

When the R/W bit is set to “1”, AK09911 performs read operation.
If a master IC generates an acknowledge instead of a stop condition after AK09911 transfers the data at a specified address, the data at the next address can be read.
Address can be 00H to 18H, 30H to 32H, and 60H to 62H. When the address is 00H to 18H, the address is incremented 00H → 01H → 02H → 03H → 10H → 11H →... → 18H,and the address goes back to 00H after 18H. When the address is 30H to 32H, the address goes back to 30H after 32H. When the address is 60H to 62H, the address goes back to 60H after 62H.
AK09911 supports one byte read and multiple byte read.

7.3.1. One Byte READ

AK09911 has an address counter inside the LSI chip. In current address read operation, the data at an address specified by this counter is read.
The internal address counter holds the next address of the most recently accessed address.
For example, if the address most recently accessed (for READ instruction) is address “n”, and a current address read operation is attempted, the data at address “n+1” is read.
In one byte read operation, AK09911 generates an acknowledge after receiving a slave address for the READ instruction (R/W bit=“1”). Next, AK09911 transfers the data specified by the internal address counter starting with the next clock pulse, then increments the internal counter by one. If the master IC generates a stop condition instead of an acknowledge after AK09911 transmits one byte of data, the read operation stops.

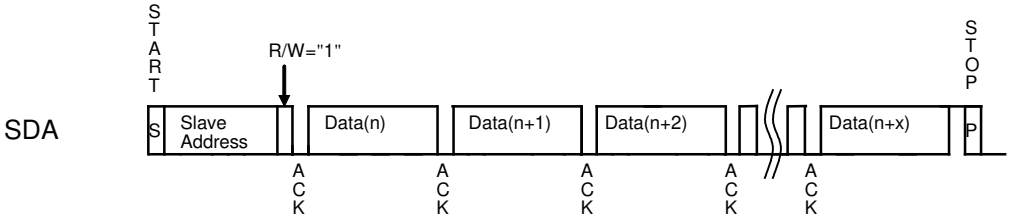


Figure 7.8. One Byte READ

7.3.2. Multiple Byte READ

By multiple byte read operation, data at an arbitrary address can be read.
The multiple byte read operation requires to execute WRITE instruction as dummy before a slave address for the READ instruction (R/W bit=“1”) is transmitted. In random read operation, a start condition is first generated then a slave address for the WRITE instruction (R/W bit=“0”) and a read address are transmitted sequentially.
After AK09911 generates an acknowledge in response to this address transmission, a start condition and a slave address for the READ instruction (R/W bit=“1”) are generated again. AK09911 generates an acknowledge in response to this slave address transmission. Next, AK09911 transfers the data at the specified address then increments the internal address counter by one. If the master IC generates a stop condition instead of an acknowledge after data is transferred, the read operation stops.

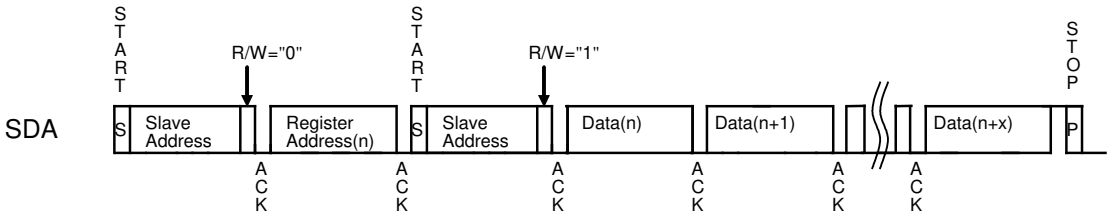


Figure 7.9. Multiple Byte READ

7.4. High-speed Mode (Hs-mode)

AK09911 supports the Hs-mode.
Hs-mode can only commence after the following conditions (all of which are in Fast/Standard-mode):

- START condition (S)
- 8-bit master code (00001XXX)
- not-acknowledge bit ($\bar{A}$)

The diagram below shows data flow of the Hs-mode.
After start condition, feed master code 00001XXX for transfer to the Hs-mode. And then AK09911 feeds back not-acknowledge bit and swich over to circuit for the Hs-mode between times t1 and tH. AK09911 can communicate at the Hs-mode from next START condition. At time tFS, AK09911 switchs its internal circuit from the Hs-mode to the First mode with the STOP condition (P). This transfer completes in the bus free time (tBUF).

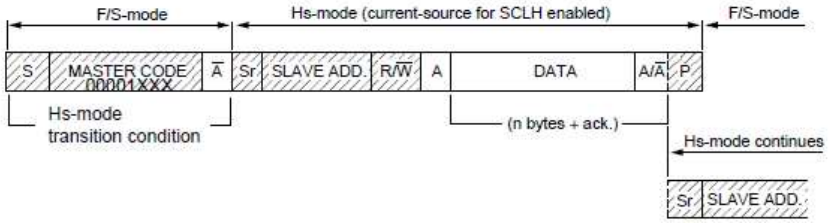


Figure 7.10. Data transfer format in Hs-mode

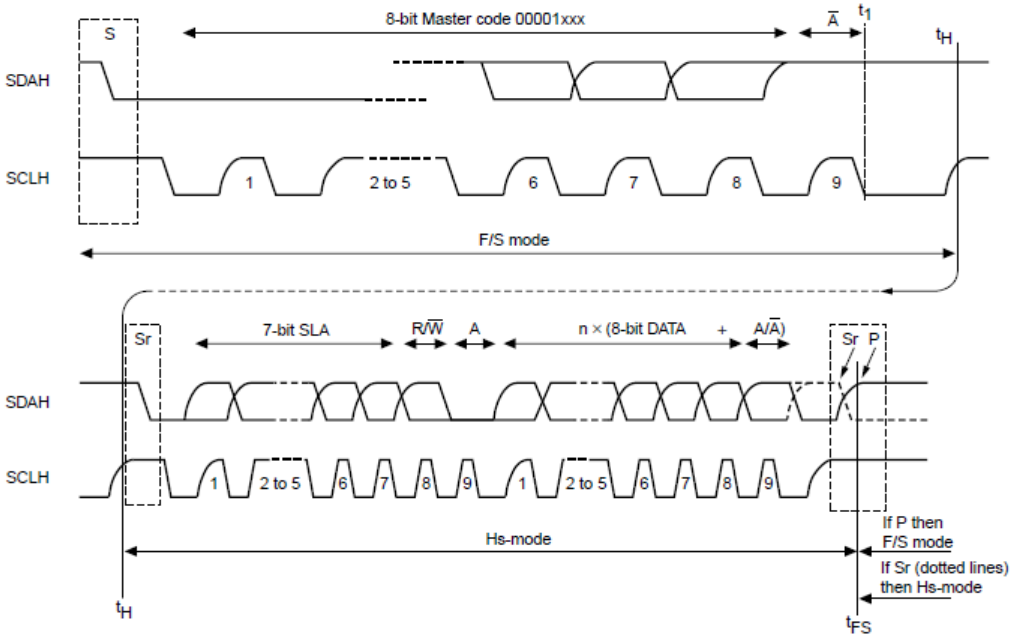


Figure 7.11. Hs-mode transfer

8. Registers

8.1. Description of Registers

AK09911 has registers of 20 addresses as indicated in Every address consists of 8 bits data. Data is transferred to or received from the external CPU via the serial interface described previously.

Table 8.1. Register Table

Name	Address	READ/ WRITE	Description	Bit width	Remarks
WIA1	00H	READ	Campany ID	8	
WIA2	01H	READ	Device ID	8	
INFO1	02H	READ	Information 1	8	
INFO2	03H	READ	Information 2	8	
ST1	10H	READ	Status 1	8	Data status
HXL	11H	READ	Measurement Magnetic Data	8	X-axis data
HXH	12H	READ		8	
HYL	13H	READ		8	Y-axis data
HYH	14H	READ		8	
HZL	15H	READ		8	Z-axis data
HZH	16H	READ		8	
TMPS	17H	READ	Dummy Register	8	Dummy
ST2	18H	READ	Status 2	8	Data status
CNTL1	30H	READ/ WRITE	Dummy Register	8	Dummy
CNTL2	31H	READ/ WRITE	Control 2	8	Control settings
CNTL3	32H	READ/ WRITE	Control 3	8	Control settings
TS1	33H	READ/ WRITE	Test	8	DO NOT ACCESS
ASAX	60H	READ	X-axis sensitivity adjustment value	8	Fuse ROM
ASAY	61H	READ	Y-axis sensitivity adjustment value	8	Fuse ROM
ASAZ	62H	READ	Z-axis sensitivity adjustment value	8	Fuse ROM

Addresses 00H to 18H, 30H to 32H and 60H to 62H are compliant with automatic increment function of serial interface respectively. Values of addresses 60H to 62H can be read only in Fuse ROM access mode. In other modes, read data is not correct. When the address is in 00H to 18H, the address is incremented 00H → 01H → 02H → 03H → 10H → 11H →... → 18H, and the address goes back to 00H after 18H. When the address is in 30H to 32H, the address goes back to 30H after 32H. When the address is in 60H to 62H, the address goes back to 60H after 62H.