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AK1228

10~2000MHz Low Noise Mixer

1. General Description

AK1228 is a high linearity and low noise mixer. Signal input frequency range coverage is from 10 to 2000MHz and output coverage is from 10 to 1000MHz. AK1228 can be driven by a single ended signal input and a low-power differential LO input that can be driven with a differential or single ended LO. The signal output ports are differential open drain outputs. The analog circuit characteristics and power consumption performances can be optimized by the resistance connected to the BIAS Pin.

2. Features

- □ Input Frequency: 10MHz to 2000MHz
- □ Output Frequency: 10MHz to 1000MHz
- □ Operating Supply Current: 4.5mA to 10.5mA
- □ Analog Circuit Characteristics: Current Consumption:10.5mA, IIP3:+12dBm, Gain:4dBm, NF:8.5dB
- □ LO Input Level: -10 to +5dBm
- □ Operating Supply Voltage: 2.7 to 5.25V
- □ Package: 16pin UQFN (0.5mm pitch, 3mm × 3mm × 0.60mm)
- □ Operating Temperature: -40 to 85°C

3. Applications

- □ Two-way Radios (PMR/LMR)
- □ Radio Communications for disaster prevention
- □ Marine Radios
- □ Amateur Radios
- □ Specified Low Power Radios
- □ Telemeter, Telecontrol
- □ Wireless Microphone

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5. Block Diagram and Pin Configurations

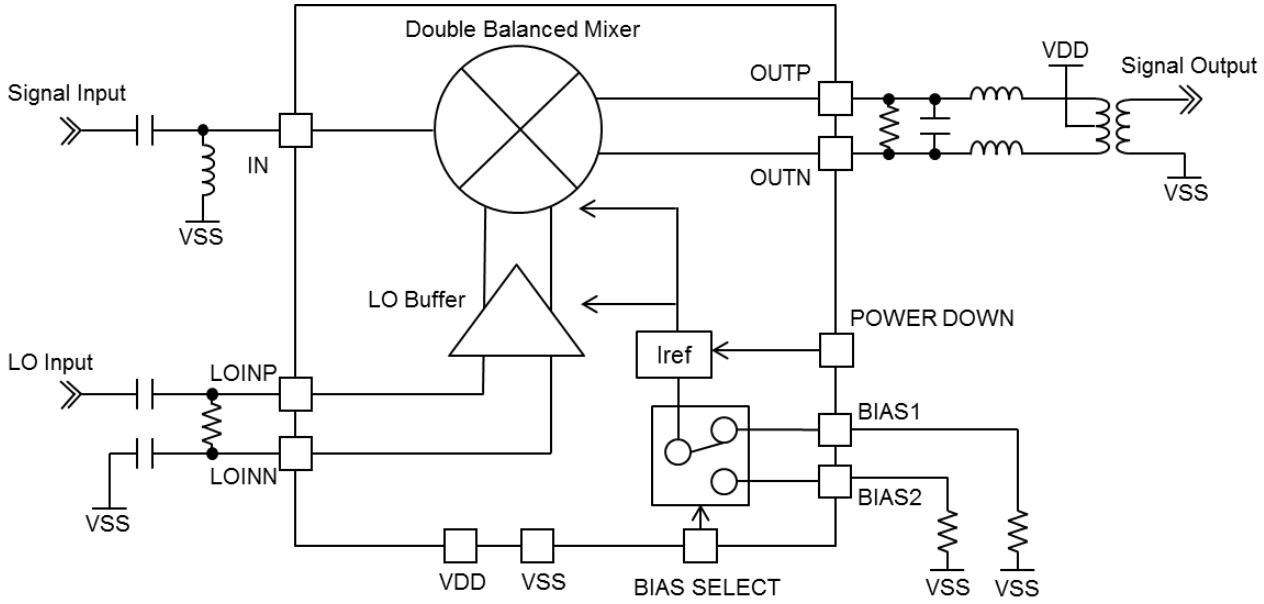


Figure 1. Block Diagram

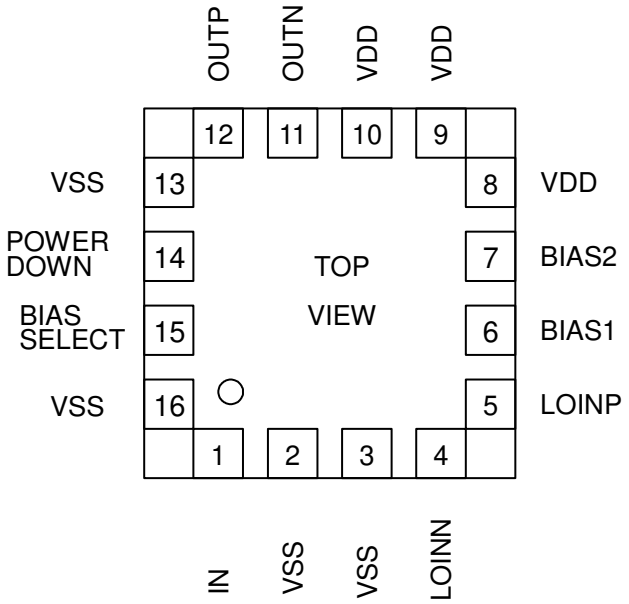


Figure 2. Package Pin Layout

6. Pin Functions Description

Table 1. Pin Function

No.	Name	I/O	Pin Function	Remarks
1	IN	AI	Signal input	Connecting a inductor between this pin and ground.
2	VSS	G	Ground pin	
3	VSS	G	Ground pin	
4	LOINN	AI	LO Input Negative	
5	LOINP	AI	LO Input Positive	
6	BIAS1	AIO	Resistance pin for current adjustment	Connecting a resistor between this pin and ground.
7	BIAS2	AIO	Resistance pin for current adjustment	Connecting a resistor between this pin and ground.
8	VDD	P	Power Supply	
9	VDD	P	Power Supply	
10	VDD	P	Power Supply	
11	OUTN	AO	Signal Output Negative	This pin is open drain output. It needs power feeding via an inductor.
12	OUTP	AO	Signal Output Positive	This pin is open drain output. It needs power feeding via an inductor.
13	VSS	G	Ground pin	
14	POWER DOWN	DI	Power Down control pin	High : Power OFF Low : Power ON
15	BIAS SELECT	DI	Bias Resistance select pin	High : BIAS2 pin is enabled Low : BIAS1 pin is enabled
16	VSS	G	Ground pin	

Note 1. The exposed pad at the center of the backside should be connected to ground.
Note 2. With the power supply voltage is not applied to VDD, do not apply a voltage to each input pin.

AI:Analog input pin	AO:Analog output pin	AIO:Analog I/O pin
P: Power supply pin	G: Ground pin	DI:Digital input pin

7.Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	Vdd	-0.3	5.5	V	
Signal Input Power	INPOW		12	dBm	
LO Input Power	LOPOW		12	dBm	
Storage Temperature	Tstg	-55	125	°C	

Exceeding these maximum ratings may result in damage to the AK1228. Normal operation is not guaranteed at these extremes.

8.Reccomended Operating Conditions

Table 3. Recommended Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating Temperature	Ta	-40		85	°C	
Supply Voltage	Vdd	2.7	5	5.25	V	

The specifications are applicable within the recommended operating range (supply voltage/operating temperature).

9. Electrical Characteristics

1.Analog Circuit Characteristics
Unless otherwise noted Signal Output = 50MHz, Output Load Resistor (Rload) = 2.2kΩ, Vdd = 2.7 to 5.25V, Ta = -40 to 85°C, LO Input Level = -10dBm to +5dBm. Test circuit is shown in Figure 3.

Table 4. Analog Circuit Characteristics

Parameter	Min.	Typ.	Max.	Unit	Remarks
Signal Input Frequency	10		2000	MHz	
LO Input Frequency	10		2000	MHz	
Signal Output Frequency	10		1000	MHz	
LO Input Power	-10	0	+5	dBm	
Current Adjustment Resistor (Rbias)	39		100	kΩ	
IDD (Rbias = 39kΩ)	7.5	10.5	15	mA	The total current of VDD, OUTP pin and OUTN pin.
IDD (Rbias = 100kΩ)	3	4.5	6.5	mA	
IDD (POWER DOWN = Vdd)		1	10	uA	
IN = 600MHz, LOIN = 550MHz(0dBm), Rbias = 39kΩ, Vdd = 3V					
Conversion Gain	1.5	4	6	dB	
SSB Noise Figure (NF)		8.5	11	dB	Design guarantee value
IP1dB	-5	-1		dBm	
IIP3	8	12		dBm	Design guarantee value

2. Digital Circuit Characteristics
This table is for POWER DOWN pin and BIAS SELECT pin.

Table 5. Digital Circuit Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
High level input voltage	Vih		0.8×Vdd			V	
Low level input voltage	Vil				0.2×Vdd	V	
High level input current	Iih	Vih = Vdd=5.25V	-1		1	μA	
Low level input current	Iil	Vil = 0V, Vdd=5.25V	-1		1	μA	

10. Typical Performance

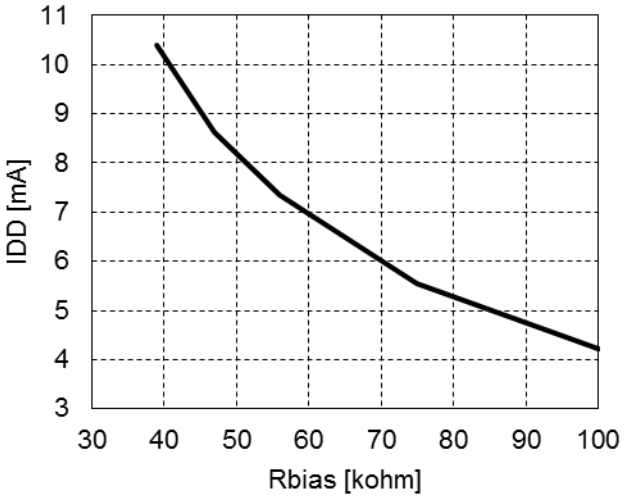
Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm, Current Adjustment Resistor (Rbias) = 39kΩ. Test circuit is shown in Figure 3.

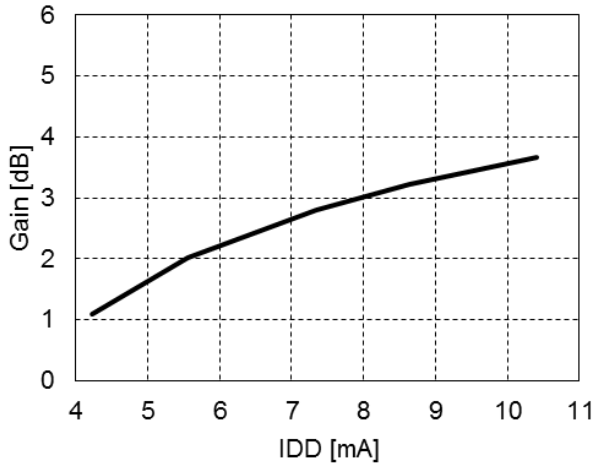
Table 6. Typical Performance

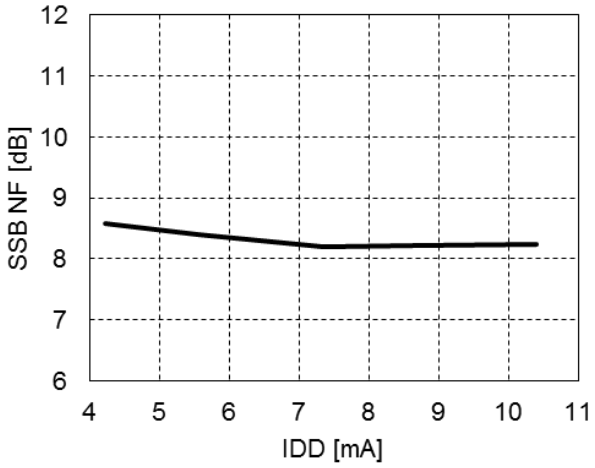
Parameter	Frequency	Min. Typ. Max.	Unit
Conversion Gain	IN = 160MHz, OUT = 70MHz , LOIN = 230MHz	3.7	dB
	IN = 400MHz, OUT = 70MHz , LOIN = 470MHz	3.7	
	IN = 800MHz, OUT = 11MHz , LOIN = 811MHz	3.3	
	IN = 1500MHz, OUT = 250MHz, LOIN = 1250MHz	2.8	
	IN = 50MHz, OUT = 450MHz, LOIN = 400MHz	2.7	
SSB Noise Figure (NF)	IN = 160MHz, OUT = 70MHz, LOIN = 230MHz	8.5	dB
	IN = 400MHz, OUT = 70MHz, LOIN = 470MHz	8.5	
	IN = 800MHz, OUT = 11MHz, LOIN = 811MHz	9.6	
	IN = 1500MHz, OUT = 250MHz, LOIN = 1250MHz	10.3	
	IN = 50MHz, OUT = 450MHz, LOIN = 400MHz	9.9	
IP1dB	IN = 160MHz, OUT = 70MHz, LOIN = 230MHz	2.0	dBm
	IN = 400MHz, OUT = 70MHz, LOIN = 470MHz	3.1	
	IN = 800MHz, OUT = 11MHz, LOIN = 811MHz	1.6	
	IN = 1500MHz, OUT = 250MHz, LOIN = 1250MHz	1.5	
	IN = 50MHz, OUT = 450MHz, LOIN = 400MHz	1.5	
IIP3	IN = 160MHz, OUT = 70MHz, LOIN = 230MHz	14.0	dBm
	IN = 400MHz, OUT = 70MHz, LOIN = 470MHz	13.7	
	IN = 800MHz, OUT = 11MHz, LOIN = 811MHz	12.0	
	IN = 1500MHz, OUT = 250MHz, LOIN = 1250MHz	10.1	
	IN = 50MHz, OUT = 450MHz, LOIN = 400MHz	13.4	

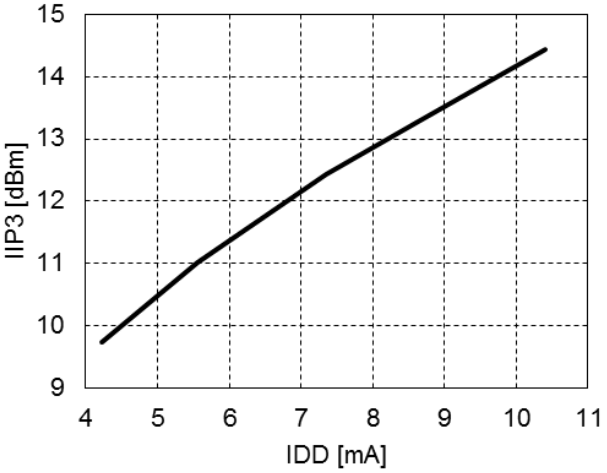
1. Current Adjustment Resistor vs. IDD, IDD vs. Gain, NF, IIP3, IP1dB

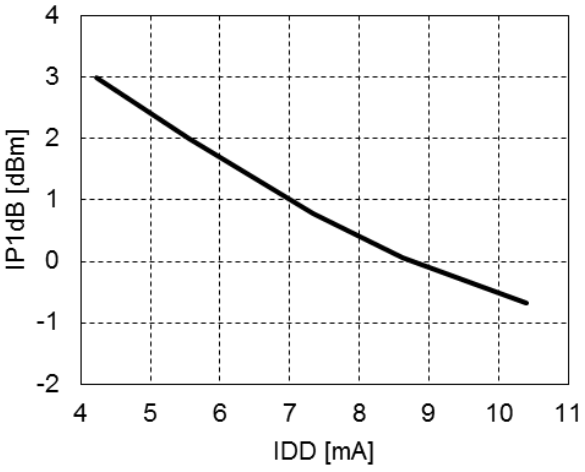
The analog circuit characteristics and power consumption performances can be optimized by the resistance connected to the BIAS Pin (Rbias). Signal Input = 600MHz, Signal Output = 50MHz, LO Input = 550MHz, Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm, Current Adjustment Resistor (Rbias) = 39kΩ.





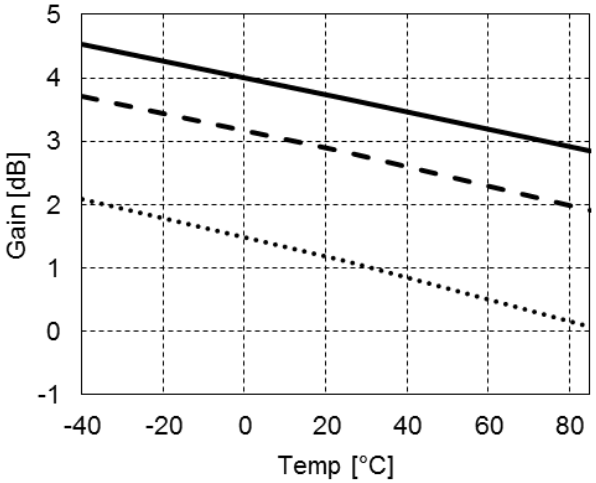


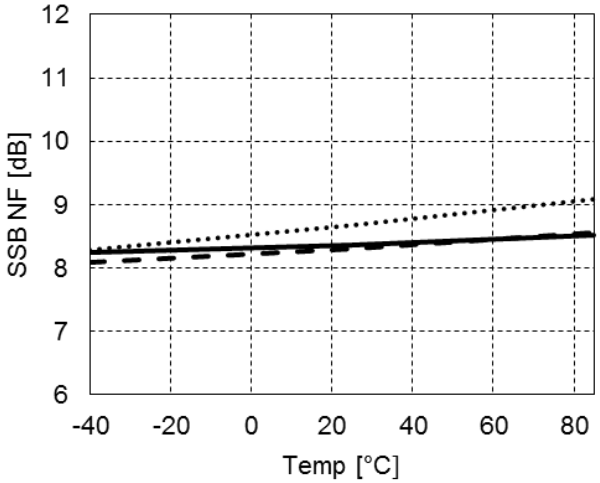


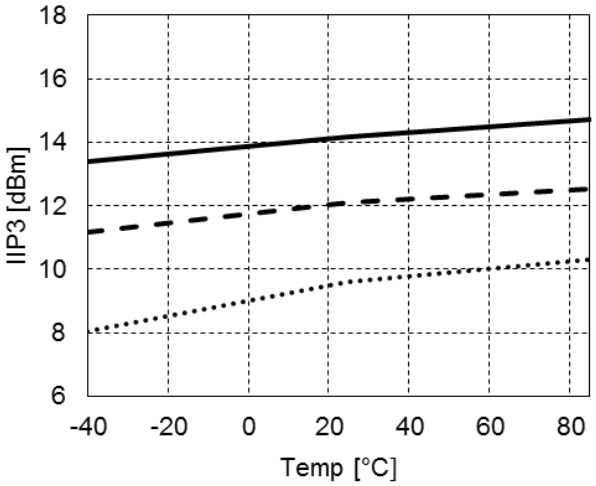


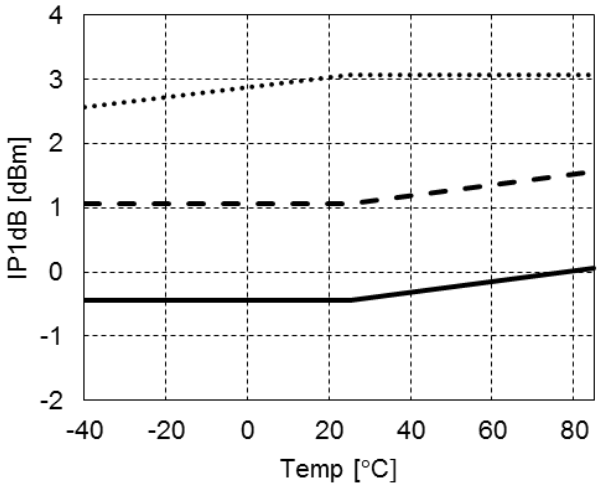
2. Temperature vs. Gain, NF, IIP3, IP1dB, IDD

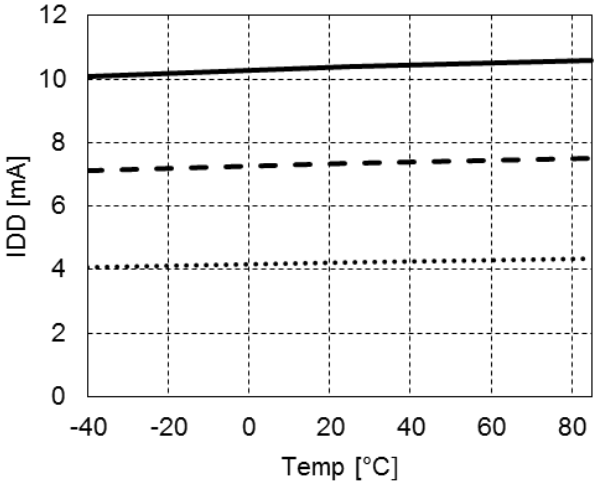
Signal Input = 600MHz, Signal Output = 50MHz, LO Input = 550MHz,Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, LO Input Level = 0dBm.











Resistance for current adjustment

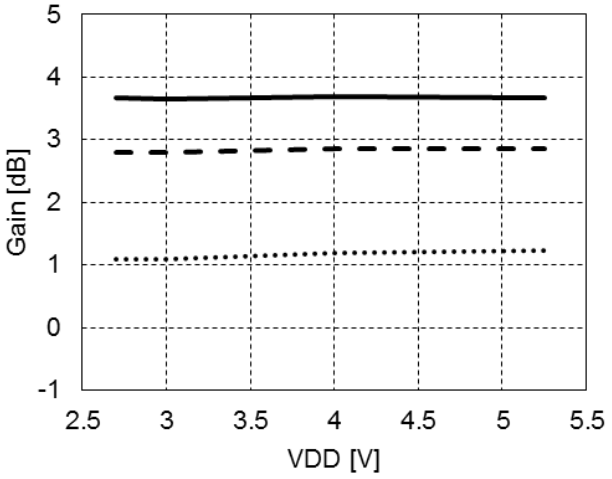
39kΩ (≅10.5mA)

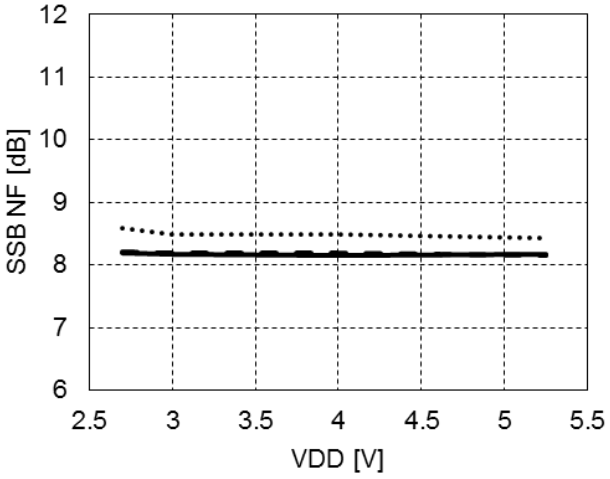
56kΩ (≅7.5mA)

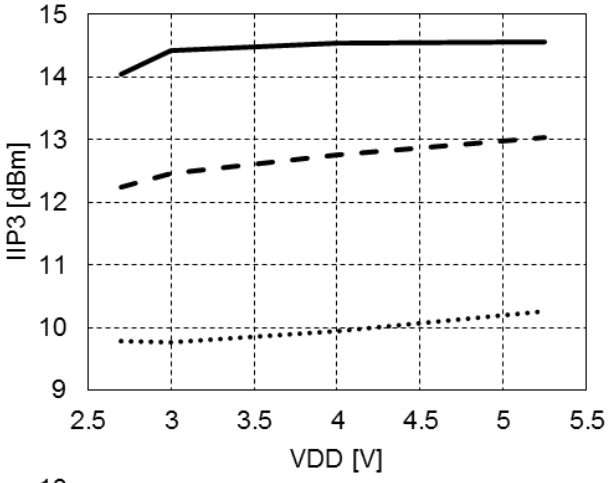
100kΩ (≅4.5mA)

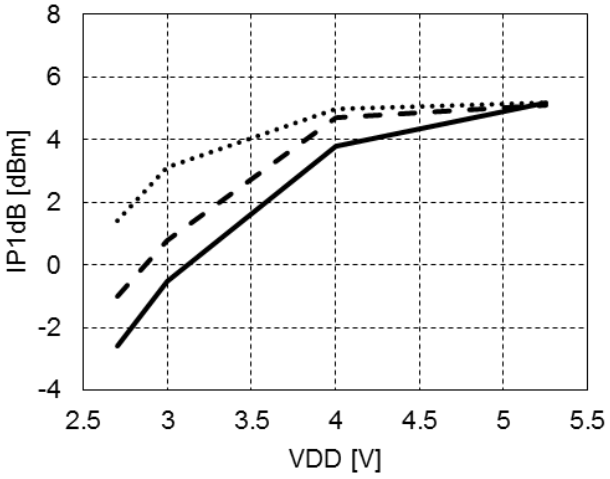
3. Supply voltage vs. Gain, NF, IIP3, IP1dB, IDD

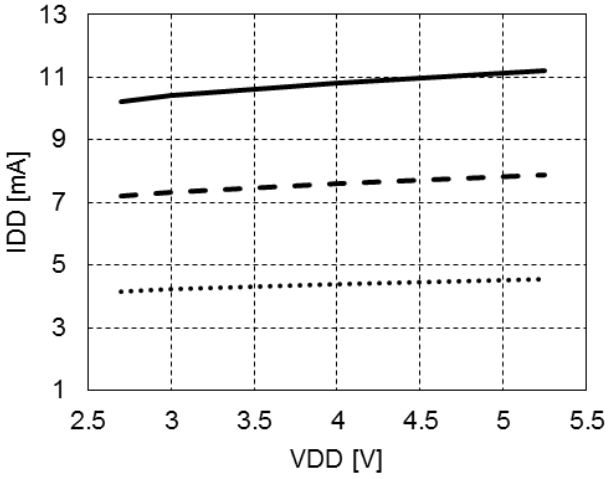
Signal Input = 600MHz, Signal Output = 50MHz, LO Input = 550MHz, Output Load Resistor (Rload) = 2.2kΩ, Ta = 25°C, LO Input Level = 0dBm.











Resistance for current adjustment

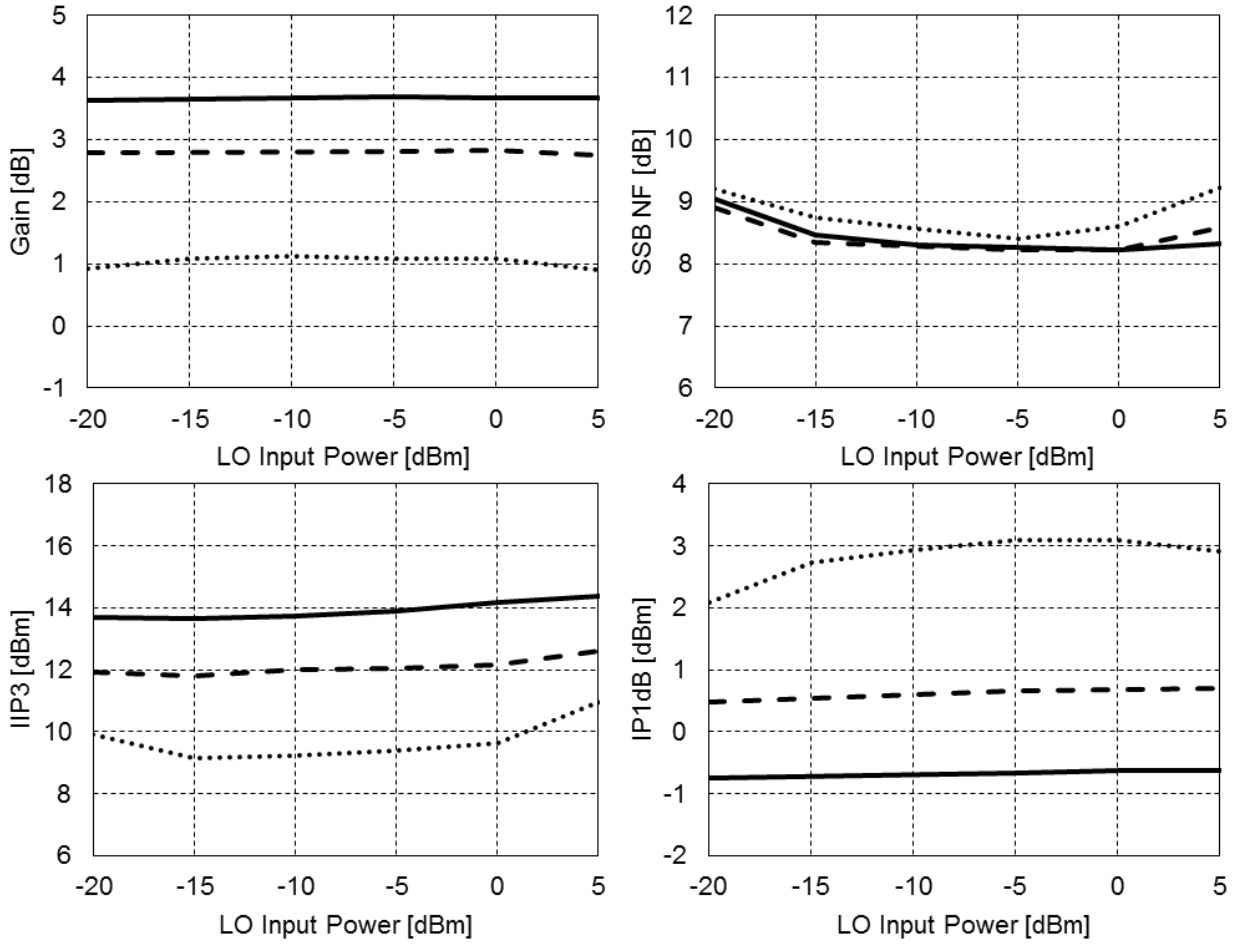
39kΩ (≅10.5mA)

56kΩ (≅7.5mA)

100kΩ (≅4.5mA)

4. LO input power vs. Gain, NF, IIP3, IP1dB

Signal Input = 600MHz, Signal Output = 50MHz, LO Input = 550MHz, Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C.



Resistance for current adjustment

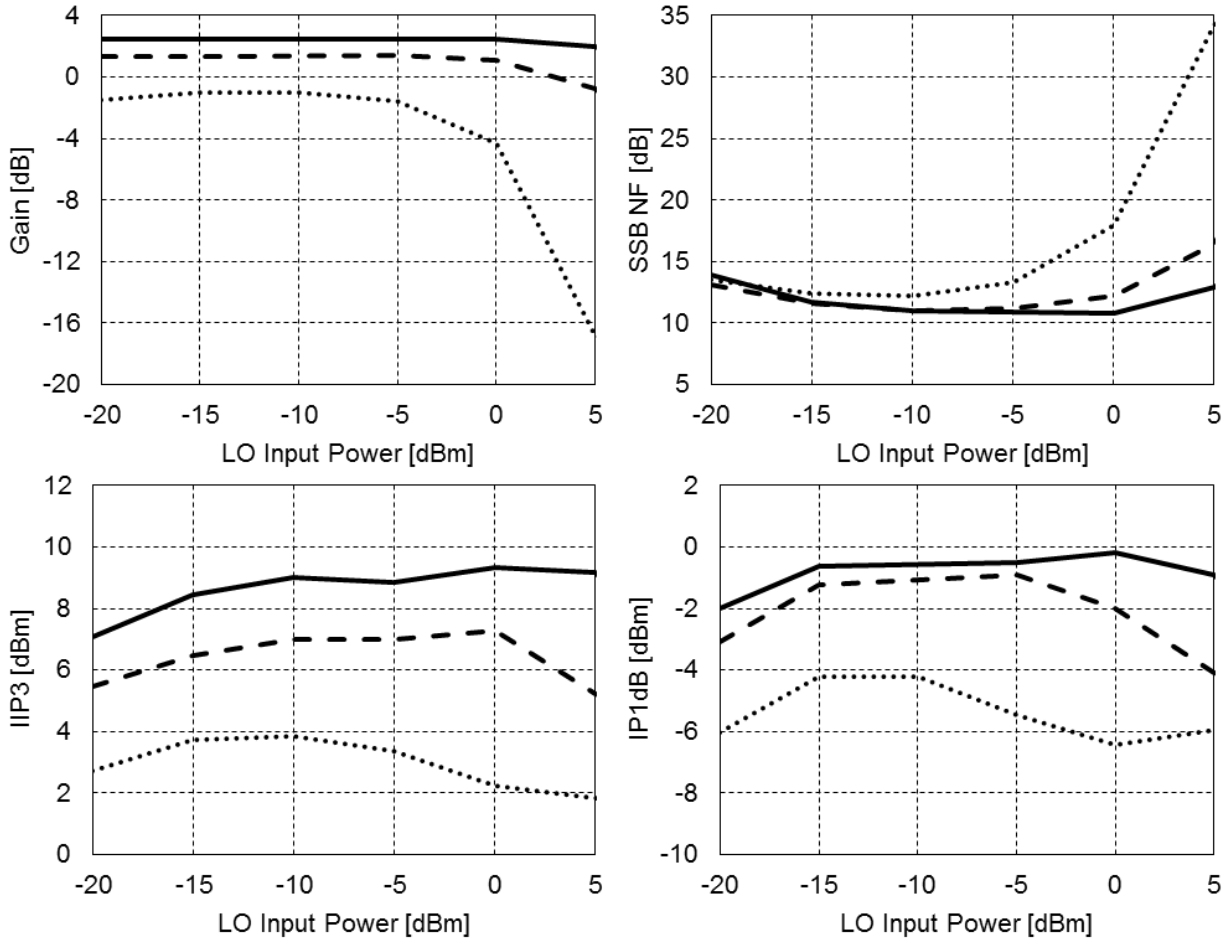
39kΩ (≅10.5mA)

56kΩ (≅7.5mA)

100kΩ (≅4.5mA)

Signal Input = 2000MHz, Signal Output = 50MHz, LO Input = 1950MHz, Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C.

For high signal input frequency usage, it is recommended to increase the current consumption and reduce the LO input level.



Resistance for current adjustment

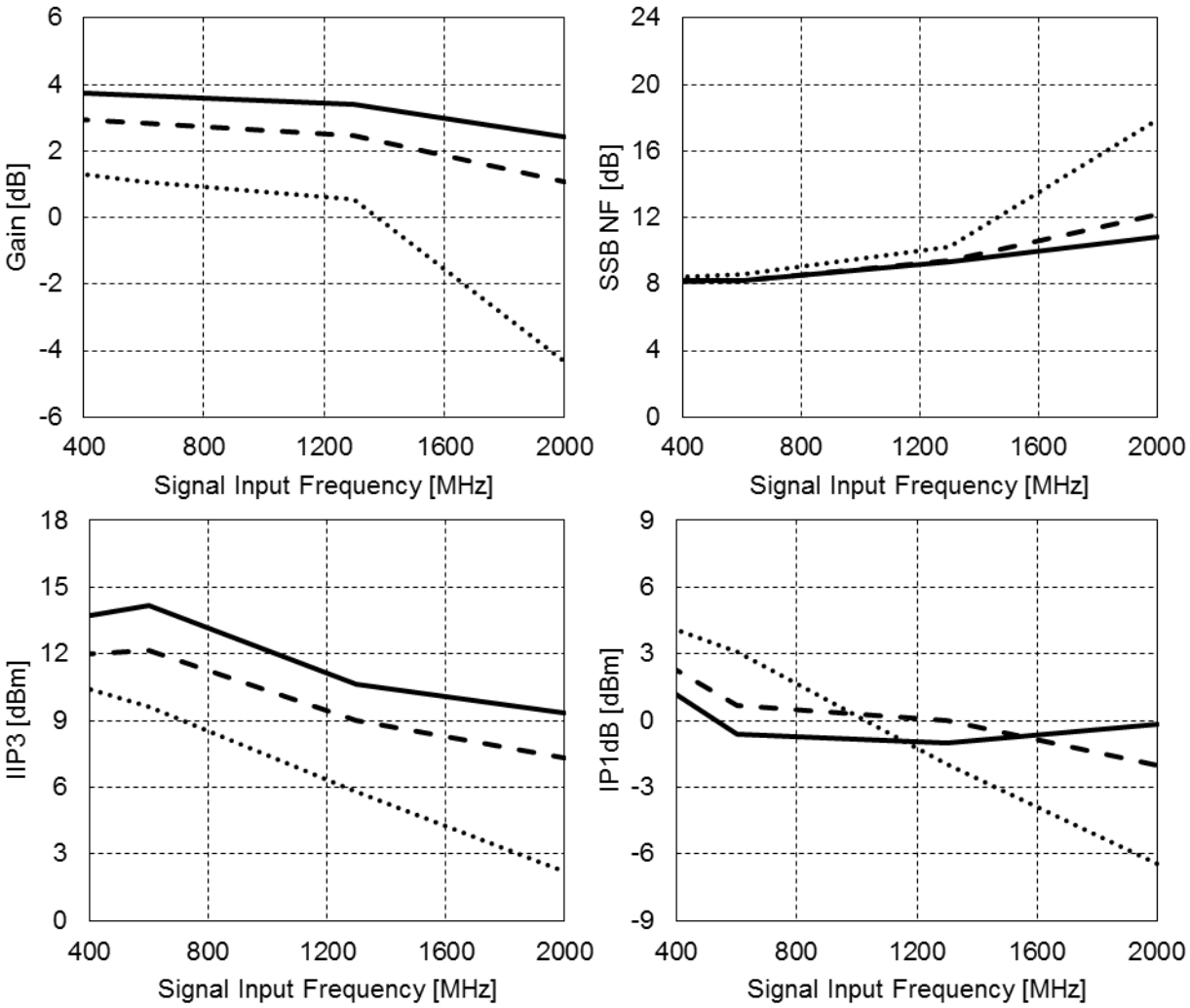
39kΩ (≅10.5mA)

56kΩ (≅7.5mA)

100kΩ (≅4.5mA)

5. Signal input frequency vs. Gain, NF, IIP3, IP1dB

Signal Input > 600MHz : LO Input frequency < Signal Input frequency (Lower LO)
Signal Input ≤ 600MHz : LO Input frequency > Signal Input frequency (Upper LO)
Signal Output = 50MHz, Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm.



Resistance for current adjustment

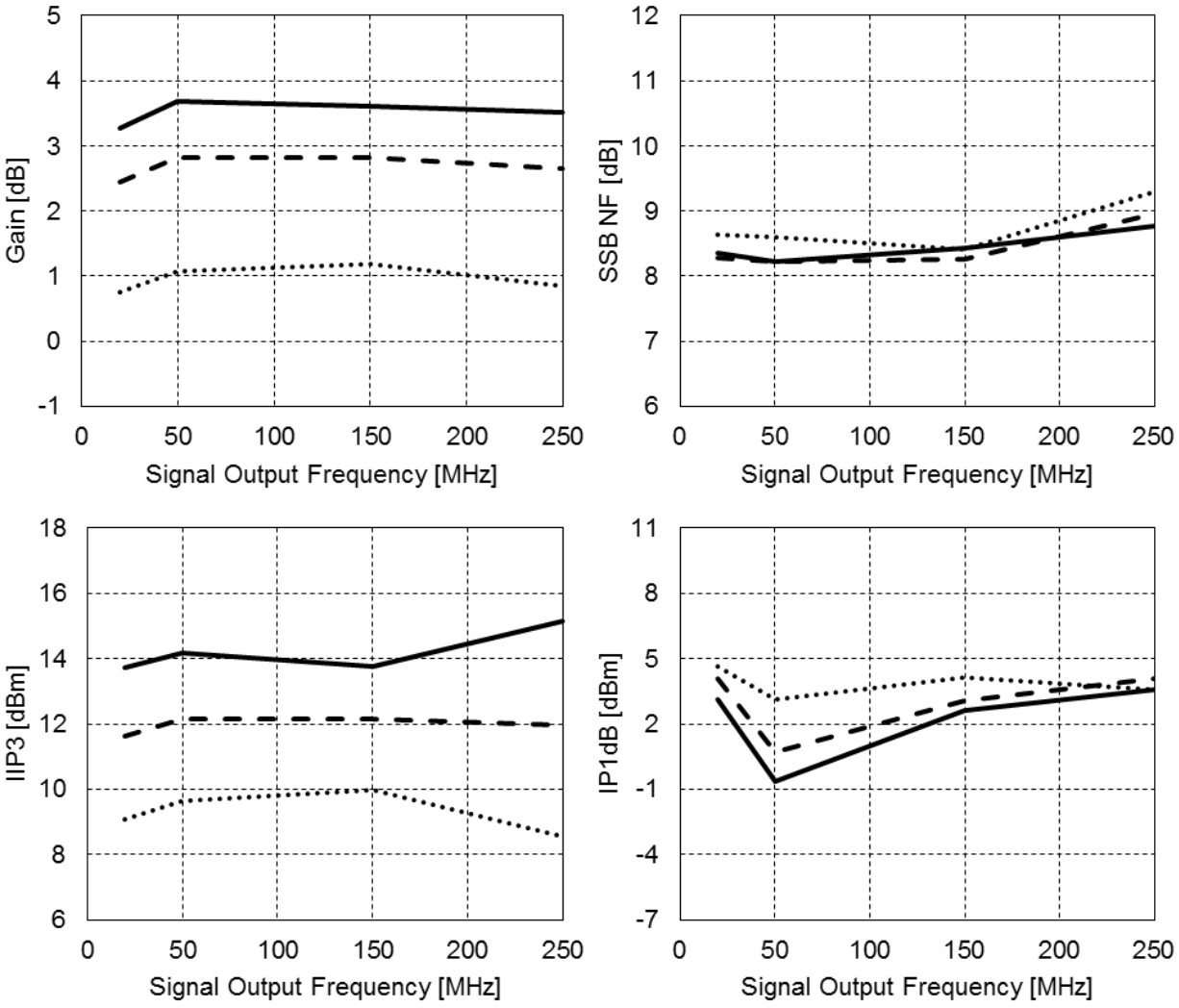
39kΩ (≅10.5mA)

56kΩ (≅7.5mA)

100kΩ (≅4.5mA)

6. Signal output frequency vs. Gain, NF, IIP3, IP1dB

Signal Output ≤ 150MHz : LO Input frequency < Signal Input frequency (Lower LO)
Signal Output > 150MHz : LO Input frequency > Signal Input frequency (Upper LO)
Signal Input = 600MHz, Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm.



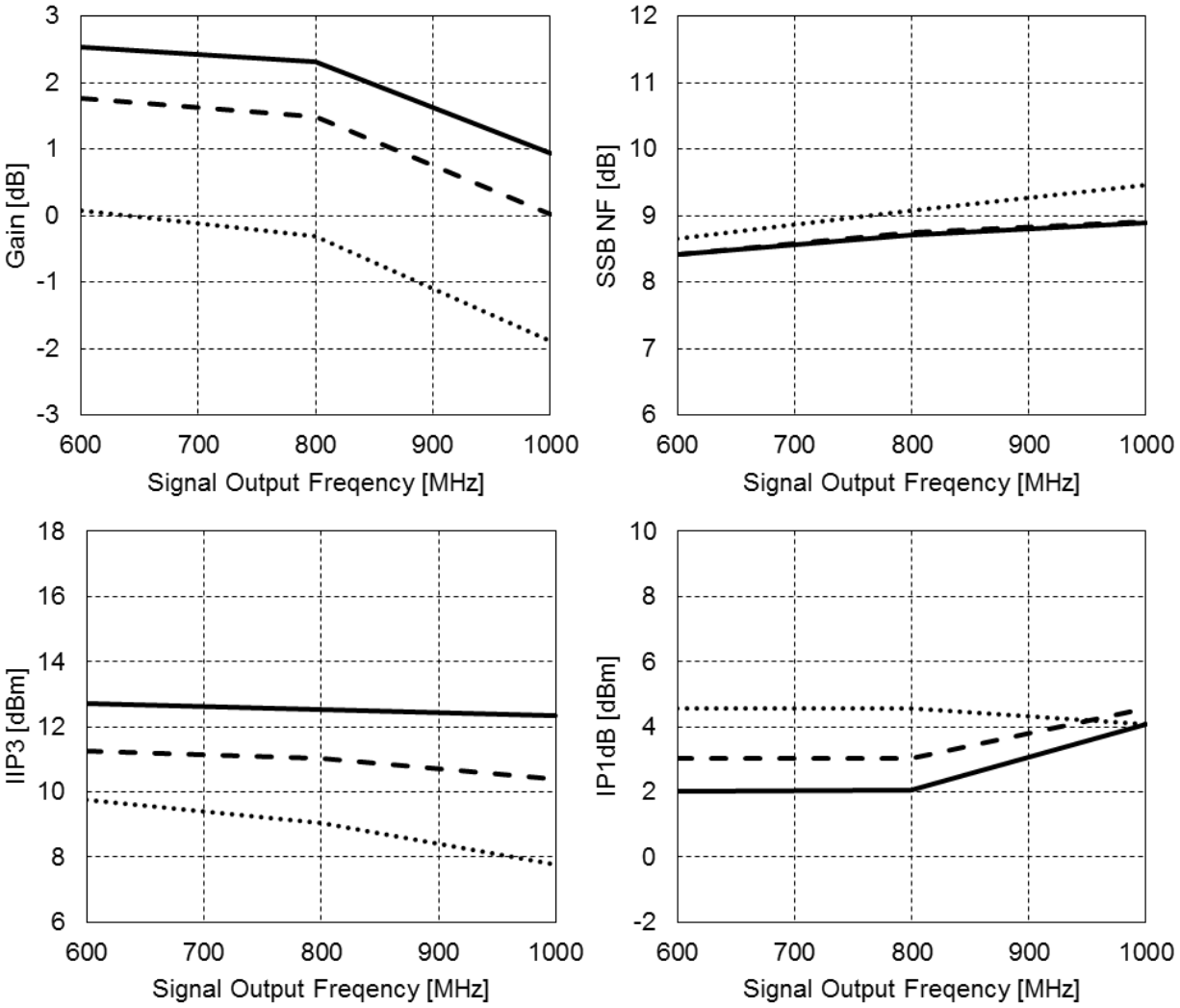
Resistance for current adjustment

39kΩ (≅10.5mA)

56kΩ (≅7.5mA)

100kΩ (≅4.5mA)

Signal Input = 140MHz, LO Input frequency < Signal Output frequency (Lower LO), Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm.



Resistance for current adjustment

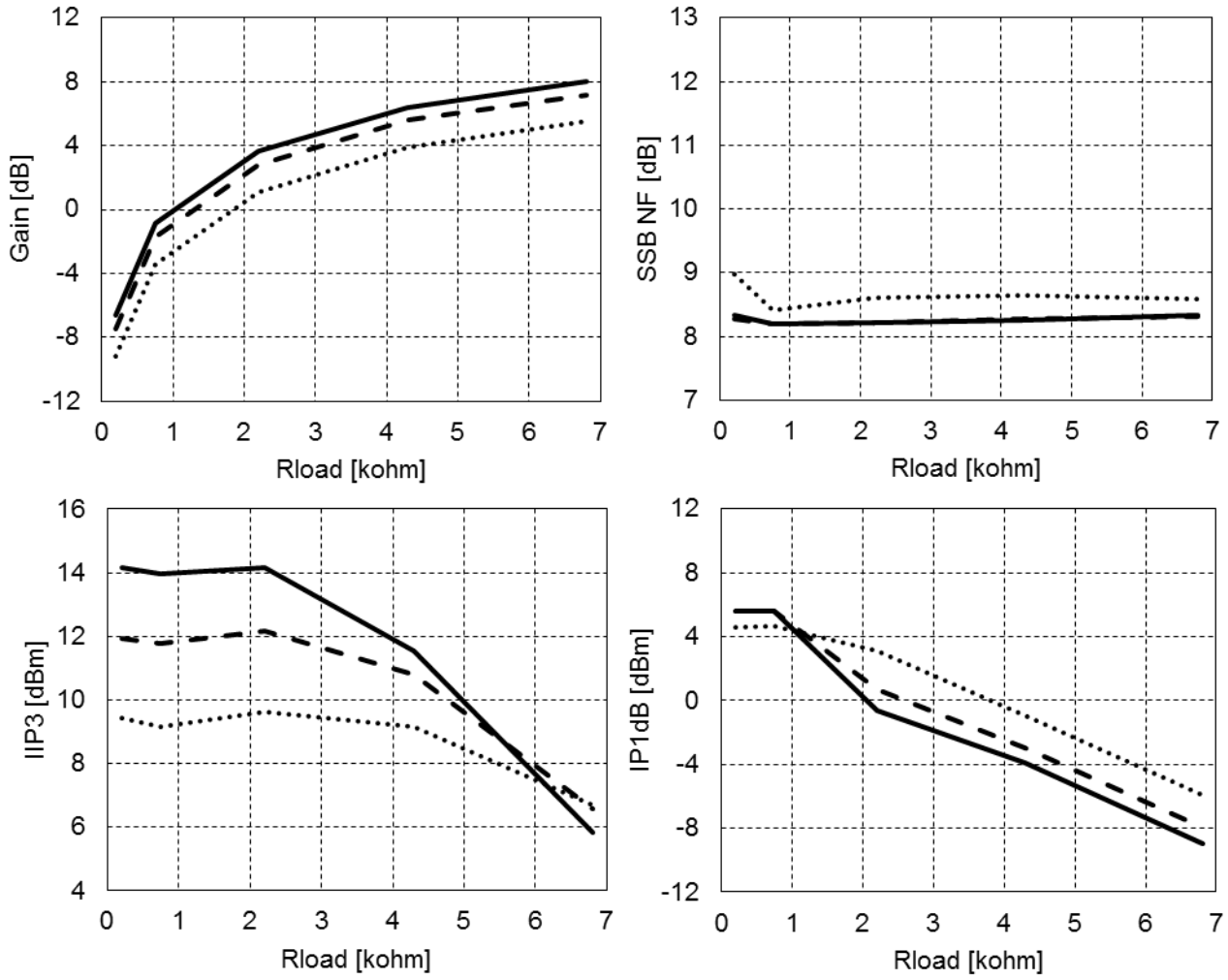
39kΩ (≅10.5mA)

56kΩ (≅7.5mA)

100kΩ (≅4.5mA)

7. Output Load Resistor (Rload) vs. Gain, NF, IIP3, IP1dB

Signal output ports are differential open drain outputs. Gain can be optimized by the resistance connected to the OUTP and OUTN Pins (Rload). Signal Input = 600MHz, Signal Output = 50MHz, LO Input = 550MHz, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm.



Resistance for current adjustment

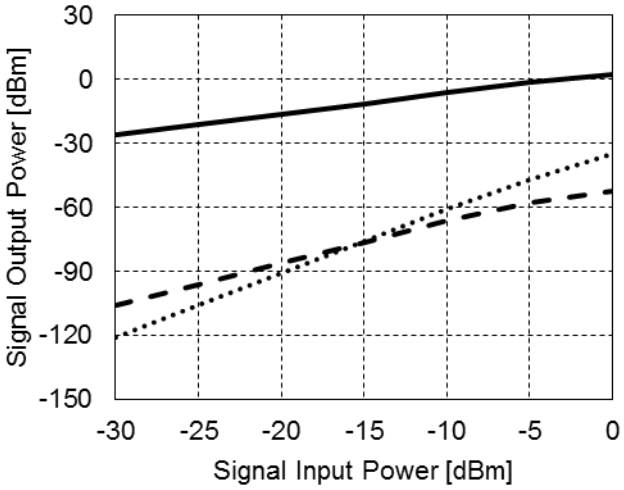
39kΩ (≅10.5mA)

56kΩ (≅7.5mA)

100kΩ (≅4.5mA)

8. Half IF, 1/3 IF

IF Signal Output = 50MHz, LO Input = 550MHz, Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm, Current Adjustment Resistor (Rbias) = 39kΩ.



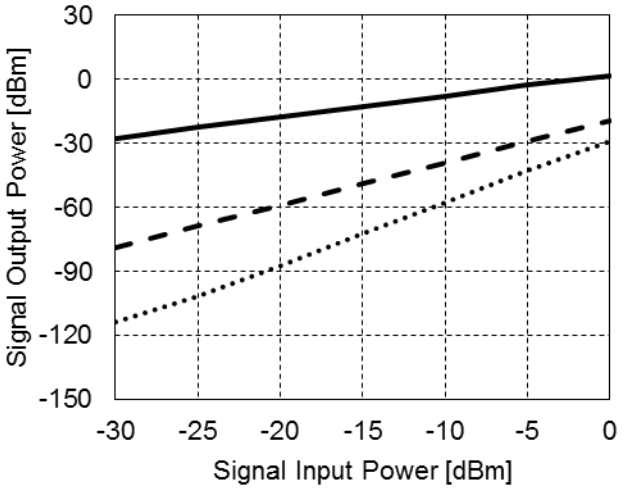
RF Signal Input Frequency

RF = 600MHz

LO + IF/2 = 575MHz

LO + IF/3 = 566.7MHz

IF Signal Output = 50MHz, LO Input = 1950MHz, Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm, Current Adjustment Resistor (Rbias) = 39kΩ.



RF Signal Input Frequency

RF = 2000MHz

LO + IF/2 = 1975MHz

LO + IF/3 = 1966.7MHz

9. Leakage

Signal Output = 50MHz, LO Input frequency < Signal Input frequency (Lower LO), Signal Input Level = -20dBm, Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm, Current Adjustment Resistor (Rbias) = 39kΩ.

Table 7. Leakage

Parameter	Signal Input Frequency	Typ. [dBc]
IN – LO Leakage	600MHz	-54
	2000MHz	-54
IN – OUT Leakage	600MHz	-48
	2000MHz	-48
LO – IN Leakage	600MHz	-47
	2000MHz	-40
LO – OUT Leakage	600MHz	-57
	2000MHz	-71

11. Typical Evaluation Board Schematic

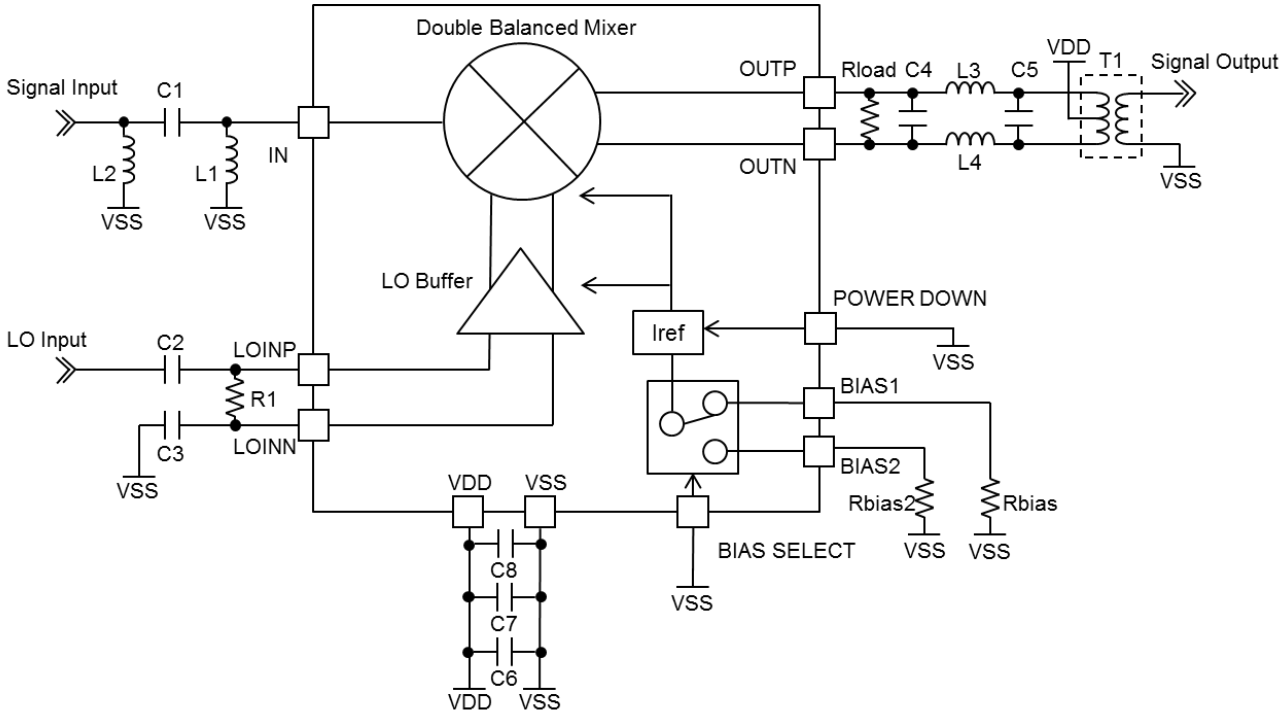


Figure 3. Typical Evaluation Board Schematic

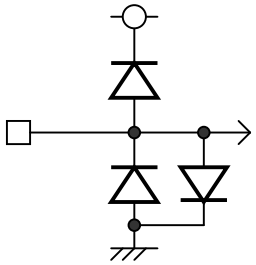
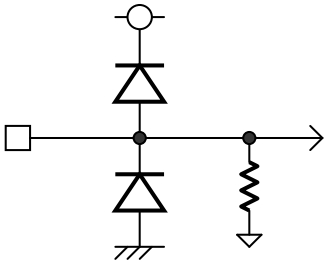
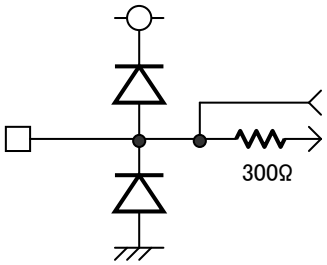
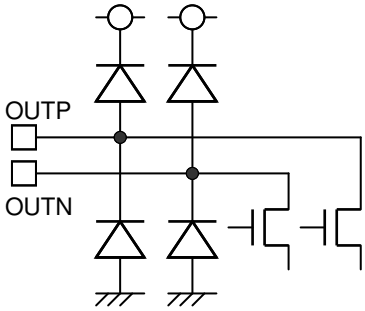
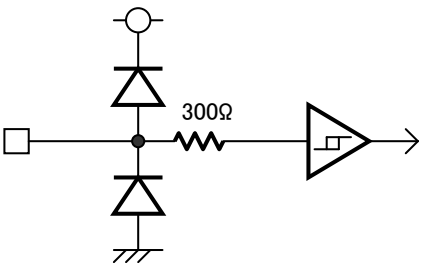
Table 8. Typical Evaluation Board Component Values for Downconversion Applications
(Signal Input = 600MHz, Signal Output = 50MHz)

Ref.	Value	Size	Part Number	Ref.	Value	Size	Part Number
T1	4:1		Mini-Circuits ADT4-6T	C1	8.2pF	1005	Murata GRM1552C1H8R2DZ01
R1	51Ω	1005	KOA RK73K1ETP510	C2	10nF	1005	Murata GRM155B31H103KA88
Rload	2.2kΩ	1005	KOA RK73K1ETP222	C3	10nF	1005	Murata GRM155B31H103KA88
Rbias	39kΩ	1005	KOA RK73K1ETP393	C4	3.3pF	1005	Murata GRM1553C1H3R3CZ01
Rbias2	100kΩ	1005	KOA RK73K1ETP104	C5	-	-	Not Mounted
L1	15nH	1005	Murata LQG15HS15NJ02	C6	10uF	1608	Murata GRM188R60J106ME47
L2	-	-	Not Mounted	C7	10nF	1005	Murata GRM155B31H103KA88
L3	1000nH	2012	Murata LQW21HN1R2J00	C8	100pF	1005	Murata GRM1552C1H101JA01
L4	1000nH	2012	Murata LQW21HN1R2J00				

Table 9. Typical Evaluation Board Component Values for Upconversion Applications
(Signal Input = 50MHz, Signal Output = 450MHz)

Ref.	Value	Size	Part Number	Ref.	Value	Size	Part Number
T1	4:1		Mini-Circuits JTX4-10T	C1	120pF	1005	Murata GRM1552C1H121JA01
R1	51Ω	1005	KOA RK73K1ETP510	C2	10nF	1005	Murata GRM155B31H103KA88
Rload	2.2kΩ	1005	KOA RK73K1ETP222	C3	10nF	1005	Murata GRM155B31H103KA88
Rbias	39kΩ	1005	KOA RK73K1ETP393	C4	-	-	Not Mounted
Rbias2	100kΩ	1005	KOA RK73K1ETP104	C5	2.7pF	1005	Murata GRM1553C1H2R7CZ01
L1	270nH	1005	Murata LQG15HSR27J02	C6	10uF	1608	Murata GRM188R60J106ME47
L2	-	-	Not Mounted	C7	10nF	1005	Murata GRM155B31H103KA88
L3	68nH	1608	Murata LQW18AN68NG00	C8	100pF	1005	Murata GRM1552C1H101JA01
L4	68nH	1608	Murata LQW18AN68NG00				

12. LSI Interface Schematic

No.	Name	I/O	Function
1	IN	I	**Signal Input pin** 
4	LOINN	I	**LO Input pins**
5	LOINP		
6	BIAS1	I/O	**Analog I/O pins**
7	BIAS2		
11	OUTN	O	**Signal Output pins**
12	OUTP		
14	POWER DOWN	I	**Digital Input pins**
15	BIAS SELECT		

13. Application Information

•Impedance matching network for Signal Input pin

Signal Input port with impedance matching network (highpass filter) is shown in Figure 4. Typical evaluation board component values in 50Ω interface are shown in Table 10.

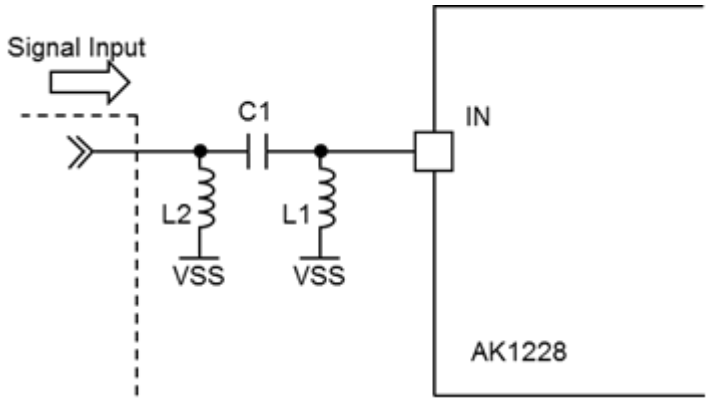


Figure 4. Signal Input port with impedance matching network

Table 10. Signal Input port with impedance matching network

Signal Input Frequency [MHz]	C1 [pF]	L1 [nH]	L2 [nH]
10	470	1500	-
160	27	82	-
300	15	47	-
400	10	22	-
600	8.2	15	-
800	5.6	9.1	-
1300	8.2	5.6	-
1500	5.6	3.3	-
2000	3.3	18	2.2

•Impedance matching network for LO Input pin

LOIN port can be matched with resistive impedance matching network in 10MHz < LO Input < 2000MHz.
Typical evaluation board component values in 50Ω interface is shown in Figure 5.

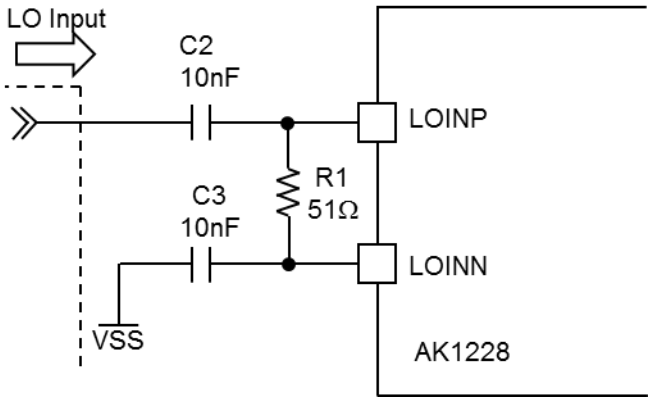


Figure 5. LO input port with impedance matching network

•Impedance matching network for Signal Output pin

Signal output port with impedance matching network (lowpass filter and balun) is shown in Figure 6.
OUTP and OUTN pins need power feeding via center tap of balun.
Typical evaluation board component values in 50Ω interface are shown in Table 11.

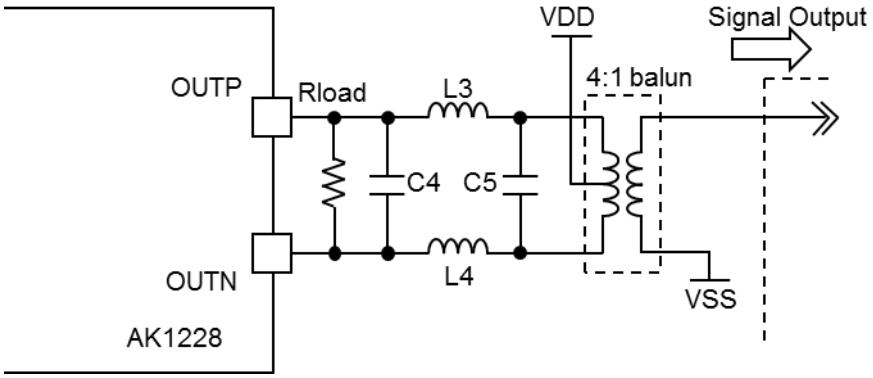


Figure 6. Signal output port with impedance matching network

Table 11. Signal output port with impedance matching network

Signal Output Frequency [MHz]	Rload [kΩ]	L3/L4 [nH]	C4 [pF]	C5 [pF]
11	2.2	4700	18	-
20	2.2	2200	10	-
50	2.2	1000	3.3	-
70	2.2	680	2.2	-
100	2.2	470	1.2	-
150	2.2	330	0.4	-
250	2.2	180	-	0.5
800	2.2	22	-	2.2

•Impedance matching network with LC

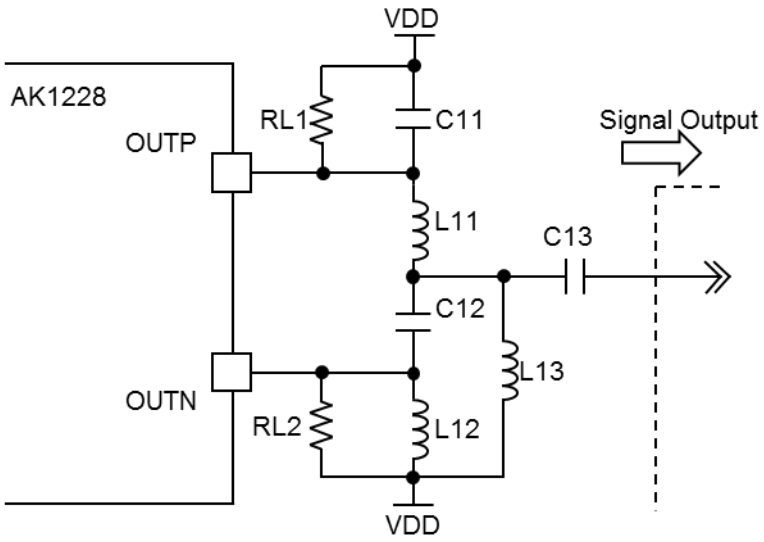


Figure 7. Impedance matching network with LC

Impedance matching network with LC is shown in Figure 7. AK1228 has open drain outputs, so RL1 + RL2 is output load resistance. C11and L11 compose lowpass filter. C12 and L12 are for highpass filter. C13 is DC blocking capacitor and L13 is RF choke. OUTP and OUTN pins need power feeding via L11, L12 and L13.

The differential voltage from OUTP/N can be converted to a single-ended by L11, L12, C11 and C12 properly.
The differential impedance (RL1 + RL2) is converted to single-ended output terminating impedance Ro.

L11, C11, L12 and C12 are calculated as below. f_{out} is signal output frequency.

$$C_{11} = C_{12} = \frac{1}{2\pi * f_{OUT} * \sqrt{(R_{L1} + R_{L2}) * R_O}}$$

$$L_{11} = L_{12} = \frac{\sqrt{(R_{L1} + R_{L2}) * R_O}}{2\pi * f_{OUT}}$$

For example, in the case of Signal Output = 50MHz, Output Load Resistor (Rload) = 2.2kΩ in 50Ω interface, L11, C11, L12 and C12 are calculated as below.

$$C_{11} = C_{12} = \frac{1}{2\pi * (50*10\text{^}6) * \sqrt{(2.2*10\text{^}3) * 50}} = 9.6\text{pF}$$

$$L_{11} = L_{12} = \frac{\sqrt{(2.2*10\text{^}3) * 50}}{2\pi * (50*10\text{^}6)} = 1056\text{nH}$$

L13 and C13 should be large enough not to affect the impedance at signal output frequency. In some cases the impedance matching can be optimized by L13 and C13.

For example, in the case of Signal Output = 50MHz, Output Load Resistor (Rload) = 2.2kΩ in 50Ω interface, it is recommended to choose 2200nH and 1000pF as L13 and C13. If any correction is needed, it can be adjusted by reducing the value of L13 and C13.

These calculated values are approximation. In some cases, some correction is needed due to the effect of parasitic capacitance of external parts or/and PCBs. The impedance matching network components should be decided through enough evaluation on AK1228.

Typical Performance using impedance matching network with LC is below. Signal Input = 600MHz, Signal Output = 50MHz, LO Input = 550MHz, Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm,

Table 12. Typical Component Values using impedance matching with LC

Ref.	Value	Size	Part Number
RL1, RL2	1.1kΩ	1005	KOA RK73K1ETP112
L11, L12	1000nH	2012	Murata LQW21HN1R0J00
C11, C12	10pF	1005	Murata GRM1552C1H100JA01
L13	2200nH	2012	Murata LQW21HN2R2J00
C13	150pF	1005	Murata GRM1552C1H151JA01

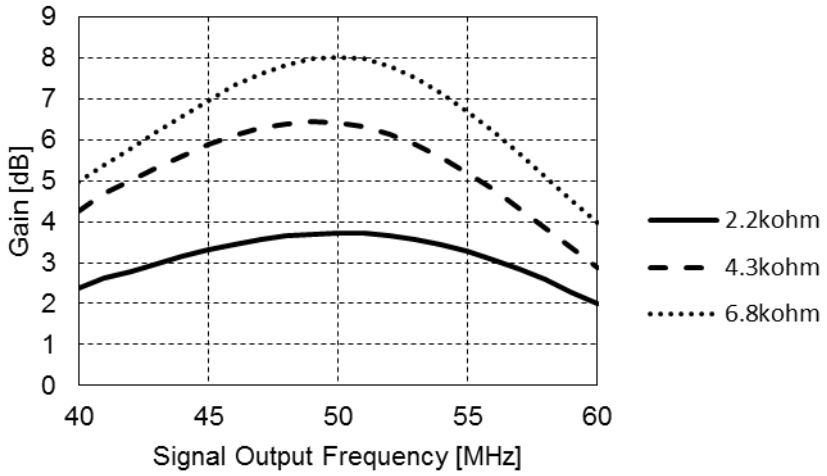
Table 13. Typical Performance using impedance matching with LC

Parameter	Rbias	Min. Typ. Max.	Unit
Conversion Gain	Rbias = 39kΩ (≅10.5mA) Rbias = 100kΩ (≅4.5mA)	3.6 1.3	dB
SSB Noise Figure (NF)	Rbias = 39kΩ (≅10.5mA) Rbias = 100kΩ (≅4.5mA)	8.6 8.5	dB
IP1dB	Rbias = 39kΩ (≅10.5mA) Rbias = 100kΩ (≅4.5mA)	2.1 3.6	dBm
IIP3	Rbias = 39kΩ (≅10.5mA) Rbias = 100kΩ (≅4.5mA)	15.5 9.6	dBm

The phase and amplitude balance is achieved at IF Output frequency by using impedance matching network with LC. The port-to-port leakage is improved with the phase and amplitude balance is achieved at RF, LO, and IF frequency with wide band balun.

•Output Load Resistor and Gain

Signal output ports are differential open drain outputs. Gain can be optimized by the resistance connected to the OUTP and OUTN Pins (Rload). Signal Input = 600±10MHz, Signal Output = 50±10MHz, LO Input = 550MHz, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm, Current Adjustment Resistor (Rbias) = 39kΩ. Test circuit is shown in Figure 3.



•The Improvement of Analog circuit characteristics with a differential LO input

AK1228 is a high linearity and low noise mixer that can be driven by a single ended LO. However it is possible to further improve the analog characteristics with a differential LO input. Gain, NF, HalfIF is improved by reducing the second-order distortion in exchange for the chip components increases four points. Test circuit is shown in Figure 8.

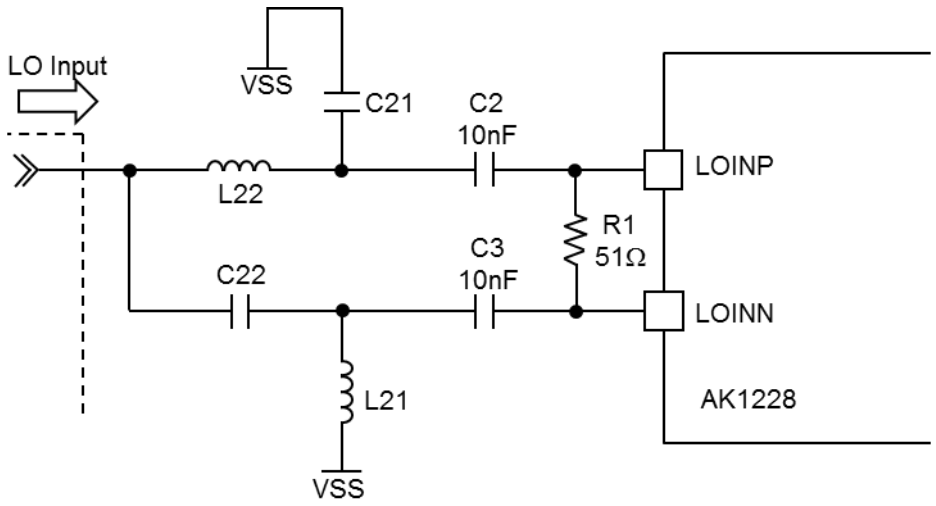


Figure 8. Example of Impedance matching network with a differential LO input

C21and L22 compose lowpass filter. C22 and L21 are for highpass filter. C2, C3 is DC blocking capacitor. The impedance of LOINP/N is high impedance so R1 is differential input resistance.

The single-ended LO input voltage can be converted to differential voltage of LOINP/N by L21, C21, L22 and C22 properly. The output resistance Ro of the previous stage is converted to a differential input resistance R1.

L21, C21, L22 and C22 are calculated as below. f_{LO} is LO input frequency.

$$C_{21} = C_{22} = \frac{1}{2\pi * f_{LO} * \sqrt{R_1 * R_{IN}}}$$

$$L_{21} = L_{22} = \frac{\sqrt{R_1 * R_{IN}}}{2\pi * f_{LO}}$$

For example, in the case of LO signal input = 1250MHz, differential input resistance R1 = 51Ω in 50Ω interface, L21, C21, L22 and C22 are calculated as below.

$$C_{21} = C_{22} = \frac{1}{2\pi * (1250 * 10\text{^}6) * \sqrt{51 * 50}} = 2.5\text{pF}$$

$$L_{21} = L_{22} = \frac{\sqrt{51 * 50}}{2\pi * (1250 * 10\text{^}6)} = 6.4\text{nH}$$

C2, C3 should be large enough not to affect the differential input impedance R1 at LO input frequency.

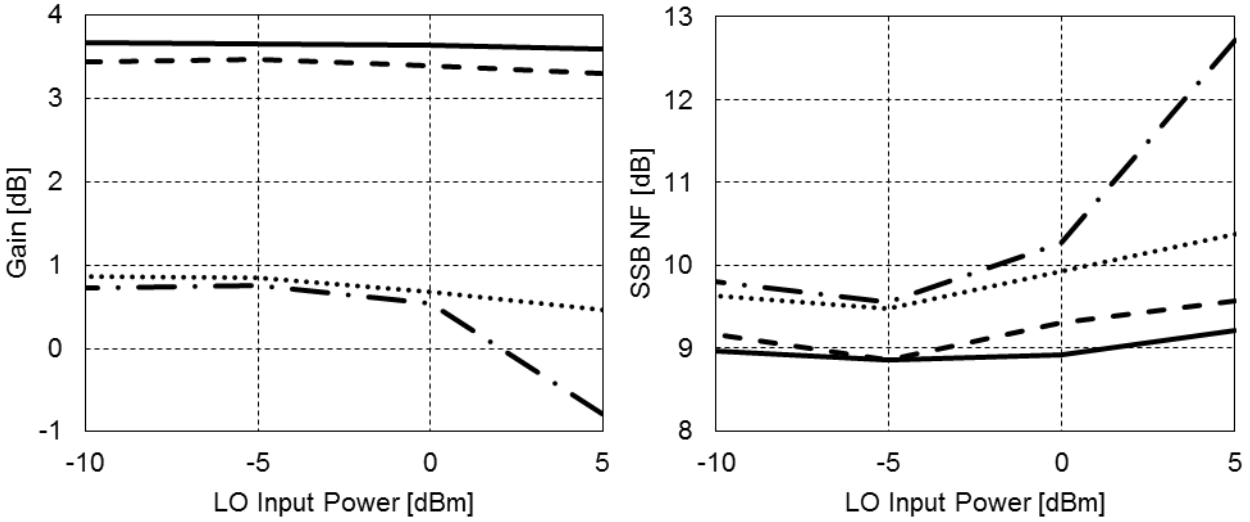
These calculated values are approximation. In some cases, some correction is needed due to the effect of parasitic capacitance of external parts or/and PCBs. The impedance matching network components should be decided through enough evaluation on AK1228.

Typical Performance using impedance matching network with a differential LO input is below. Signal Input = 1300MHz, Signal Output = 50MHz, LO Input = 1250MHz, Output Load Resistor (Rload) = 2.2kΩ, Vdd = 3V, Ta = 25°C, LO Input Level = 0dBm.

Table 14. Typical Component Values using impedance matching with a differential LO input

Ref.	Value	Size	Part Number
R1	51Ω	1005	KOA RK73K1ETP510
C2, C3	10nF	1005	Murata GRM155B31H103KA88
L21, L22	6.2nH	1005	Murata LQW15AN6N2C00
C21, C22	2.4pF	1005	Murata GJM1553C1H2R4CB01

Gain/NF performance



HalfIF performance (Signal input Frequency = LO + IF/2 = 1275MHz)