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AK1545

3.5GHz Low Noise Integer-N Frequency Synthesizer

1. Overview

The AK1545 is an Integer-N PLL (Phase Locked Loop) frequency synthesizer, covering a wide range of frequency from 500MHz to 3.5GHz. Consisting of a highly accurate charge pump, a reference divider, a programmable divider and a dual-modulus prescaler (P/P+1), this product provides high performance, very low Phase Noise. An ideal PLL can be achieved by combining the AK1545 with the external loop filter and VCO (Voltage Controlled Oscillator). Access to the registers is controlled via a 3-wire serial interface. The operating supply voltage is from 2.7V to 5.5V, and the charge pump circuit and the serial interface can be driven by individual supply voltage.

2. Features

☐ Operating frequency : 500MHz to 3.5GHz

☐ Programmable charge pump current : 250μA and 1mA

☐ Fast lock mode : The charge pump current is switched by this function.

☐ Supply Voltage : 2.7 to 5.5 V (AVDD, DVDD pins)

☐ Separate Charge Pump Power Supply : AVDD to 5.6V (CPVDD pin)

☐ Excellent Phase Noise : -217dBc/Hz

☐ On-chip lock detection feature of PLL : Selectable Phase Frequency Detector (PFD) Output or Digital filtered lock detect

☐ Package : 16pin TSSOP

☐ Operating temperature : -40°C to 85°C

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- Table of Contents -

In this specification, the following notations are used for specific signal and register names.

[Name]   : Pin name

<Name> : Register group name (Address name)

{Name}   : Register bit name

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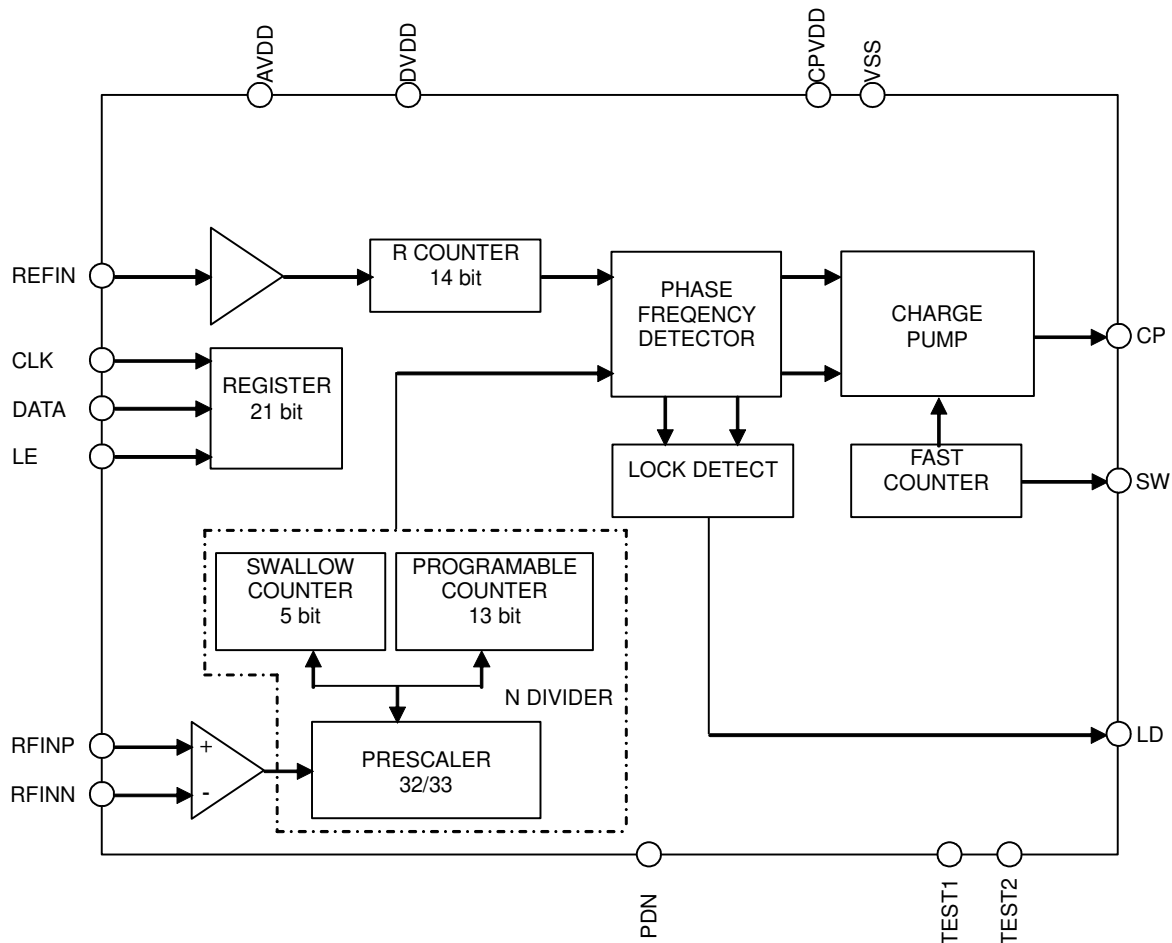
3. Block Diagram

Fig. 1 Block Diagram

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4. Pin Functional Description and Assignments

Table 1 Pin Functions

No.	Name	I/O	Pin Functions	Power Down (Note 1)	Remarks
1	SW	DO	Fast lock switch output		
2	CP	AO	Charge pump output	"Hi-Z"	
3	VSS	G	Ground		
4	TEST1	DI	TEST input 1. This pin must be connected to ground.		Schmidt trigger input
5	RFINN	AI	Complementary input to the RF Prescaler		
6	RFINP	AI	Input to the RF Prescaler		
7	AVDD	P	Power supply for analog blocks		
8	REFIN	AI	Reference signal input		
9	TEST2	DI	TEST input 2. This pin must be connected to ground.		Schmidt trigger input
10	PDN	DI	Power down		Schmidt trigger input
11	CLK	DI	Serial clock input		Schmidt trigger input
12	DATA	DI	Serial data input		Schmidt trigger input
13	LE	DI	Load enable input		Schmidt trigger input
14	LD	DO	Lock detect output		
15	DVDD	P	Power supply for digital blocks		
16	CPVDD	P	Power supply for charge pump		

Note 1)   "Power Down" means the state of [PDN] ="Low" after power on.

The following table shows the meaning of abbreviations used in the "I/O" column.

AI: Analog input pin	AO: Analog output pin	AIO: Analog I/O pin	DI: Digital input pin
DO: Digital output pin	P: Power supply pin	G: Ground pin	

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2. Pin Assignments

```
         ┌─────────────────────┐
SW    │ 1 ○          16 │  CPVDD
         │                     │
CP    │ 2            15 │  DVDD
         │                     │
VSS   │ 3            14 │  LD
         │                     │
TEST1 │ 4    TOP     13 │  LE
         │      VIEW            │
RFINN │ 5            12 │  DATA
         │                     │
RFINP │ 6            11 │  CLK
         │                     │
AVDD  │ 7            10 │  PDN
         │                     │
REFIN │ 8             9 │  TEST2
         └─────────────────────┘
```
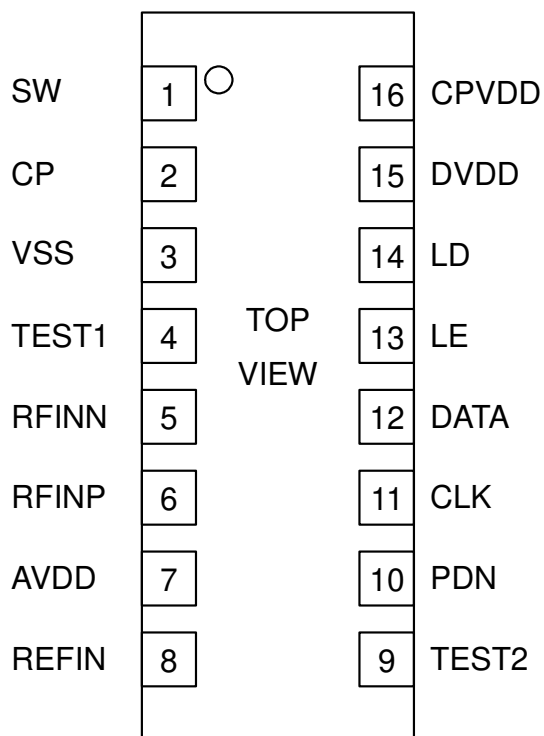
16pin TSSOP

Fig. 2 Pin Assignment

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5. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD1	-0.3	6.5	V	[AVDD], [DVDD] (Note 1)
	VDD2	-0.3	6.5	V	[CPVDD] (Note 1)
Ground Level	VSS	0	0	V	[VSS]
Analog Input Voltage	VAIN	VSS-0.3	VDD1+0.3	V	[RFINN], [RFINP], [REFIN] (Notes 1 & 2)
Digital Input Voltage	VDIN	VSS-0.3	VDD1+0.3	V	[CLK], [DATA], [LE], [PDN] (Notes 1 & 2)
Input Current	IIN	-10	10	mA	
Storage Temperature	Tstg	-55	125	°C	

Note 1)   0V reference for all voltages.

Note 2)   Maximum must not be over 6.5V.

Exceeding these maximum ratings may result in damage to the AK1545. Normal operation is not guaranteed at these extremes.

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6. Recommended Operating Range

Table 3 Recommended Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating Temperature	Ta	-40		85	°C	
Supply Voltage	VDD1	2.7		5.5	V	Applied to the [AVDD],[DVDD] pins
	VDD2	VDD1		5.6	V	Applied to the [CPVDD] pin

Note 1)   VDD1 and VDD2 can be driven individually within the Recommended Operating Range.

Note 2)   All specifications are applicable within the Recommended Operating Range (operating temperature / supply voltage).

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7. Electrical Characteristics

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1. Digital DC Characteristics

Table 4 Digital DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
High level input voltage	Vih		0.8×VDD1			V	Note 1)
Low level input voltage	Vil				0.2×VDD1	V	Note 1)
High level input current	Iih	Vih = VDD1=5.5V	-1		1	μA	Note 1)
Low level input current	Iil	Vil = 0V, VDD1=5.5V	-1		1	μA	Note 1)
High level output voltage	Voh	Ioh = -500μA	VDD1-0.4			V	Note 2)
Low level output voltage	Vol	Iol = 500μA			0.4	V	Note 3)
High level output voltage2	Voh	Ioh = -500μA	VDD2-0.4			V	Note 4)

Note 1)   Applied to the [CLK], [DATA], [LE] and [PDN] pins.

Note 2)   Applied to the [LD] pins.

Note 3)   Applied to the [LD],[SW] pins.

Note 4)   Applied to the [SW] pins.

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2. Serial Interface Timing

<Write-In Timing>
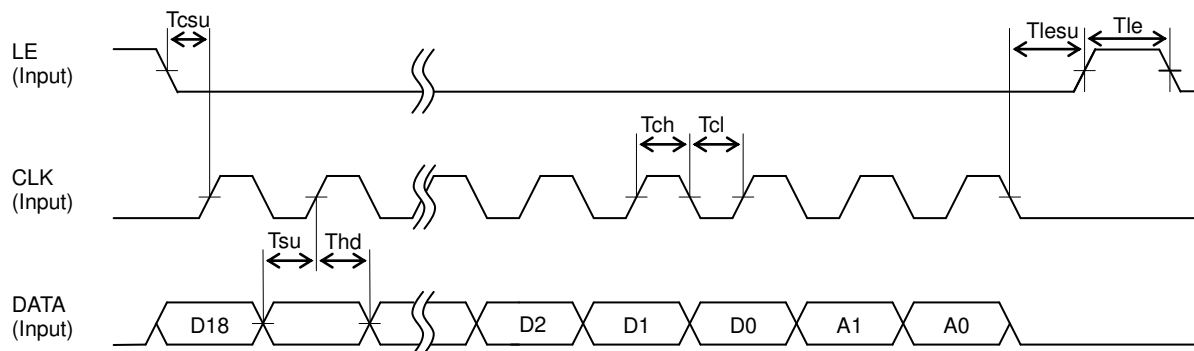
Fig. 3 Serial Interface Timing Chart

Table 5 Serial Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock L level hold time	Tcl	25			ns	
Clock H level hold time	Tch	25			ns	
Clock setup time	Tcsu	10			ns	
Data setup time	Tsu	10			ns	
Data hold time	Thd	10			ns	
LE setup time	Tlesu	10			ns	
LE pulse width	Tle	20			ns	

3. Analog Circuit Characteristics

VDD1＝2.7V to 5.5V, VDD2=VDD1 to 5.6V, −40°C ≤ Ta ≤ 85°C, unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Remarks
RF Characteristics					
Input Sensitivity	-10		2	dBm	
Input Frequency	500		3500	MHz	
REFIN Characteristics					
Input Sensitivity	0.4		VDD1	Vpp	
Input Frequency	5		100	MHz	
Maximum Allowable Prescaler Output Frequency			120	MHz	
Phase Detector					
Phase Detector Frequency			55	MHz	
Charge Pump					
Charge Pump High Value		1		mA	
Charge Pump Low Value		250		μA	
Icp TRI-STATE Leak Current		1		nA	0.6≤Vcpo≤VDD2-0.7, Ta=25°C
Mismatch between Source and Sink Currents (Note 1)		3		%	Vcpo=VDD2/2, Ta=25°C
Icp vs. Vcpo (Note 2)		2		%	0.5≤Vcpo≤VDD2-0.5, Ta=25°C
Noise Characteristic					
Normalized Phase Noise Floor		-217		dBc/Hz	
Current Consumption					
IDD1			10	μA	[PDN]="0" or {PD1}=1
IDD2 (Note3, Note4)		12	18	mA	[PDN]="1", {PD1}=0, IDD for VDD1
IDD3 (Note4)		0.4	0.7	mA	[PDN]="1", {PD1}=0, IDD for VDD2

Note 1) Mismatch between Source and Sink Currents : [(|Isink|-|Isource|)/{(|Isink|+|Isource|)/2}] × 100 [%]

Note 2) See "Charge Pump Characteristics - Voltage vs. Current". Vcpo is the output voltage at [CP].

Icp vs. Vcpo : [{1/2×(|I1|-|I2|)}/{1/2×(|I1|+|I2|)}]×100 [%]

Note 3) When [PDN] = "1" and {PD1}=0, the total power supply current of the AK1545 is "IDD2+IDD3+ Charge

pump current".

Note 4) RFIN=3.5GHz,5dBm, REFIN=100MHz,10dBm, {R}=100,{B}=109,{A}=12

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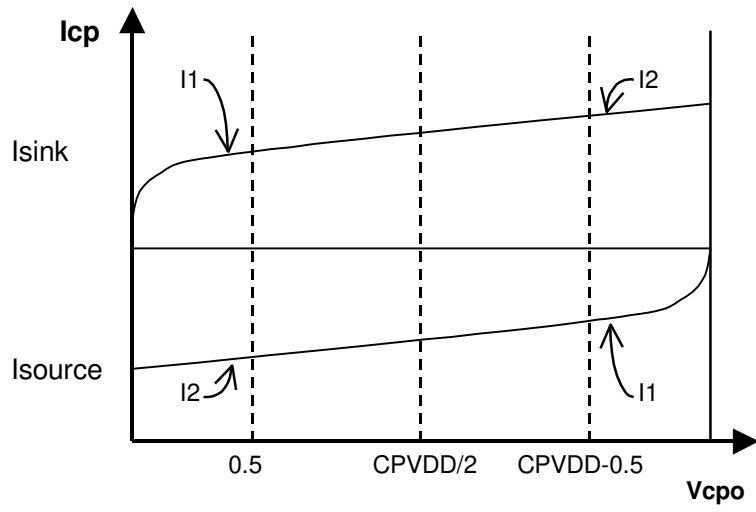
Fig. 4 Charge Pump Characteristics - Voltage (Vcpo) vs. Current (Icp)

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8. Block Functional Descriptions

1. Frequency Setup

The following formula is used to calculate the frequency setting for the AK1545.

Frequency setting (external VCO output frequency) = F_{PFD} x N

Where :

N	:	Dividing number N = [(P x B) + A]
F_{PFD}	:	Phase detector frequency F_{PFD} = [REFIN] pin input frequency / R counter dividing number
P	:	32
B	:	B (Programmable) counter value (See <Address1>:{B[12:0]})
A	:	A (Swallow) counter value (See <Address1>:{A[4:0]})

Calculation example

The output frequency of external reference frequency oscillator is 10MHz, and F_{PFD} is 1MHz and VCO frequency is 3000MHz.

AK1545 setting :

R (Reference counter) =10000000/1000000 = 10 (<Address0>:{R[13:0]}= "10")

P=32

B=93 (<Address1>:{B[12:0]}="93")

A=24 (<Address1>:{A[4:0]}="24")

Frequency setting = 1M × [(32×93) + 24] = 3000MHz

Lower limit for setting consecutive dividing numbers

In the AK1545, it is not possible to set consecutive dividing numbers below the lower limit.

(The lower limit is determined by a dividing number set for the prescaler.)

The following table shows an example where consecutive dividing numbers below the lower limit cannot be set. The consecutive dividing numbers can be set when B ≥ P-1.

P=32 (Dual modulus prescaler 32/33)

P	B[12:0]	A[5:0]	N [(P×B) + A]	Remarks
32	30	30	990	991 cannot be set as an N divider.
32	31	0	992	This is the lower limit. 992 or over can consecutively be set as an N divider.
32	31	1	993	
.	.	.	.	
32	4097	15	131119	
.	.	.	.	
32	8191	30	262142	
32	8191	31	262143	

2. Charge Pump, Loop Filter and Fast Lock Up Mode

The current setting of charge pump and loop filter can switch with the built-in timer for Fast Lock.
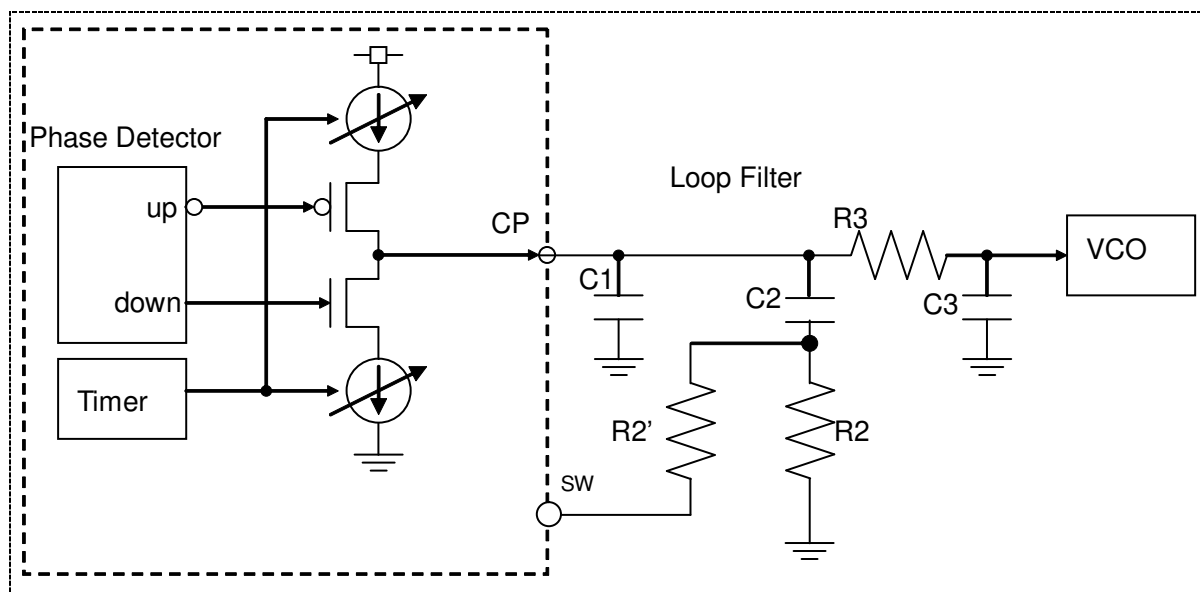

Fig. 5 Loop Filter Schematic

Fast Lock Mode 1

The output level of [SW] pin is programmed to a low state, and the charge pump current is switched to the high value (1 mA). [SW] is used to switch a resistor in the loop filter and to ensure stability while in the fast lock up mode by altering the loop bandwidth.

When the {CPGAIN} bit in the N register is set to "1", the AK1545 enters the fast lock up mode. When the {CPGAIN} bit in the N register is set to "0", the AK1545 exits the fast lock up mode.
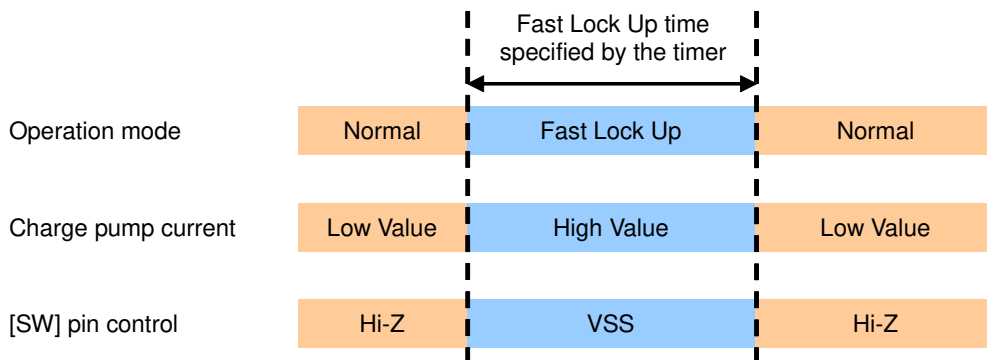
Fast Lock Mode 2

The output level of [SW] pin is programmed to a low state, and the charge pump current is switched to the high value (1 mA). [SW] is used to switch a resistor in the loop filter and to ensure stability while in the fast lock up mode by altering the loop bandwidth.

When the {CPGAIN} bit in the N register is set to "1", the AK1545 enters the fast lock up mode. The AK1545 exits the fast lock up mode after the expiration of the timer. The timer configuration is set by the value in {TIMER [3:0]}. After the timeout, the {CPGAIN} bit in the N register is automatically reset to 0, and the device reverts to normal mode instead of the fast lock up mode.

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Fig. 6 Fast Lock Up Mode Timing Chart

Table 6 Fast Lock Mode Function

Function	{FASTEN}={D7}	{FASTMODE}={D9}	{CPGAIN}	[SW]-pin state
Fast Lock Mode disable	0	X	0	{D9} state
			1	
Fast Lock Mode 1	1	0	0	Hi-Z
			1	VSS
Fast Lock Mode 2	1	1	(*1) Controlled by the value in {TIMER [3:0]}.	

(*1) When the timer is counting, {CPGAIN} ="1" and [SW] pin is low state. After the timeout, its function reverts to normal mode ({CPGAIN} ="0" and [SW] pin is Hi-Z state) instead of the fast lock up mode.

[SW]-pin Functions

SW pin is a General Purpose Output (GPO) pin which can be controlled by FASTEN register.

(1) {FASTEN} ="0"

The value of D9 register comes out from the SW pin.

AK1545

SW

■FASTMODE＝[D9]＝0 : SW＝"LOW" (CPVSS)

■FASTMODE＝[D9]＝1 : SW＝"HIGH" (CPVDD)
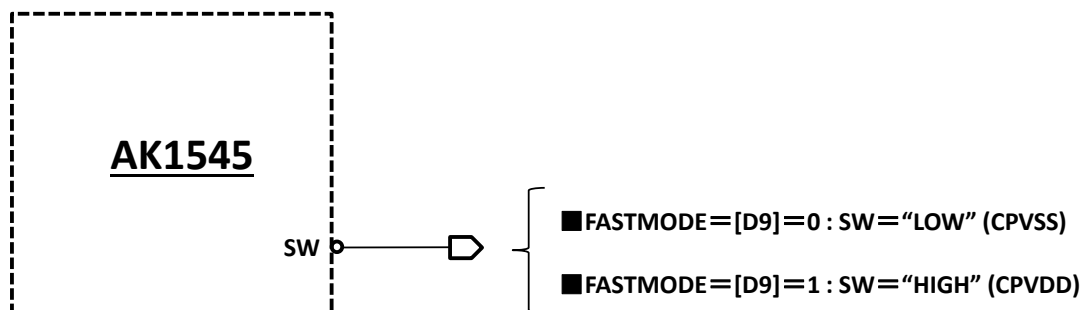
(2) {FASTEN} ="1"

Works as shown in the "Fast Lock UP Mode Timing Chart" above.

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3. Lock Detect

Lock detect output can be selected by {LD[2:0]} in <Address2>. When {LD} is set to "101Bin", the phase detector outputs an un-manipulated phase detection(comparison) result. (This is called "analog lock detect".) When {LD} is set to "001Bin", the lock detect signal is output according to the on-chip logic. (This is called "digital lock detect".)

The lock detect can be done as following:
The [LD] pin is in unlocked state (which outputs "Low") when a frequency setup (N register or R register settings) is made.

Case of Lock to Unlock is as following.
R=1: The [LD] pin outputs "High" when a phase error smaller than a half cycle of [REFIN] (1/2T) is detected for the counter value N times consecutively.
R>1: The [LD] pin outputs "High" when a phase error smaller than a cycle of [REFIN] (T) is detected for the counter value N times consecutively.

Case of Unlock to Lock is as following.
R=1: The [LD] pin outputs "Low" when a phase error larger than a half cycle of [REFIN] (1/2T) is detected for the counter value N times consecutively.
R>1: The [LD] pin outputs "Low" when a phase error larger than a cycle of [REFIN] (T) is detected for the counter value N times consecutively.

The counter value N can be set by {LDP} in <Address0>. The N is different between "unlocked to locked" and "locked to unlocked".

Table 7 Lock Detect Precision

{LDP}	unlocked to locked	locked to unlocked
0	N=15	N=3
1	N=31	N=7

The lock detect signal is shown below:
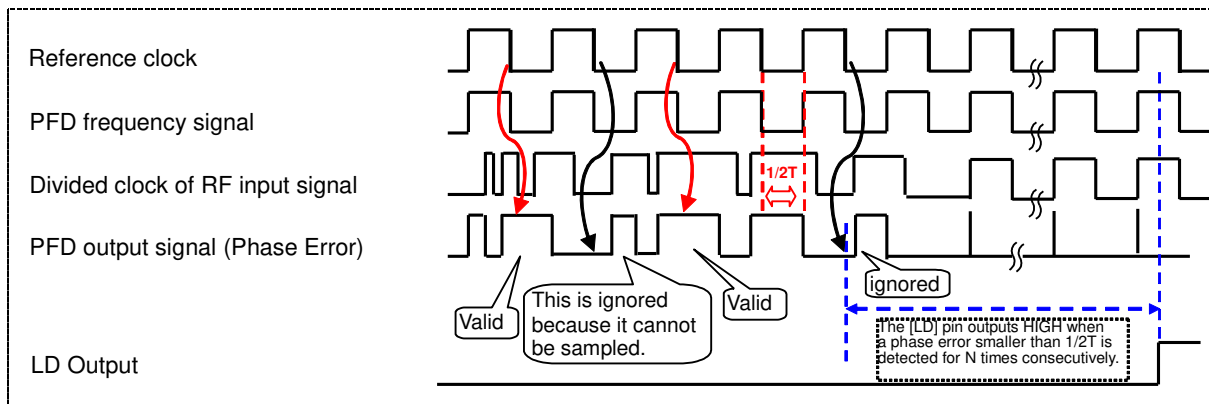
Case of "R = 1"
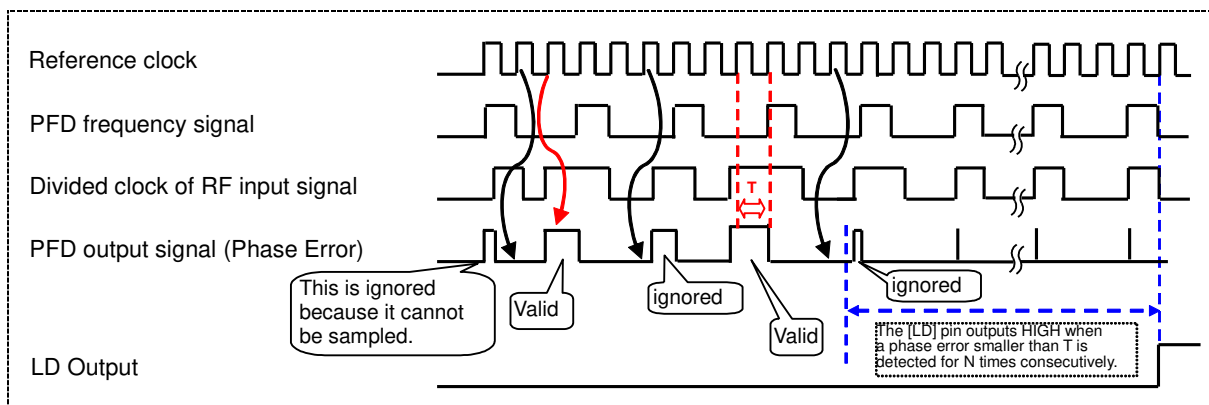
Case of "R > 1"

Fig. 7 Digital Lock Detect Operations

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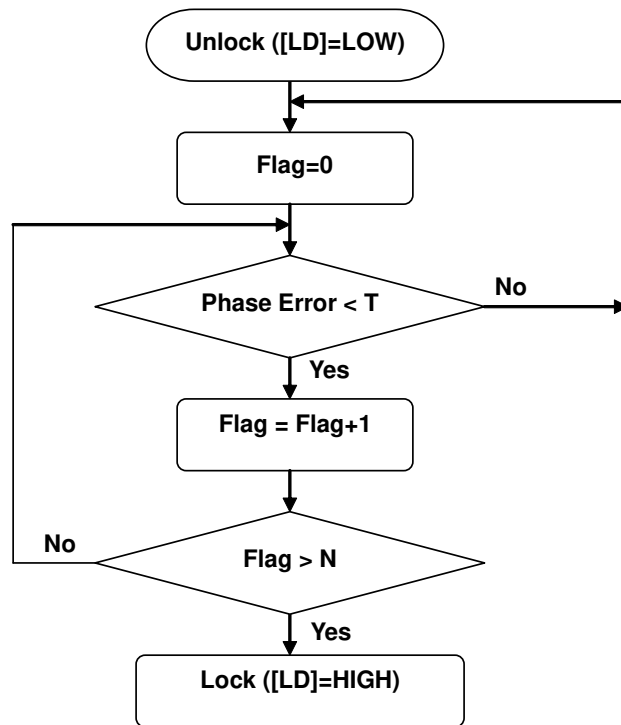
Fig. 8 Unlocked → Locked
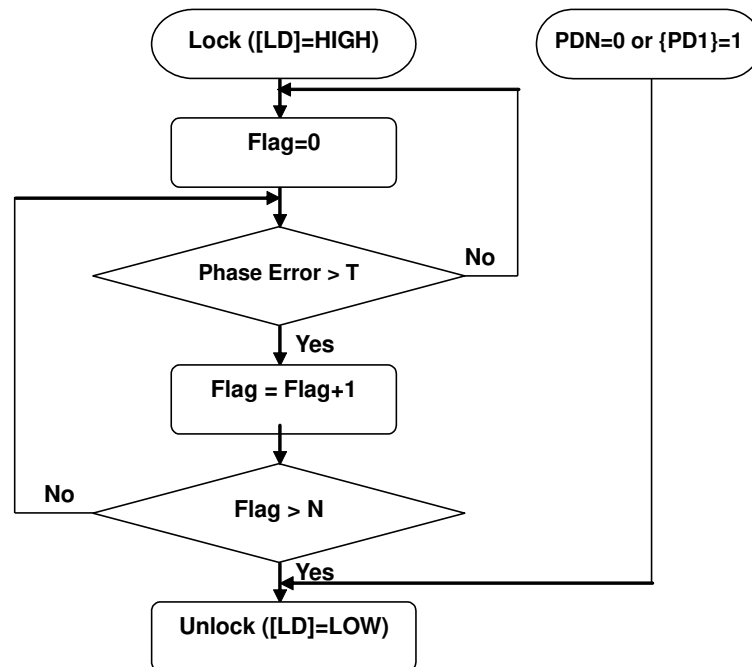
Fig. 9 Locked → Unlocked

4. Reference counter

The reference input can be set with a dividing number in the range of 1 to 16383 using {R [13:0]}, which is an 14-bit address of {D[13:0]} in <Address0>. 0 cannot be set as a dividing number.

5. Prescaler

The dual modulus prescaler (P/P + 1) and the swallow counter are used to provide a large dividing ratio. AK1545 has a Dual modulus prescaler 32/33.

6. Power-down and Power-save mode

It is possible to operate in the power-down or power-save mode if necessary by using the external control pin.

Power On

Follow the power-up sequence.

Normal Operation

Table 8 Power-down and Power-save mode

[PDN]	<Address2>		Function
	{PD2}	{PD1}	
"Low"	X	X	Power Down
"High"	X	0	Normal Operation
"High"	0	1	Asynchronous Power Down
"High"	1	1	Synchronous Power Down

X : Don't care

9. Register Map

Name	Data	Address	
R Counter	D18 - D0	0	0
N Counter (A and B)		0	1
Function		1	0
Initialization		1	1

Name	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
R Count	LDP	0	0	0	0	R [13]	R [12]	R [11]	R [10]	R [9]	R [8]	R [7]	R [6]	R [5]	R [4]	R [3]	R [2]	R [1]	R [0]	0x0
N Count	CPGA IN	B [12]	B [11]	B [10]	B [9]	B [8]	B [7]	B [6]	B [5]	B [4]	B [3]	B [2]	B [1]	B [0]	A [4]	A [3]	A [2]	A [1]	A [0]	0x1
Func.	0	PD2	0	0	0	TIMER [3]	TIMER [2]	TIMER [1]	TIMER [0]	FAST MODE	0	FAST EN	CP HiZ	CP POLA	LD [2]	LD [1]	LD [0]	PD1	CNTR RST	0x2
Initial.	0	PD2	0	0	0	TIMER [3]	TIMER [2]	TIMER [1]	TIMER [0]	FAST MODE	0	FAST EN	CP HiZ	CP POLA	LD [2]	LD [1]	LD [0]	PD1	CNTR RST	0x3

Notes for writing into registers

After powers on AK1545, [PDN] must be "0" or {PD1} must be "1".

After powers on AK1545, the initial registers value are not defined. It is required to write the data in all addresses in order to commit it.

[Examples of writing into registers]

(Ex. 1) Power-On
- Bring [PDN] to "0 (Low)"
- Apply VDD
- Program Address0, Address1 and Address2
- Bring [PDN] to "1 (High)"

(Ex. 2) Changing frequency settings : Initialization
- Program Address3
- Program Address1

(Ex. 3) Changing frequency settings : Counter reset
- Program Address2.   As part of this, load "1" to both {PD1} and {CNTR_RST}.
- Program Address1
- Program Address2.   As part of this, load "0" to both {PD1} and {CNTR_RST}.

(Ex. 4) Changing frequency settings : PDN pin method
- Bring [PDN] to "0 (Low)"
- Program Address1
- Bring [PDN] to "1 (High)"

10. Function Description - Registers

< Address0 : R Counter >

D18	D[17:14]	D[13:0]	Address
LDP	0	R[13:0]	00

D[17:14] : These bits are set to the following for normal operation

D17	D16	D15	D14
0	0	0	0

LDP : Lock Detect Precision

The counter value for digital lock detect can be set.

D18	Function	Remarks
0	15 times Count	unlocked to locked
	3 times Count	locked to unlocked
1	31 times Count	unlocked to locked
	7 times Count	locked to unlocked

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R[13:0] : Reference clock division number

The following settings can be selected for the reference clock division.

The allowed range is 1 (1/1 division) to 16383 (1/16383 division). 0 cannot be set.

The maximum frequency for F_{PFD} is 55MHz.

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Remarks
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1/1 division	
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1/2 division	
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1/3 division	
0	0	0	0	0	0	0	0	0	0	0	1	0	0	1/4 division	
						DATA									
1	1	1	1	1	1	1	1	1	1	1	1	0	1	1/16381 division	
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1/16382 division	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1/16383 division	

< Address1 : N Counter >

D18	D[17:5]	D[4:0]	Address
CPGAIN	B[12:0]	A[4:0]	01

CPGAIN : Sets the charge pump current

D18	Function	Remarks
0	250μA	
1	1mA	

B[12:0] : B (Programmable) counter value

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	Function	Remarks
0	0	0	0	0	0	0	0	0	0	0	0	0	0	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	1	1 Dec	Prohibited
0	0	0	0	0	0	0	0	0	0	0	1	0	2 Dec	Prohibited
0	0	0	0	0	0	0	0	0	0	0	1	1	3 Dec	
						DATA								
1	1	1	1	1	1	1	1	1	1	1	0	1	8189 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	0	8190 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	1	8191 Dec	

A[4:0] : A (Swallow) counter value

D4	D3	D2	D1	D0	Function	Remarks
0	0	0	0	0	0	
0	0	0	0	1	1 Dec	
0	0	0	1	0	2 Dec	
0	0	0	1	1	3 Dec	
		DATA				
1	1	1	0	1	29 Dec	
1	1	1	1	0	30 Dec	
1	1	1	1	1	31 Dec	

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* Requirements for A[4:0] and B[12:0]

The data at A[4:0] and B[12:0] must meet the following requirements:

A[4:0] ≥ 0, B[12:0] ≥ 3, B[12:0] ≥ A[4:0]

See "Frequency Setup" in section "Block Functional Descriptions" for details of the relationship between a frequency division number N and the data at A[4:0] and B[12:0].

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< Address2 : Function >

D18	D17	D[16:14]	D[13:10]	D9	D8	D7
0	PD2	0	TIMER[3:0]	FASTMODE	0	FASTEN

D6	D5	D[4:2]	D1	D0	Address
CPHIZ	CPPOLA	LD[2:0]	PD1	CNTR_RST	02

PD2, PD1 : Power Down Select

[PDN]	<Address2>		Function
	{PD2}	{PD1}	
"Low"	X	X	Power Down
"High"	X	0	Normal Operation
"High"	0	1	Asynchronous Power Down
"High"	1	1	Synchronous Power Down

X : Don't care

{PD2}=1 and {PD1}=1 : All circuits powers down at the timing when the Phase detector frequency signal reverses.

{PD2}=0 and {PD1}=1 : All circuits goes into Power Down at the rise up of LE signal that latches 1 into {PD1}.

TIMER[3:0] : Sets the Fast Lock Timer

This is enabled when { FASTMODE } ="1", {FASTEN} = "1" and {CPGAIN}="1".

The charge pump current is set into high value (1mA) designate during switchover time which is set by {TIMER[3:0]}.

The following formula shows the relationship between the switchover time and the counter value.

Switchover time = $1 / F_{PFD}$ x Counter Value

Counter Value = 3 + Timer[3:0] x 4