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AK1573/AK1573B/AK1573C

Frequency Synthesizer with Integrated VCO

1. General Description

AK1573 is the Integer-N frequency synthesizer with integrated VCO (Voltage Controlled Oscillator). It is composed of programmable charge pump, reference divider, programmable divider, dual modulus prescaler ($P / P + 1$). With the feature of high-performance, low noise and small size, it can be used as a local signal source of a variety of frequency conversion.

By combining with an external loop filter, AK1573 form a complete Phase Locked Loop.

Access to the register is controlled by the serial interface of the 3-wire and Power supply voltage is 2.7V to 3.3V.

2. Features

- Normalized Phase Noise -223dBc/Hz
- Low Noise Integrated VCO -86dBc/Hz@10kHz
-112dBc/Hz@100kHz
- Operating Supply Voltage 2.7 to 3.3V
- Low Current Consumption@0dBm Output

AK1573	43mA
AK1573B	44mA
AK1573C	46mA
- Programmable to Divide by 1, 2, 4, 8, 16, 32, 64
- Programmable Output Power -12dBm to +6dBm
- Fast Lock-up Function
- Analog or Digital Lock Detect Function
- Output Mute Function
- Package 24pin QFN (0.5mm pitch 4x4mm)
- Operating Temperature Range -40 °C to 85 °C
- Frequency Coverage Options

	AK1573	AK1573B	AK1573C
VCO Frequency [MHz]	1480 to 2240	1728 to 2600	2100 to 3000
Divide by 1	1480 to 2240	1728 to 2600	2100 to 3000
Divide by 2	740 to 1120	864 to 1300	1050 to 1500
Divide by 4	370 to 560	432 to 650	525 to 750
Divide by 8	185 to 280	216 to 325	262.5 to 375
Divide by 16	92.5 to 140	108 to 162.5	131.25 to 187.5
Divide by 32	46.25 to 70	54 to 81.25	65.625 to 93.75
Divide by 64	30 to 35	30 to 40.625	32.8125 to 46.875

3. Ordering Guide

- AK1573	24-pin QFN (4.0mm x 4.0mm, 0.5mm pitch)
- AK1573B	24-pin QFN (4.0mm x 4.0mm, 0.5mm pitch)
- AK1573C	24-pin QFN (4.0mm x 4.0mm, 0.5mm pitch)
- AKD1573	AK1573 Evaluation Board
- AKD1573B	AK1573B Evaluation Board
- AKD1573C	AK1573C Evaluation Board

4. Applications

- Public safety and Community/Emergency Wireless System
- Wireless applications
- Cellular BTS

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6. Block Diagram and Functions

6.1. Block Diagram

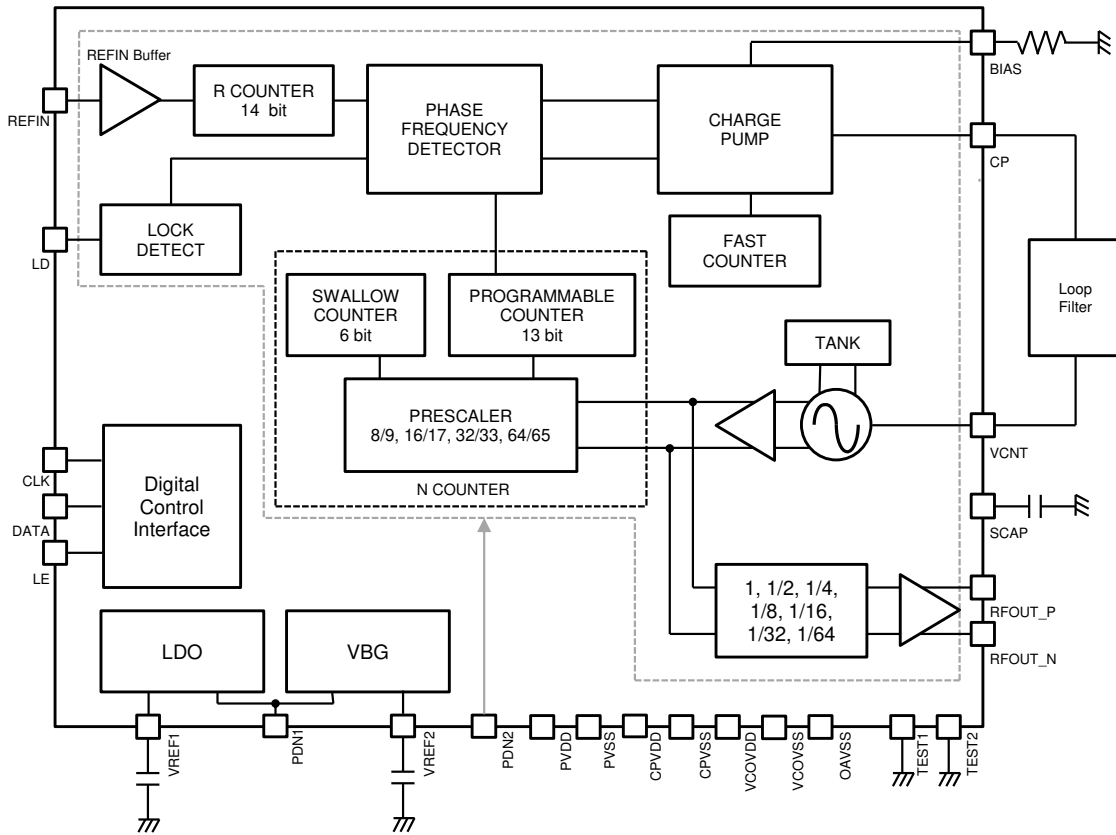


Figure.1 Block Diagram

6.2. Functions

Block	Function
N counter	It is composed of prescaler, Swallow Counter and Programmable Counter. VCO output signal is divided by N and passed to phase frequency detector (PFD).
VCO Divider	It divides VCO output signal and passes it to output buffer. Dividing ratio of 1, 2, 4, 8, 16, 32 and 64 can be selected.
R counter	It divides a reference signal by R and passes it to phase frequency detector (PFD).
VCO (Voltage Controlled Oscillator)	It generates a signal of the frequency corresponding to a voltage inputted to VCNT pin.
PFD(Phase Frequency Detector)	It outputs a signal corresponding to phase difference between N counter and R counter.
Charge Pump	Sweep or pull-in a current corresponding to a signal from PFD.

7. Pin Configurations and Functions
--

No.	Pin Name	I/O	Pin function	Power Down	Description
1	BIAS	AI	Charge pump current setting pin		Connect a 27kΩ resistor to the ground
2	VREF2	AO	Internal reference voltage output pin	"L"	Connect a 470nF capacitor to the ground
3	VCNT	AI	VCO control voltage input pin		
4	SCAP	AO	VCO Bias stabilizing connection pin	"L"	Connect a 100pF capacitor to the ground
5	VCOVSS	G	Ground of VCO block		
6	VCOVDD	P	Power supply of VCO block		
7	TEST1	DI	TEST1 pin Connect to the ground		Pull Down Schmitt trigger input
8	TEST2	DI	TEST2 pin Connect to the ground		Pull Down Schmitt trigger input
9	PDN1	DI	Power down 1 pin. When PDN1 = "L", device is powered down and the registers are not retained.		Schmitt trigger input
10	OAVSS	G	Ground of Local buffer		
11	RFOUT_P	AO	Local signal output pin		Open collector Connect a inductor and a register to VDD
12	RFOUT_N	AO	Local signal complementary output pin		
13	PVDD	P	Power supply of Prescaler and LDO		
14	PVSS	G	Ground of Prescaler and LDO		
15	VREF1	AO	Output pin of LDO	"L"	Connect a 220nF capacitor to the ground
16	REFIN	DI	Reference signal input pin		
17	PDN2	DI	Power down 2 pin. When PDN2 = "L", all blocks except LDO and VBG are powered down but the registers are retained		Schmitt trigger input
18	CLK	DI	Serial clock input pin.		Schmitt trigger input
19	DATA	DI	Serial data input pin.		Schmitt trigger input
20	LE	DI	Load enable input pin.		
21	LD	DO	Lock detect output pin	"L"	
22	CVPSS	G	Ground of Charge Pump		
23	CP	AO	CP signal output pin	Tri-State	
24	CPVDD	P	Power supply of Charge Pump		

AI: Analog input pin
DI: Digital input pin

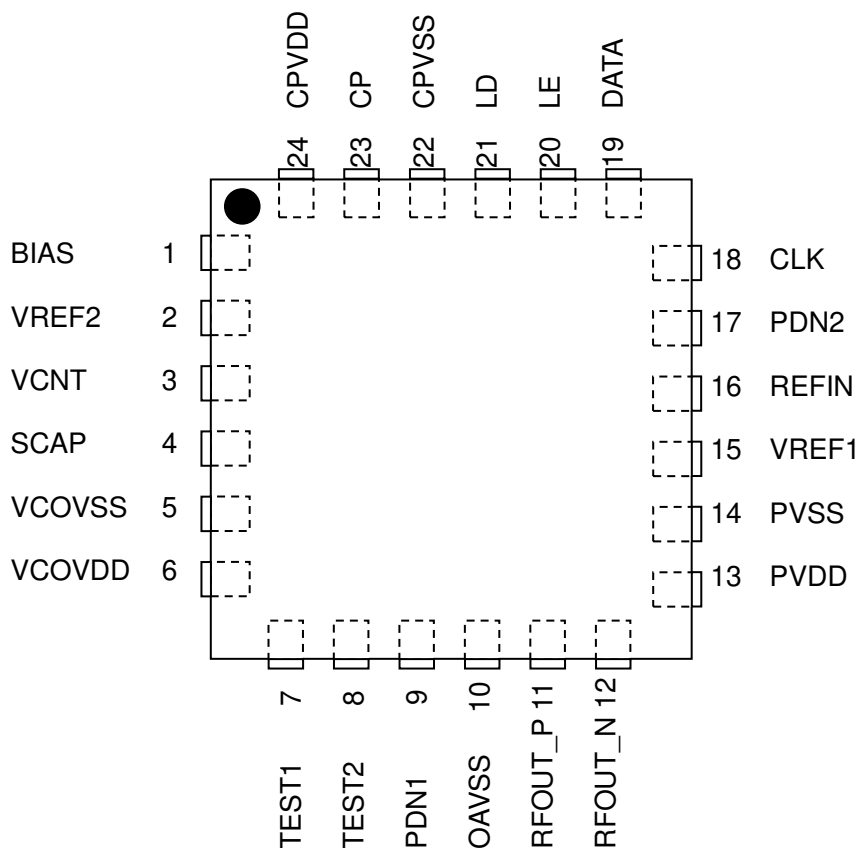
AO: Analog output pin
DO: Digital output pin

AIO: Analog I/O pin
P: Power supply pin

G: Ground pin

* "Power Down" means the state in which power supply is applied and PDN1 / PDN2 pins = "L".

* The exposed pad at the center of the backside should be connected to the ground



24-pin QFN (0.5mm pitch, 4mm × 4mm)

Figure.2 Package pin layout (Top view)

8. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Description
Supply Voltage	VDD	-0.3	3.6	V	* 1, 2
Ground Level	VSS	0	0	V	* 3
Analog input voltage	VAIN	VSS-0.3	VDD+0.3	V	* 1, 4, 6
Digital input voltage	VDIN	VSS-0.3	VDD+0.3	V	* 1, 5, 6
Input current	IIN	-10	10	mA	
Storage Temperature	Tstg	-55	125	°C	

Note

- * 1. All voltage reference ground level: 0V
- * 2. Applied to the VCOVDD / PVDD / CPVDD pins
- * 3. Applied to the CPVSS / PVSS / VCOVSS / OAVSS pins
- * 4. Applied to the VCNT / REFIN pins
- * 5. Applied to the CLK / DATA / LE / PDN1 / PDN2 / TEST1 / TEST2 pins
- * 6. The maximum value must not exceed the absolute maximum rating of 3.6V.

Exceeding these maximum ratings may result in damage to the AK1573. Normal operation is not guaranteed at these extremes.

9. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Description
Operating Temperature	Ta	-40		85	°C	
Supply Voltage	VDD	2.7	3.0	3.3	V	Applied to the VCOVDD / PVDD / CPVDD pins

10. Electrical Characteristics

10.1. Digital DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Description
High level input voltage	Vih		0.8×VDD			V	* 1.
Low level input voltage	Vil				0.2×VDD	V	* 1.
High level input current 1	Iih1	Vih = VDD=3.3V	-1		1	μA	* 2
High level input current 2	Iih2	Vih = VDD=3.3V	16.5	33	66	μA	* 3
Low level input current	Iil	Vil = 0V, VDD=3.3V	-1		1	μA	* 1
High level output voltage	Voh	Ioh = -500μA	VDD-0.4			V	* 4
Low level output voltage	Vol	Iol = 500μA			0.4	V	* 4

Note

- * 1. Applied to the CLK / DATA / LE / PDN1 / PDN2 pins
- * 2. Applied to the CLK / DATA / LE / PDN1 / PDN2 pins
- * 3. Applied to the TEST1 / TEST2 pins
- * 4. Applied to the LD pin

10.2. Serial Interface Timing

<Write-In Timing>

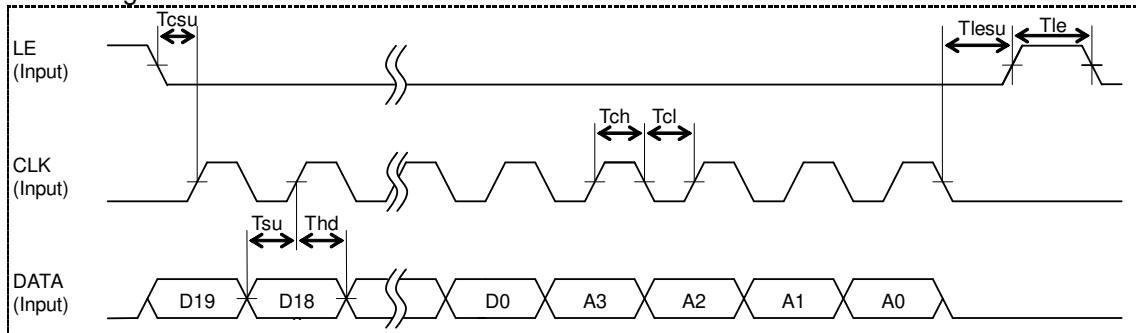


Figure.3 Serial Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Description
Clock L level hold time	Tcl	25			ns	
Clock H level hold time	Tch	25			ns	
Clock setup time	Tcsu	10			ns	
Data setup time	Tsu	10			ns	
Data hold time	Thd	10			ns	
LE setup time	Tlesu	10			ns	
LE pulse width	Tle	25			ns	

10.3. Analog Circuit Characteristics

VDD=2.7 to 3.3V, -40°C<Ta<85°C, BIAS resistance =27kΩ unless otherwise specified.

The exposed pad at the center of the backside should be connected to the ground

Parameter	Min.	Typ.	Max.	Unit	Description
REFIN					
Input sensitivity	0.4		VDD	Vpp	REFIN frequency < 200MHz
	0.4		2	Vpp	REFIN frequency ≥ 200MHz
Input Frequency Range	10		300	MHz	
Maximum available prescaler output Frequency			300	MHz	Design guarantee value
Phase Frequency Detector(PFD)					
PFD Frequency			104	MHz	Design guarantee value
Charge Pump					
Maximum Charge Pump current		2800		μA	
Minimum Charge pump current		350		μA	
Icp TRI-STATE leak current		1		nA	Ta = 25°C, Vcpo = VDD / 2 Vcpo : CP pin voltage
Sink / Source current mismatch * 1		1	10	%	Vcpo = VDD / 2, Ta = 25°C Vcpo : CP pin voltage
Icp vs. Vcpo * 2		3	15	%	0.5 ≤ Vcpo ≤ VDD - 0.5 Ta = 25°C
VCO					
Operating Frequency Range	1480		2240	MHz	AK1573
	1728		2600	MHz	AK1573B
	2100		3000	MHz	AK1573C
VCO tuning Sensitivity		fvco×0.02		MHz/V	fvco : Oscillation Frequency
Phase Noise @ 1.6GHz (AK1573) @ 1.8GHz (AK1573B) @ 2.1GHz (AK1573C) OUTLV[2:0] bits ≥ "011"	10kHz offset		-86	dBc/Hz	VCOI bit = "1"
	100kHz offset		-112	dBc/Hz	VCOI bit = "1"
	1MHz offset		-133	dBc/Hz	VCOI bit = "1"
	10MHz offset		-151	dBc/Hz	VCOI bit = "1"
Normalized Phase Noise		-223		dBc/Hz	Note 3
Output Buffer					
OUTPUT Power @1GHz		6		dBm	OUTLV[2:0] bits = "111"
		3		dBm	OUTLV[2:0] bits = "101"
		1		dBm	OUTLV[2:0] bits = "011"
		-5		dBm	OUTLV[2:0] bits = "001"
Output Frequency	30			MHz	Design guarantee value
Regulator					
VREF1 start-up time			10	ms	

Note

* 1. Sink/Source current mismatch : $\frac{(|I_{sink}| - |I_{source}|)}{(|I_{sink}| + |I_{source}|)/2} * 100$ [%]

* 2. Icp v.s. Vcpo : $\frac{\{1/2 * (|I1| - |I2|)\}}{\{1/2 * (|I1| + |I2|)\}} * 100$ [%]

* 3. Measured in-band phase noise with the loop locked. Normalized Phase Noise is calculated from following equation. REFIN frequency = 120MHz, F_{PFD} = 10MHz.

$$(PN_{total} = PN_{synth} - 10 \text{ Log } F_{PFD} - 20 \text{ Log } N)$$

PN_{total} : Normalized Phase Noise

PN_{synth} : In-band Phase Noise

F_{PFD} : PFD Frequency

Parameter	Min.	Typ.	Max.	Unit	Description	
Current Consumption						
IDD1			10	μA	PDN1 pin = PDN2 pin = "L" (Full power down)	
IDD2 @1.6GHz (AK1573)						
@ OUTLV[2:0] bits = "001" VCOI bits = "0"		33		mA	PDN1 pin = PDN2 pin = "H" DIV[2:0] bits = "000" PRE[1:0] bits = "00"	
@ OUTLV[2:0] bits = "011" VCOI bits = "0"		43				
@ OUTLV[2:0] bits = "111" VCOI bits = "0"		62				
@ OUTLV[2:0] bits = "111" VCOI bits = "1"		66	93			
IDD2 @1.8GHz (AK1573B)						
@ OUTLV[2:0] bits = "001" VCOI bits = "0"		34		mA		
@ OUTLV[2:0] bits = "011" VCOI bits = "0"		44				
@ OUTLV[2:0] bits = "111" VCOI bits = "0"		62				
@ OUTLV[2:0] bits = "111" VCOI bits = "1"		66	93			
IDD2 @2.1GHz (AK1573C)						
@ OUTLV[2:0] bits = "001" VCOI bits = "0"		37		mA		
@ OUTLV[2:0] bits = "011" VCOI bits = "0"		46				
@ OUTLV[2:0] bits = "111" VCOI bits = "0"		64				
@ OUTLV[2:0] bits = "111" VCOI bits = "1"		68	93			
IDD3 @1.6GHz (AK1573) @1.8GHz (AK1573B) @2.1GHz (AK1573C) DIV[2:0] bits ≥ "100"		75	105	mA	PDN1 pin = PDN2 pin = "H" DIV[2:0] bits ≠ "000" PRE[1:0] bits = "00"	
IDD4		0.5	1	mA	PDN1 pin = "H", PDN2 pin = "L" (power down except VBG / LDO)	
CP current adjusting resistance						
BIAS resistance	22	27	33	kΩ	Connect to BIAS pin	

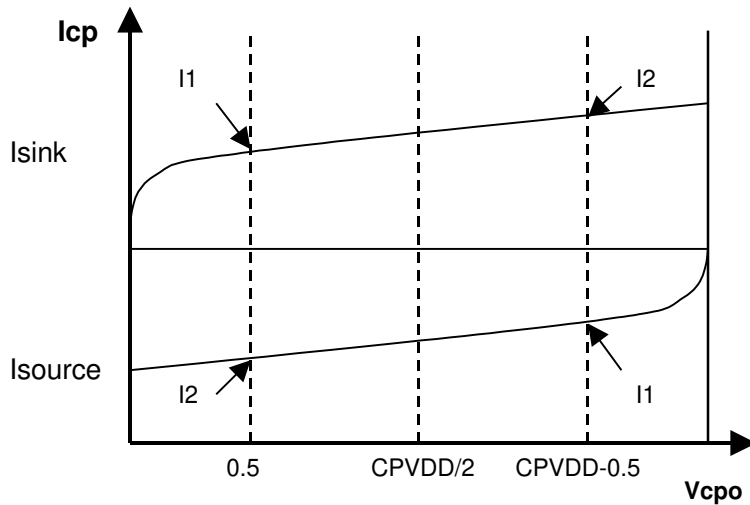


Figure.4 Charge Pump Characteristics – Voltage vs Current

10.4. Loop filter

Figure.5 shows loop filter topology used to evaluate AK1573, AK1573B and AK1573C.

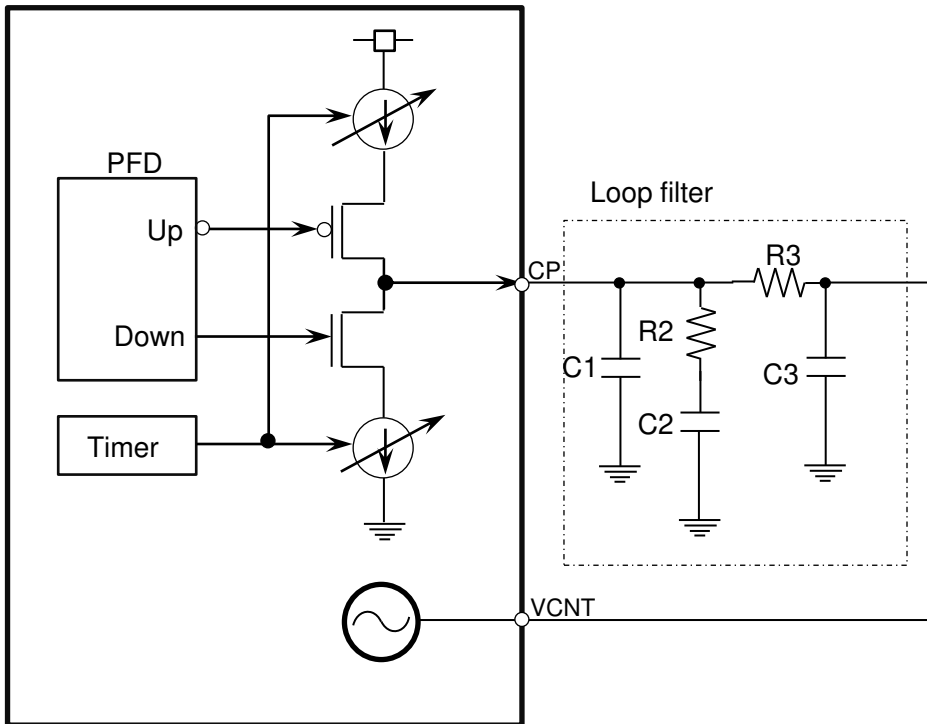


Figure.5 Loop Filter Schematic

11. Typical Characteristics

VDD=3.0V, Ta=25°C, BIAS resistance =27kΩ.

1. Analog Characteristics

AK1573

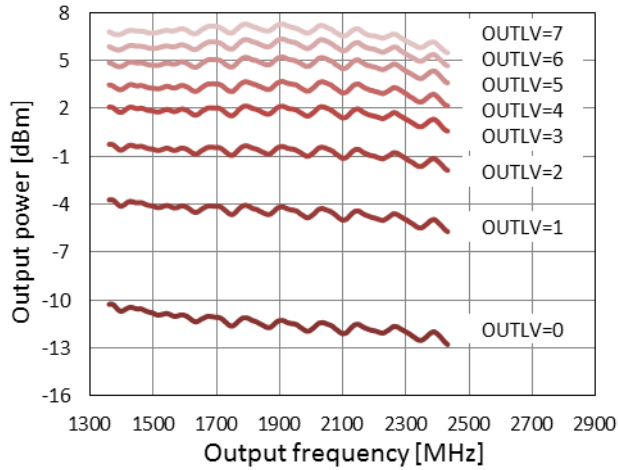
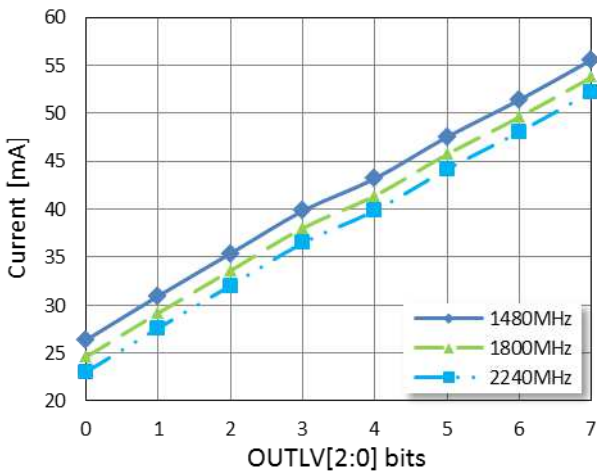
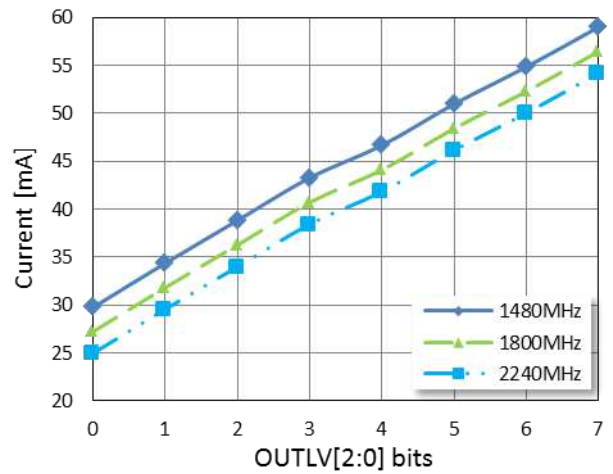


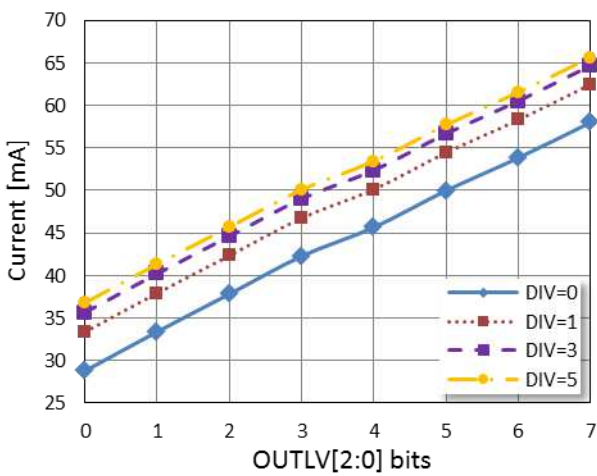
Figure.6 Output power vs. Output frequency



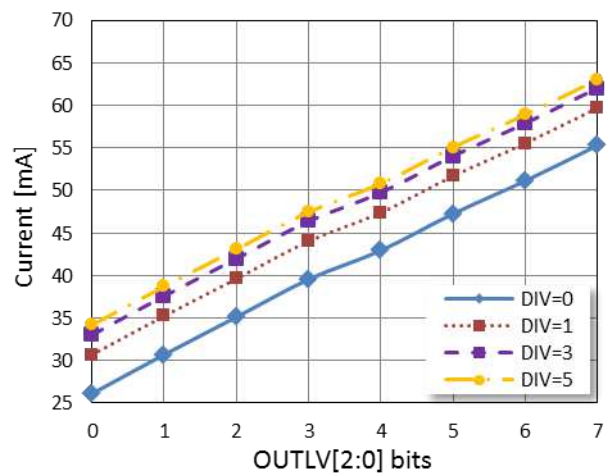
(a) VCOI bit = "0", DIV[2:0] bits = "000"



(b) VCOI bit = "1", DIV[2:0] bits = "000"



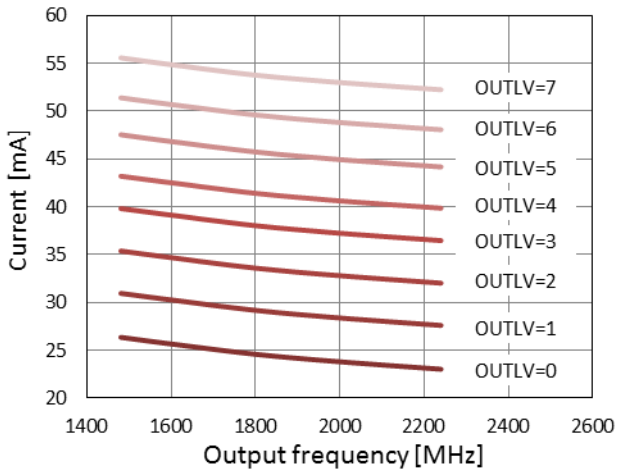
(c) Output frequency=1600MHz, VCOI bit="1"



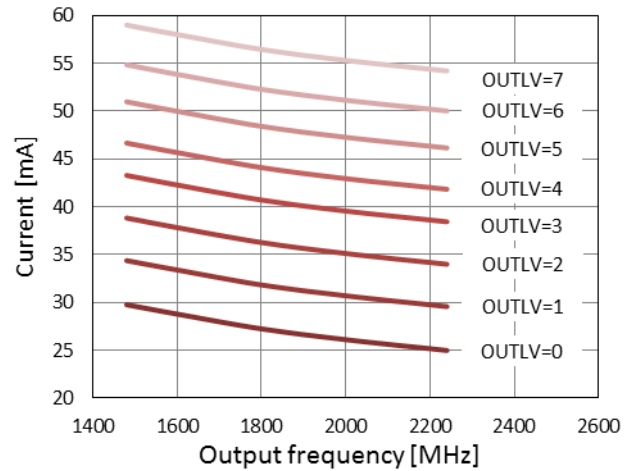
(d) Output frequency=2000MHz, VCOI bit="1"

Figure.7 Current vs. OUTLV[2:0] bits

REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = "111"



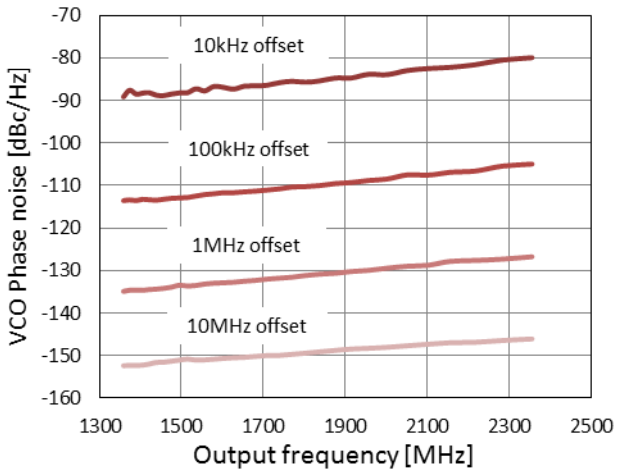
(a) VCOI bit = "0"



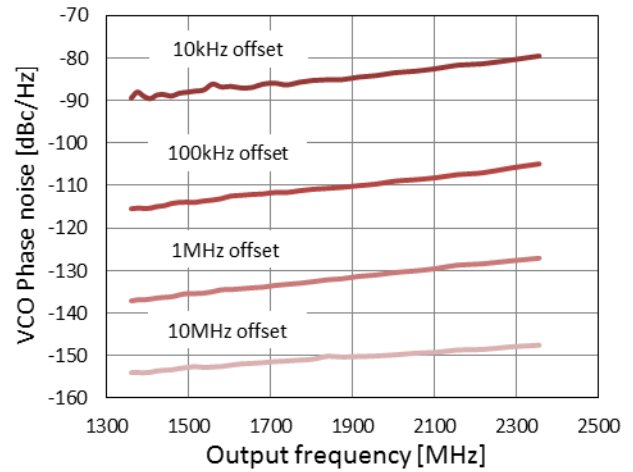
(b) VCOI bit = "1"

Figure.8 Current vs. Output frequency

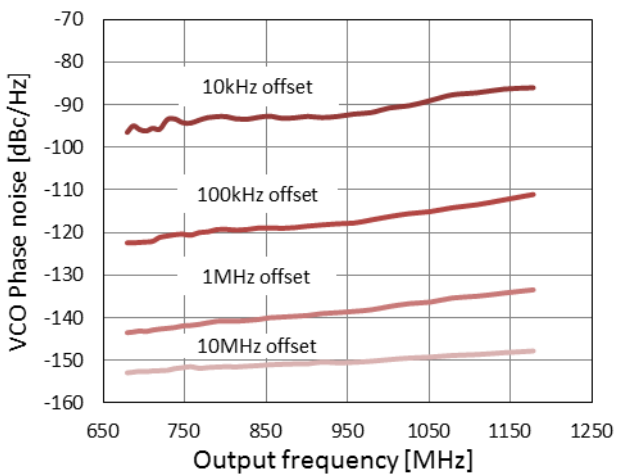
REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = "111", DIV[2:0] bits = "000"



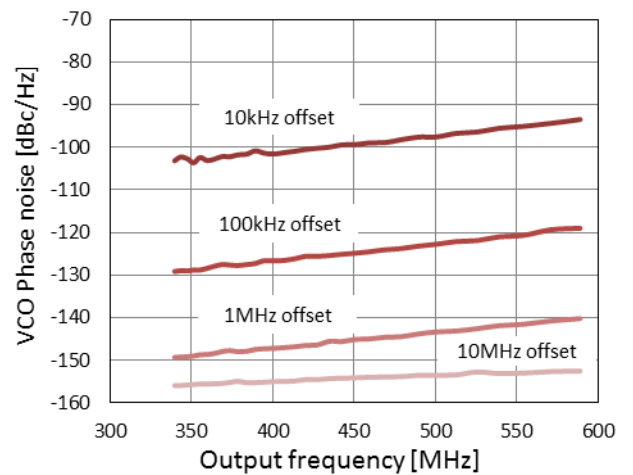
(a) VCOI bit = "0", DIV[2:0] bits = "000"



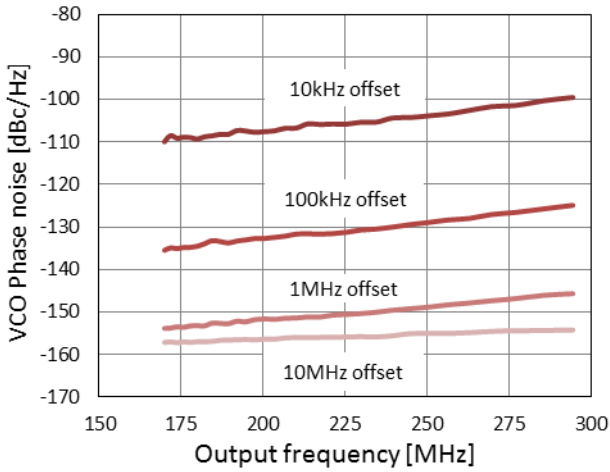
(b) VCOI bit = "1", DIV[2:0] bits = "000"



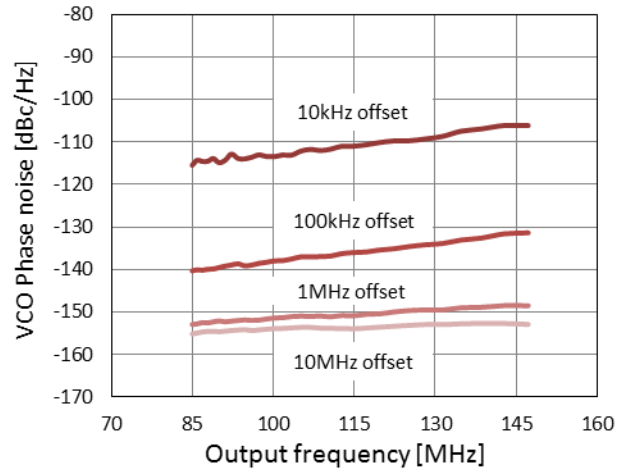
(c) VCOI bit = "1", DIV[2:0] bits = "001"



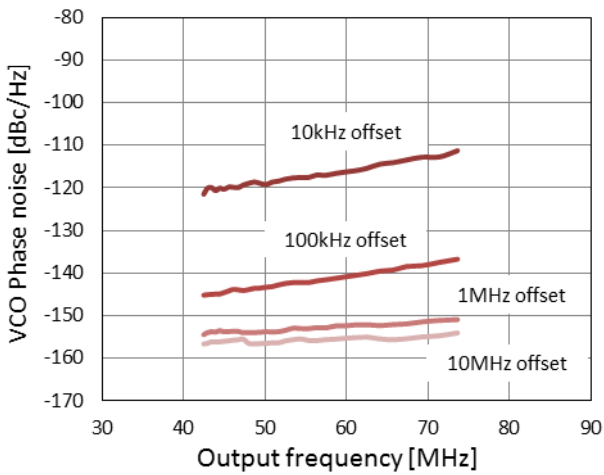
(d) VCOI bit = "1", DIV[2:0] bits = "010"



(e) VCOI bit = "1", DIV[2:0] bits = "011"



(f) VCOI bit = "1", DIV[2:0] bits = "100"



(g) VCOI bit = "1", DIV[2:0] bits = "101"

Figure.9 VCO Phase Noise vs. Output frequency
OUTLV[2:0] bits = "111"

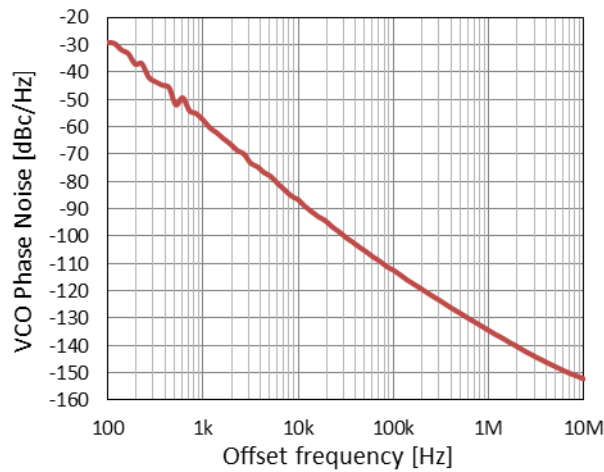


Figure.10 VCO Phase Noise vs. Offset frequency
Output frequency = 1602.8MHz, VCOI bit = "1", OUTLV[2:0] bits = "111"

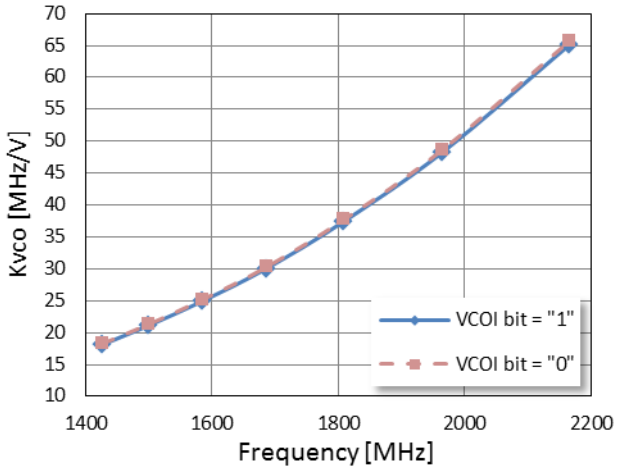


Figure.11 VCO Tuning Sensitivity

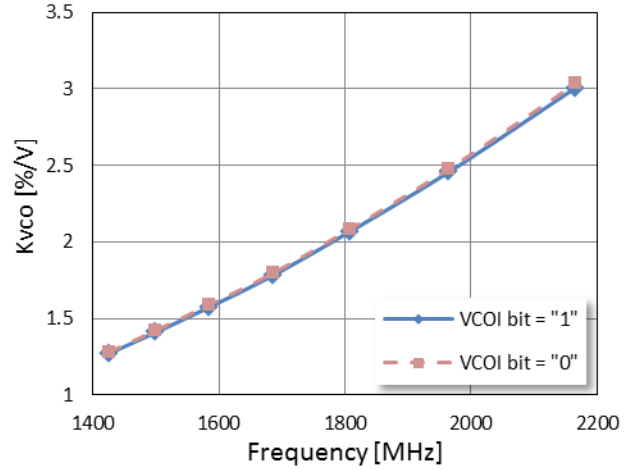
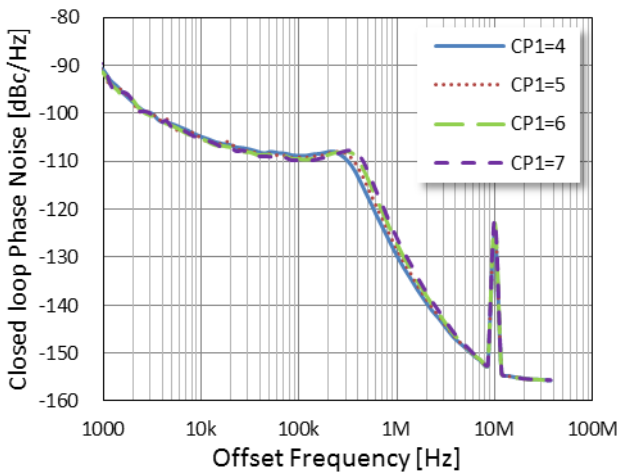
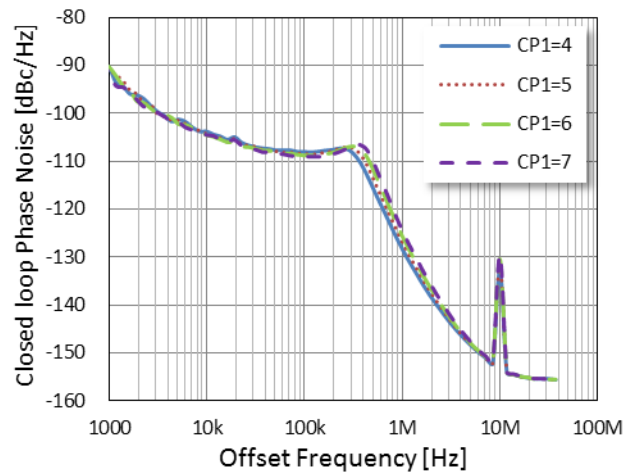


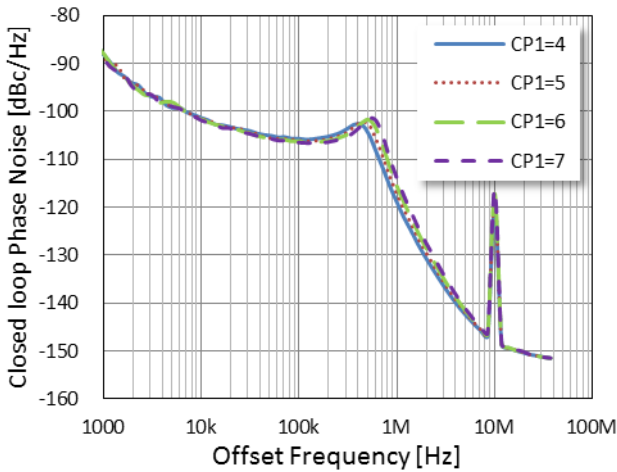
Figure.12 VCO Tuning Sensitivity



(a) Output frequency = 1500MHz



(b) Output frequency = 1600MHz



(c) Output frequency = 2100MHz

Figure.13 Closed loop Phase Noise

REFIN frequency = 120MHz, R counter = 12, Prescaler = 8/9
 Loop Filter : C1 = 33pF, C2 = 1500pF, C3 = N/A, R2 = 10kΩ, R3 = 0Ω

AK1573B

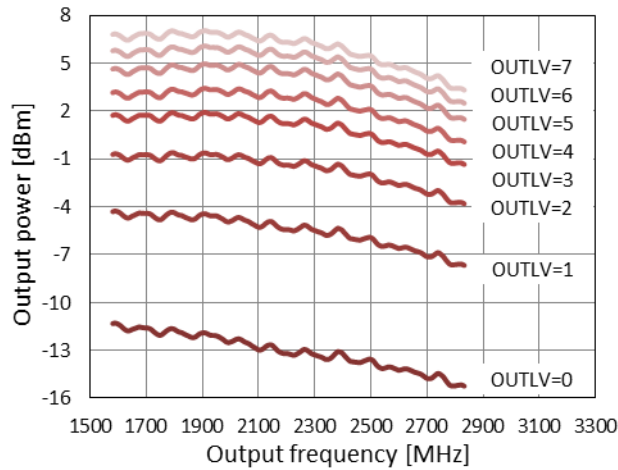
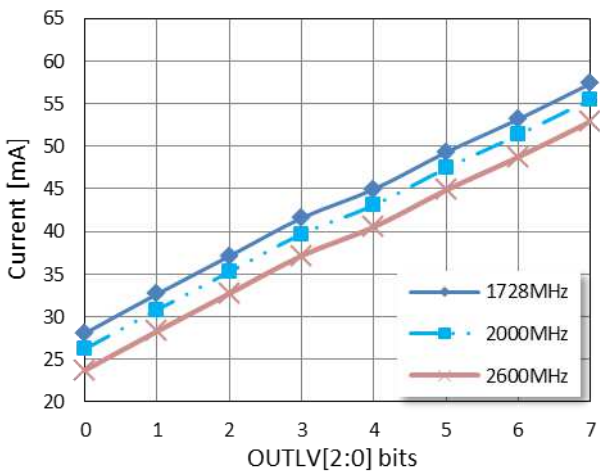
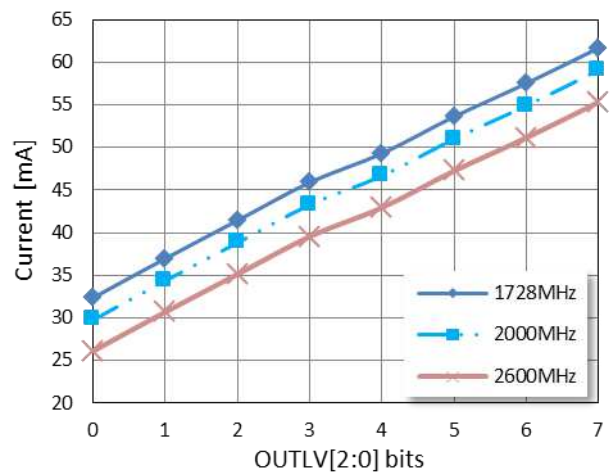


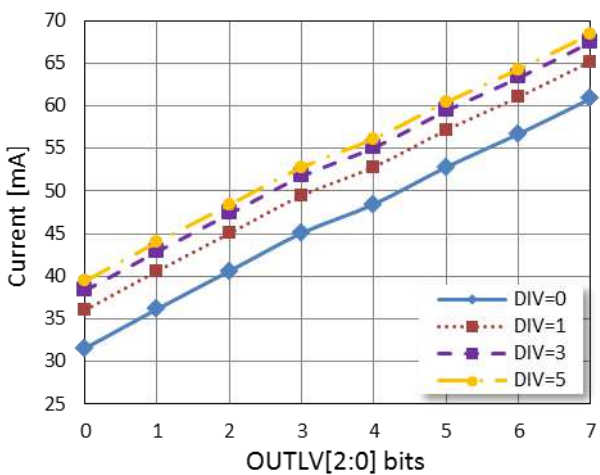
Figure.14 Output power vs. Output frequency



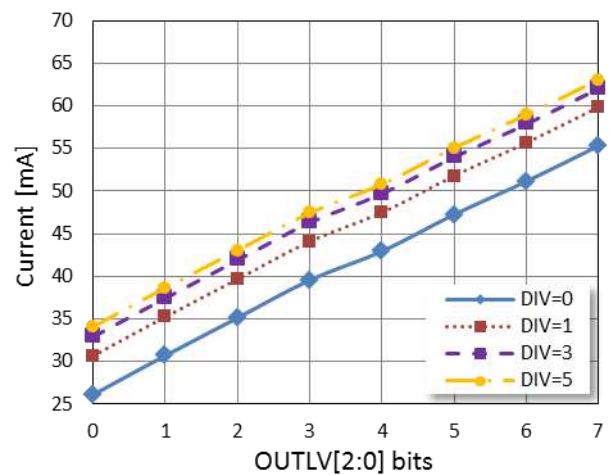
(a) VCOI bit = "0", DIV[2:0] bits = "000"



(b) VCOI bit = "1", DIV[2:0] bits = "000"

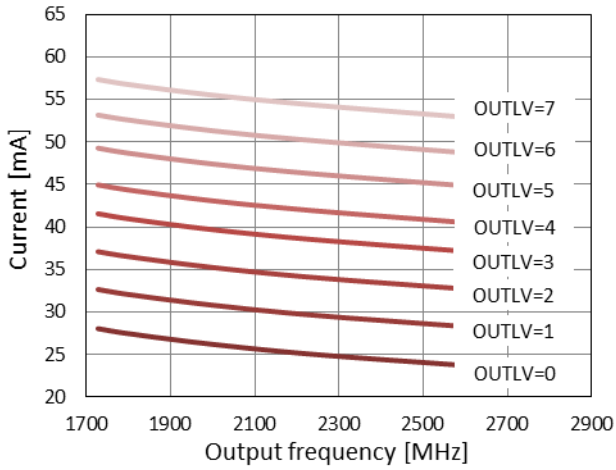


(c) Output frequency=1800MHz, VCOI bit="1"

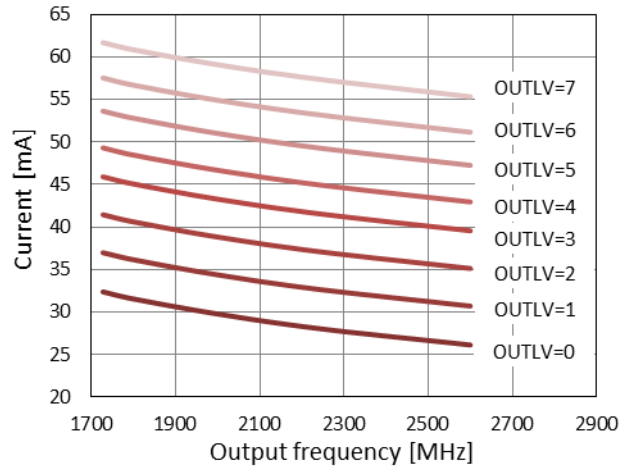


(d) Output frequency=2600MHz, VCOI bit="1"

Figure.15 Current vs. OUTLV[2:0] bits
REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = "111"



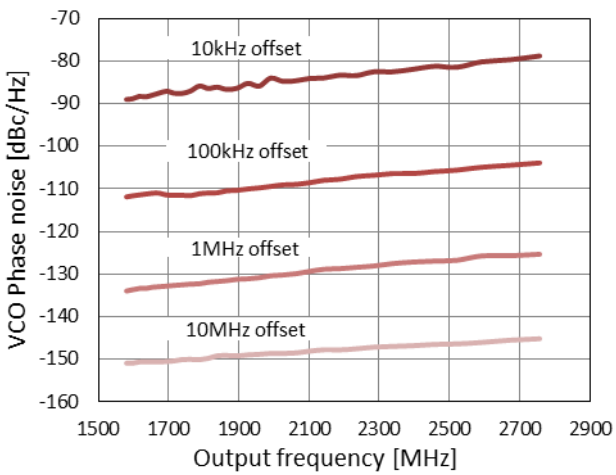
(a) VCOI bit = "0"



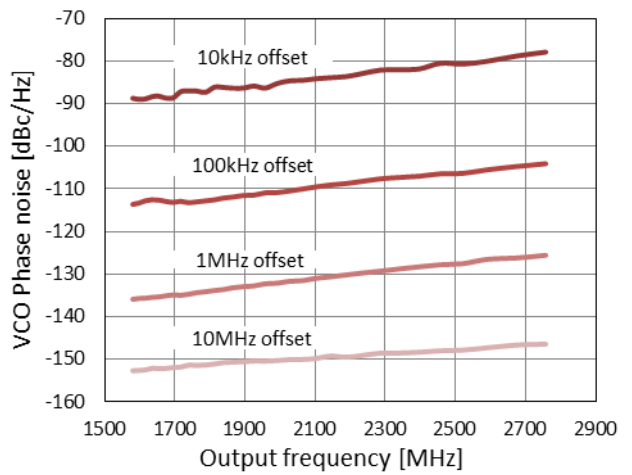
(b) VCOI bit = "1"

Figure.16 Current vs. Output frequency

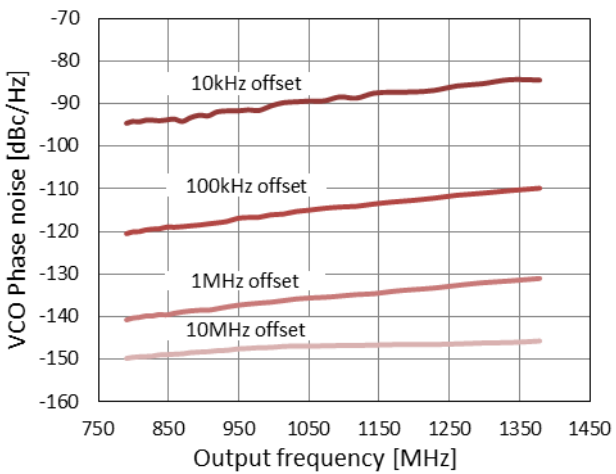
REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = "111", DIV[2:0] bits = "000"



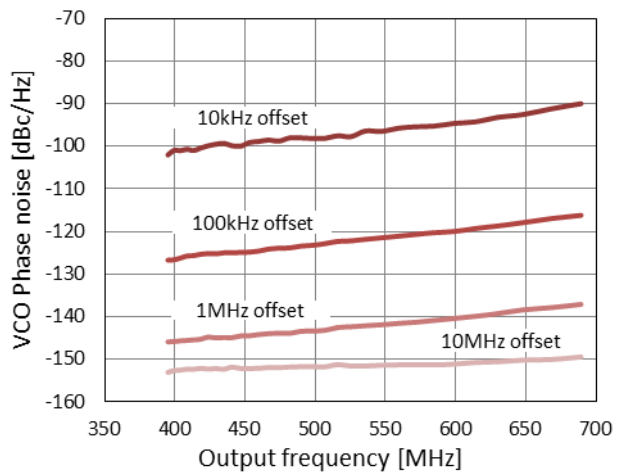
(a) VCOI bit = "0", DIV[2:0] bits = "000"



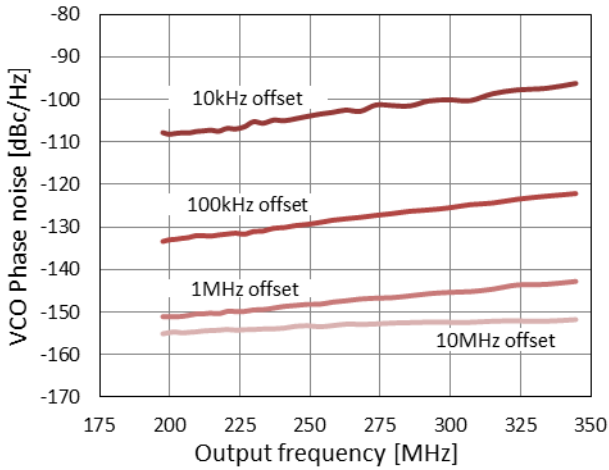
(b) VCOI bit = "1", DIV[2:0] bits = "000"



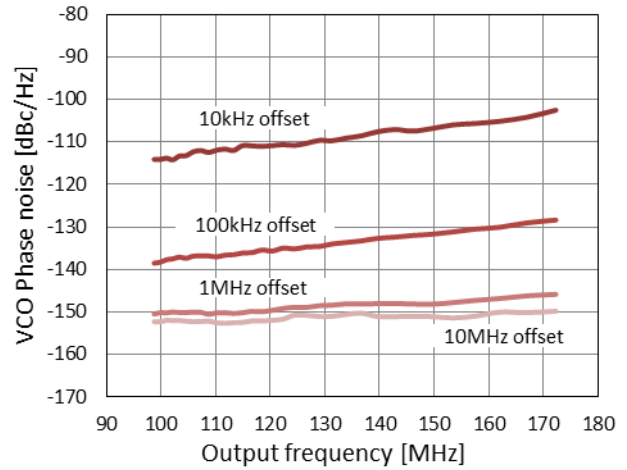
(c) VCOI bit = "1", DIV[2:0] bits = "001"



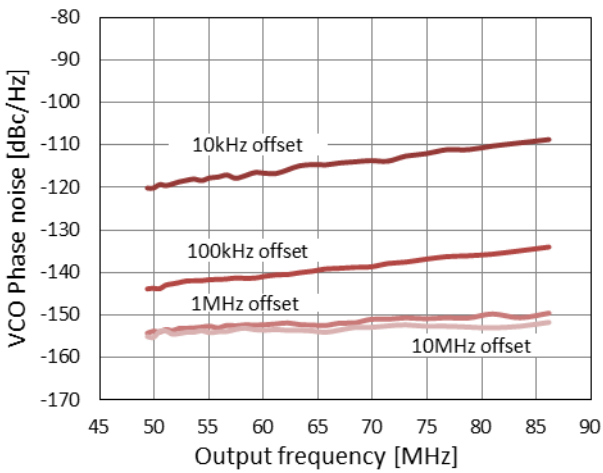
(d) VCOI bit = "1", DIV[2:0] bits = "010"



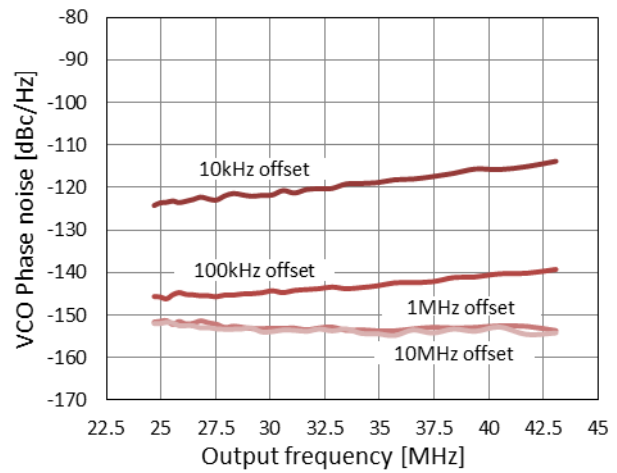
(e) VCOI bit = "1", DIV[2:0] bits = "011"



(f) VCOI bit = "1", DIV[2:0] bits = "100"



(g) VCOI bit = "1", DIV[2:0] bits = "101"



(h) VCOI bit = "1", DIV[2:0] bits = "110"

Figure.17 VCO Phase Noise vs. Output frequency
OUTLV[2:0] bits = "111"

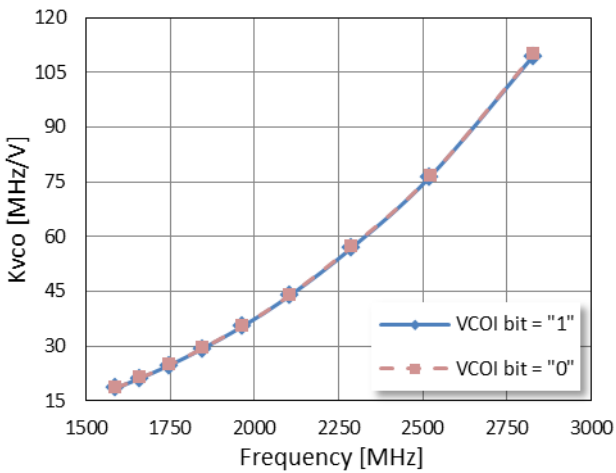


Figure.18 VCO Tuning Sensitivity

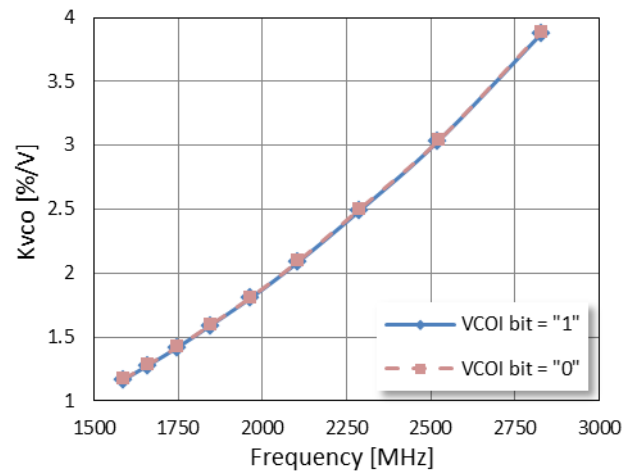


Figure.19 VCO Tuning Sensitivity

AK1573C

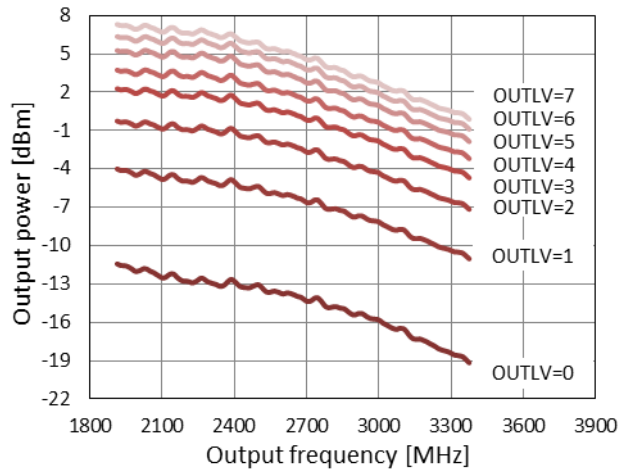
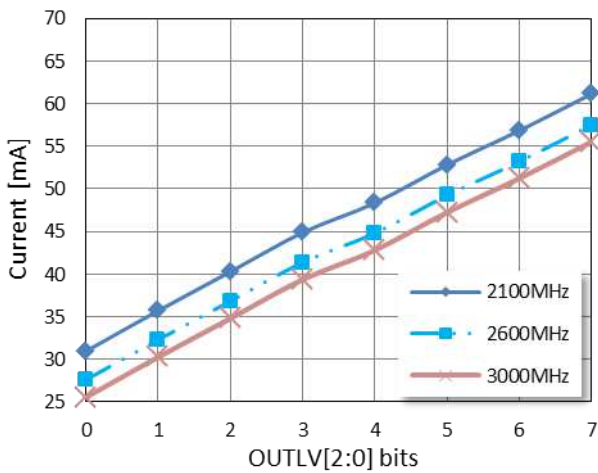
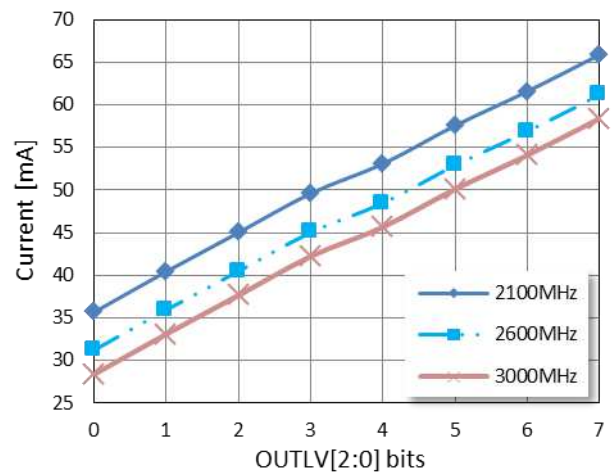


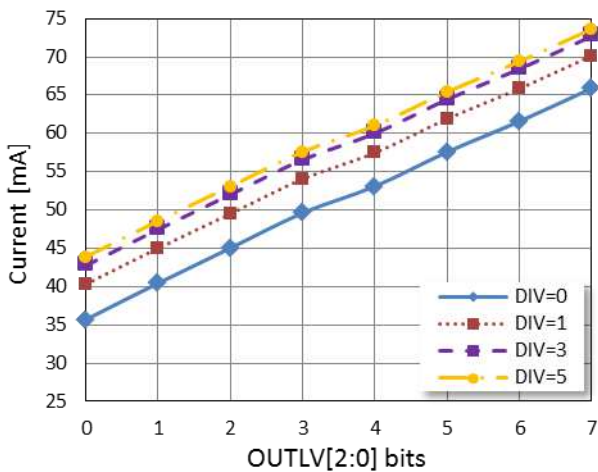
Figure.20 Output power vs. Output frequency



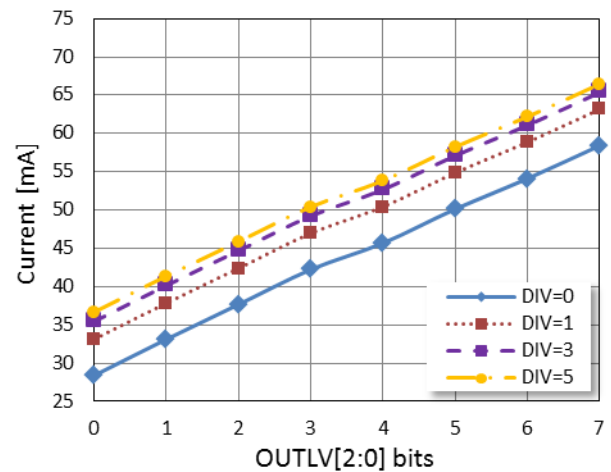
(a) VCOI bit = "0", DIV[2:0] bits = "000"



(b) VCOI bit = "1", DIV[2:0] bits = "000"

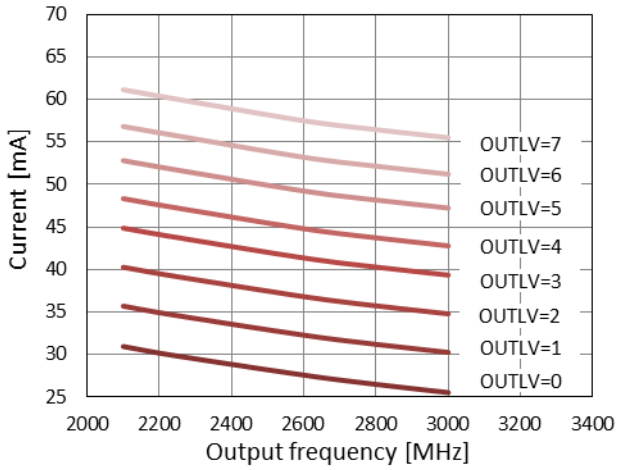


(c) Output frequency=2100MHz, VCOI bit="1"

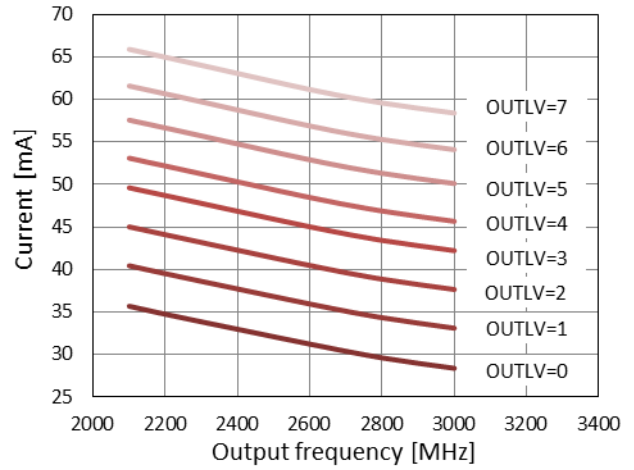


(d) Output frequency=3000MHz, VCOI bit="1"

Figure.21 Current vs. OUTLV[2:0] bits
REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = "111"



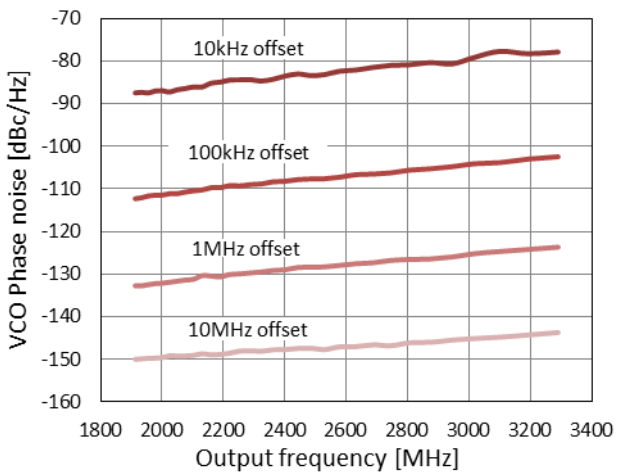
(a) VCOI bit = "0"



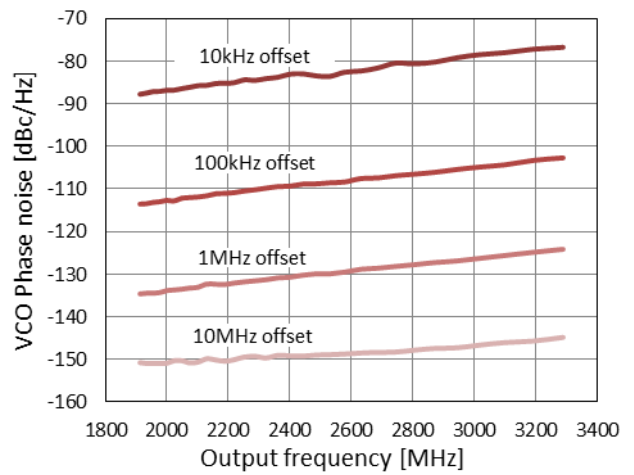
(b) VCOI bit = "1"

Figure.22 Current vs. Output frequency

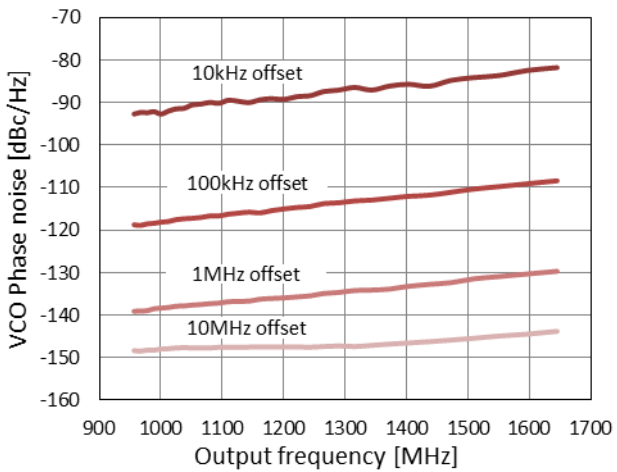
REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = "111", DIV[2:0] bits = "000"



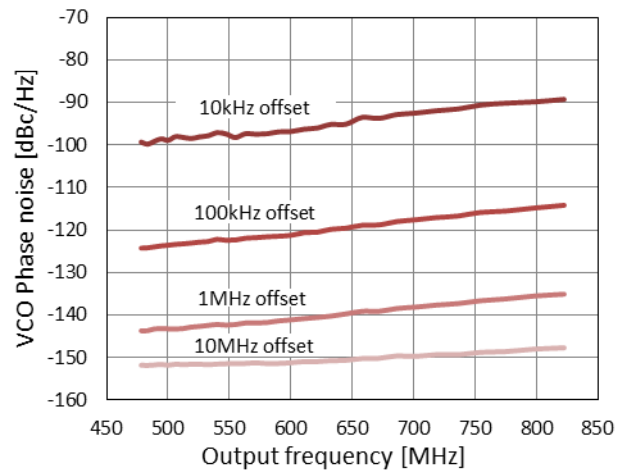
(a) VCOI bit = "0", DIV[2:0] bits = "000"



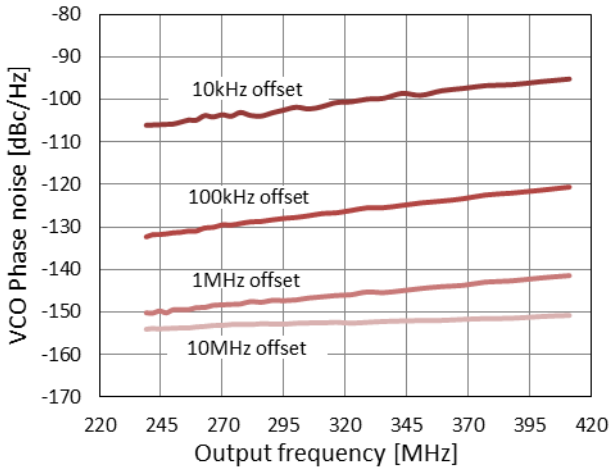
(b) VCOI bit = "1", DIV[2:0] bits = "000"



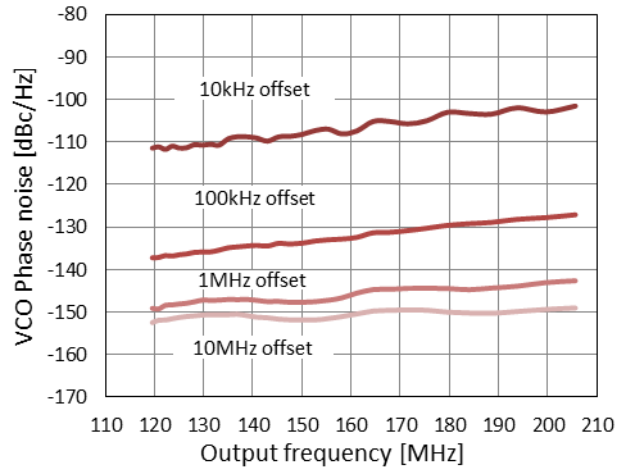
(c) VCOI bit = "1", DIV[2:0] bits = "001"



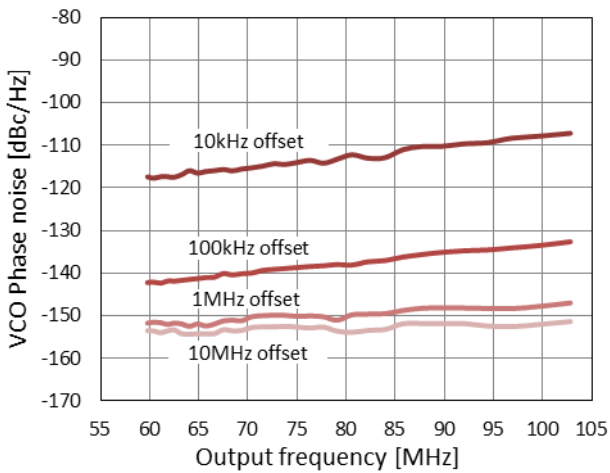
(d) VCOI bit = "1", DIV[2:0] bits = "010"



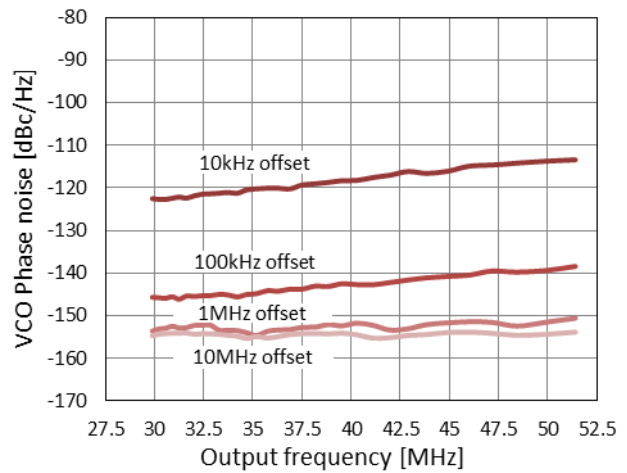
(e) VCOI bit = "1", DIV[2:0] bits = "011"



(f) VCOI bit = "1", DIV[2:0] bits = "100"



(g) VCOI bit = "1", DIV[2:0] bits = "101"



(h) VCOI bit = "1", DIV[2:0] bits = "110"

Figure.23 VCO Phase Noise vs. Output frequency
OUTLV[2:0] bits = "111"

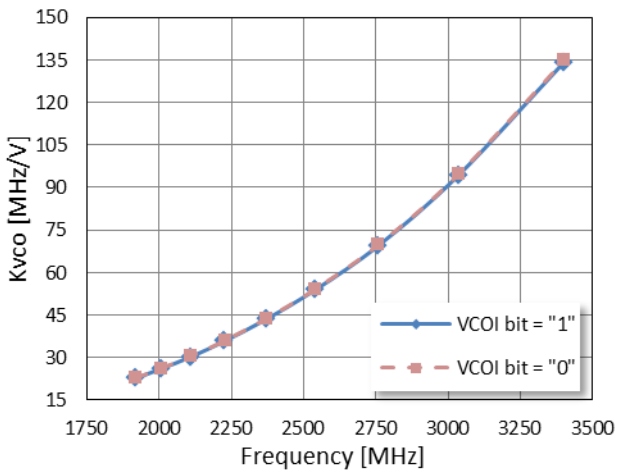


Figure.24 VCO Tuning Sensitivity

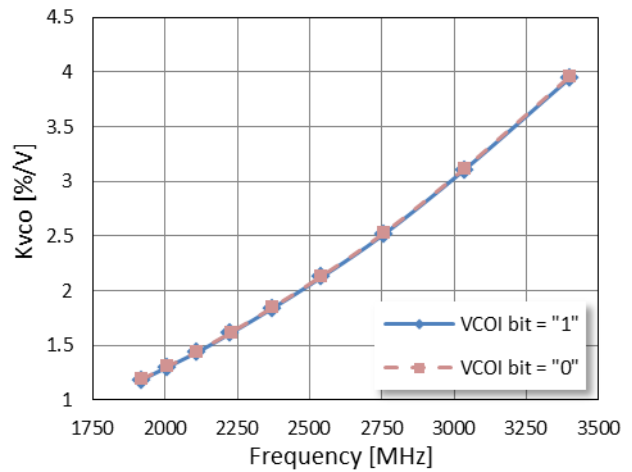


Figure.25 VCO Tuning Sensitivity

12. Register Map

Name	Data	Address			
A/B	D19 to D0	0	0	0	1
C/P		0	0	1	0
Ref/Pres		0	0	1	1
Function		0	1	0	0

	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
A/B	Don't care	B [12]	B [11]	B [10]	B [9]	B [8]	B [7]	B [6]	B [5]	B [4]	B [3]	B [2]	B [1]	B [0]	A [5]	A [4]	A [3]	A [2]	A [1]	A [0]	0x01
C/P	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	CP2 [2]	CP2 [1]	CP2 [0]	Don't care	Don't care	Don't care	CP1 [2]	CP1 [1]	CP1 [0]	0x02
Ref/Pres	CALTM [3]	CALTM [2]	CALTM [1]	CALTM [1]	PRE [1]	PRE [0]	R [13]	R [12]	R [11]	R [10]	R [9]	R [8]	R [7]	R [6]	R [5]	R [4]	R [3]	R [2]	R [1]	R [0]	0x03
Function	Don't care	Don't care	LDCNT SEL	FAST EN	CPHiZ	LD	DIV[2]	DIV[1]	DIV[0]	MTLD	OUTLV [2]	OUTLV [1]	OUTLV [0]	Don't care	Don't care	VCOI	FAST [3]	FAST [2]	FAST [1]	FAST [0]	0x04
Software Reset	Don't care																			0x05	

■ Notes on writing registers

1. When PDN1 pin = "H" and LDO (VREF1 pin) is active, access to the register is available
2. The setting of <Address0x02> and <Address0x03> will be reflected to the behavior of AK1573 when the register <Address0x01> is written
3. <Address0x04> can be written independently.
4. After PDN1 pin turns to "H", all of the register values are indefinite. It is needed to write the data to all the registers to confirm.

Examples of the register setting**Ex.1 Power on setting**

1. Set PDN1 pin = "L" and PDN2 pin = "L"
2. Power on VCOVDD, PVDD and CPVDD
Note) All VDD should be powered on simultaneously
3. Set PDN1 pin = "H" and PDN2 pin = "L" (VBG / LDO are powered on)
4. Write the data to the register <Address0x04>
5. Set PDN1 pin = "H" and PDN2 pin = "H" (All blocks are powered on)
6. Write the data to the register <Address0x01> and <Address0x02>
7. Write the data to the register <Address0x01>

Ex.2 Change frequency settings

1. Write the data to the register <Address0x01>

Ex.3 Change Charge Pump settings

1. Write the data to the register <Address0x02>
2. Write the data to the register <Address0x01>

Ex.4 Change Reference dividing ratio

1. Write the data to the register <Address0x03>
2. Write the data to the register <Address0x01>

< Address0x01 : N counter >

D[18:6]**B[12:0] : B (Programmable) counter setting**

Set the dividing ratio of B (Programmable) counter.
The setting range is shown in the following table.

B[12:0]	Programmable counter dividing ratio	Remark
0	-	Prohibited
1	-	Prohibited
2	-	Prohibited
3	3	
:	:	
8191	8191	

D[5:0]**A[5:0] : A (Swallow) counter setting**

Set the dividing ratio of A (Swallow) counter.
The setting range is shown in the following table.

A[5:0]	Swallow counter dividing ratio	Remark
0	0	
1	1	
2	2	
:	:	
63	63	

The data at A[5:0] bits and B[12:0] bits must meet the following requirements:

$$B[12:0] \text{ bits} \geq 3, B[12:0] \text{ bits} \geq A[5:0] \text{ bits}$$

See "13. Frequency Setting" for details of the relationship between a frequency dividing ratio N and the data at A[5:0] bits and B[12:0] bits.

It is prohibited to set frequency once again until VCO calibration and Fast lock-up mode is completed.

< Address0x02 : C/P >

D[8: 6]**CP2[2:0] : Charge pump current setting for Fast Lockup operation****D[2:0]****CP1[2:0] : Charge pump current setting for normal operation**

AK1573 provides two settings for charge pump current. CP1[2:0] bits are for normal operation and CP2[2:0] bits are for Fast Lockup mode.

The following formula shows the relationship among the resistance value, the register setting and the electric current.

$$\text{Charge pump current (Icp) [A]} = \text{Icp_min [A]} \times [(\text{CP1[2:0] bits or CP2[2:0] bits setting}) + 1]$$

$$\text{Charge pump minimum current (Icp_min) [A]} = 9.45 / \text{BIAS Resistance } [\Omega]$$

The following table shows the typical Icp for each status.

Icp (typ.) unit : μA

CP1[2:0], CP2[2:0]	BIAS		
	33k Ω	27k Ω	22k Ω
0	286	350	430
1	573	700	859
2	859	1050	1289
3	1146	1400	1718
4	1432	1750	2148
5	1718	2100	2577
6	2005	2450	3007
7	2291	2800	3436

< Address0x03 : Ref/Pres >

D[19:16]

CALTM[3:0] Set the calibration precision of VCO

The register CALTM[3:0] bits set the calibration precision and time. The larger CALTM[3:0] bits are set, the higher calibration precision becomes, but the longer calibration time is required as trade-off. Set the value calculated by the following formula to get enough calibration precision. However, CALTM[3:0] bits should be set from 0 to 10. Over 11 are prohibited. See "15. VCO" for details of the VCO calibration.

$$\text{CALTM[3:0] bits} \geq 10 - \log(\text{B[12:0] bits}) / \log(2)$$

The calibration time can be estimated as following formula;

$$\text{Calibration time} = 1 / F_{\text{PFD}} \times 11 \times 2^{\text{CALTM[3:0] bits}}$$

D[15:14]

PRE[1:0] : Selects a dividing ratio for the prescaler

- 00: P=8
- 01: P=16
- 10: P=32
- 11: P=64

The prescaler value should be selected so that the prescaler output frequency is less than or equal to 300MHz.

D[13:0]**R[13:0] : 14bit Reference Counter**

The following settings can be selected for the reference clock division.
The allowed range is 1 (1/1 division) to 16383 (1/16383 division). 0 cannot be set.
The maximum PFD frequency is 104MHz.

R[13:0]	Dividing Ratio
0	Prohibited
1	1
2	2
3	3
4	4
:	:
:	:
:	:
16381	16381
16382	16382
16383	16383

< Address0x04 : Function >

D[17]**LDCNTSEL : Lock Detect Precision**

Set the counter value for digital lock detect.

LDCNTSEL	Function	
0	15 times Count	unlocked to locked
	3 times Count	locked to unlocked
1	31 times Count	unlocked to locked
	7 times Count	locked to unlocked

D[16]**FASTEN : Enables the Fast Lock mode**

See "14. Fast Lock-up mode" for details of the Fast Lock-up function.

- 0: Fast Lockup disable
- 1: Fast Lockup enable

D[15]**CPHIZ : TRI-STATE output setting for charge pump**

- 0: Charge pumps are activated
- 1: Tri-State

D[14]**LD : Selects output from LD pin**

See "12. Lock detect" for details of the Lock detect function.

- 0: Digital lock detect
- 1: Analog lock detect