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AK2306/2306LV

Dual PCM CODEC for ISDN/VoIP TERMINAL ADAPTER

GENERAL DESCRIPTION

AK2306 is a dual PCM CODEC-Filter most suitable for ISDN Terminal Adapter.

It includes Selectable A-law/u-law function, Internal Gain Adjustment from +6dB to –18dB by 1dB step control, Selectable 16Hz/20Hz Ring Tone Generator for SLIC. All of these functions are controlled by the internal register accessed through the serial interface.

PCM interface of AK2306 accepts Long Frame, Short Frame clock formats and GCI format. 64 x N kHz(128k-4096kHz) clock input is available for PCM interface.

AK2306 and AK2306LV are pin-compatible, but different products which power supply voltage are 5.0V and 3.3V,respectively.

FEATURE

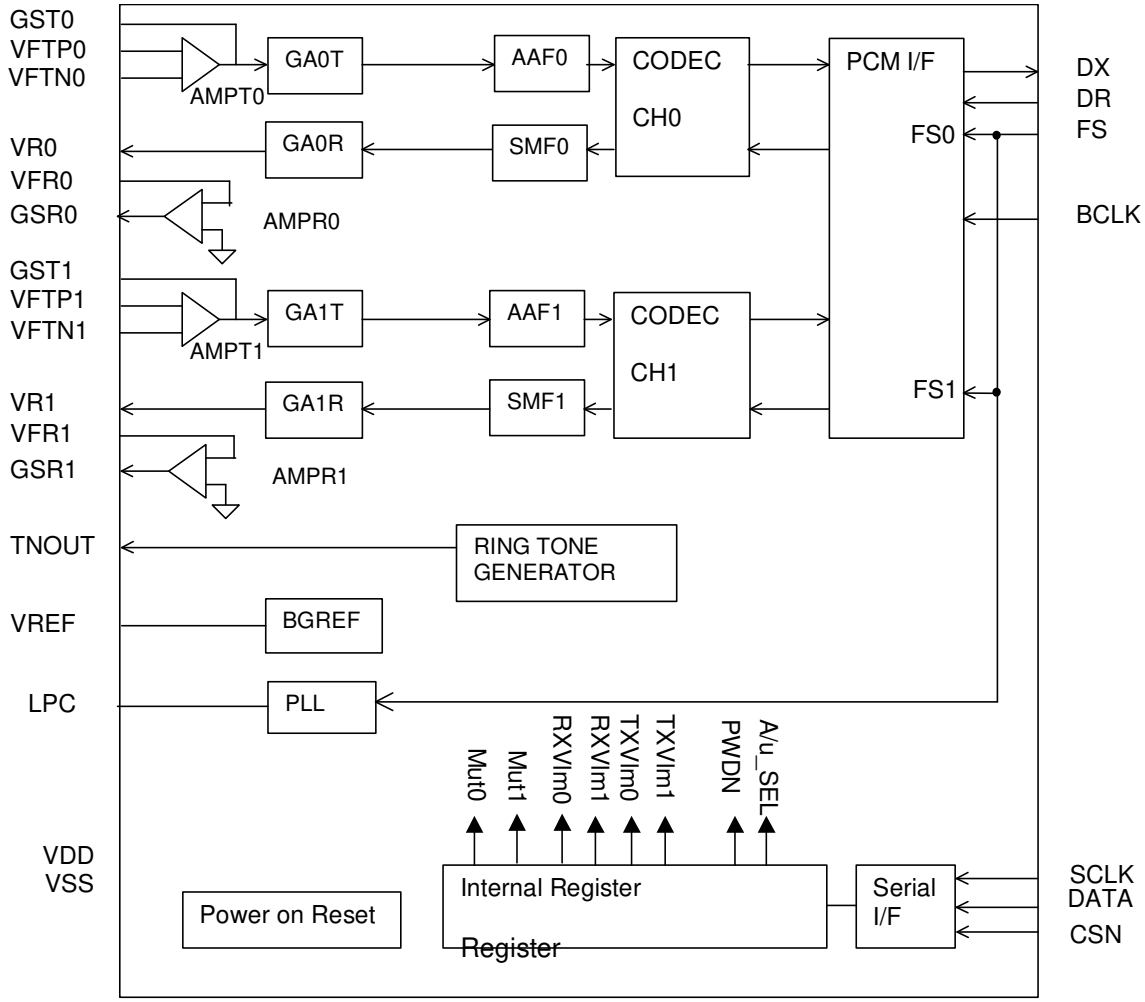
- Dual PCM CODEC and Filtering systems for ISDN Terminal Adapter
- Selectable Ring Tone Generator for SLIC
  16Hz or 20Hz tone is available.
- Independent functions on each channel controlled by the internal register
  - Power Down Mode
  - Mute
  - Gain Adjustment: +6 to -18dB (1dB step)
- Selectable PCM Data Interface Timing: Long Frame / Short Frame/GCI
- Variable PCM Data Rate: 64k x N [Hz] (128k - 4.096MHz)
- OP Amp for External Gain Adjustment
- A-law/u-law Register Selectable
- Serial Interface to access the internal register
- Power on Reset
- Single Power Supply Voltage
  - +5.0V ± 5% (AK2306)
  - +3.3V ± 0.3V (AK2306LV)
- Low Power Consumption

PACKAGE

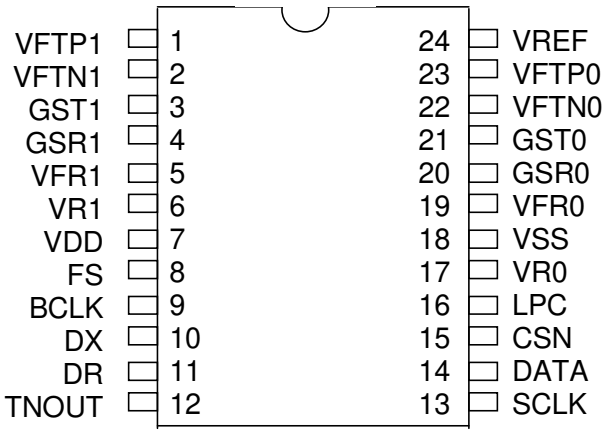
- 24pinSSOP
  8 .2 x 7.9 mm (0.65mm pin pitch)

CONTENTS

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN CONDITION

Pin#	Name	I/O	Pin type	AC load (MAX.)	DC load (MIN.)	Outout status (Power down mode)	Output status (Reset)	Remarks
	VFTP1		Analog					
	VFTN1		Analog					
	GST1		Analog	50pF	10kΩ(*1)	Hi-Z	Hi-Z	
	GSR1	O	Analog	50pF	10kΩ (*1)	Hi-Z	Hi-Z	
	VFR1	I	Analog					
	VR1	O	Analog	50pF	10kΩ	Hi-Z	Hi-Z	
	VDD	-						
	FS	I	TTL/CMOS(*3)					
	BCLK	I	TTL/CMOS(*3)					
	DX	O	CMOS	15pF		Hi-Z	Hi-Z	
	DR	I	TTL/CMOS(*3)					
	TNOUT	O	CMOS	15pF		L	L	
	SCLK	I	TTL/CMOS(*3)					
	DATA	I/O	TTL/CMOS(*3)	15pF		Input	Input	
	CSN	I	TTL/CMOS(*3)					
	LPC	O	Analog					0.22uF (*2)
	VSS	-						
	VR0	O	Analog	50pF	10kΩ	Hi-Z	Hi-Z	
	VFR0	I	Analog					
	GSR0	O	Analog	50pF	10kΩ (*1)	Hi-Z	Hi-Z	
	GST0	I	Analog	50pF	10kΩ (*1)	Hi-Z	Hi-Z	
	VFTN0	O	Analog					
	VFTP0	O	Analog					
	VREF	O	Analog					1.0 uF (*2)

*1) DC load(MIN.) includes a feedback resistance of input/output op-amp.
*2)External capacitance should be connected to VSS.
*3)TTL level is applied only for the input level of AK2306. Output level for both AK2306 and AK2306LV,and the input level of AK2306LV are CMOS level.

PIN FUNCTION

Pin#	Name	I/O	Function
1	VFTP1	I	**Positive analog input of the transmit OPamp(AMPT1) for channel 1.** Transmit gain is defined by the ratio of R2/R1. R1 is the external input resister connected to this pin. R2 is the external feedback resister connected between this pin and GST1.
2	VFTN1	I	**Negative analog input of the transmit OPamp(AMPT1) for channel 1.**
3	GST1	O	**Output of the transmit OPamp(AMPT1) for channel 1.** The external feedback resister is connected between this pin and VFTP1.
4	GSR1	O	**Output of the receive OPamp(AMPR1) for channel 1.**
5	VFR1	I	**Negative analog input of the receive OPamp(AMTR1) for channel 1.** Receive gain is defined by the ratio of R4/R3. R3 is the external input resister connected to this pin. R4 is the external feedback resister connected between this pin and VR1.
6	VR1	O	**Analog Output equivalent to the received PCM data for channel 1.** Output gain is adjusted by the GA1R.
22	VFTN0	I	**Negative analog input of the transmit OPamp(AMPT0) for channel 0.** Transmit gain is defined by the ratio of R2/R1. R1 is the external input resister connected to this pin. R2 is the external feedback resister connected between this pin and GST0.
23	VFTP0	I	**Positive analog input of the transmit OPamp(AMPT0) for channel 0.**
21	GST0	O	**Output of the transmit OPamp(AMPT0) for channel 0.** The external feedback resister is connected between this pin and VFTP0.
17	VR0	O	**Analog Output equivalent to the received PCM data for channel 0.** Output gain is adjusted by the GA0R
19	VFR0	I	**Negative analog input of the receive OPamp(AMTR0) for channel 0.** Receive gain is defined by the ratio of R4/R3. R3 is the external input resister connected to this pin. R4 is the external feedback resister connected between this pin and VR0.
20	GSR0	O	**Output of the receive OPamp(AMPR0) for channel 0.**
10	DX	O	**Serial output of PCM data.** The channel 1 data is output following the channel 0 data. The PCM data rate is synchronized with BCLK. This output remains in the high impedance state except for the period of transmitting PCM data.
11	DR	I	**Serial input of PCM data.** The channel 1 data is received following the channel 0 data. The PCM data rate is synchronized with BCLK.
8	FS	I	**Frame sync input.** This clock is input for the internal PLL which gerenates the internal system clocks. FS must be 8kHz clock which is synchronized with BCLK.
9	BCLK	I	**Bit clock of PCM data interface.** This clock defines the input/output timing of DX and DR. The frequency of BCLK should be 64 x N kHz(128k – 4096kHz).

Pin#	Name	I/O	Function
12	TNOUT	O	**Ring Tone output pin.** 16Hz or 20Hz tone is selected by the internal register.
14	DATA	I/O	**Data input of serial interface.**
13	SCLK	I	**Clock input of serial interface.**
15	CSN	I	**Read and write enable of serial interface.**
16	LPC	O	**Pin for PLL loop filter.** External capacitance(Min 0.22uF) should be connected between this pin and VSS.
24	VREF	O	**Analog ground output.** External capacitance(1.0 uF) should be connected between this pin and VSS.
7	VDD	-	**Positive supply voltage.** +5V(AK2306) or +3.3V(AL2306LV) supply.
18	VSS	-	**Ground.**

CIRCUIT DESCRIPTION

Block	Function
AMPT0,1	Op-amp for input gain adjustment. This op-amp has differential inputs. Adjusting the gain with external resistors. The resistor larger than 10kΩ is recommended for the feedback resistor. <NOTE> AMPT0(1) becomes automatically power down, when CODEC ch0(1) is power down.
AMPR0,1	Op-amp for output gain adjustment. This op-amp is used as an inverting amplifier. Adjusting the gain with external resistors. The resistor larger than 10kΩ is recommended for the feedback resistor.
AAF	Integrated anti-aliasing filter which prevents signals around the sampling rate from folding back into the voice band. AAF is a 2nd order RC low-pass filter.
A/D	Converts analog signal to 8bit PCM data according to the companding schemes of ITU recommendation G.711; A-law or u-law. The band limiting filter is also integrated. The selection of companding schemes is set by ALAWN register as follows: "H": u-Law "L": A-Law
D/A	Expands 8bit PCM data according to A-law or u-law. The selection of companding schemes is set by ALAWN register as follows: "H": u-Law "L": A-Law
SMF	Extracts the inband signal from D/A output. It also corrects the sinx/x effect of D/A output.
BGREF	Provides the stable analog ground voltage using an on-chip band-gap reference circuit which is temperature compensated. The output voltage is 2.4V for +5V operation(AK2306) or 1.5V for +3.3V operation(AK2306LV).
RING TONE GENERATOR	Generates two kinds of tone; 16Hz or 20Hz. Tone selection and Tone ON/OFF is controlled by the registers.
GA0T/R GA1T/R GATN	Gain selects of analog I/O signals. It is posibble to select gain from +6dB to -18dB (1dB/step). Gain is defined by the internal register.
SERIAL I/F	Interface to the internal register by using SCLK, DATA, and CSN pins.
PLL	PLL generates system clock of AK2306. Reference clock is FS (8KHz). More than 0.22uF of an external capacitance should be connected between LPC and VSS.
PCM I/F	PCM data rate is available for 64xN(N = 2 to 64)kHz which synchronizes with BCLK. Two kinds of data format (Long Frame, Short Frame) are available. Each data format is automatically detected. PCM data stream, which includes ch0 and ch1 data, is output through DX pin and input through DR pin. Ch1 PCM data stream always follows ch0 PCM data stream.

FUNCTIONAL DESCRIPTION

PCM Data Interface

AK2306 supports the following 3 PCM data formats

- **Long Frame Sync(LF)**
- **Short Frame Sync(SF)**
- **GCI**

PCM data of both channels are multiplexed and interfaced through the common pins(DR,DX).The first 8bit is defined as B1 channel and the seconds 8bit is defined as B2 channel in the PCM data stream.
The order of PCM data is MSB first in each channel.

Selection of the interface mode

The GCI and ordinary PCM interface(LF,SF) are selectable through the CPU register as following table.
LF and SF is automatically selected by AK2306 by means of detecting the length of 8KHz frame signal.

Register for PCM Interface mode select (Address:101 Bit:0)

PCMIF	PCM Interface	Comments
0	LF or SF	LF/SF are selected automatically
1	GCI	

∗ Default on power-on reset =LF/SF mode(PCMIF=0).

LONG FRAME(LF) / SHORT FRAME (SF)

Automatic LF/SF selection

AK2306 monitors the duration of the “H” level of FS and automatically selects LF or SF interface format.

period of FS=”H”	Interface format
more than 2 clocks of BCK	LF
1 clock of BCK	SF

Timing of the interface

8 bits PCM data is accommodated in 1 frame(125us) defined by 8kHz frame sync signal.
Although there are 64 time slots at maximum in 8kHz frame(when BCK=4.096MHz), PCM data for AK2306 occupy first and second time slot for channel 0 and channel 1,respectively as is indicated in figures of next page.

- Frame Sync signal (FS)

8kHz reference signal. This signal indicated the timing and the frame position of 8kHz PCM interface. All the internal clock of the LSI is generated based on this FS signal.

- Bit Clock (BCLK)

BCLK defines the PCM data rate. BCLK can be varied from 128kHz to 4.096MHz by 64kHz step.

- Position of the Ch0,Ch1 PCM data in the DX/DR data flow

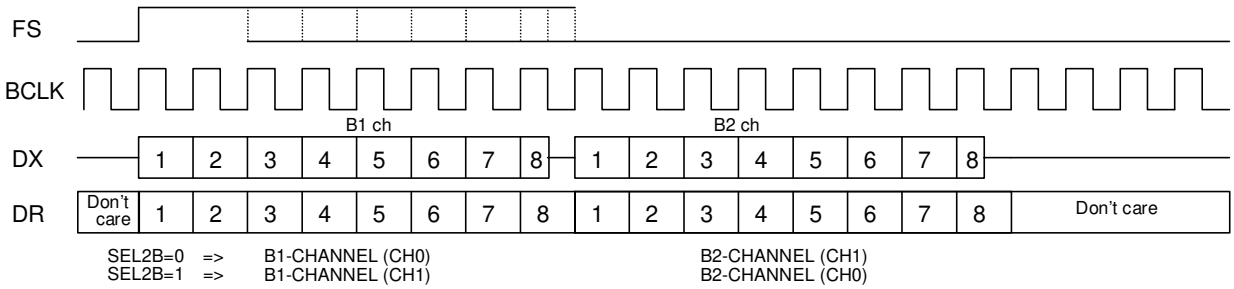
B1 and B2 channel of the PCM data channel are assigned to Analog Ch0 and Ch1 as is defined by SEL2B register.

CH0,1selection (Address:100 Bit:5)

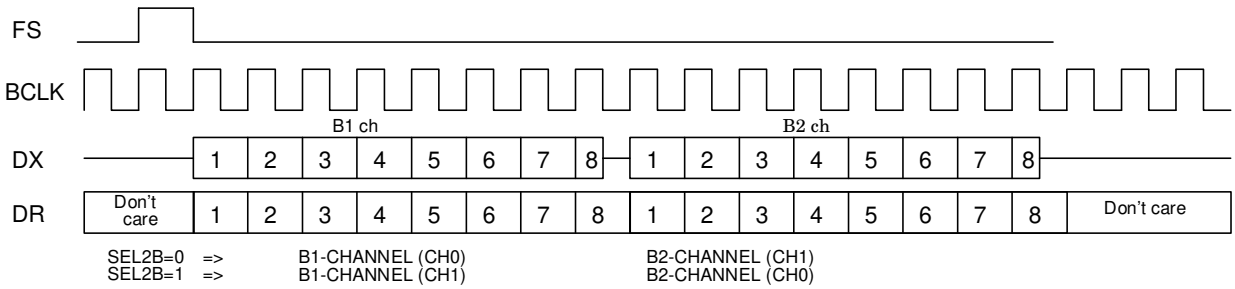
SEL2B	CH0	CH1	Remarks
0	B1	B2	Default on Reset
1	B2	B1	

<2ch Multiplexed>

LongFrame



ShortFrame



<Non Multiplex>

Not supported

! Important Notice

Please don't stop feeding FS and BCLK except Full power down mode.

Internal PLL does free running when either FS or BCLK is not provided. In this case, the frequency of Ring Tone output is not guaranteed.

GCI (General Circuit Interface)

GCI format is used for ISDN application. The data format and clocking is showed as Fig X.

timing of the interface

8 bits PCM data is accommodated in 1 frame(125us) defined by 8kHz frame sync signal.
Although there are 32 time slots at maximum in 8kHz frame(when BCK=4.096MHz), PCM data on GCI occupy first and second time slot for channel 0 and channel 1,respectively.

Frame Sync signal (FS)

8kHz reference signal. This signal indicated the timing and the frame position of 8kHz GCI. All the internal clock of the LSI is generated based on this FS signal. High level duration of the FS is 1 clock period of BCLK.

Bit Clock (BCLK)

BCLK defines the GCI data rate. The bit rate of GCI data is half of BCLK. BCLK can be varied from 512kHz to 4.096MHz by 128kHz step.

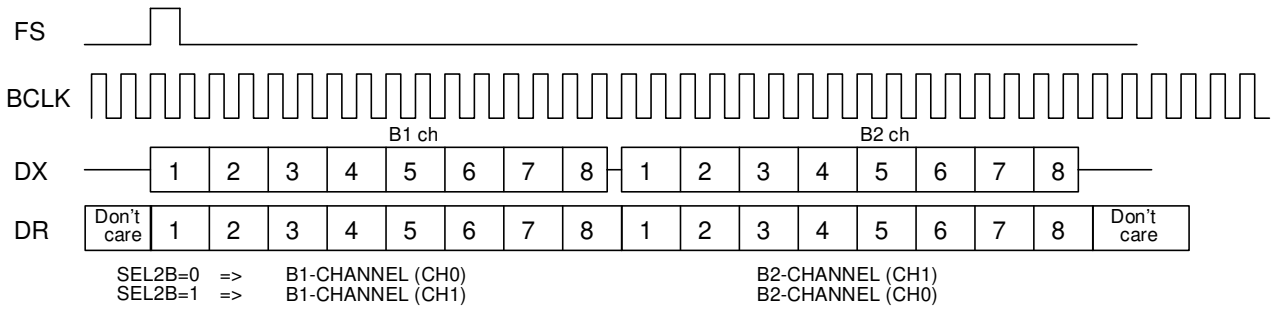
Position of the Ch0,Ch1 GCI data in the DX/DR data flow

B1 and B2 channel of the GCI data channel are assigned to Analog Ch0 and Ch1 as is defined by SEL2B register as same way as PCM interface.

CH0,1selection(Address:100 Bit:5)

SEL2B	CH0	CH1	Remarks
0	B1	B2	Default on Reset
1	B2	B1	

<2ch Multiplex>



<Non Multiplex>

Not supported

! Important Notice

Please don't stop feeding FS and BCLK except Full power down mode.

Internal PLL does free running when either FS or BCLK is not provided. In this case, the frequency of Ring Tone output is not guaranteed.

MUTE

The output on each channel can be muted independently through the CPU register as shown in the table.

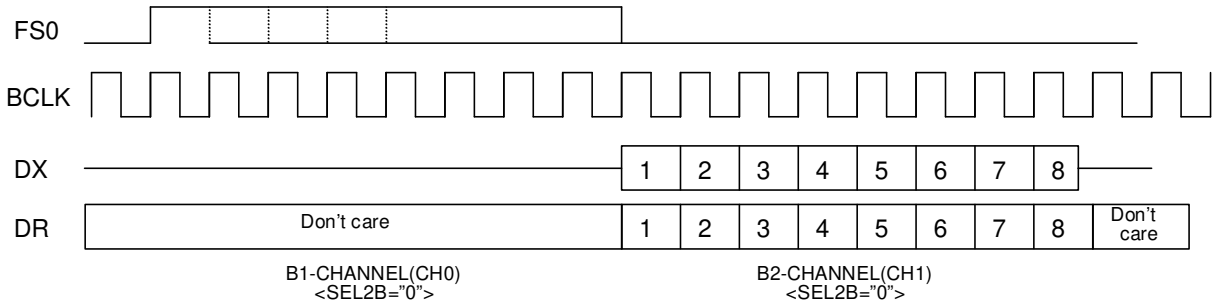
Mute register(Address:100 Bit:5,4)

MTCH0,1	Operation	DX pin	VRX pin
0	Normal	PCM data output	CODEC analog output
1	Mute	High-Impedance(*1)	AGND*

(*1)
MTCH0 and MTCH1 are the mute control bit for CH0 and CH1,respectively. B1 and B2 channel muted by MTCH0/1 is defined by SEL2B bit shown in the PCM Interface section.

<EXAMPLE>

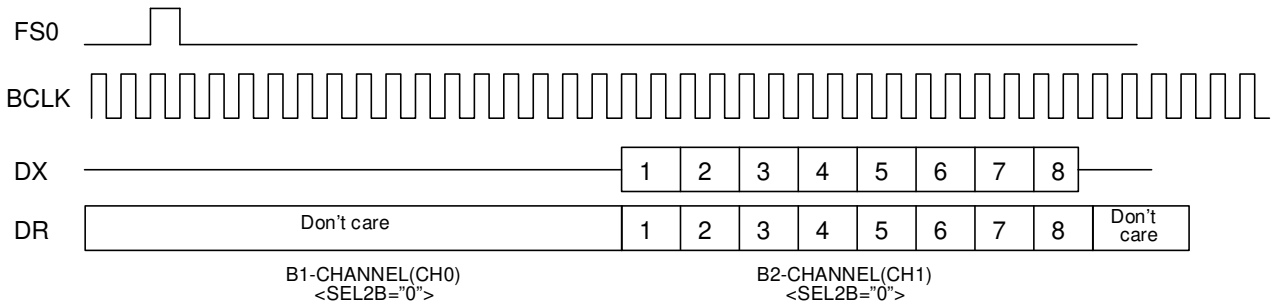
LF Mode CH0 mute (MTCH=1, MTCH1=0, SEL2B=0)



VRX0 : CODEC CH0 analog output is always at AGND level.

VRX1 : CODEC CH1 analog output is the signal converted from the PCM data of CH1 input through DR pin.

GCI mode CH0 mute (MTCH0=1, MTCH1=0, SEL2B=0)



VRX0 : CODEC CH0 analog output is always at AGND level.

VRX1 : CODEC CH1 analog output is the signal converted from the PCM data of CH1 input through DR pin.

GAIN ADJUSTMENT

Analog input/output gain can be adjusted at the range from +6dB to –18dB by 1.0dB step through CPU register.

VR Register(Address:011 –000 Bit:4 –0)

GanT4 GanR4	GanT3 GanR3	GAnT2 GAnR2	GAnT1 GAnR1	GAnT0 GAnR0	Gain [dB]	Remarks
0	0	0	0	0	+6	
0	0	0	0	1	+5	
0	0	0	1	0	+4	
0	0	0	1	1	+3	
0	0	1	0	0	+2	
0	0	1	0	1	+1	
0	0	1	1	0	0	Default
0	0	1	1	1	-1	
0	1	0	0	0	-2	
0	1	0	0	1	-3	
0	1	0	1	0	-4	
0	1	0	1	1	-5	
0	1	1	0	0	-6	
0	1	1	0	1	-7	
0	1	1	1	0	-8	
0	1	1	1	1	-9	
1	0	0	0	0	-10	
1	0	0	0	1	-11	
1	0	0	1	0	-12	
1	0	0	1	1	-13	
1	0	1	0	0	-14	
1	0	1	0	1	-15	
1	0	1	1	0	-16	
1	0	1	1	1	-17	
1	1	---	---	---	-18	

RING TONE GENERATOR

Ring tone generator generates two kinds of ring tone, 16Hz and 20Hz. The frequency of the tone can be selected by CPU register.

Tone frequency selection

Tone Selection register (Address: 101, Bit: 3)

TNFQ	Tone Frequency	Remarks
0	16Hz	Default
1	20Hz	

Tone output enable

Tone output can be enabled/disabled through CPU register.

RING TONEGEN Enable (Address: 100, Bit: 2)

PDTN	RING TONE GENERATOR	Remarks
1	Power Down*	Default
0	Tone output enabled	

* When Power down is selected, TNOUT pin output is fixed to “L” level.

RESET

Power on Reset

AK2306 automatically generates the internal reset pulse which resets all the circuit that is necessary to start the initialization after the power on reset. The CPU registers are set to the default value.

After the internal reset pulse is generated, CODEC Ch0/Ch1 starts the initialization procedure by being fed FS signal, and it takes 180ms(typ.), 350ms(max) to complete the initialization after the detectio n of power on.

Power up slope to enable the Power-on Reset

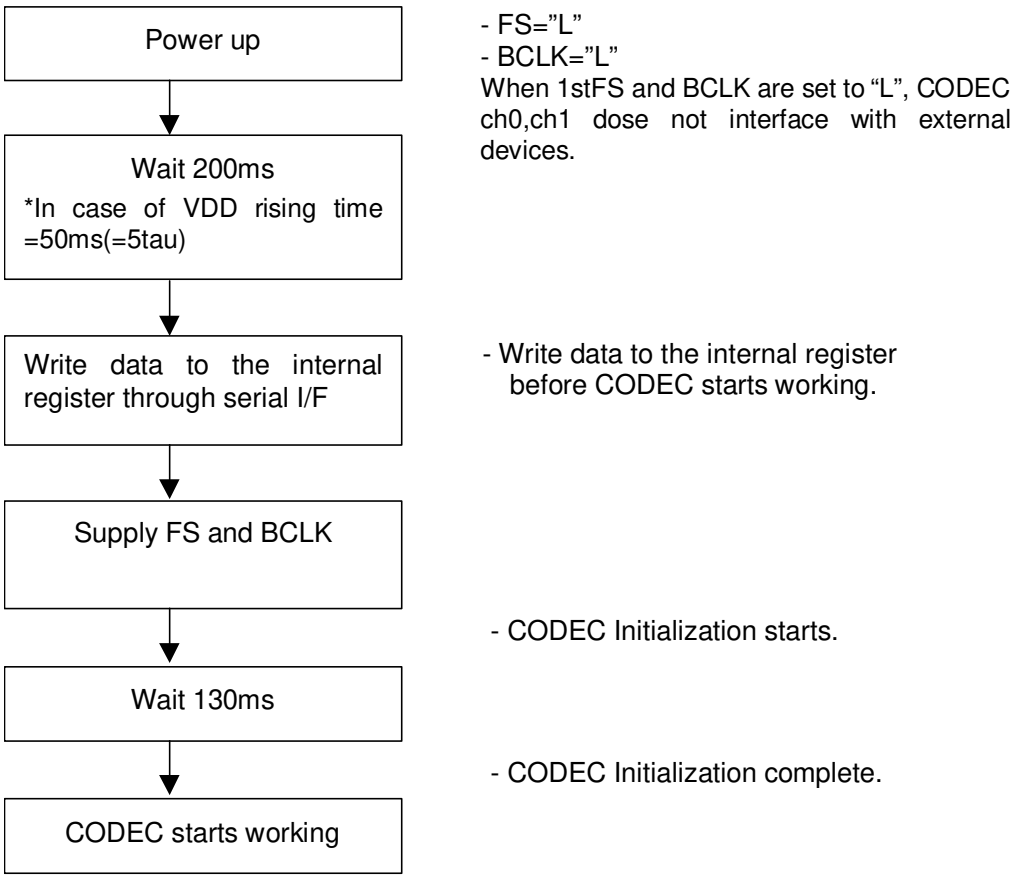
When power-up slope is no longer than 50ms(=5tau:tau is time constant), Power On Reset works normally.

When the time is longer than 50ms, Power On Reset is not activated and no internal registers are initialized. In this case all registers must be written through CPU interface.

NOTE) For stable operation after power up, we recommend to write all register value through CPU interface after power up.

Recommended start up procedure

The following start up procedure is recommended when AK2306/LV is going to power up.



POWER DOWN

Power consumption is reduced in the power down mode.
In the power down mode, the current fed to analog circuits and the clock for digital circuits, are stopped, and the relating circuits hold its status.

There are two power down modes.
- **Power down for all circuits**
- **Power down by block**

* In the power down mode, the output pins of corresponding blocks turn to Hi-Z except TNOUT pin.(See page 5)

POWER DOWN MODE SETTING
2 power down modes

Mode	Circuits	Registers	Operation for "0"/"1"	Note
All circuit	All	PD	"0" : Normal "1" : Power down	- CPU Registers are not reset. **- Serial I/F is available.** - No need to supply FS, BCLK.
Block	CODEC CH0	PDCH0	"0" : Normal "1" : Power down	- Keep supplying FS, even when CODEC CH0,1 are in power down mode (see page10,11). - When CODEC CHn(n=0,1) is in power down mode, the functions below are active: (1) AMPTn(n=0,1) Input/Output (2) TNOUT Output **Please refer next page table in deltail.**
	CODEC CH1	PDCH1		
	RING TONEGEN	PDTN		

CANCELLATION OF POWER DOWN : CODEC
When power down mode for CODEC CH0/CH1 is cleared, the CODEC circuitry starts to be initialized.
It takes 130mS(typ.).

When full circuit power down mode for CODEC is cleared, AK2306/LV starts the same wake up sequence as one at power on. It takes 250ms(Typ)

Wake up time for Tone generator is 125us(Typ).

POWER DOWN BLOCK		ALL BLOCK	CODEC CH0	CODEC CH1	CODEC CH0&1	RING TONEGEN
REGISTER		PD	PDCH0	PDCH1	PDCH0 PDCH1	PDTN
Channel 0	AMPT0	OFF				
	GA0T	OFF	OFF		OFF	
	AAF0	OFF	OFF		OFF	
	CODEC CH0	OFF	OFF		OFF	
	SMF0	OFF	OFF		OFF	
	GA0R	OFF				
	AMPR0	OFF				
Channel 1	AMPT1	OFF				
	GA1T	OFF		OFF	OFF	
	AAF1	OFF		OFF	OFF	
	CODEC CH1	OFF		OFF	OFF	
	SMF1	OFF		OFF	OFF	
	GA1R	OFF				
	AMPR1	OFF				
PCM I/F		OFF			OFF	
RING TONEGEN		OFF				OFF
PLL		OFF				
BGREF		OFF				
SERIAL I/F						

SERIAL INTERFACE

The internal registers can be read/written with SCLK, DATA, and CSN pins.

1word consists of 16bits. The first 4bits are the instruction code which specifies read/write.
The following 3bits specify the address. The rest of 8bits are for setting registers.

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
I3	I2	I1	I0	A2	A1	A0	*	D7	D6	D5	D4	D3	D2	D1	D0
Instruction code (4bit)				Address (3bit)			*	Data for internal registers (8bit)							

*)Dummy bit for adjusting the I/O timing when reading register.

INSTRUCTION CODEC

I3	I2	I1	I0	Read/Write
1	1	1	0	Read
1	1	1	1	Write
Other codes				No action

SCLK and WRITE/READ

(1) Input data are loaded into the internal shift register at the rising edge of SCLK.
(2) The rising edge of SCLK is counted after the falling edge of CSN.
(3) When CSN is "L" and more than 16 SCLK pulses:
[WRITE] Data are loaded into the internal register at the rising edge of the SCLK 16th pulse.
[READ] DATA pin is switched to an input pin at the falling edge of the SCLK 16th pulse.

CSN and WRITE / READ CANCELLATION

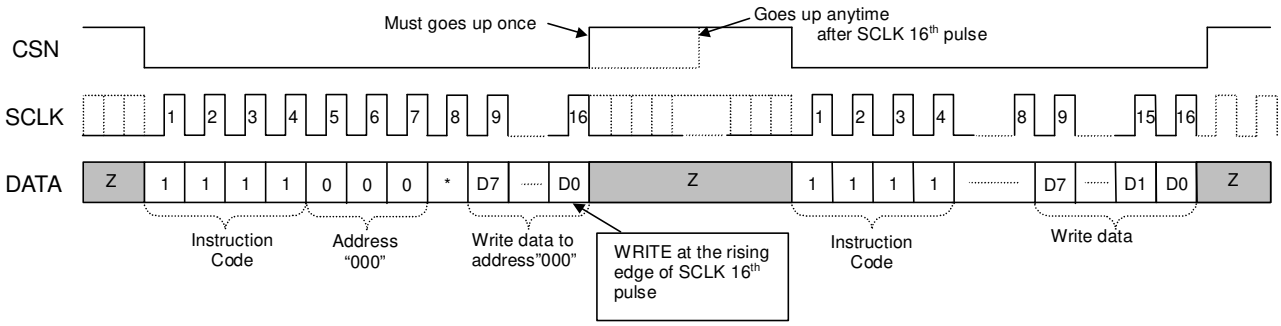
(1) WRITE is cancelled when CSN goes up before the rising edge of the SCLK 16th pulse.
(2) READ is cancelled when CSN goes up before the falling edge of the SCLK 16th pulse.

SERIAL WRITE / READ (SERIAL ACCESS)

(1) CSN must go up to "H" before the next access in successive access.
(2) When the next access is going to be done , if CSN remains to be "L", successive access can not be done.

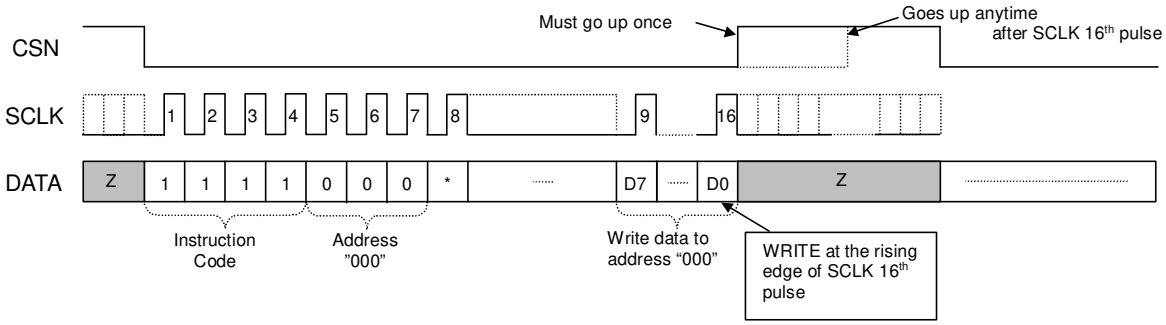
WRITE

Continuous SCLK

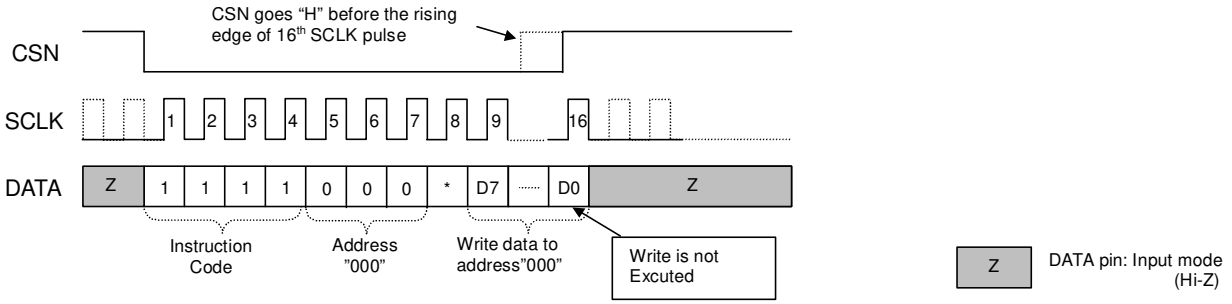


Burst SCLK

SCLK can be stop at "H" level or "L" level at anytime during the write cycle. After resuming the SCLK, write cycle is retrieved
normally.

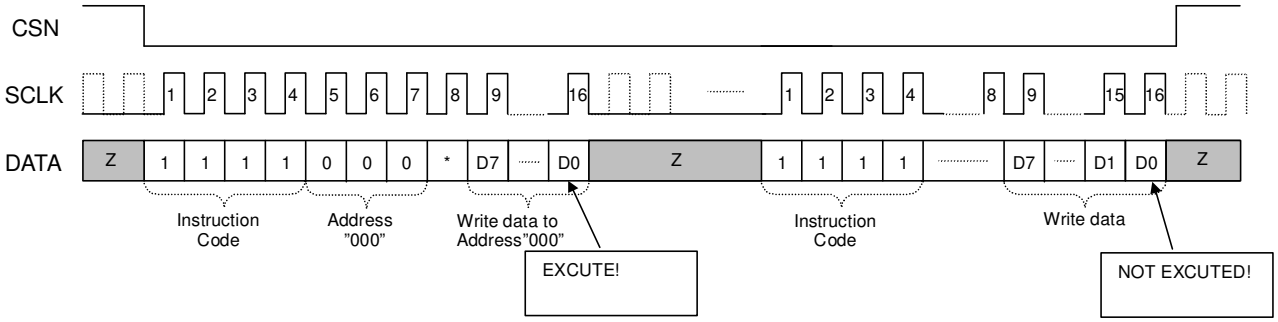


CANCELLATION



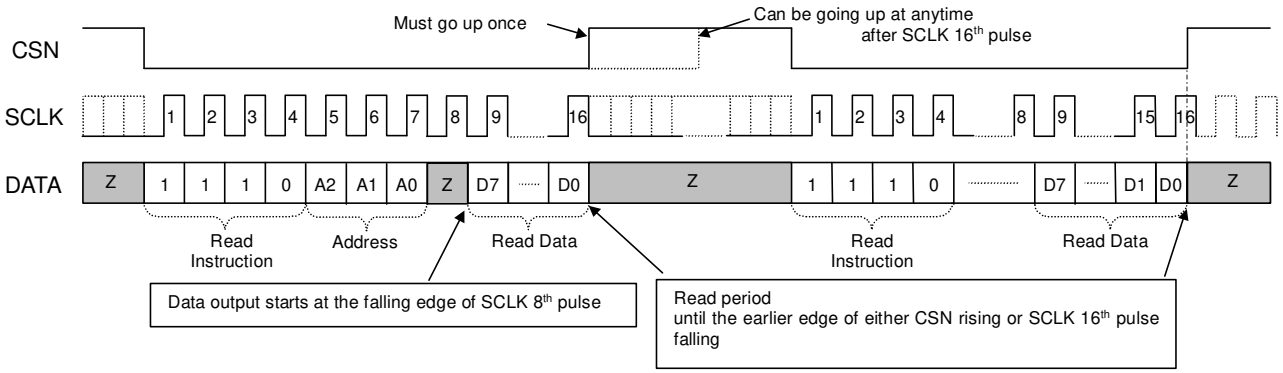
SERIAL ACCESS

Serial access with CSN staying "L" during the serise of write cycle.

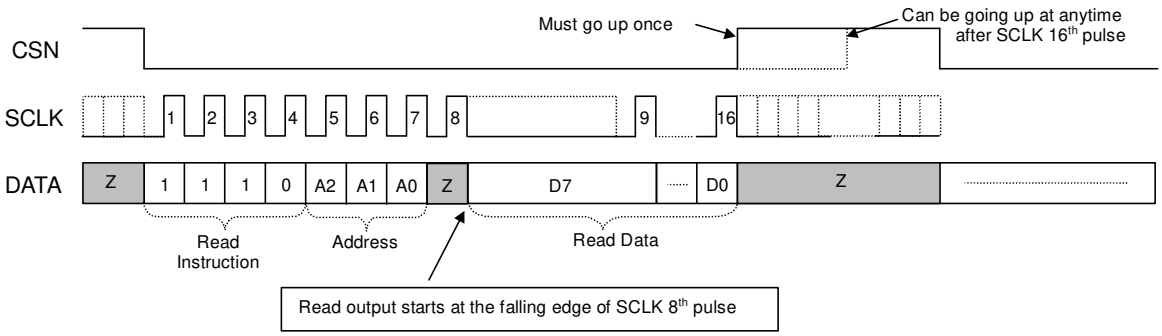


READ

CONTINOUS SCLK

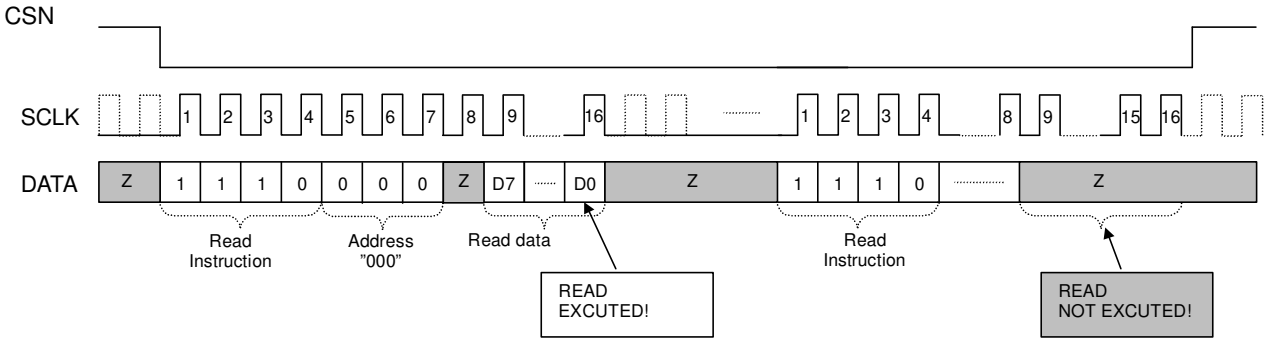


Burst SCLK

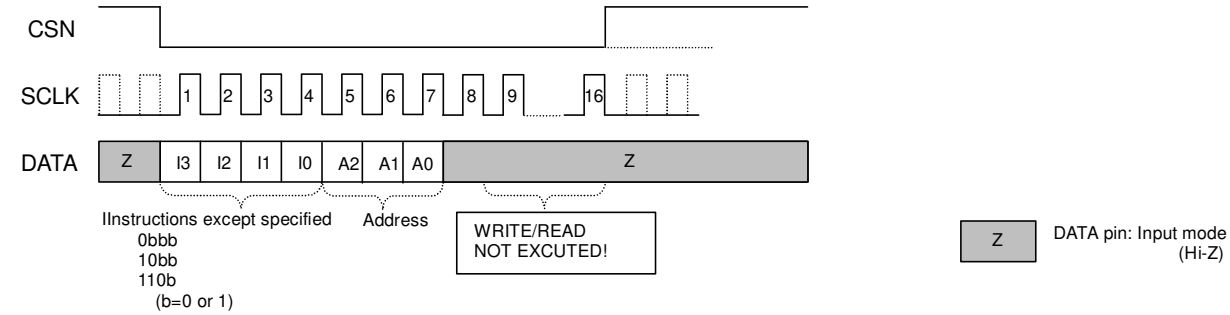


SERIAL ACCESS

Serial access with CSN staying "L" during the serise of read cycle.



DISCORD OF INSTRUCTION CODE



REGISTER MAP

Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A2	A1	A0	*	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	*	0	0	-	GA0R4	GA0R3	GA0R2	GA0R1	GA0R0
0	0	1	*	0	0	-	GA1R4	GA1R3	GA1R2	GA1R1	GA1R0
0	1	0	*	0	0	-	GA0T4	GA0T3	GA0T2	GA0T1	GA0T0
0	1	1	*	0	0	-	GA1T4	GA1T3	GA1T2	GA1T1	GA1T0
1	0	0	*	0	0	MTCH1	MTCH0	PD	PDTN	PDCH1	PDCH0
1	0	1	*	0	0	0	0	TNFQ	ALAWN	SEL2B	PCMIF
1	1	0	*	Reserved							
1	1	1	*	Reserved							

*)Dummy Bit

Note) All registers except address(000 - 011), Bit5(D5) can be read/write.

Note) Please write “all 0’s” for address(000 - 100), Bit7,6(D7,D6) and address(101), Bit7,6,5,4(D7 - D4) for normal operation.

Note) Address(000 - 011),Bit5(D5) can not be write and “0” data will be output when it is accessed to read.

INITIALIZATION OF REGISTERS

The registers are initialized at POWER ON RESET only.
Power on reset may not be excuted due to the difference of power up time constant. Thus it is highly recommended that all the register (address(000 – 101)) are to be written at the time of the power up and after the abnormal circumstances happens such as micro interrupt of the power line or mal operation due to lightning.

REGISTER FUNCTION

Address	Bit	Name	Default	Function	Refer
000	0	GA0R0	0	**Receive gain adjustment on ch0**	
	1	GA0R1	1	+6 to –18dB by 1.0dB step	
	2	GA0R2	1		
	3	GA0R3	0	00000: +6dB 11xxx: -18dB	
	4	GA0R4	0		
	5	-			
	6	0	0	Test mode	
	7	0	0	Please write all “0”.	
001	0	GA1R0	0	**Receive gain adjustment on ch1**	
	1	GA1R1	1	+6 to –18dB by 1.0dB step	
	2	GA1R2	1		
	3	GA1R3	0	00000: +6dB 11xxx: -18dB	
	4	GA1R4	0		
	5	-			
	6	0	0	Test mode	
	7	0	0	Please write all “0”.	

Address	Bit	Name	Default	Function	Refer
010	0	GA0T0	0	**Transmit gain adjustment on ch0** +6 to –18dB by 1.0dB step 00000: +6dB 11xxx: -18dB	
	1	GA0T1	1		
	2	GA0T2	1		
	3	GA0T3	0		
	4	GA0T4	0		
	5	-			
	6	0	0	Test mode Please write all “0”.	
	7	0	0		
011	0	GA1T0	0	**Transmit gain adjustment on ch1** +6 to –18dB by 1.0dB step 00000: +6dB 11xxx: -18dB	
	1	GA1T1	1		
	2	GA1T2	1		
	3	GA1T3	0		
	4	GA1T4	0		
	5	-			
	6	0	0	Test mode Please write all “0”.	
	7	0	0		
100	0	PDCH0	0	**CODEC CH0,1 Power down control** 0: Power ON 1: Power OFF	
	1	PDCH1	0		
	2	PDTN	1	**RING TONEGEN Power down control** 0: Power ON 1: Power OFF	
	3	PD	0	**Full Power down** 0: Power ON 1: Power OFF	
	4	MTDX0	0	**Mute control: VR0.VR1,DX pin** 0: Normal output 1: Mute	
	5	MTDX1	0		
	6	0	0	Test mode Please write all “0”.	
	7	0	0		
101	0	PCMIF	0	**PCM Interface select** 0: LF/SF 1: GCI	
	1	SEL2B	0	**PCM data channel select** 0: CH0 -> B1 1: CH1 -> B1	
	2	ALAWN	1	**A/u-law select** 0: A-law 1: u-law	
	3	TNFQ	0	**Tone frequency select** 0: 16Hz 1: 20Hz	
	4	0	0	Test mode Please write all “0”.	
	5	0	0		
	6	0	0		
	7	0	0		
110	0		0	Reserved	
	1		0		
	2		0		
	3		0		
	4		0		
	5		0		
	6		0		
	7		0		

Address	Bit	Name	Default	Function	Refer
111	0		0	Reserved	
	1		0		
	2		0		
	3		0		
	4		0		
	5		0		
	6		0		
	7		0		

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Power Supply Voltages Analog/Digital Power Supply	VDD	-0.3	6.5	V
VSS Voltage	VSS	-0.1	0.1	V
Digital Input Voltage	VTD	-0.3	VDD+0.3	V
Analog Input Voltage	VTA	-0.3	VDD+0.3	V
Input current (except power supply pins)	IIN	-10	10	mA
Storage Temperature	Tstg	-55	125	°C

Warning: Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies Analog/Digital power supply(AK2306)	VDD	4.75	5.0	5.25	V
Power Supplies Analog/Digital power supply(AK2306 LV)	VDD	3.0	3.3	3.6	V
Ambient Operating Temperature	Ta	-40		85	°C
Frame Sync Frequency	FS		8		kHz

Note) All voltages reference to ground : VSS=0V

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, guaranteed for VDD=+5V +/– 5%(AK2306), VDD=+3.3V+/-0.3V(AK2306LV),
Ta = –40 ~ +85 °C, FS=8kHz.

DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Consumption BCLK=2048kHz	PDD1	PDCH0,1 PDDT0,1=0,0 All output unloaded		65		mW
	PDD2	PDCH0,1 PDDT0,1=1,0 All output unloaded		35		
Output High Voltage (CMOS level)	VOH	IOH=-1.6mA	0.8VDD			V
Output Low Voltage (CMOS level)	VOL	IOL=1.6mA			0.4	V
Input High Voltage1 (CMOS level)	VIH1		0.7VDD			V
Input High Voltage2 (TTL level)	VIH2		2.4			V
Input Low Voltage1 (CMOS level)	VIL1				0.3VDD	V
Input Low Voltage2 (TTL level)	VIL2				0.8	V
Input Leakage Current	Ii		-10		+10	uA
Input Capacitance	Ci				5	pF
Output Leakage Current	Io	Tri-state mode	-10		+10	uA
Power Consump.@PD	PDDd		-	2.5	-	mW