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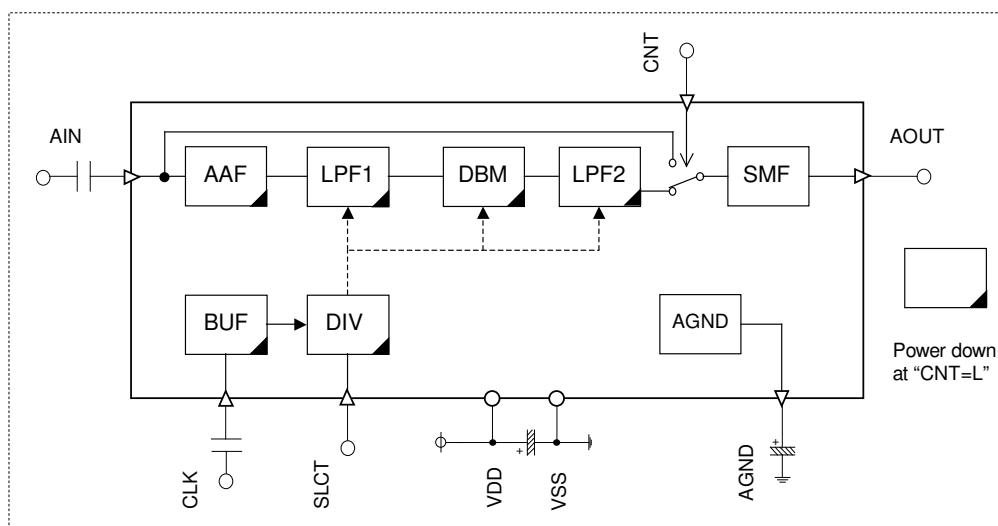
# AK2360A

## Scrambler IC for two-way radio

### Features

- Frequency inversion type scrambler for a voice encryption two-way radio
- High quality decoded voice:  $S/N=47\text{dB(Typ)}$ ,  $S/(N+D)=50\text{dB(Typ)}$
- Allowing selection of an inverted frequency (3.397kHz or 3.039kHz) and voice passage band
- Scrambler bypass function included
- Based on 5.3125MHz (1/4 for 21.25MHz) external clock supply
- Operating voltage: 2.6V to 3.3V
- Operating temperature:  $-30^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Package: 8-pin SON

### Block Diagram



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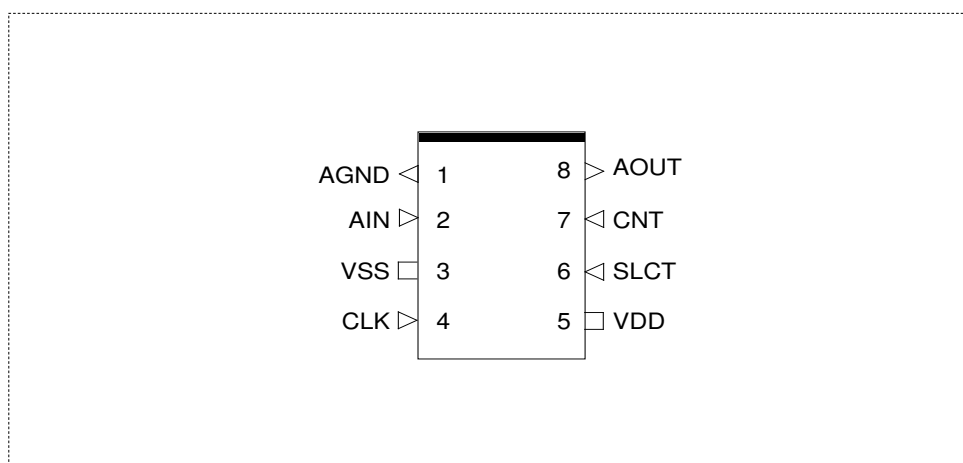
## General Description

The AK2360A is a radio scrambler IC device suitable for half-duplex communication. As the scrambler method, a simple frequency inversion method is used in which audio signal components are inverted about the carrier frequency by using the double balanced mixer (DBM).

The inverted frequency and voice passage band can be changed according to the input to the SLCT pin. The scrambler can be bypassed by using the CNT pin, and part of the circuit blocks is placed in the power-down state accordingly.

A signal-to-noise ratio of 40dB or more and a distortion of 43dB or more can be obtained by inserting filters before and after DBM as shown in the block diagram, therefore allowing less sound quality deterioration when the scrambler is used.

### □ Pin assignments (Top view)



## Circuit Configuration

Block	Function
AAF	Active low-pass filter to prevent aliasing noise generated in the following switched capacitor filter (SCF) block
LPF1	Low-pass filter for limiting the band of the audio signal input from the AIN pin
DBM	Double balanced modulator for performing frequency inversion. The carrier frequency can be changed according to the input level on the SLCT pin.
LPF2	Low-pass filter for removing upper wave components generated by mixing by DBM
SMF	Smoothing filter for removing harmonics components generated in LPF2 and clock components
BUF	Buffer circuit for adjusting the level of the clock signal input from the CLK pin
DIV	Divides the clock signal and generates a clock signal for the SCF circuit and the carrier frequency for DBM.
AGND	A block for generating the reference voltage (1/2VDD) of the internal analog circuit

<b>Pin Functions</b>
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Pin No.	Pin name	Pin type	Function									
1	AGND	AO	Analog ground output pin A capacitor is connected to this pin to stabilize the analog ground level.									
2	AIN	AI	Audio signal input pin									
3	VSS	PWR	Negative power supply pin Apply 0V.									
4	CLK	AI	Clock signal input pin See "Recommended External Application Circuits".									
5	VDD	PWR	Positive power supply pin Connect this pin to a power supply ranging from 2.6V to 3.3V with less noise. Connect a bypass capacitor of 0.1μF or higher between this pin and the VSS pin.									
6	SLCT	DI	Carrier frequency switching pin This pin changes the carrier frequency and voice passage band for the scrambler.  <table style="margin-left: auto; margin-right: auto; border: none;"> <tr> <td style="padding: 0 10px;">Input level</td> <td style="padding: 0 10px;">Carrier frequency</td> <td style="padding: 0 10px;">Voice passage band</td> </tr> <tr> <td style="padding: 0 10px;">High</td> <td style="padding: 0 10px;">3.376kHz</td> <td style="padding: 0 10px;">290Hz to 3090Hz</td> </tr> <tr> <td style="padding: 0 10px;">Low</td> <td style="padding: 0 10px;">3.020kHz</td> <td style="padding: 0 10px;">260Hz to 2760Hz</td> </tr> </table> <div style="text-align: right; margin-top: 5px;">*1)</div>	Input level	Carrier frequency	Voice passage band	High	3.376kHz	290Hz to 3090Hz	Low	3.020kHz	260Hz to 2760Hz
Input level	Carrier frequency	Voice passage band										
High	3.376kHz	290Hz to 3090Hz										
Low	3.020kHz	260Hz to 2760Hz										
7	CNT	DI	Scrambler bypass pin This pin causes the AAF block through LPF2 block to be bypassed. When bypassed, these blocks are placed in the power-down state.  <table style="margin-left: auto; margin-right: auto; border: none;"> <tr> <td style="padding: 0 10px;">Input level</td> <td style="padding: 0 10px;">Setting</td> </tr> <tr> <td style="padding: 0 10px;">High</td> <td style="padding: 0 10px;">Scrambler enables.</td> </tr> <tr> <td style="padding: 0 10px;">Low</td> <td style="padding: 0 10px;">Scrambler bypasses.</td> </tr> </table> <div style="text-align: right; margin-top: 5px;">*1)</div>	Input level	Setting	High	Scrambler enables.	Low	Scrambler bypasses.			
Input level	Setting											
High	Scrambler enables.											
Low	Scrambler bypasses.											
8	AOUT	AO	Audio signal output pin <span style="float: right;">*2)</span>									

Note) **A**: Analog, **D**: Digital, **PWR**: Power, **I**: Input, **O**: Output

\*1) A pull-up resistor of 50kΩ or more is included.

\*2) Load impedance > 10kΩ, load capacitance < 50pF

### Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	VDD	-0.3	4.6	V
Ground level	VSS	0	0	V
Input voltage	V <sub>IN</sub>	-0.3	VDD+0.3	V
Input current (excluding power supply pin)	I <sub>IN</sub>	-10	+10	mA
Storage temperature	T <sub>stg</sub>	-55	130	°C

Note) All voltages are relative to the VSS pin.

Caution) If the device is used in conditions exceeding these values, the device may be destroyed.  
Normal operations are not guaranteed in such extreme conditions.

### Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature	T <sub>a</sub>		-30		85	°C
Operating power supply voltage	VDD		2.6	3.0	3.3	V
Analog reference voltage	AGND			1/2VDD		V

Note) All voltages are relative to the VSS pin.

### Digital DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V <sub>IH</sub>	SLCT, CNT	0.8VDD			V
Low level input voltage	V <sub>IL</sub>	SLCT, CNT			0.2VDD	V
High level input current	I <sub>IH</sub>	V <sub>IH</sub> =VDD SLCT, CNT			10	μA
Low level input current	I <sub>IL</sub>	V <sub>IL</sub> =0V SLCT, CNT	-66			μA
Pull-up resistance	R <sub>UP</sub>	SLCT, CNT	50			kΩ

### Clock Input Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Clock cycle	T <sub>WP</sub>	CLK		188		ns	f=5.3125MHz
Input amplitude	V <sub>CLK</sub>	CLK	0.2		VDD-0.1	V <sub>PP</sub>	Clipped sine wave

<b>Current Consumption</b>
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Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	IDD0	When scrambler is bypassed (CNT=V <sub>IL</sub> ) with CLK=5.3125MHz, V <sub>CLK</sub> =0.2V <sub>pp</sub>		0.7	1.1	mA
	IDD1	When scrambler is operating (CNT=V <sub>IH</sub> ) with CLK=5.3125MHz, V <sub>CLK</sub> =0.2V <sub>pp</sub>		1.65	2.6	

<b>Analog Characteristics</b>
-------------------------------

Unless otherwise specified, the following apply: CLK = 5.3125MHz, SLCT = V<sub>IH</sub>, CNT = V<sub>IH</sub>, f = 1kHz@AIN, dBm = 0dBm (= 0.775Vrms) at 1mW with a 600Ω load.

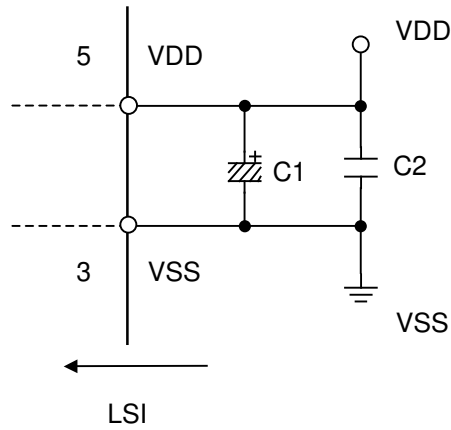
Parameter	Condition	Min.	Typ.	Max.	Unit	Remarks
Standard input level	@AIN		-11.5		dBm	
Output level	AIN to AOUT AIN=-11.5dBm When CNT=V <sub>IH</sub> : (3.397-1.0)kHz When CNT=V <sub>IL</sub> : 1.0kHz	-12.5	-11.5	-10.5	dBm	
S/N ratio	AIN to AOUT AIN=-11.5dBm When CNT=V <sub>IH</sub> and CNT=V <sub>IL</sub> : 30kHz low-pass filtering	40	47		dB	
S/(N+D)	AIN to AOUT AIN=-2.7dBm When CNT=V <sub>IH</sub> and CNT=V <sub>IL</sub> : 30kHz low-pass filtering	43	50		dB	
High frequency rejection level	AIN to AOUT AIN=-11.5dBm Measurement frequency:(3.397+1.0)kHz		-65	-51.5	dBm	
Carrier signal leakage level	AIN to AOUT AIN=No input Measurement frequency: 3.397kHz		-75	-51.5	dBm	
Original signal leakage level	AIN to AOUT AIN=-11.5dBm Measurement frequency: 1.0kHz		-85	-51.5	dBm	

Note) Under connecting 10kΩ and 50pF load to AGND(=1/2VDD) equivalent offset level AOUT pin.

Recommended External Application Circuits

1) Power supply stabilizing capacitance

Connect capacitors between the VDD and VSS pins to eliminate ripple and noise included in power supply. For maximum effect, the capacitors should be placed at a shortest distance between the pins.

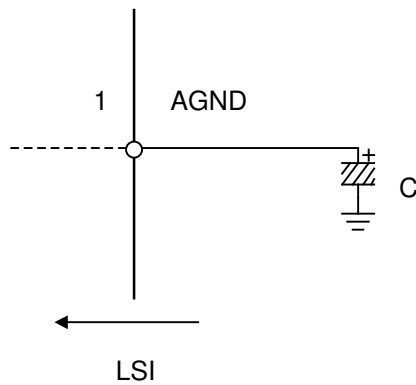


C1 = 22 $\mu$ F (Electrolytic cap)

C2 = 0.1 $\mu$ F (Ceramic cap)

2) AGND stabilizing capacitance

It is recommended that a capacitor with 1.0 $\mu$ F or larger be connected between the AGND pin and VSS to stabilize the AGND signal. The capacitor should be placed as close to the AGND pin as possible.

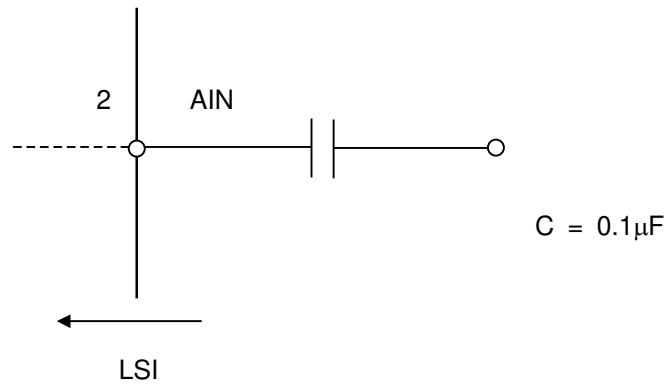


C = 1.0 $\mu$ F (Electrolytic cap)



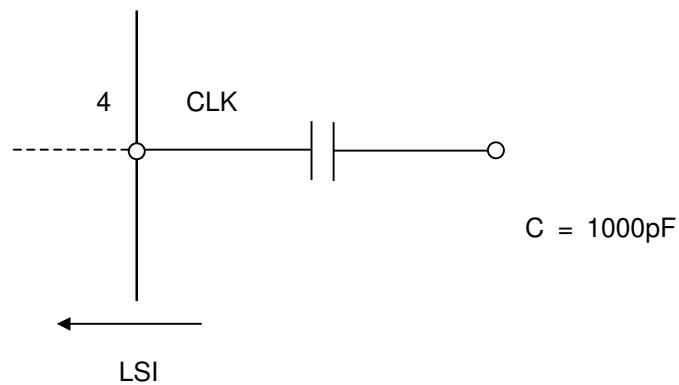
## 3) External AIN capacitance

Connect a capacitor to the AIN pin to adjust the input signal DC offset and the internal operation point of the LSI device. This configures a high-pass filter with  $f_c$  being about 3Hz.



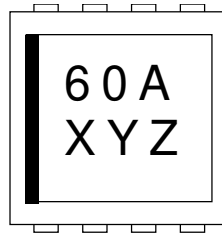
## 4) External CLK capacitance

Connect a capacitor to the CLK pin to adjust the DC offset of the clipped sine signal and the internal operation point of the LSI device.



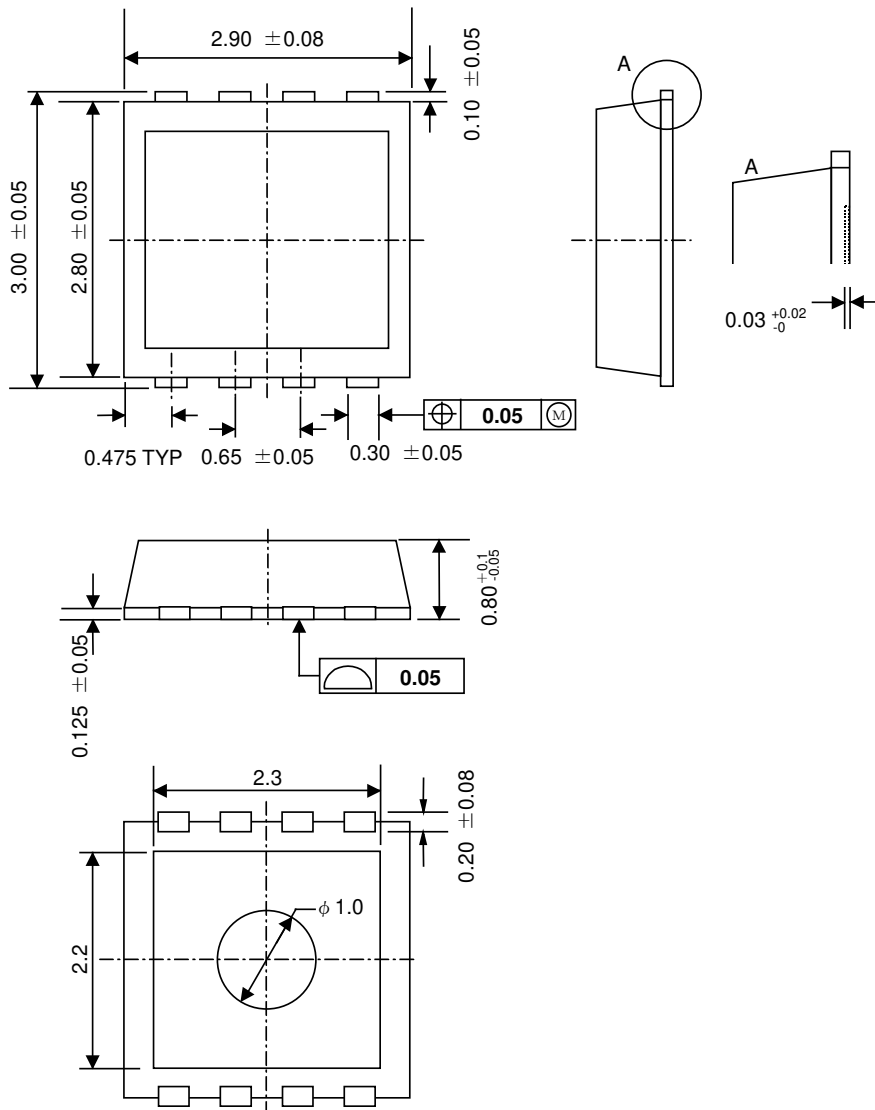
Package

Marking



X: Date of manufacturing    Lowest 1 digit of the year  
 Y: Date of manufacturing    Month  
 Z: Production lot number

Outline dimensions



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