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AK4115

High Feature 192kHz 24bit Digital Audio Interface Transceiver

GENERAL DESCRIPTION

The AK4115 is a 24-bit stereo digital audio transceiver that supports sampling rates up to 216kHz. The channel status bit decoder supports both consumer and professional modes and can automatically detect Non-PCM bit streams such as Dolby Digital or MPEG. The AK4115 supports a wide array of features a couple of them being; differential cable driver and receiver support, and an internal PLL that can support clock sources such as bi-phase and "word clock". Control of AK4115 is achieved though a μP or pin-strapping (parallel mode) and it is packaged in a space- saving 64pin-LQFP.

* Dolby Digital is a trademark of Dolby Laboratories.

FEATURES

- ☐ **AES3, IEC60958, S/PDIF, EIAJ CP1201 Compatible**
- ☐ **Very Low Jitter Analog PLL**
- ☐ **Synchronous / Asynchronous Mode**
- ☐ **Include Two X'tal Oscillators**
- ☐ **Clock Source: PLL or External Clock**
  - **Reference Clock for PLL:**
    - **Biphase signal: 22kHz to 216kHz**
    - **External Clock (ELRCK pin): 22kHz to 216kHz**
- ☐ **8-channel Receiver input**
  - **One channel supports Differential Input**
- ☐ **2-channel Transmission output (Through output or DIT)**
  - **One channel supports Differential Output (RS422 Line Output Buffer)**
- ☐ **Auxiliary Digital Input**
- ☐ **De-emphasis for 32kHz, 44.1kHz and 48kHz**
- ☐ **Detection Functions**
  - **Non-PCM Bit Stream Detection**
  - **DTS-CD Bit Stream Detection**
  - **Sampling Frequency Detection:**
    (22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz)
  - **Unlock & Parity Error Detection**
  - **DAT Start ID Detection**
- ☐ **Up to 24bit Audio Data Format**
- ☐ **Audio Interface: Master or Slave Mode**
- ☐ **192-bit Channel Status Buffer**
- ☐ **Burst Preamble bit Pc and Pd Buffer for Non-PCM bit stream**
- ☐ **Q-subcode Buffer for CD bit stream**
- ☐ **Serial μP Interface: 4-wire or I^2C (max. 400kHz)**
- ☐ **Two Master Clock Outputs: 64fs/128fs/256fs/512fs**
- ☐ **Operating Voltage: 2.7 to 3.6V with 5V Logic Tolerance**
- ☐ **Package: 64pin LQFP**
- ☐ **Ta: -20 to 85°C**

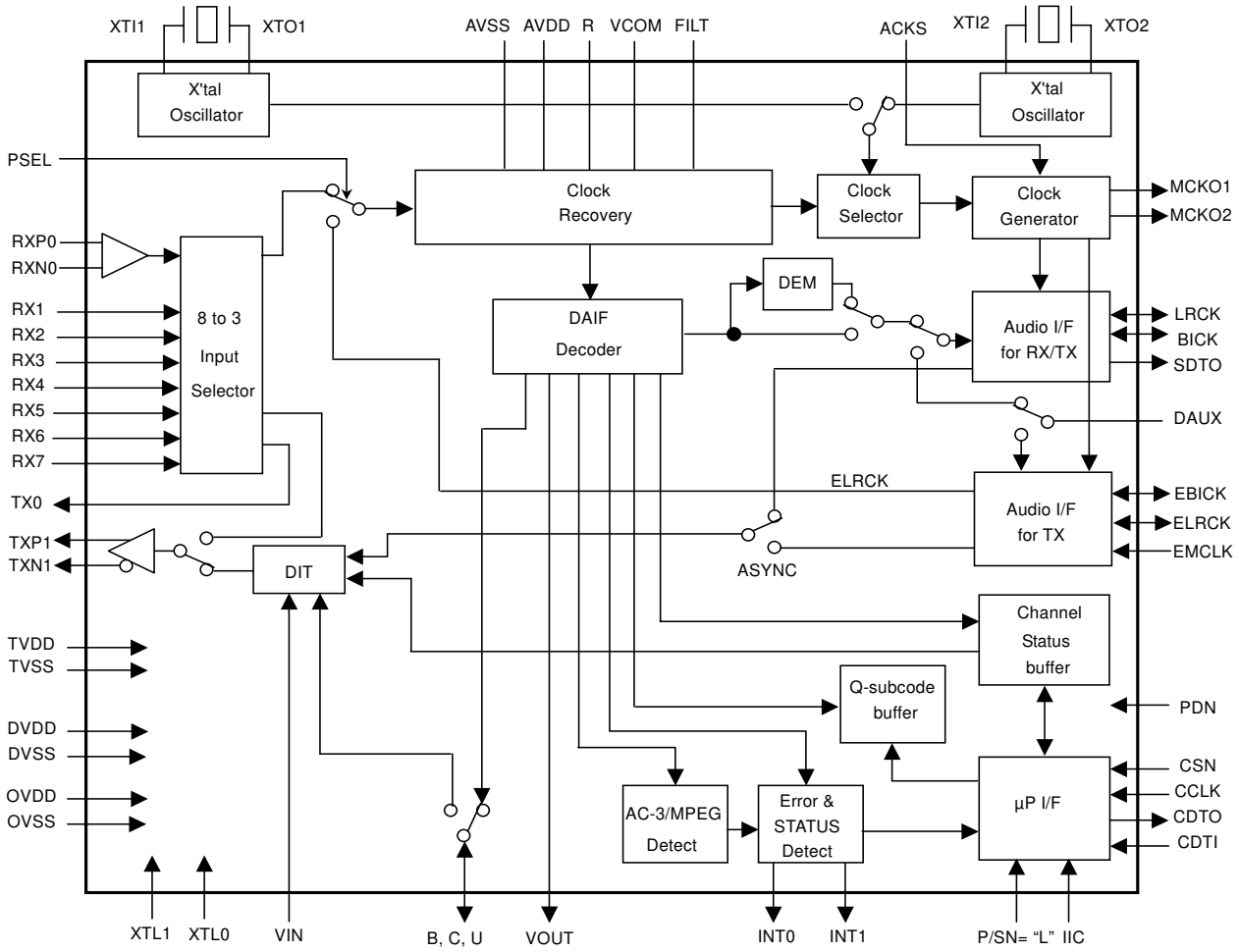


Figure 1. AK4115 Block Diagram in serial mode

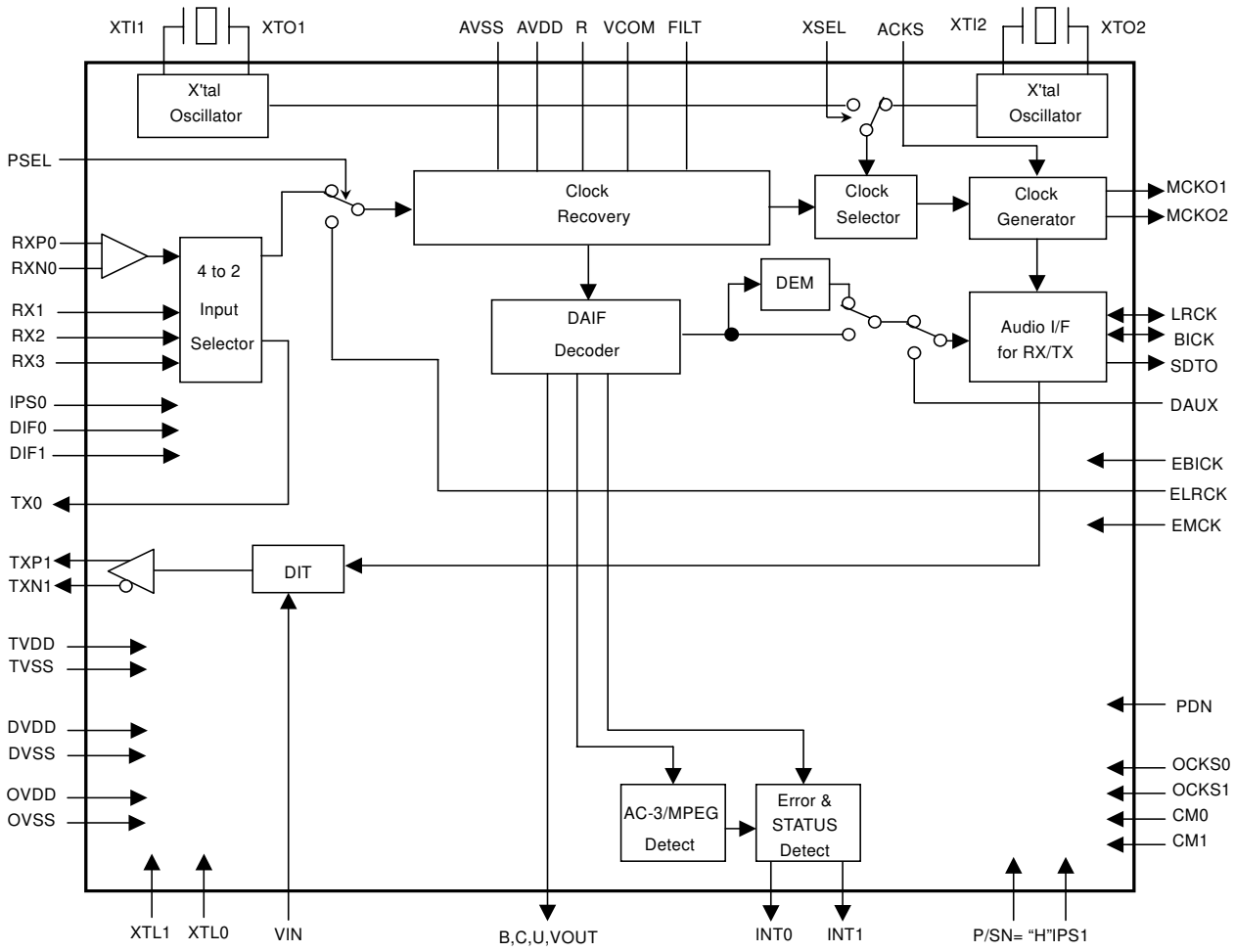
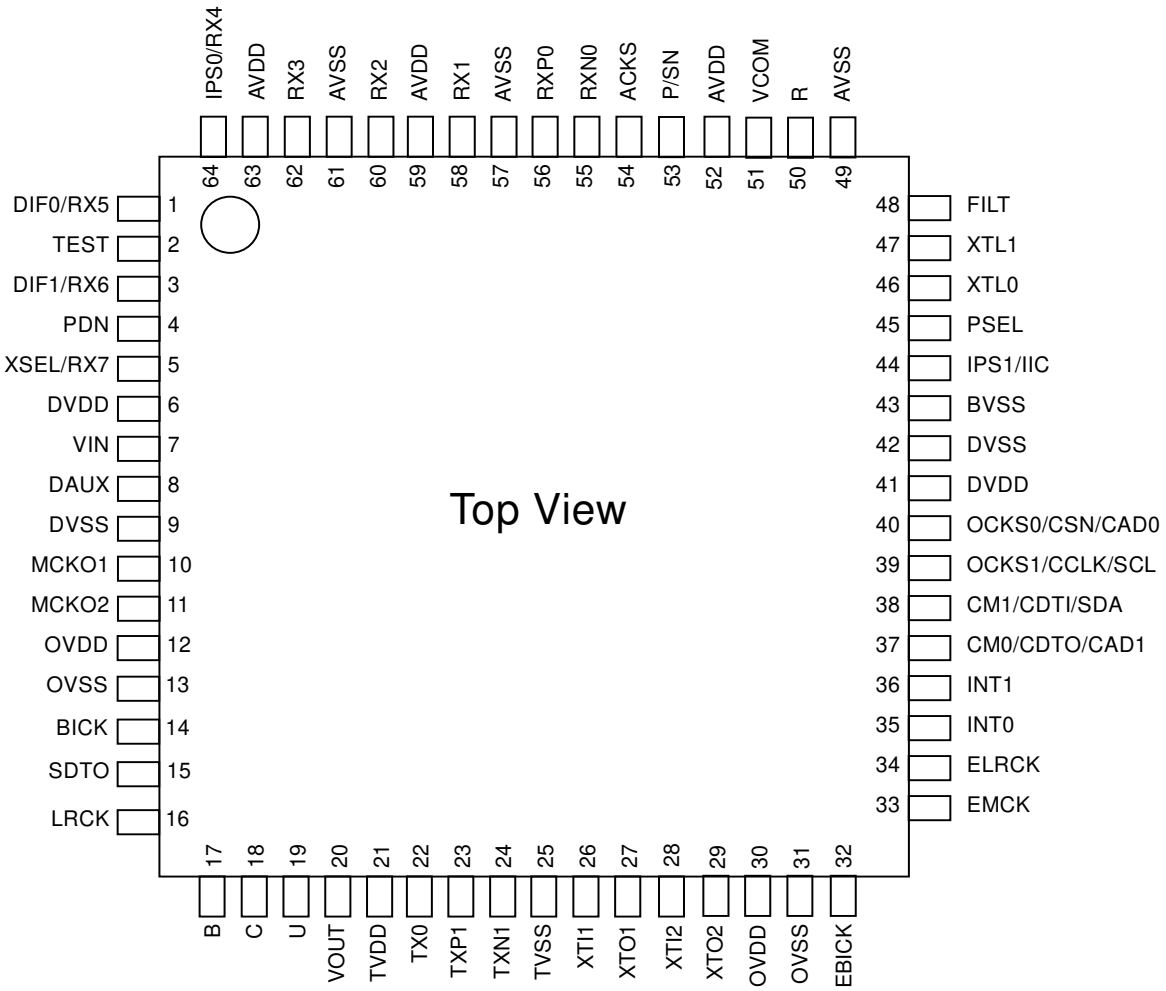


Figure 2. AK4115 Block Diagram in parallel mode

■ Ordering Guide

AK4115VQ	-20 ~ +85 °C	64pin LQFP (0.5mm pitch)
AK4115	Evaluation board for AK4115	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DIF0	I	Audio Data Interface Format #0 Pin in parallel mode
	RX5	I	Receiver Channel #5 Pin in serial mode (Internal biased pin)
2	TEST	I	TEST Pin This pin must be connected to AVSS.
3	DIF1	I	Audio Data Interface Format #1 Pin in parallel mode
	RX6	I	Receiver Channel #6 Pin in serial mode (Internal biased pin)
4	PDN	I	Power-Down Mode Pin When "L", the AK4115 is powered-down and reset.
5	XSEL	I	X'tal Oscillator Selection Pin in parallel mode "L": X'tal #1 is powered-up. "H": X'tal #2 is powered-up. XSEL pin and XSEL bit are ORed.
	RX7	I	Receiver Channel #7 Pin in serial mode (Internal biased pin)
6	DVDD	-	Digital Power Supply Pin, 3.3V
7	VIN	I	V-bit Input Pin for Transmitter Output
8	DAUX	I	Auxiliary Audio Data Input Pin
9	DVSS	-	Digital Ground Pin
10	MCKO1	O	Master Clock Output #1 Pin
11	MCKO2	O	Master Clock Output #2 Pin
12	OVDD	-	Digital Power Supply Pin, 3.3V
13	OVSS	-	Digital Ground Pin
14	BICK	I/O	Audio Serial Data Clock Pin
15	SDTO	O	Audio Serial Data Output Pin
16	LRCK	I/O	Channel Clock Pin
17	B	I/O	Block-Start Input/Output Pin
18	C	I/O	C-bit Input/Output Pin
19	U	I/O	U-bit Input/Output Pin
20	VOUT	O	V-bit Output Pin for Receiver
21	TVDD	-	Input tolerance & TX Output Buffer Power Supply Pin, 3.3V or 5V
22	TX0	O	Transmit Channel (Through Data) Output #0 Pin
23	TXP1	O	Transmit Channel Positive Output #1 Pin
24	TXN1	O	Transmit Channel Negative Output #1 Pin
25	TVSS	-	Input & TX Output Buffer Ground pin
26	XTI1	I	X'tal #1 Input Pin
27	XTO1	O	X'tal #1 Output Pin
28	XTI2	I	X'tal #2 Input Pin
29	XTO2	O	X'tal #2 Output Pin
30	OVDD	-	Digital Power Supply Pin, 3.3V
31	OVSS	-	Digital Ground Pin
32	EBICK	I/O	External Serial Data Clock Pin
33	EMCK	I	External Master Clock Input Pin
34	ELRCK	I/O	External Channel Clock Pin
35	INT0	O	Interrupt #0 Pin
36	INT1	O	Interrupt #1 Pin

Note 1. Do not allow digital input pins except internal biased pins to float.

PIN/FUNCTION (Continued)

No.	Pin Name	I/O	Function
37	CM0	I	Master Clock Operation Mode #0 Pin in parallel mode
	CDTO	O	Control Data Output Pin in serial mode, IIC pin = "L".
	CAD1	I	Chip Address #1 Pin in serial mode, IIC pin = "H".
38	CM1	I	Master Clock Operation Mode #1 Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial mode, IIC pin = "L".
	SDA	I/O	Control Data Pin in serial mode, IIC pin = "H". An external pull-up resistor is required.
39	OCKS1	I	Output Clock Select #1 Pin in parallel mode
	CCLK	I	Control Data Clock Pin in serial mode, IIC pin = "L"
	SCL	I	Control Data Clock Pin in serial mode, IIC pin = "H" An external pull-up resistor is required.
40	OCKS0	I	Output Clock Select #0 Pin in parallel mode
	CSN	I	Chip Select Pin in serial mode, IIC pin = "L".
	CAD0	I	Chip Address #0 Pin in serial mode, IIC pin = "H".
41	DVDD	-	Digital Power Supply Pin, 3.3V
42	DVSS	-	Digital Ground Pin
43	BVSS	-	Substrate Ground Pin
44	IPS1	I	Input Channel Select #1 Pin in parallel mode
	IIC	I	IIC Select Pin in serial mode "L": 4-wire Serial, "H": I^2C
45	PSEL	I	PLL Source Select Pin "L": S/PDIF Input, "H": ELRCK Input Clock PSEL pin and PSEL bit are ORed in serial mode.
46	XTL0	I	X'tal Frequency Select #0 Pin
47	XTL1	I	X'tal Frequency Select #1 Pin
48	FILT	O	PLL Loop Filter Pin
49	AVSS	-	Analog Ground Pin
50	R	O	External Resistor Pin 10kΩ ±1% resistor should be connected to AVSS externally.
51	VCOM	O	Common Voltage Output Pin 4.7μF capacitor should be connected to AVSS externally.
52	AVDD	-	Analog Power Supply Pin, 3.3V
53	P/SN	I	Parallel/Serial Select Pin "L": Serial Mode, "H": Parallel Mode
54	ACKS	I	Master Clock Frequency Auto Setting Mode Pin. "L": Disable, "H": Enable ACKS pin and ACKS bit are ORed in serial mode.
55	RXN0	I	Receiver Channel #0 Negative Input Pin (Internal biased pin) In serial mode, this channel is selected as default channel.
56	RXP0	I	Receiver Channel #0 Positive Input Pin (Internal biased pin) In serial mode, this channel is selected as default channel.
57	AVSS	-	Analog Ground Pin
58	RX1	I	Receiver Channel #1 Pin (Internal biased pin)
59	AVDD	-	Analog Power Supply Pin, 3.3V
60	RX2	I	Receiver Channel #2 Pin (Internal biased pin)
61	AVSS	-	Analog Ground Pin
62	RX3	I	Receiver Channel #3 Pin (Internal biased pin)
63	AVDD	-	Analog Power Supply Pin, 3.3V
64	IPS0	I	Input Channel Select #0 Pin in parallel mode
	RX4	I	Receiver Channel #4 Pin in serial mode (Internal biased pin)

Note 1. Do not allow digital input pins except internal biased pins to float.

■ Handling of Unused Pin

The unused I/O pin should be processed appropriately as below.

1. Serial Mode (P/SN pin = "L")

Classification	Pin Name	Setting
Analog Input	RXP0, RXN0, RX7-1	These pins should be open.
	TEST	This pin should be connected to AVSS.
Analog Output	FILT	This pin should be open.
Digital Input	VIN, DAUX, XTI1, XTI2, EMCK	These pin should be connected to DVSS.
Digital Output	MCKO1, MCKO2, VOUT, TX0, TXP1, TXN1, XTO1, XTO2, INT0, INT1, CDTO (IIC pin = "L")	These pins should be open.
Digital Input/Output	B, U, C	These pins should be open when BCU_IC bit is "1". These pins should be DVSS when BCU_IO bit is "0".
	EBICK, ELRCK	These pins should be open in master mode. These pins should be connected to DVSS in slave mode.

2. Parallel Mode (P/SN pin = "H")

Classification	Pin Name	Setting
Analog Input	RXP0, RXN0, RX3-1	These pins should be open.
	TEST	This pin should be connected to AVSS.
Analog Output	FILT	This pin should be open.
Digital Input	VIN, DAUX, XTI1, XTI2, EMCK, EBICK, ELRCK	These pin should be connected to DVSS.
Digital Output	MCKO1, MCKO2, VOUT, TX0, TXP1, TXN1, XTO1, XTO2, INT0, INT1, B, U, C	These pins should be open.

ABSOLUTE MAXIMUM RATINGS

(AVSS=OVSS=DVSS=TVSS=BVSS=0V; Note 2)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	-0.3	4.6	V
	Digital	DVDD	-0.3	4.6	V
	Logic Output Buffer	OVDD	-0.3	4.6	V
	Input tolerance and TX Buffer	TVDD	-0.3	6.0	V
	| BVSS – AVSS | (Note 3)	ΔGND1	-	0.3	V
	| BVSS – OVSS | (Note 3)	ΔGND2	-	0.3	V
	| BVSS – DVSS | (Note 3)	ΔGND3	-	0.3	V
	| BVSS – TVSS | (Note 3)	ΔGND4	-	0.3	V
Input Current (Any pins except supplies)		IIN	-	±10	mA
Input Voltage (Note 4)		VIN	-0.3	"TVDD+0.3" or 6.0	V
Ambient Temperature (Power applied)		Ta	-20	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltages with respect to ground.

Note 3. AVSS, OVSS, DVSS, BVSS and TVSS must be connected to the same ground plane.

Note 4. All input pins. The maximum value is low value either "TVDD+0.3V" or "6.0V".
Pull-up resistor at SDA and SCL pins should be connected to (TVDD+0.3)V or less voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS=OVSS=DVSS=TVSS=BVSS=0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies: (Note 5)	Analog	AVDD	2.7	3.3	3.6	V
	Digital	DVDD	2.7	3.3	3.6	V
	Logic Output Buffer	OVDD	2.7	3.3	3.6	V
	Input tolerance and TX Buffer	TVDD	DVDD	5.0	5.5	V
	Difference	AVDD – DVDD	-0.3	0	0.3	V
		AVDD – OVDD	-0.3	0	0.3	V
		OVDD – DVDD	-0.3	0	0.3	V

Note 2. All voltages with respect to ground.

Note 5. The power up sequence among AVDD, DVDD, OVDD and TVDD is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

S/PDIF RECEIVER CHARACTERISTICS

(Ta=25°C; AVDD=OVDD=DVDD=2.7~3.6V; TVDD=2.7~5.5V)

Parameter	Symbol	min	typ	max	Units
Input Resistance	Zin	-	10	-	kΩ
Input Voltage	VTH	200	-	-	mVpp
Input Sample Frequency	fs	22	-	216	kHz
Time deviation Jitter					
RX input (PSEL = "0")		-	100	-	ps RMS
ELRCK input (PSEL = "1")		-	300	-	ps RMS
Cycle - to - Cycle Jitter					
RX input (PSEL = "0")		-	70	-	ps RMS
ELRCK input (PSEL = "1")		-	70	-	ps RMS

DC CHARACTERISTICS

(Ta=25°C; AVDD=OVDD=DVDD=2.7~3.6V; TVDD=2.7~5.5V; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
Power Supply Current					
Normal operation: PDN pin = "H" (Note 6)					
AVDD+DVDD+OVDD:		-	28	42	mA
TVDD:		-	30	45	mA
Power down: PDN pin = "L" (Note 7)					
AVDD+DVDD+OVDD+TVDD:		-	10	100	μA
High-Level Input Voltage	VIH	70%DVDD	-	TVDD	V
Low-Level Input Voltage	VIL	DVSS-0.3	-	30%DVDD	V
Input Level at AC coupling (Only ELRCK pin)	VAC	0.5	-	TVDD	Vpp
Except for TX0, TXN1 and TXP1 pins					
High-Level Output Voltage (Iout=-400μA)	VOH	OVDD-0.4	-	-	V
Low-Level Output Voltage					
(Except SDA pin: Iout=400μA)	VOL	-	-	0.4	V
(SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
TX0 Output Level					
Output Level (Note 8)	VTXO0	0.4	0.5	0.6	V
TXN1 and TXP1 pins					
Professional mode (TVDD= 4.5 ~ 5.5V)					
Output Impedance (Rp + Rn + R1) (Note 9)	RTXPN	88	110	132	Ω
Consumer Mode (TVDD = 2.7 ~ 5.5V)					
Output Level (Note 10)	VTXO1	0.4	0.5	0.6	V
Input Leakage Current	Iin	-	-	± 10	μA

Note 6. AVDD, OVDD, DVDD = 3.3V, TVDD=5.0V, C_L=20pF, fs=216kHz, X'tal=24.576MHz, Clock Operation Mode 2, OCKS1=1, OCKS0=1, TX0 output circuit: Figure 23, TX1 output circuit: Figure 25.
AVDD=10mA (typ), OVDD+DVDD=18mA (typ)

Note 7. RX inputs are open and all digital input pins are held TVDD or DVSS.

Note 8. By using Figure 23 or Figure 24.

Note 9. Rp: Output impedance of TXP1, Rn: Output impedance of TXN1, R1 = 75Ω. By using Figure 25.

Note 10. By using Figure 26

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=OVDD=DVDD=2.7~3.6V, TVDD=2.7~5.5V; C_L=20pF)

Parameter			Symbol	min	typ	max	Units
Master Clock Timing							
Crystal Resonator		Frequency	fXTAL	11.2896	-	24.576	MHz
External Clock		Frequency	fECLK	11.2896	-	27.648	MHz
		Duty	dECLK	40	50	60	%
MCKO1 Output		Frequency	fMCK1	2.816	-	27.648	MHz
		Duty	dMCK1	40	50	60	%
MCKO2 Output		Frequency	fMCK2	1.408	-	27.648	MHz
		Duty	dMCK2	40	50	60	%
PLL Clock Recover Frequency (RX7-0)			fpll	22	-	216	kHz
LRCK Frequency			fs	22	-	216	kHz
Duty Cycle (at Slave Mode)			dLCK	45	-	55	%
Duty Cycle (at Master Mode)			dLCK	-	50	-	%
Audio Interface Timing 1							
Slave Mode							
BICK Period			tBCK	72	-	-	ns
BICK Pulse Width Low			tBCKL	27	-	-	ns
Pulse Width High			tBCKH	27	-	-	ns
LRCK Edge to BICK "↑" (Note 11)			tLRB	15	-	-	ns
BICK "↑" to LRCK Edge (Note 11)			tBLR	15	-	-	ns
LRCK to SDTO (MSB) (3.0V ≤ DVDD,OVDD ≤ 3.6V)			tLRM	-	-	20	ns
BICK "↓" to SDTO (3.0V ≤ DVDD,OVDD ≤ 3.6V)			tBSD	-	-	20	ns
LRCK to SDTO (MSB) (2.7V ≤ DVDD,OVDD < 3.0V)			tLRM	-	-	25	ns
BICK "↓" to SDTO (2.7 V≤ DVDD,OVDD < 3.0V)			tBSD	-	-	25	ns
DAUX Hold Time			tDXH	15	-	-	ns
DAUX Setup Time			tDXS	15	-	-	ns
Master Mode							
BICK Frequency			fBCK	-	64fs	-	Hz
BICK Duty			dBCK	-	50	-	%
BICK "↓" to LRCK			tMBLR	-15	-	15	ns
BICK "↓" to SDTO			tBSD	-	-	15	ns
DAUX Hold Time			tDXH	15	-	-	ns
DAUX Setup Time			tDXS	15	-	-	ns
Master Clock Timing 2							
EMCK		Frequency	fECLK2	2.816	-	27.648	MHz
		Duty	dECLK2	40	50	60	%
ELRCK		PLL Lock Range	fEPLL	22	-	216	kHz
		Frequency	fs	22	-	216	kHz
		Duty	dLCK	40	50	60	%
Audio Interface Timing 2							
Slave Mode							
EBICK Period			tEBCK	72	-	-	ns
EBICK Pulse Width Low			tEBCKL	27	-	-	ns
Pulse Width High			tEBCKH	27	-	-	ns
ELRCK Edge to BICK "↑" (Note 12)			tELRB	15	-	-	ns
EBICK "↑" to ELRCK Edge (Note 12)			tEBLR	15	-	-	ns
DAUX Hold Time			tEDXH	15	-	-	ns
DAUX Setup Time			tEDXS	15	-	-	ns
Master Mode							
EBICK Frequency			fEBCK	-	64fs	-	Hz
EBICK Duty			dEBCK	-	50	-	%
EBICK "↓" to ELRCK			tEMBLR	-15	-	15	ns
DAUX Hold Time			tEDXH	15	-	-	ns
DAUX Setup Time			tEDXS	15	-	-	ns

Note 11. BICK rising edge must not occur at the same time as LRCK edge.

Note 12. EBICK rising edge must not occur at the same time as ELRCK edge.

SWITCHING CHARACTERISTICS (Continued)

(Ta=25°C; AVDD=OVDD=DVDD=2.7~3.6V, TVDD=2.7~5.5V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (4-wire serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	50	-	-	ns
CDTI Hold Time	tCDH	50	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
CDTO Delay	tDCD	-	-	45	ns
CSN "↑" to CDTO Hi-Z	tCCZ	-	-	70	ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 13)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive load on bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Reset Timing					
PDN Pulse Width	tPW	150	-	-	ns

Note 13. Data must be held for sufficient time to bridge the 300ns transition time of SCL.

Note 14. I^2C-bus is a tradmark of NXP B.V.

■ Timing Diagram

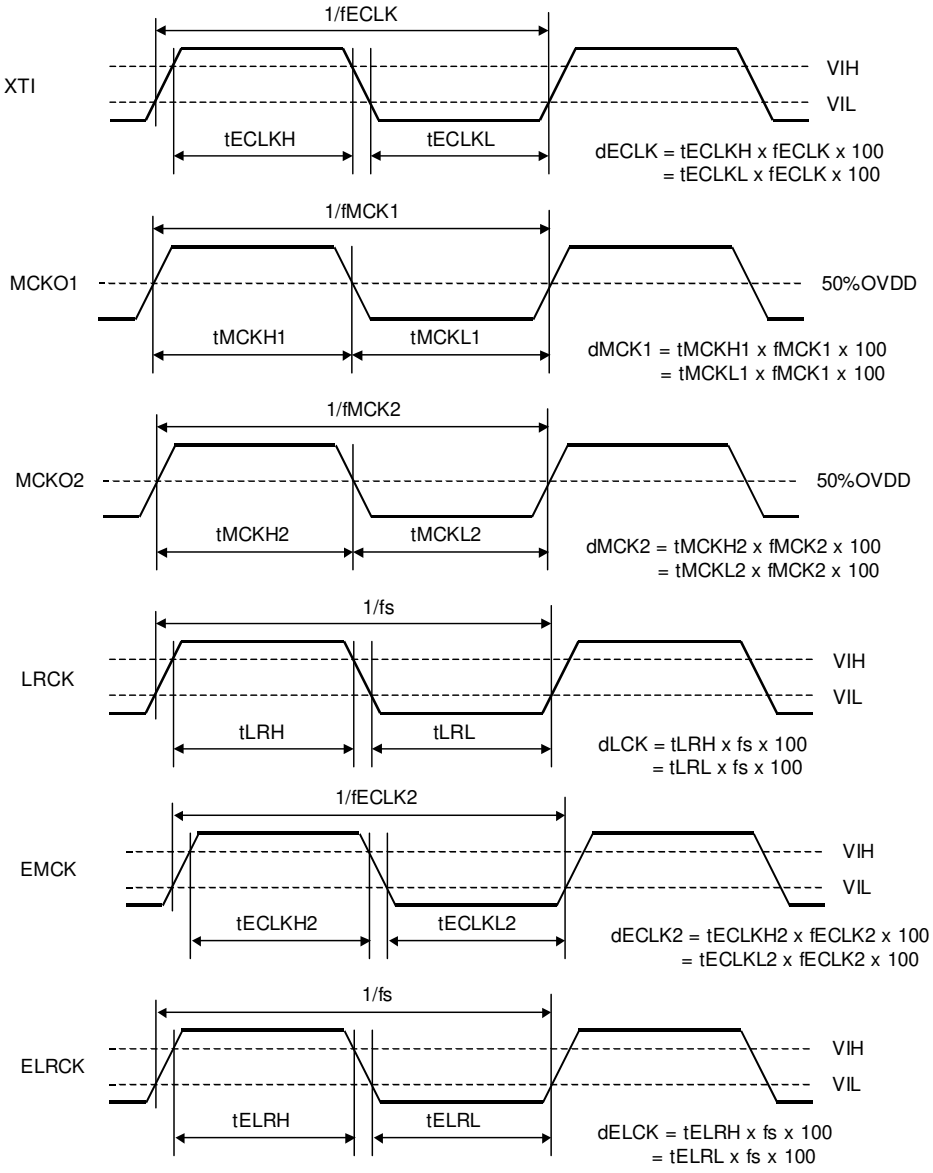


Figure 3. Clock Timing

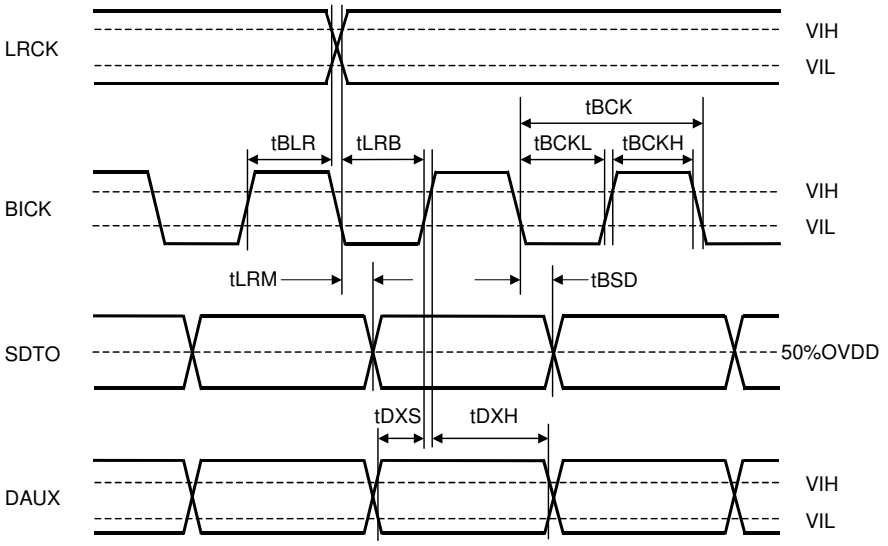


Figure 4. Serial Interface Timing 1 (Slave Mode)

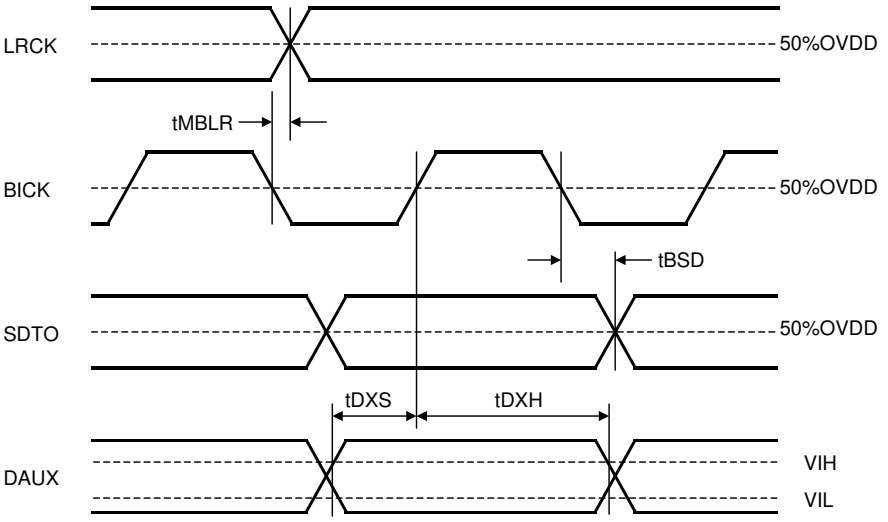


Figure 5. Serial Interface Timing 1 (Master Mode)

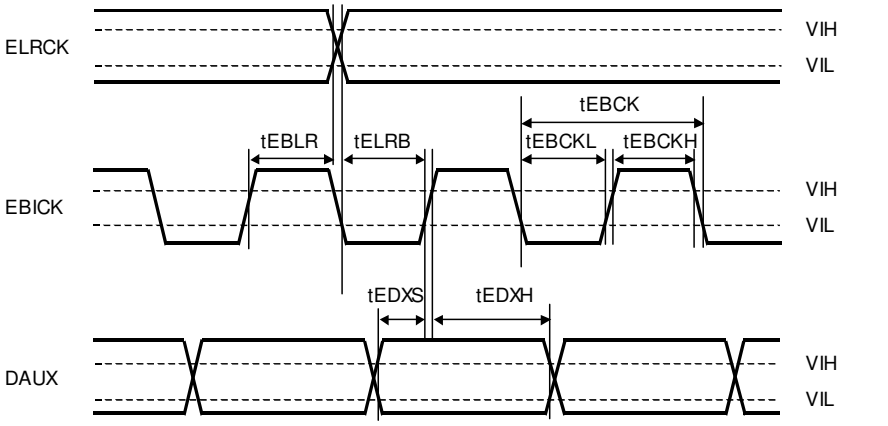


Figure 6. Serial Interface Timing 2 (Slave Mode)

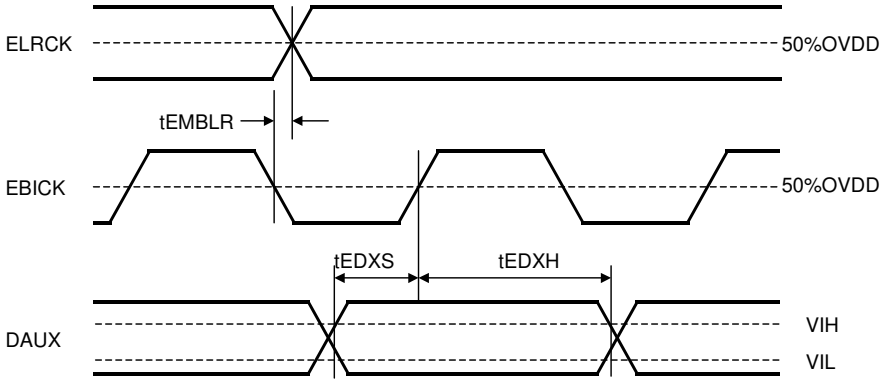


Figure 7. Serial Interface Timing 2 (Master Mode)

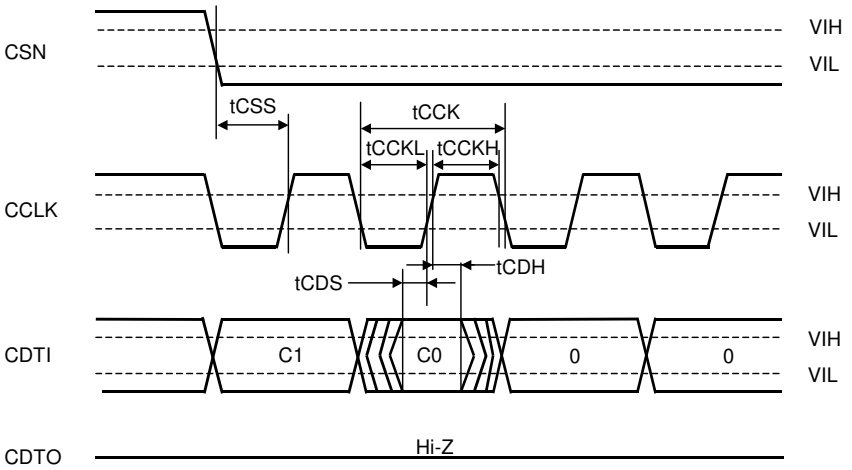


Figure 8. WRITE/READ Command Input Timing in 4-wire serial mode

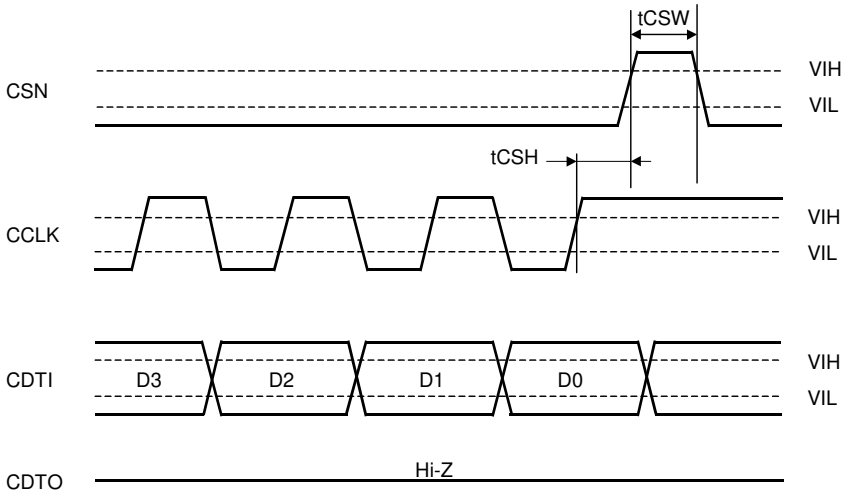


Figure 9. WRITE Data Input Timing in 4-wire serial mode

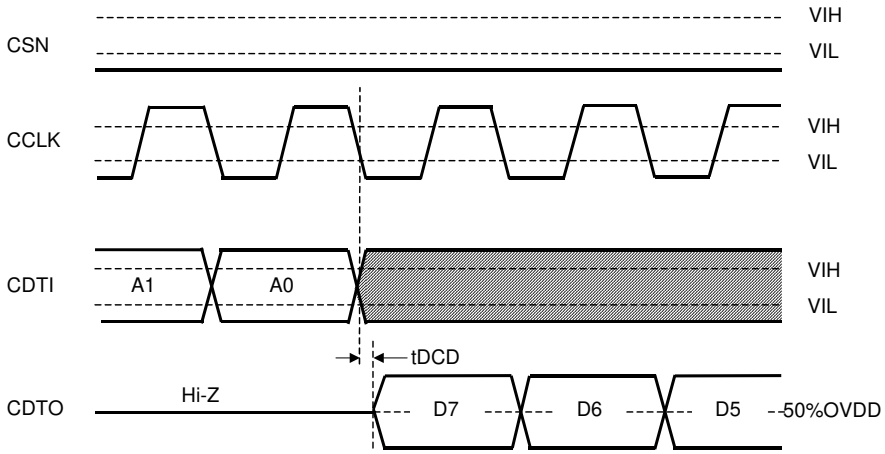


Figure 10. READ Data Output Timing 1 in 4-wire serial mode

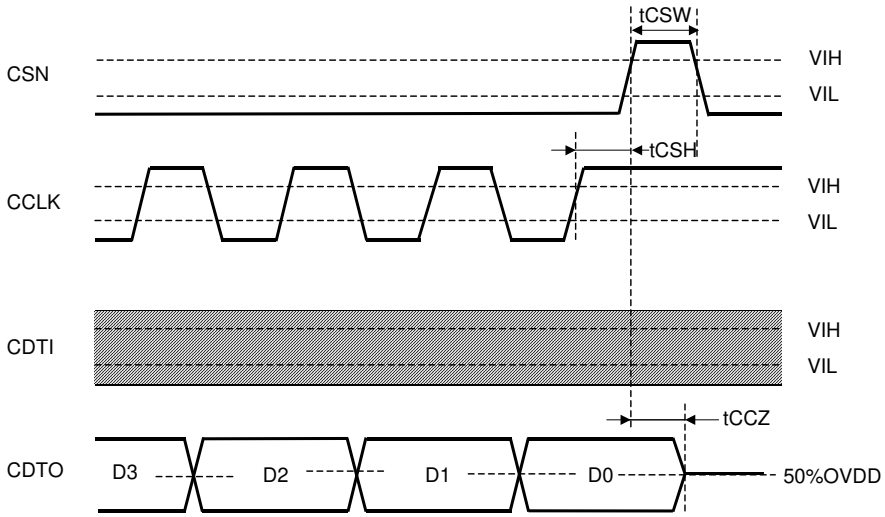


Figure 11. READ Data Input Timing 2 in 4-wire serial mode

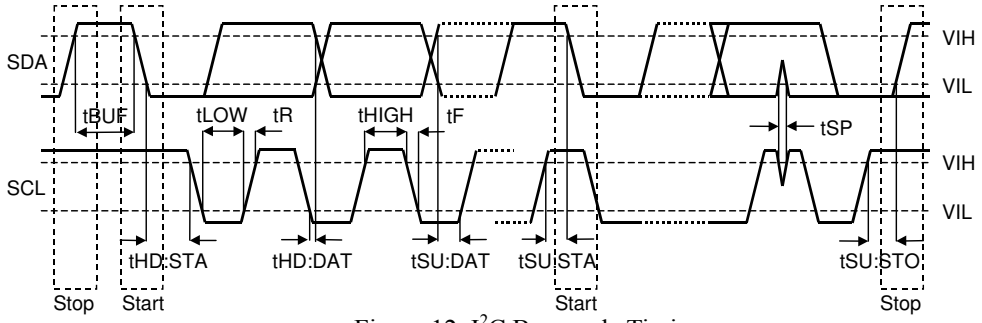


Figure 12. I^{2}C Bus mode Timing

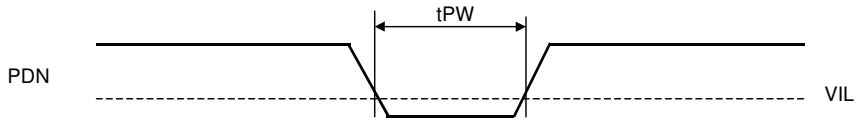


Figure 13. Power Down & Reset Timing

OPERATION OVERVIEW

■ Non-PCM (Dolby Digital, MPEG, etc) and DTS-CD Bitstream Detection

The AK4115 has a non-PCM bitstream auto-detection function, When the 32-bit mode Non-PCM preamble based on Dolby "Dolby Digital Data Stream in IEC 60958 Interface" is detected, the NPCM bit sets to "1". The 96-bit sync code consists of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872 and 0x4E1F. Detection of this pattern will set the NPCM bit to "1". Once the NPCM bit is set to "1", it will remain "1" until 4096 frames pass through the chip without an additional sync pattern being detected. When those preambles are detected, the burst preambles Pc (burst information: Figure 51) and Pd (length code: Figure 52) that follow those sync codes are stored to registers. The AK4115 has also a DTS-CD bitstream auto-detection function. When the AK4115 detects DTS-CD bitstream, the DTSCD bit sets to "1". If the next sync code does not occur within 4096frames, the DTSCD bit sets to "0" until no-PCM bitstream is detected again. The ORed value of NPCM and DTSCD bits are output to AUTO bit. The AK4115 detects the 14-bit sync word and the 16-bit sync word of a DTS-CD bitstream, the detection function can be set ON/OFF by DTS14 and DTS16 bits in serial mode. In parallel mode, the logical OR value of the AUTO and DTS-CD bits are outputted to the INT1 pin. The DTS-CD bit detects both the 14-bit sync word and the 16-bit sync word.

■ 216kHz Clock Recovery

The integrated low jitter PLL has a wide lock range from 22kHz to 216kHz. The AK4115 has a sampling frequency detection function (22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz) that uses either a clock comparison against the X'tal oscillator from the setting of XTL1-0, or the channel status information. The PLL loses lock when the received sync interval is incorrect.

■ Reference Clock for PLL

The reference clock for the PLL can select the bi-phase signal or the clock supplied from the ELRCK pin. The bi-phase signals are supplied to RX7-0 pins and the ELRCK pin is supplied to a sampled clock (1fs) from the word clock (typically used by studio equipment). This is selected by the PSEL bit or the PSEL pin. PSEL bit and PSEL pin are ORed internally.

PSEL	Reference Clock for PLL	
0	RX Input	Default
1	ELRCK Input	

Table 1. Setting of PLL Reference Clock

■ PLL Lock Time

The lock time at PSEL = "0" depends on sampling frequency (fs) and FAST bit (See Table 2). FAST bit is useful at lower sampling frequency and is fixed to "1" in parallel mode. When PSEL is "1", the lock time is 35ms (max) and is not related to the setting of the FAST bit. The lock time in Table 2 does not include the power-up time of VCOM voltage. Therefore, the power-up time of VCOM voltage must be added when PDN pin changes from "L" to "H". The power-up time of VCOM voltage is max. 15ms (Capacitor value of VCOM pin = 4.7μF).

PSEL	FAST bit	PLL Lock Time	
0	0	≤ (20ms + 384/fs)	Default
0	1	≤ (20ms + 1/fs)	
1	-	≤ 35ms	

Table 2. PLL Lock Time (fs: Sampling Frequency)

■ Word Clock (Studio Sync Clock)

The word clock is used to synchronize clocks among studio equipment and is always synchronized to the sampling frequency (1fs). The internal PLL generates MCLK, BICK and LRCK from the word clock supplied to the ELRCK pin. The PLL lock range is 22kHz to 216kHz. The word clock (ELRCK pin) can receive signal levels of 0.5Vpp(min) when AC coupled. In master mode, the clock phase between ELRCK pin and LRCK pin is within ± 5%. When the AK4115 is supplied with a bi-phase signal and a word clock (ELRCK), the phase error between the LRCK and ELRCK is within ±1/(128fs). Therefore, use LRCK and not ELRCK for the serial data output stream. When the word clock is not synchronized to the bi-phase signal, WSYNC bit should be set to "0".

■ DIT/DIR Mode

The AK4115 operates in either synchronous mode or asynchronous mode. In synchronous mode, transmitter and receiver are operated by the same clock source. In asynchronous mode, transmitter and receiver are operated by different a sampling frequencies that are selected by the ASYNC bit. Frequency multiples are not required in asynchronous mode.

1. Synchronous Mode: ASYNC bit = "0"

PSEL and CM1-0 select the clock source and the data source for SDTO. In Mode 2, the clock source is switched from PLL to X'tal when the PLL goes to the unlock state. In Mode 3, the clock source is fixed to X'tal, but PLL is also operation and the recovered data such as channel status bit can be monitored. For Mode 2 and Mode 3, it is recommended that the frequency of X'tal is different from the recovered frequency of the PLL. In Modes 4-6, the PLL source is ELRCK and MCKO1/2, BICK and LRCK are generated by the PLL. The data source of SDTO is always DAUX.

Mode	PSEL	CM1	CM0	UNLOCK	PLL Status	X'tal Status	Clock source	Clock I/O	SDTO
0	0	0	0	-	ON	ON (Note 16)	PLL (RX)	Note 17	RX
1	0	0	1	-	OFF	ON	X'tal	Note 17	DAUX
2	0	1	0	0	ON	ON	PLL (RX)	Note 17	RX
				1	ON	ON	X'tal	Note 17	DAUX
3	0	1	1	-	ON	ON	X'tal	Note 17	DAUX
4	1	0	0	-	ON	ON (Note 16)	PLL (ELRCK)	Note 17	DAUX
5	1	0	1	-	OFF	ON	X'tal	Note 17	DAUX
6	1	1	0	0	ON	ON	PLL (ELRCK)	Note 17	DAUX
				1	ON	ON	X'tal	Note 17	DAUX

Note 15. ON: Oscillation (Power-up), OFF: STOP (Power-down)
Note 16: When the X'tal is not used as clock comparison for fs detection (i.e. XTL1,0= "1,1"), the X'tal is OFF.
Note 17. MCKO1/2, BICK, LRCK

Table 3. Clock operation for DIT/DIR in synchronous mode

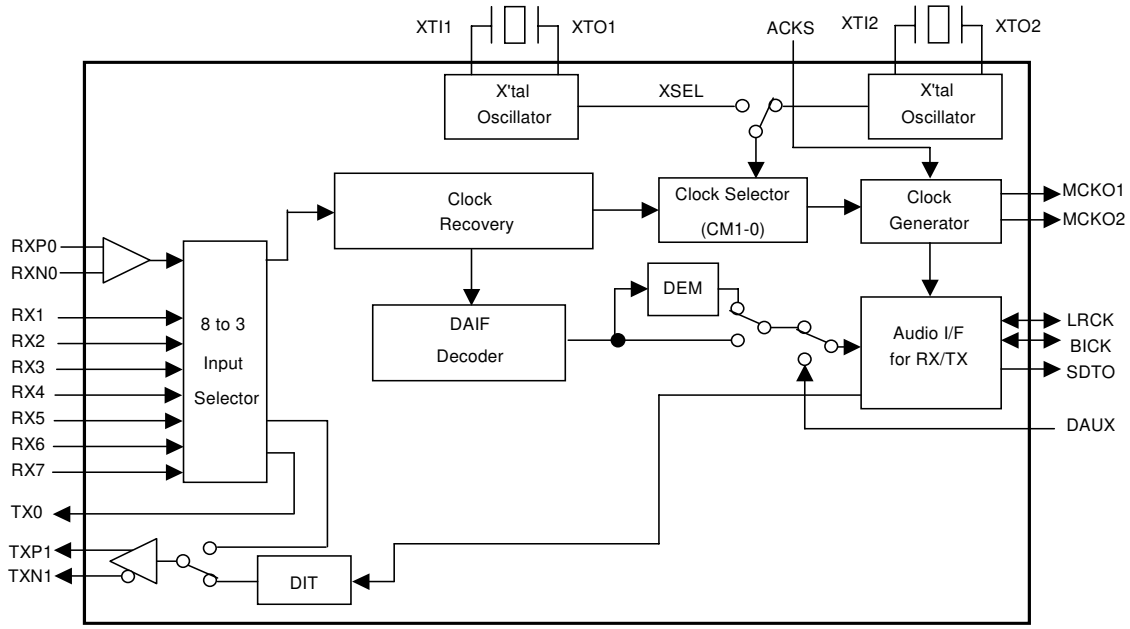


Figure 14. Clocks for DIT/DIR in synchronous mode (PSEL bit = "0")

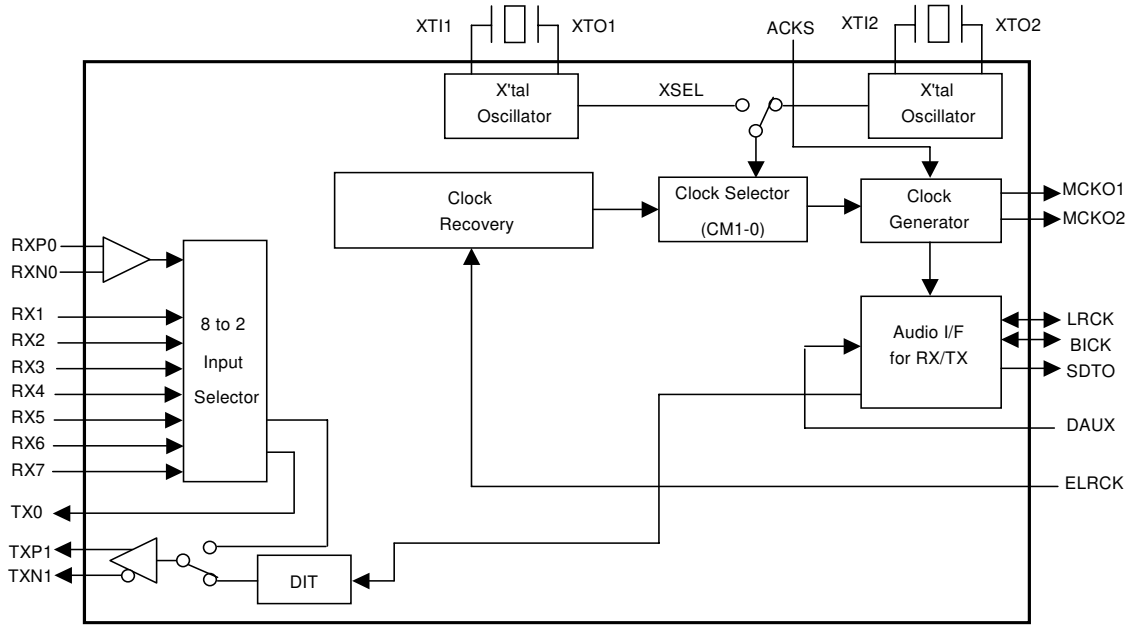


Figure 15. Clocks for DIT/DIR in synchronous mode (PSEL bit = "1")

2. Asynchronous Mode: ASYNC bit = "1", PSEL = "0"

When ASYNC bit is "1", DIT and DIR can operate at different sample rates(non-multiples). In Mode1, Mode2 (When the PLL is the unlock state) and Mode3, SDTO is fixed "L". The input timing of DAUX should be synchronized with ELRCK and EBCIK. The master clock of TX can be selected to either X'tal or EMCK by the MSEL bit (See Table 4).

MSEL bit	Master Clock	
0	X'tal	Defalut
1	EMCK	

Table 4. Master clock setting for TX in asynchronous mode.

Mode	CM1	CM0	UNLOCK	PLL Status	X'tal Status	RX			TX	
						Clock Source	Clock I/O	SDTO	Clock Source	Clock I/O
0	0	0	-	ON	ON (Note 19)	PLL (RX)	Note 20	RX	X'tal or EMCK (Note 22)	Note 21
1	0	1	-	OFF	ON	X'tal	Note 20	"L"	X'tal or EMCK	Note 21
2	1	0	0	ON	ON	PLL (RX)	Note 20	RX	X'tal or EMCK	Note 21
			1	ON	ON	X'tal	Note 20	"L"	X'tal or EMCK	Note 21
3	1	1	-	ON	ON	X'tal	Note 20	"L"	X'tal or EMCK	Note 21

Note 18. ON: Oscillation (Power-up), OFF: STOP (Power-down)

Note 19 When the X'tal is not used as clock comparison for sampling frequency detection (i.e. XTL1,0 = "1,1"), the X'tal is OFF.

Note 20: MCKO1/2, BICK, LRCK

Note 21. EMCK or X'tal, EBICK, ELRCK, DAUX

Note 22. When X'tal is OFF, the clock source supports EMCK only.

Table 5. Clock operation for DIT/DIR in asynchronous mode

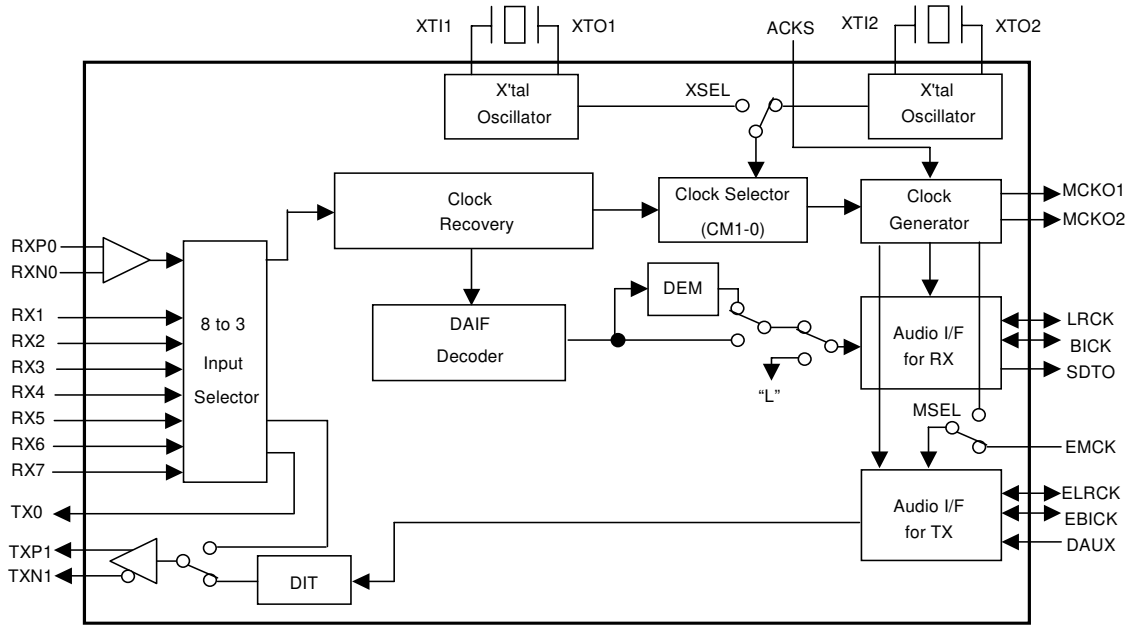


Figure 16. Clocks for DIT/DIR in asynchronous mode

■ Block start, Channel status bit, User bit and Validity bit

The AK4115 can control and monitor block start, channel status bits, user bits and validity bit for RX and TX. B, C and U pins are bi-directional and the direction of input/output can be selected by the BCU_IO bit. B, C, U and VOUT pins become "L" (BCU_IO bit = "1") in an unlocked state of Mode 2.

a. Serial mode & Except AES3 mode (P/SN pin = "L", AES3 bit = "0")

ASYNC bit	BCU_IO bit	Block Start (B pin)	RX			TX		
			Channel Status bit	User bit	Validity bit	Channel Status bit	User bit	Validity bit
0	0	Input	CR191-0 bits	N/A	VOUT pin VRX bit (Note 24)	C pin CT191-0 bits (Note 25)	U pin	VIN pin VTX bit (Note 26)
	1	Output	C pin CR191-0 bits (Note 23)	U pin	VRX bit VOUT pin (Note 24)	CT191-0 bits	All "0" data (Note 27)	VIN pin VTX bit (Note 26)
1	0	Input	CR191-0 bits	N/A	VRX bit	C pin CT191-0 bits (Note 25)	U pin	VIN pin VTX bit (Note 26)
	1	Output	C pin CR191-0 bits (Note 23)	U pin	VOUT pin VRX bit (Note 24)	CT191-0 bits	All "0" data	VTX bit

Note 23. Channel status bit for RX can be monitored by both C pin and CR191-0 bits.
Note 24. Validity bit for RX can be monitored by both VOUT pin and VRX bit.
Note 25. C pin and CT191-0 bits are ORed internally.
Note 26. VIN pin and VTX bit are ORed internally.
Note 27. When UDIT bit is "1", the recovered U bits are used for DIT(DIR-DIT loop mode of U bit).

Table 6. Block start, Channel Status bit, User bit and Validity bit in serial mode except AES3 mode (N/A: Not available)

b. Serial mode & AES3 mode (P/SN pin = "L", AES3 bit = "1", ASYNC bit = "0")

DIF1 bit	BCU_IO bit	Block Start (B pin)	RX			TX		
			Channel Status bit	User bit	Validity bit	Channel Status bit	User bit	Validity bit
0	0	Input	CR191-0 bits SDTO pin (Note 28)	SDTO pin	VOUT pin VRX bit SDTO pin (Note 31)	C pin CT191-0 bits (Note 32)	U pin	VIN pin VTX bit (Note 34)
	1	Output	C pin CR191-0 bits SDTO pin (Note 29)	U pin SDTO pin (Note 30)	VOUT pin VRX bit SDTO pin (Note 31)	CT191-0 bits	All "0" data (Note 35)	VIN pin VTX bit (Note 34)
1	0	Input	CR191-0 bits SDTO pin (Note 28)	SDTO pin	VOUT pin VRX bit SDTO pin (Note 31)	CT191-0 bits DAUX pin (Note 33)	DAUX pin	DAUX pin
	1	Output	C pin CR191-0 bits SDTO pin (Note 29)	U pin SDTO pin (Note 30)	VOUT pin VRX bit SDTO pin (Note 31)	CT191-0 bits DAUX pin (Note 33)	DAUX pin	DAUX pin

Note 28. Channel status bit for RX can be monitored by CR191-0 bits and SDTO pin.
Note 29. Channel status bit for RX can be monitored by C pin, CR191-0 bits and SDTO pin.
Note 30. User bit for RX can be monitored by U pin and SDTO pin.
Note 31. Validity bit for RX can be monitored by VOUT pin, VRX bit and SDTO pin.
Note 32. C pin and CT191-0 bits are ORed internally.
Note 33. Channel status bit can select either CT191-0 bits or DAUX pin by the setting of CTX bit.
Note 34. VIN pin and VTX bit are ORed internally.
Note 35. When UDIT bit is "1", the recovered U bits are used for DIT(DIR-DIT loop mode of U bit).

Table 7. Block start, Channel Status bit, User bit and Validity bit in serial mode & AES3 mode

c. Parallel mode (P/SN pin = "H")

Block Start (B pin)	RX			TX		
	Channel Status bit	User bit	Validity bit	Channel Status bit	User bit	Validity bit
Output	C pin	U pin	VOUT pin	Default value of CT191-0 bits	All "0" data	VIN pin

Table 8. Block start, Channel Status bit, User bit and Validity bit in parallel mode

1. Channel Status bit

1-1. RX

The data recovered from the bi-phase input signal is stored in CR191-0 bits. When the BCU_IO bit = "1", the channel status bits are available on the C pin according to the block signal timing. The channel status bits are outputted from SDTO pin with audio data in AES3 mode.

1-2. TX

The channel status bit can controlled by the CT191-0 bits. When BCU_IO bit is "0", the channel status bits are also controlled by C pin. CT191-0 bits and the signal on the C pin are ORed internally.

The input to C pin is ignored in AES3 mode. When CTX bit is set to "0", the channel status bits on DAUX pin are outputted with audio data from TX. When CTX bit is set to "1", the values of CT191-0 bits are outputted with audio data from TX.

When the CCRE bit is "1" and AK4115 is in professional mode (bit0 = "1"), the CRC code can be generated according to the professional mode definition in the AES3 standard. When the CCRE bit is "0", the CRC data is not generated and the data from the CT191-0 bits is passed to the TX directly. In the consumer mode (bit0 = "0"), the CRC code is not generated.

In the consumer mode (bit0 = "0"), bits20-23(audio channel) must be controlled by the CT20 bit. When the CT20 bit is "1", the AK4115 corresponds to "stereo mode", bits20-23 are set to "1000"(left channel) in sub-frame 1, and is set to "0100"(right channel) in sub-frame 2. When the CT20 bit is "0", bits20-23 is set to "0000" in both sub-frame 1 and sub-frame 2.

All CR191-0 bits are transferred to CT191-0 bits when the CTRAN bit changes from "0" to "1". The transferred CT191-0 bits are valid after the next block start signal is detected. CTRAN bit goes to "0" after finishing the transfer. Don't write to the CT191-0 bits when the CTRAN bit = "1".

2. User bit

2-1. RX

When the BCU_IO bit is "1", the recovered user bit is available on the U pin according to block start timing. The user bits are outputted from SDTO pin with audio data in AES3 mode.

2-2. TX

When the BCU_IO bit is "0", the user bit is sent to the U pin according to block start timing. When BCU_IO bit is "1" and the ASYNC bit is "0"(synchronous mode), the user bit is controlled by the UDIT bit. When the UDIT bit is "0", user bit is set to "0". When the UDIT bit is "1", the recovered U bits are used for DIT(DIR-DIT loop mode of U bit). This mode (UDIT bit = "1") is enabled when the PLL is locked. The input to U pin is ignored in AES3 mode and the user bits on DAUX pin are outputted with audio data from TX.

3. Validity bit

3-1. RX
In synchronous mode, the validity bit is available on the VOUT pin according to block start timing. In asynchronous mode, the validity bit is available on the VOUT pin according to LRCK timing. The VRX bit is available in both modes. The validity bit is outputted from SDTO pin with audio data in AES3 mode.

3-2. TX

The validity bit is controlled by the VIN pin or the VTX bit. Since the validity bit does not usually update every sub-frame cycle, it can be controlled by the VIN pin according to LRCK timing in synchronous mode. In asynchronous mode, it can be controlled by the VIN pin according to ELRCK timing. When the validity bit timing is synchronized with the block start timing , the BCU_IO bit should be "0". In asynchronous mode, the validity bit cannot be controlled by the VIN pin when BCU_IO bit is set to "0".

The input to VIN pin and VTX bit are ignored in AES3 mode and the validity bit on DAUX is outputted with audio data from TX.

4. Block Start Signal Timing

In synchronous mode, the block start signal timing depends on LRCK. In asynchronous mode, it depends on ELRCK. The channel status, user and validity bits are captured with the current audio sample. When the block start signal is an input (BCU_IO bit = "0"), the block start signal should stay high for more than one sub-frame. When the block start signal is an output (BCU_IO bit = "1"), the block start signal goes high at the start of frame 0 and remains high until the end of frame 39.

The input to B pin is ignored in AES3 mode and the B bit on DAUX is used as the block start timing.

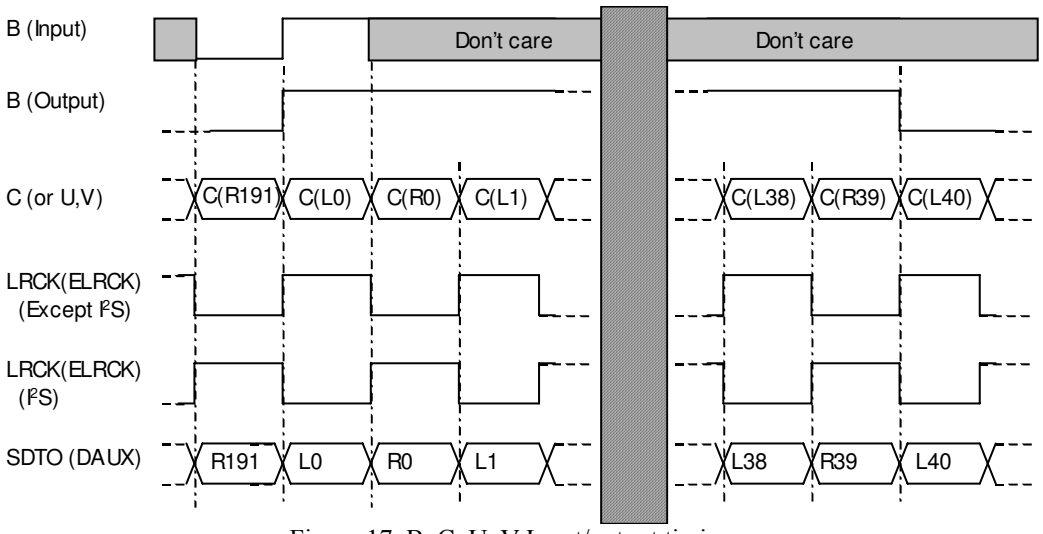


Figure 17. B, C, U, V Input/output timings

■ Master Clock Output

The AK4115 has two master clock outputs, MCKO1 and MCKO2. MCKO2 has two modes. These modes can be selected by the XMCK bit.

1) When XMCK bit = "0"

These clocks are derived from either the recovered clock or the X'tal oscillator. The frequencies of the master clock outputs (MCKO1 and MCKO2) are set by OCKS0 and OCKS1 as shown in Table 9. The 512fs clock is changed into the 256fs clock when sampling frequency is 96kHz or 192kHz. The 512fs or 256fs clock is changed into the 128fs clock when sampling frequency is 192kHz.

No.	OCKS1	OCKS0	MCKO1 pin	MCKO2 pin	X'tal	fs (max)	
0	0	0	256fs	256fs	256fs	96 kHz	Default
1	0	1	256fs	128fs	256fs	96 kHz	
2	1	0	512fs	256fs	512fs	48 kHz	
3	1	1	128fs	64fs	128fs	192 kHz	

Table 9. Master Clock Output Frequency

2) When XMCK bit = "1"

MCKO2 outputs the input clock of the XTI pin. The settings of CM1-0 and OCKS1-0 bits are ignored. The output frequency can be set by the DIV bit. MCKO1 outputs a clock that is selected by the CM1-0 bits and OCKS1-0 bits.

XMCK bit	DIV bit	MCKO2 Clock Source	MCKO2 Frequency
1	0	X'tal (Note 36)	x 1
1	1	X'tal (Note 36)	x 1/2

Note 36. MCKO2 Clock Source is selected by XSEL bit.

Table 10. Select output frequency of MCKO2

■ Master Clock Auto Setting Mode

The master clock auto setting mode detects the MCLK/LRCK ratio (selects Normal/Double/Quad automatically). When ACKS is "1", this mode is enabled. The frequencies of MCKO1 and MCKO2 are shown in Table 11. In this mode, the settings of OCKS1-0 are ignored. This mode is only supported when the sampling frequency detection circuit is enabled in PLL mode.(refer to "Sampling Frequency and Pre-emphasis Detection" section.) When ELRCK is selected and XTL1-0 = "11", this mode is not supported. In X'tal mode, the frequencies of MCKO1/MCKO2 depend upon OCKS1-0. The ACKS pin and ACKS bit are ORed internally.

Mode	MCKO1	MCKO2	Sampling Frequency Range
Normal Speed	512fs	256fs	22kHz to 48kHz
Double Speed	256fs	128fs	64kHz to 96kHz
Quad Speed	128fs	64fs	176.4kHz to 216kHz

Table 11. Master Clock Frequency Select (Master Clock Auto Setting Mode)

■ X'tal Oscillator

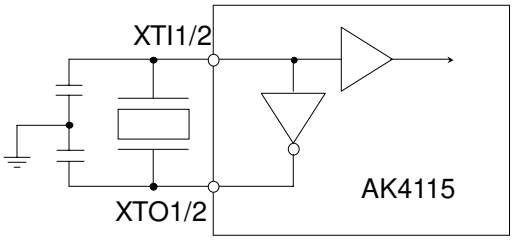
The AK4115 has two X'tal oscillators. They can not operate at the same time. The operation of the X'tal oscillator is selected by the XSEL bit or the XSEL pin.

XSEL	Status	
	X'tal #1	X'tal #2
0	Power-Up	Power-Down
1	Power-Down	Power-Up

Table 12. Setting of X'tal oscillator

The following circuits are available to feed the clock to the XTI1/2 pins of AK4115.

1) X'tal



Note: External capacitance depends upon the crystal oscillator (typ. 5-10pF)

Figure 18. X'tal mode

2) External clock

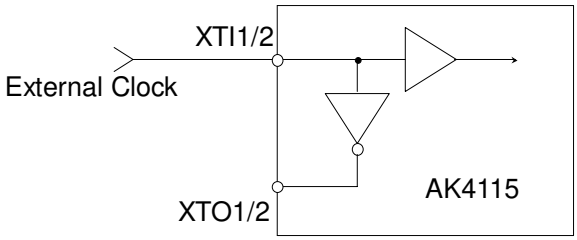


Figure 19. External clock mode

3) Fixed to the Clock Operation Mode 0

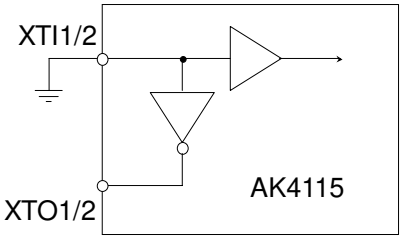


Figure 20. OFF mode