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AK4116

Low Power 48kHz Digital Audio Receiver

GENERAL DESCRIPTION

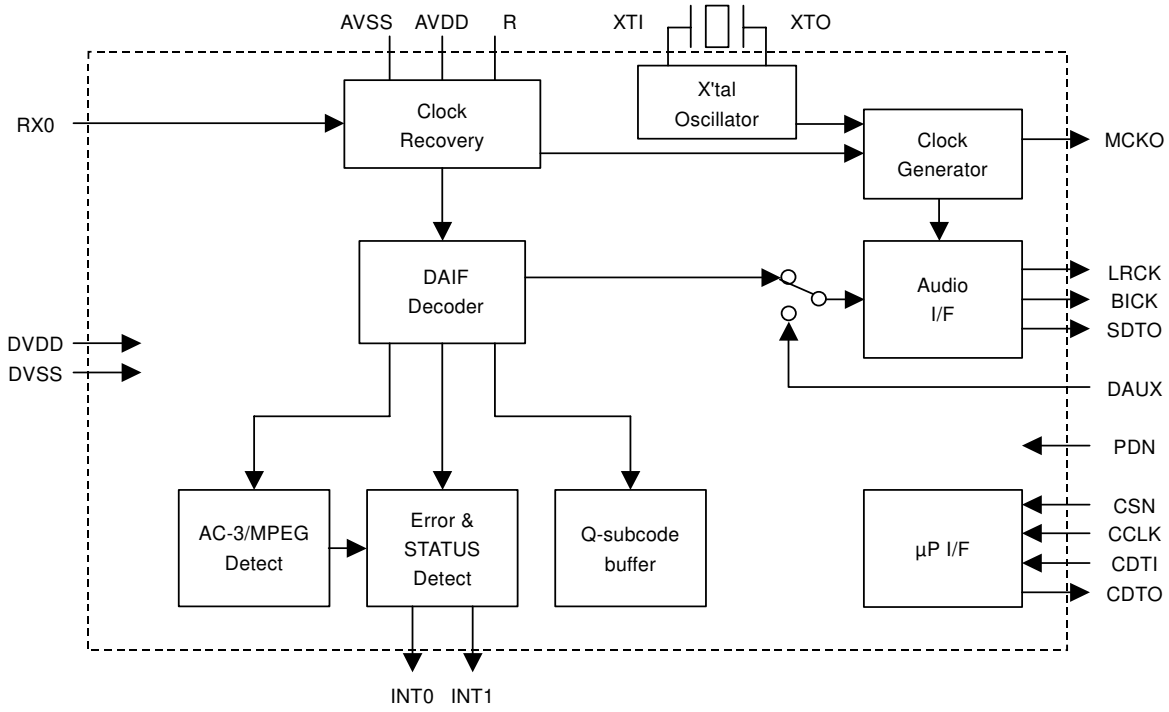
The AK4116 is a low power S/PDIF AES/EBU receiver supporting resolution up to 24-bit. The integrated channel status decoder supports both consumer and professional modes. The AK4116 can automatically detect a Non-PCM bit stream. Combining the AK4116 with a multi-channel codec such as AKM's AK4527B or AK4529 can create a complete AC-3 system. Mode settings can be controlled via microprocessor serial interface. The small 20pin QFN package saves board space.

*AC-3 is a trademark of Dolby Laboratories.

FEATURES

- **AES3, IEC60958, S/PDIF, EIAJ CP1201 Compatible**
- **Low jitter Analog PLL**
- **PLL Lock Range : 32kHz to 48kHz**
- **Clock Source: PLL or X'tal**
- **Auxiliary digital input**
- **Detection Functions**
  - **Non-PCM Bit Stream Detection**
  - **DTS-CD Bit Stream Detection**
  - **Sampling Frequency Detection (32kHz, 44.1kHz, 48kHz)**
  - **Unlock & Parity Error Detection**
  - **Validity Flag Detection**
- **Up to 24bit Audio Data Format**
- **Audio I/F: Left justified, Right justified (16bit, 18bit, 20bit, 24bit), I^2S**
- **40-bit Channel Status Buffer**
- **Burst Preamble bit Pc and Pd Buffer for Non-PCM bit stream**
- **Q-subcode Buffer for CD bit stream**
- **4-wire Serial µP I/F**
- **Master Clock Output: 256fs**
- **Operating Voltage: 2.7 to 3.6V**
- **Power Supply Current: 7mA (PLL mode)**
  2mA (X'tal mode)
- **Small Package: 20pin QFN**
- **Ta: -40 to 85°C**

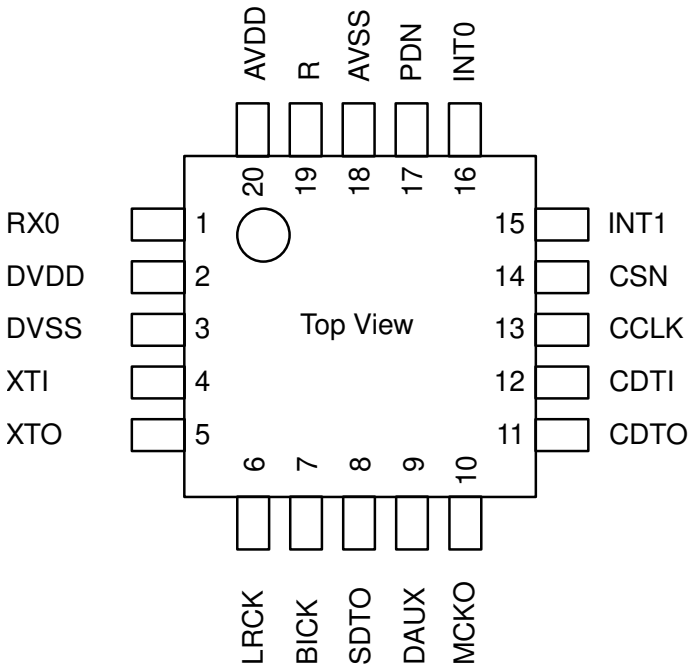
■ Block Diagram



■ Ordering Guide

AK4116VN	-40 ~ +85 °C	20pin QFN (0.5mm pitch)

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	RX0	I	Receiver Channel 0 (Internal Biased Pin)
2	DVDD	-	Digital Power Supply Pin
3	DVSS	-	Digital Ground Pin
4	XTI	I	X'tal Input Pin
5	XTO	O	X'tal Output Pin
6	LRCK	O	Output Channel Clock Pin
7	BICK	O	Audio Serial Data Clock Pin
8	SDTO	O	Audio Serial Data Output Pin
9	DAUX	I	Auxiliary Audio Data Input Pin
10	MCKO	O	Master Clock Output Pin
11	CDTO	O	Control Data Output Pin
12	CDTI	I	Control Data Input Pin
13	CCLK	I	Control Data Clock Pin
14	CSN	I	Chip Select Pin
15	INT1	O	Interrupt 1 Pin
16	INT0	O	Interrupt 0 Pin
17	PDN	I	Power-Down & Reset Pin When "L", the AK4116 is powered-down and reset, and all output pins go to "L" and the control registers are reset to default state.
18	AVSS	-	Analog Ground Pin
19	R	-	External Resistor Pin 12kΩ-5% ~ 13kΩ+5% resistor to AVSS externally.
20	AVDD	-	Analog Power Supply Pin

Note 1: All input pins except internal biased pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 2)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	-0.3	4.6	V
	Digital	DVDD	-0.3	4.6	V
	|AVSS-DVSS| (Note 3)	ΔGND		0.3	V
Input Current (Any pins except supplies)		IIN	-	±10	mA
Input Voltage (Except RX0, RX1 pins)		VIN1	-0.3	DVDD+0.3	V
(RX0, RX1 pins)		VIN2	-0.3	AVDD+0.3	V
Ambient Temperature (Power applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltages with respect to ground.

Note 3. AVSS and DVSS must be connected to the same ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog	AVDD	2.7	3.3	3.6	V
	Digital	DVDD	2.7	3.3	AVDD	V

Note 2. All voltages with respect to ground.

S/PDIF RECEIVER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.7~3.6V)

Parameter	Symbol	min	typ	max	Units
Input Resistance	Zin	-	10	-	kΩ
Input Voltage	VTH	350			mVpp
Input Sample Frequency	fs	32	-	48	kHz

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.7~3.6V; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
Power Supply Current					
Normal operation (PDN= "H") (Note 4)					
CM1-0= "00" (Note 5)			7	14	mA
CM1-0= "01" (Note 6)			2	-	mA
Power down (PDN = "L") (Note 7)			10	100	μA
High-Level Input Voltage	VIH	70%DVDD	-	DVDD+0.3	V
Low-Level Input Voltage	VIL	DVSS-0.3	-	30%DVDD	V
High-Level Output Voltage (Iout=-400μA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage (Iout=400μA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	± 10	μA

Note 4. AVDD=DVDD=3.3V.

Note 5. fs=48kHz, X'tal=24.576MHz, C_L=20pF. AVDD=5mA (typ), DVDD=9mA (typ).

Note 6. fs=48kHz, X'tal=24.576MHz. The external load current is not included.

Note 7. RX inputs are open and all digital input pins are held at DVDD or DVSS.

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.7~3.6V; C_L=20pF)

Parameter			Symbol	min	typ	max	Units
Master Clock Timing							
Crystal Resonator	Frequency		fXTAL	11.2896		24.576	MHz
External Clock	Frequency		fECLK	2.048		24.576	MHz
	Duty Cycle		dECLK	40	50	60	%
MCKO Output	Frequency		fMCK	1.024		24.576	MHz
	Duty Cycle	(Note 8)	dMCK	40	50	60	%
PLL Clock Recover Frequency (RX0)			fpll	32	-	48	KHz
LRCK Timing							
Frequency	PLL mode		fs	32		48	kHz
	X'tal mode		fs	44.1		48	kHz
	External Clock mode		fs	8		48	kHz
Duty Cycle			dLCK	45		55	%
Audio Interface Timing							
BICK Frequency			fBCK		64fs		Hz
BICK Duty			dBCK		50		%
BICK "↓" to LRCK			tMBLR	-20		20	ns
BICK "↓" to SDTO			tBSD			15	ns
DAUX Hold Time			tDXH	20			ns
DAUX Setup Time			tDXS	20			ns
Control Interface Timing							
CCLK Period			tCCK	200			ns
CCLK Pulse Width Low			tCCKL	80			ns
Pulse Width High			tCCKH	80			ns
CDTI Setup Time			tCDS	50			ns
CDTI Hold Time			tCDH	50			ns
CSN "H" Time			tCSW	150			ns
CSN "↓" to CCLK "↑"			tCSS	50			ns
CCLK "↑" to CSN "↑"			tCSH	50			ns
CDTO Delay			tDCD			45	ns
CSN "↑" to CDTO Hi-Z			tCCZ			70	ns
Reset Timing							
PDN Pulse Width			tPW	150			ns

Note 8. Except the external clock input.

■ Timing Diagram

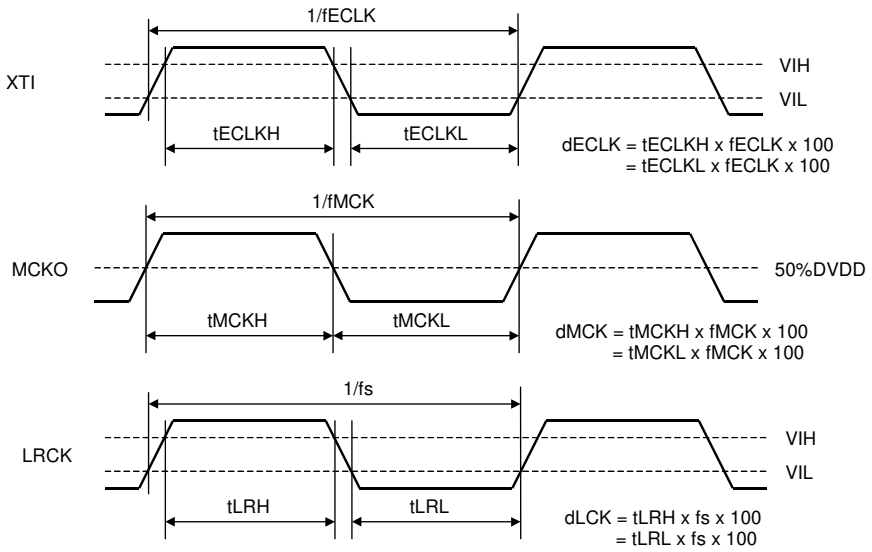


Figure 1. Clock Timing

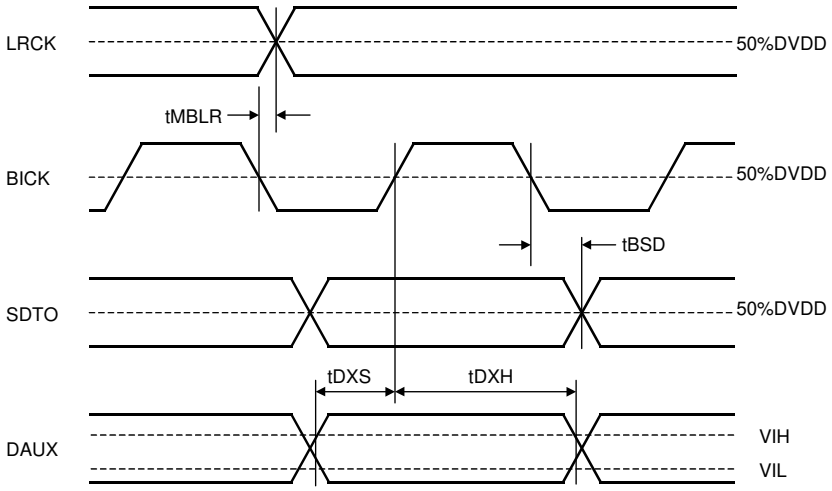


Figure 2. Serial Interface Timing

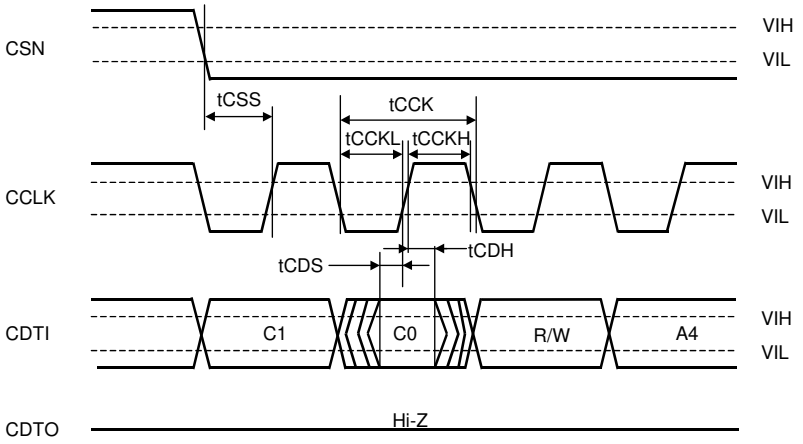


Figure 3. WRITE/READ Command Input Timing

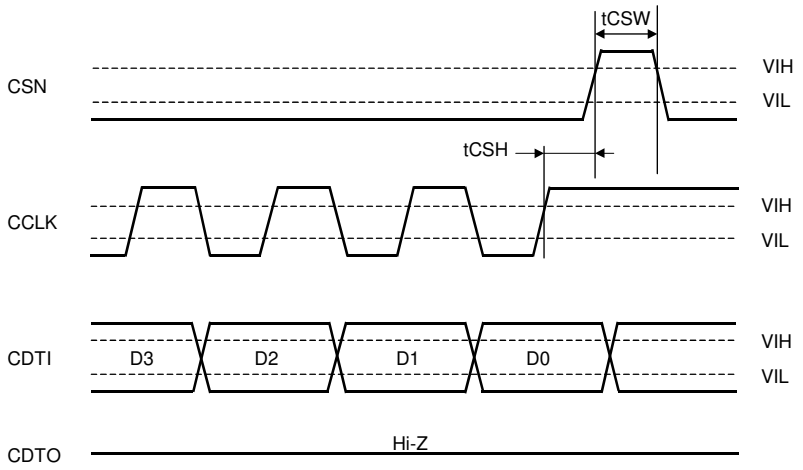


Figure 4. WRITE Data Input Timing

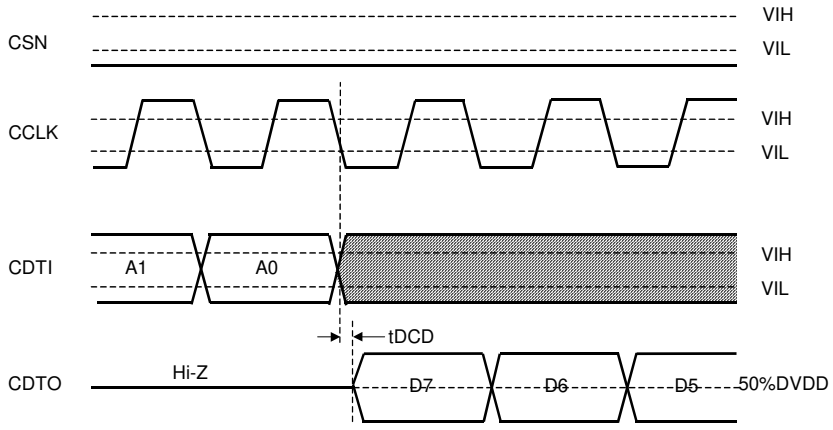


Figure 5. READ Data Output Timing 1

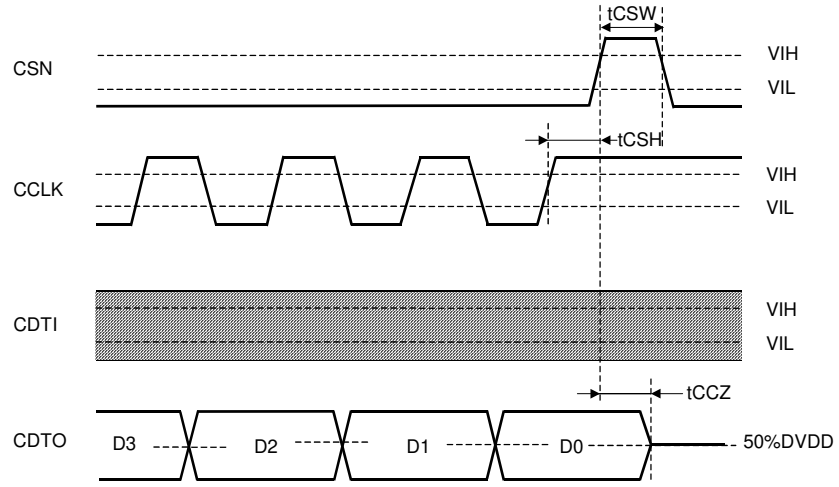


Figure 6. READ Data Input Timing 2

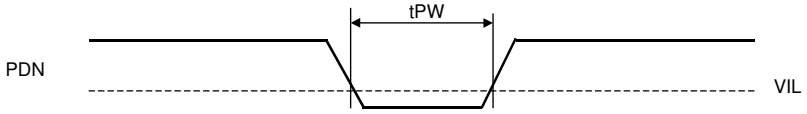


Figure 7. Power Down & Reset Timing

OPERATION OVERVIEW

■ Non-PCM (AC-3, MPEG, etc.) and DTS-CD Bitstream Detection

The AK4116 has a Non-PCM steam auto-detection function. When the 32-bit mode Non-PCM preamble based on Dolby "AC-3 Data Stream in IEC60958 Interface" is detected, the NPCM bit goes to "1". The 96-bit sync code consists of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872 and 0x4E1F. Detection of this pattern will set the NPCM to "1". Once the NPCM is set to "1", it will remain "1" until 4096 frames pass through the chip without an additional sync pattern being detected (Timing diagram: Figure 26 and Figure 27). When those preambles are detected, the burst preambles Pc (burst information: Table 8) and Pd (length code: Table 9) that follow those sync codes are stored to registers. The AK4116 also has a DTS-CD bitstream auto-detection function. When AK4116 detects DTS-CD bitstreams, the DTSCD bit goes to "1". If the next sync code does not occur within 4096 frames, the DTSCD bit goes to "0" until either the AK4116 detects the stream again. OR'ed value of the NPCM and DTSCD bits are output to the AUTO bit. The AK4116 detects 14bit sync word of a DTS-CD bitstearm, while it does not detect 16bit sync word (0x7FFE8001).

■ Clock Recovery

The on-chip, low jitter PLL has a wide lock range of 32kHz to 48kHz and a lock time of less than 20ms. The AK4116 has a sampling frequency detect function (32kHz, 44.1kHz and 48kHz) that uses either clock comparison against the X'tal oscillator or the channel status information. The PLL loses lock when the received sync interval is incorrect.

■ Clock Operation Mode

The AK4116 has two sources for MCKO and SDTO.

1) MCKO and SDTO source is recovered by PLL from RX input.
2) MCKO source is X'tal or External clock. SDTO source is DAUX input.

The CM1-0 bits select the clock operation mode (Table 1). In Mode 2, the clock source is switched from PLL to X'tal when the PLL loses lock. In Mode3, even though the clock source is fixed to X'tal, the PLL is also operating. This allows the monitoring of recovered data such as C bits. For Mode2 and 3, it is recommended that the X'tal frequency and PLL recovery frequency be set differently.

Mode	CM1	CM0	UNLCK	PLL	X'tal	Clock source	SDTO	
0	0	0	-	ON	ON(Note)	PLL	RX	Default
1	0	1	-	OFF	ON	X'tal	DAUX	
2	1	0	0	ON	ON	PLL	RX	
			1	ON	ON	X'tal	DAUX	
3	1	1	-	ON	ON	X'tal	DAUX	

ON: Oscillation (Power-up), OFF: STOP (Power-down)
Note : When the X'tal is not used as clock comparison for fs detection (i.e. XTL1,0= "1,1"), the X'tal is off.

Table 1. Clock Operation Mode select

■ Master Clock Output

The AK4116 has a master clock output pin, MCKO. In PLL mode, PLL lock range is up to 48kHz and the MCKO frequency is fixed to 256fs.

In the X'tal mode, XCKS1-0 bits select the ratio of the X'tal frequency to fs (sampling frequency). The DIV bit selects the ratio (x1 or x1/2) of the MCKO frequency to the X'tal frequency (Table 2).

XCKS1	XCKS0	X'tal or EXT	MCKO		fs [kHz]						
					EXTCLK [MHz]			X'tal [MHz]			
			DIV=0	DIV=1	2.048	4.096	8.192	11.2896	12.288	24.576	
0	0	128fs	128fs	64fs	16	32	N/A	N/A	N/A	N/A	
0	1	256fs	256fs	128fs	8	16	32	44.1	48	N/A	Default
1	0	512fs	512fs	256fs	N/A	8	16	N/A	N/A	48	
1	1	1024fs	1024fs	512fs	N/A	N/A	8	N/A	N/A	N/A	

Table 2. Master Clock Frequency Select
(X'tal mode: Clock operation mode 1, 2(UNLCK=1), 3)

■ Clock Source

The following circuits are available to feed a clock into the XTI pin of AK4116.

1) X'tal mode

The X'tal with proper value should be connected between XTI and XTO pins.

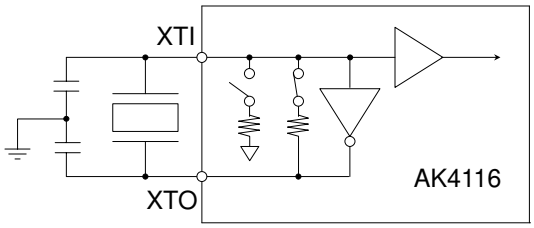


Figure 8. X'tal mode (EXCK= "0")
Note: External capacitance depends on the crystal oscillator (Typ.10-40pF).

2) External clock mode

EXCK bit should be set to "1" and the proper frequency clock input into the XTI pin. XTO pin should be left open.

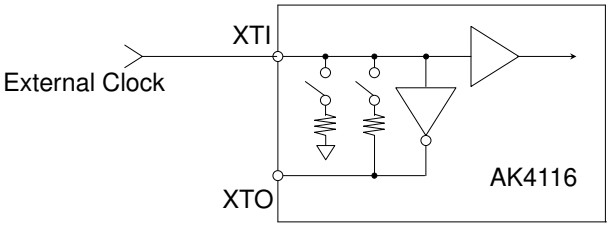


Figure 9. External clock mode (EXCK= "1")

3) OFF mode

CM1-0 bits should be set to "00" and XTL1-0 bits to "11" respectively. XTI and XTO pins should be left open. The XTI pin can also be connected to ground externally.

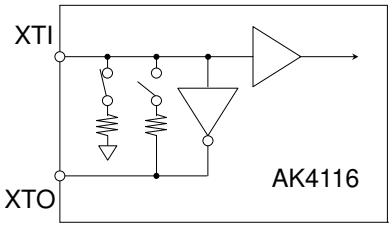


Figure 10. OFF mode (CM1-0= "00", XTL1-0= "11")

■ Sampling Frequency and Pre-emphasis Detection

The AK4116 has two methods for detecting the sample frequency:

1) Clock comparison between recovered clock and the X'tal oscillator
FS3-0 bits indicate the detected RX input frequency referred to X'tal frequency. XTL1-0 bits select the reference X'tal frequency (Table 3).

2) Sampling frequency information on channel status
When XTL1-0= "11", FS3-0 bits indicate the decoded sampling frequency information from channel status.

XTL1	XTL0	X'tal Frequency	
0	0	11.2896MHz	Default
0	1	12.288MHz	
1	0	24.576MHz	
1	1	(Use channel status)	

Table 3. Reference X'tal frequency

Register output				fs	Except XTL1-0= "11"	XTL1-0= "11"		
					Clock comparison (Note 1)	Consumer mode (Note 2)	Professional mode	
FS3	FS2	FS1	FS0			Byte3 Bit3,2,1,0	Byte0 Bit7,6	Byte4 Bit6,5,4,3
0	0	0	0	44.1kHz	44.1kHz ± 3%	0 0 0 0	0 1	0 0 0 0
0	0	0	1	Reserved	Reserved	0 0 0 1	(Others)	
0	0	1	0	48kHz	48kHz ± 3%	0 0 1 0	1 0	0 0 0 0
0	0	1	1	32kHz	32kHz ± 3%	0 0 1 1	1 1	0 0 0 0
1	0	0	0	Reserved	Reserved	(1 0 0 0)	0 0	1 0 1 0
1	0	1	0	Reserved	Reserved	(1 0 1 0)	0 0	0 0 1 0
1	1	0	0	Reserved	Reserved	(1 1 0 0)	0 0	1 0 1 1
1	1	1	0	Reserved	Reserved	(1 1 1 0)	0 0	0 0 1 1

Note 1: At least ±3% range is identified as the value in the Table 4. In case of an intermediate frequency of these two, FS3-0 bits indicate the nearer value. When the frequency is much larger than 48kHz or much smaller than 32kHz, FS3-0 bits indicate any values except 32kHz, 44.1kHz and 48kHz.
Note 2: In consumer mode, Byte3 Bit3-0 are copied to FS3-0.

Table 4. Sampling frequency information

The pre-emphasis information is detected and reported on the PEM bit. This information is extracted from channel 1 by default (CS12=0). It can be switched to channel 2 by changing the CS12 bit in the control register.

PEM	Pre-emphasis	Consumer mode	Professional mode
		Byte 0 Bits 3-5	Byte 0 Bits 2-4
0	OFF	≠ 0X100	≠110
1	ON	0X100	110

Table 5. Pre-emphasis information

■ System Reset and Power-Down

The AK4116 has a full power-down mode for all circuits that is activated by the PDN pin, and a partial power-down mode activated by the PWN bit. The RSTN bit initializes the internal registers and timing. The AK4116 should be reset once at power-up by bringing PDN pin = "L".

PDN Pin:

All analog and digital circuits are placed in power-down and reset modes by bringing PDN= "L". All the registers are initialized and clocks are stopped. Read/write operations to the registers are disabled.

RSTN Bit (Address 00H; D0):

All the registers except RSTN, PWN, XTL1-0 and EXCK are initialized by bringing RSTN bit = "0". The internal timings are also initialized. When RSTN bit= "0", clocks are output, but SDTO is "L". All register writes except RSTN, PWN, XTL1-0 and EXCK are disabled. Reading from the registers is enabled.

PWN Bit (Address 00H; D1):

Clock recovery mode is initialized by bringing PWN bit = "0". Clocks from the PLL are stopped while the X'tal clocks continue to be output. Unlike the PDN pin operation described above, internal registers and mode settings are not initialized. Read/write operations to the registers are enabled.

■ Biphase signal input circuit

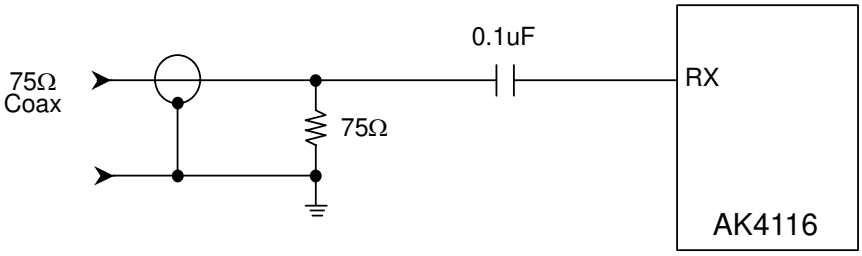


Figure 11. Consumer Input Circuit (Coaxial Input)

Note: When using a coaxial input, if the coupling level to this input from the next RX input line pattern exceeds 50mV, incorrect operation may occur. This can be reduced or prevented by adding a decoupling capacitor.

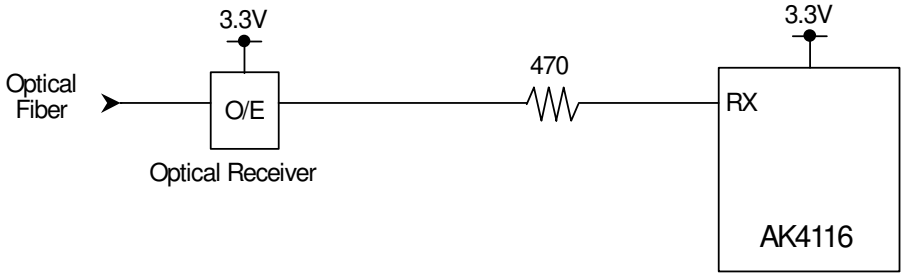


Figure 12. Consumer Input Circuit (Optical Input; Using 3.3V Optical Receiver)

■ Q-subcode buffers

The AK4116 has a Q-subcode buffer for CD application. The AK4116 takes Q-subcode into registers under the following conditions:

1) The sync word (S0,S1) is consists of least 16 “0”s.
2) The start bit is “1”.
3) Those 7bits Q-W follows to the start bit.
4) The distance between two start bits is 8-16 bits.

The QINT bit in the control register goes “1” when the new Q-subcode differs from old one, and goes “0” when QINT bit is read.

	1	2	3	4	5	6	7	8	*
S0	0	0	0	0	0	0	0	0	0…
S1	0	0	0	0	0	0	0	0	0…
S2	1	Q2	R2	S2	T2	U2	V2	W2	0…
S3	1	Q3	R3	S3	T3	U3	V3	W3	0…
:	:	:	:	:	:	:	:	:	:
S97	1	Q97	R97	S97	T97	U97	V97	W97	0…
S0	0	0	0	0	0	0	0	0	0…
S1	0	0	0	0	0	0	0	0	0…
S2	1	Q2	R2	S2	T2	U2	V2	W2	0…
S3	1	Q3	R3	S3	T3	U3	V3	W3	0…
:	:	:	:	:	:	:	:	:	:
		↑							(*) number of "0" : min=0; max=8.
		Q							

Figure 13. Configuration of U-bit(CD)

Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15	Q16	Q17	Q18	Q19	Q20	Q21	Q22	Q23	Q24	Q25
CTRL				ADRS				TRACK NUMBER								INDEX							

Q26	Q27	Q28	Q29	Q30	Q31	Q32	Q33	Q34	Q35	Q36	Q37	Q38	Q39	Q40	Q41	Q42	Q43	Q44	Q45	Q46	Q47	Q48	Q49
MINUTE								SECOND								FRAME							

Q50	Q51	Q52	Q53	Q54	Q55	Q56	Q57	Q58	Q59	Q60	Q61	Q62	Q63	Q64	Q65	Q66	Q67	Q68	Q69	Q70	Q71	Q72	Q73
ZERO								ABSOLUTE MINUTE								ABSOLUTE SECOND							

Q74	Q75	Q76	Q77	Q78	Q79	Q80	Q81	Q82	Q83	Q84	Q85	Q86	Q87	Q88	Q89	Q90	Q91	Q92	Q93	Q94	Q95	Q96	Q97
ABSOLUTE FRAME								CRC															

$G(x)=x^{16}+x^{12}+x^{5}+1$

Figure 14. Q-subcode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Q-subcode Address / Control	Q9	Q8	· · ·	· · ·	· · ·	· · ·	Q3	Q2
12H	Q-subcode Track	Q17	Q16	· · ·	· · ·	· · ·	· · ·	Q11	Q10
13H	Q-subcode Index	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·
14H	Q-subcode Minute	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·
15H	Q-subcode Second	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·
16H	Q-subcode Frame	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·
17H	Q-subcode Zero	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·
18H	Q-subcode ABS Minute	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·
19H	Q-subcode ABS Second	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·
1AH	Q-subcode ABS Frame	Q81	Q80	· · ·	· · ·	· · ·	· · ·	Q75	Q74

Figure 15. Q-subcode register map

■ Interrupt Handling

There are eight events which cause the INT1-0 pins to go “H”.

1. UNLCK: PLL unlock state detect
   “1” when the PLL loses lock. The AK4116 loses lock when the distance between two preambles is not correct or when those preambles are not correct.
2. PAR: Parity error or biphase coding error detection
   “1” when parity error or biphase coding error is detected, updated every sub-frame cycle. Reading this register resets it.
3. AUTO: Non-PCM or DTS-CD Bit Stream detection
   The OR function of NPCM and DTSCD bits is output to the AUTO bit.
4. V: Validity flag detection
   “1” when validity flag is detected. Updated every sub-frame cycle.
5. AUDION: Non-audio detection
   “1” when the “AUDIO” bit in recovered channel status indicates “1”. Updated every block cycle.
6. STC: Sampling frequency or pre-emphasis information change detection
   “1” when FS3-0 or PEM bit changes. Reading this register resets it.
7. QINT: U bit (Q-subcode) sync flag
   “1” when the Q-subcode differs from old one, and stays “1” until this register is read. Updated every sync code cycle for Q-subcode. Reading this register resets it.
8. CINT: Channel status sync flag
   “1” when received C bits differ from old ones, and stays “1” until this register is read. Updated every block cycle. Reading this register resets it.

INT1-0 pins output an OR’ed signal based on the above eight interrupt events. When masked, the interrupt event does not affect the operation of the INT1-0 pins (the masks do not affect the resisters (UNLCK, PAR, etc.) themselves). Once INT0 pin goes to “H”, it maintains “H” for 1024 cycles (this value can be changed by the EFH1-0 bits) after all events not masked by mask bits are cleared. INT1 pin immediately goes to “L” when those events are cleared.

UNLCK, AUTO, V and AUDION bits indicate the interrupt status events above in real time. Once PAR, STC, QINT or CINT bit goes to “1”, it stays “1” until the register is read. INT pin holds “H” for one sub-frame, then goes to “L” in this case.

When the AK4116 loses lock, the channel status bits are initialized. In this initial state, INT0 outputs the OR’ed signal between UNLCK and PAR bits. INT1 outputs the OR’ed signal to AUTO, V and AUDION. INT1-0 pins are “L” when the PLL is OFF (Clock Operation Mode 1).

Event			SDTO Pin
UNLCK	PAR	Others	
1	x	x	“L”
0	1	x	Previous Data
0	0	x	Output

Table 6. Interrupt handling

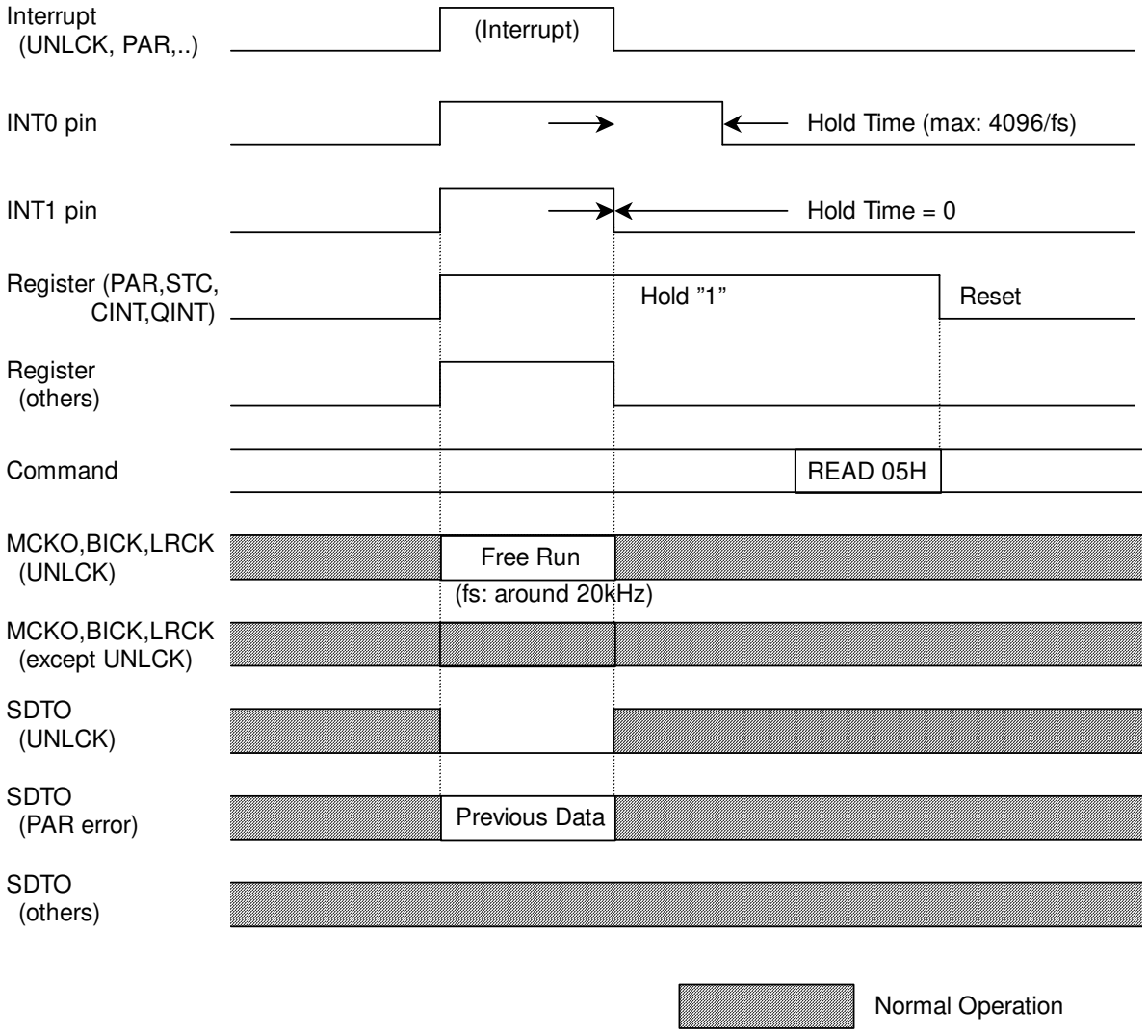


Figure 16. INT1-0 pin timing

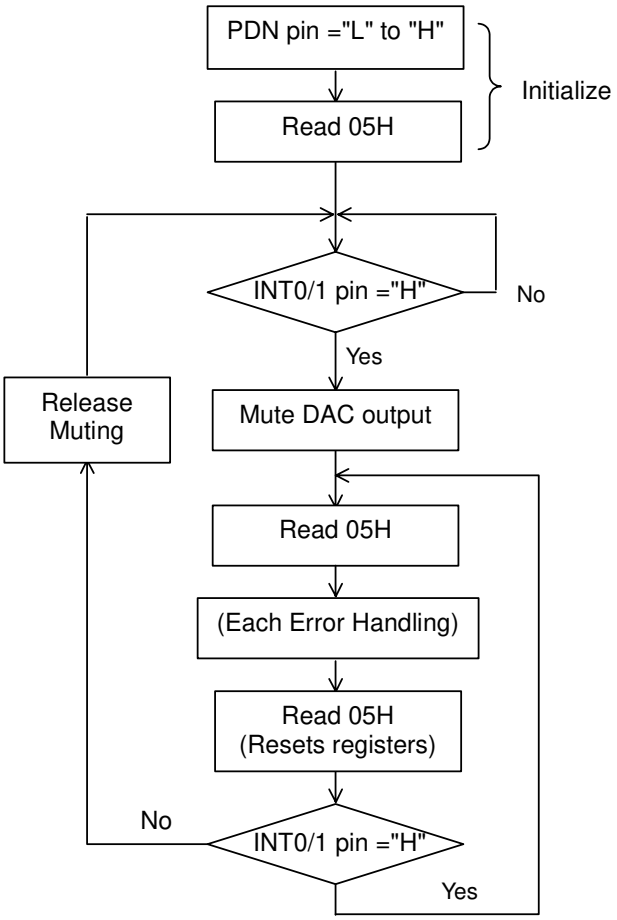


Figure 17. Interrupt Handling Sequence Example 1

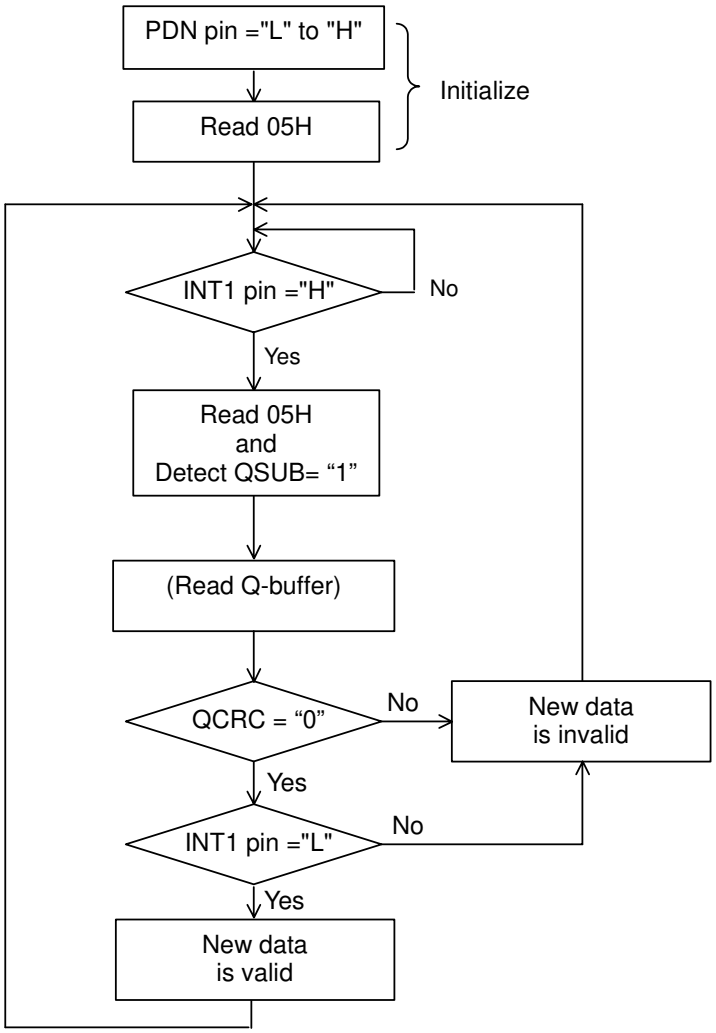


Figure 18. Interrupt Handling Sequence Example (for Q/CINT)

■ Audio Serial Interface Format

The DIF2-0 bits can select six serial data formats as shown in Table 7. In all formats, the serial data is MSB-first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK and the DAUX is latched on the rising edge of BICK. BICK outputs 64fs clock. When the SDTO format is equal or less than 20 bits (Mode 0-2), LSBs in the sub-frame are truncated. In Modes 3-7, the last four LSBs are auxiliary data (see Figure 19).

When a Parity Error, Biphase Error or Frame Length Error occurs in a sub-frame, the AK4116 continues to output the last normal sub-frame data from SDTO repeatedly until the error is removed. When an Unlock Error occurs, the AK4116 outputs "0" from SDTO. When using the DAUX pin, the data is transformed and output from SDTO. The DAUX pin is used in Clock Operation Modes 1, 3 and in the unlock state of Mode 2. The input data format to DAUX should be left-justified except in Mode 5. In Mode 5, both the input data format of DAUX and the output data format of SDTO are I^2S.

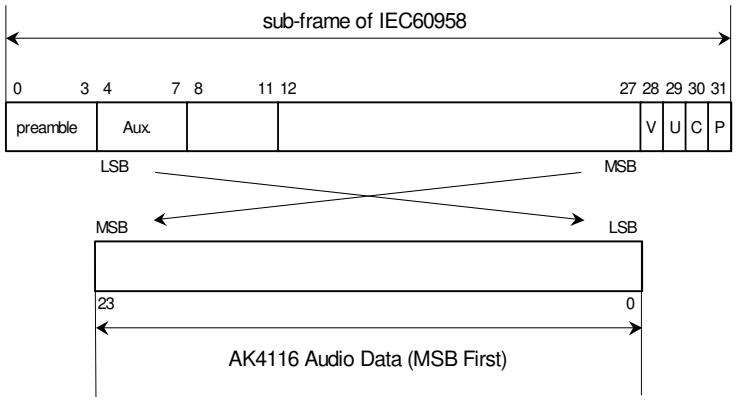


Figure 19. Bit configuration

Mode	DIF2	DIF1	DIF0	DAUX	SDTO	LRCK	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	Default
5	1	0	1	24bit, I^2S	24bit, I^2S	L/H	
6	1	1	0	Reserved			
7	1	1	1				

Table 7. Audio data format

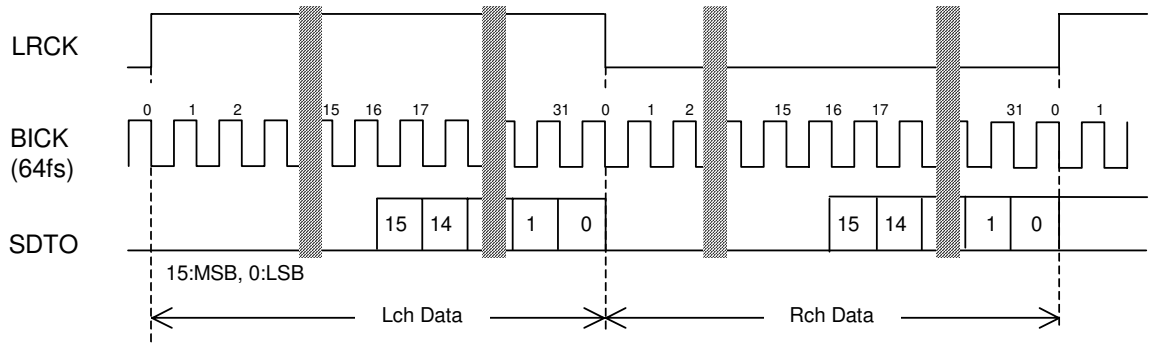


Figure 20. Mode 0 Timing

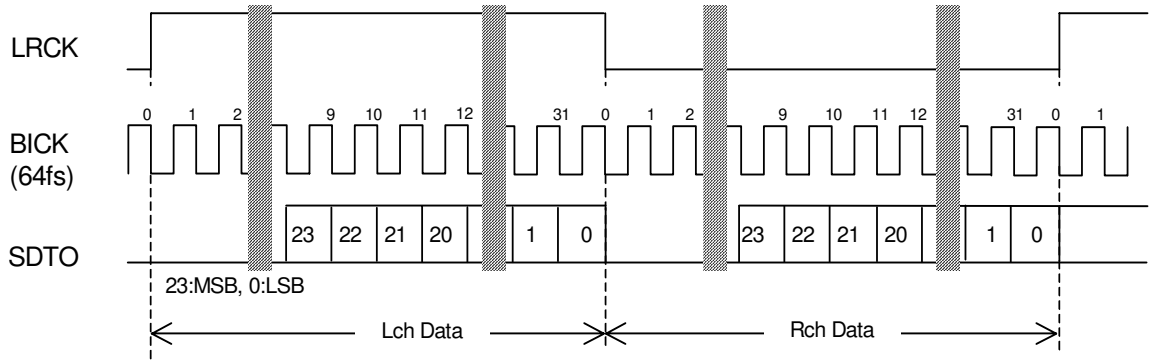


Figure 21. Mode 3 Timing

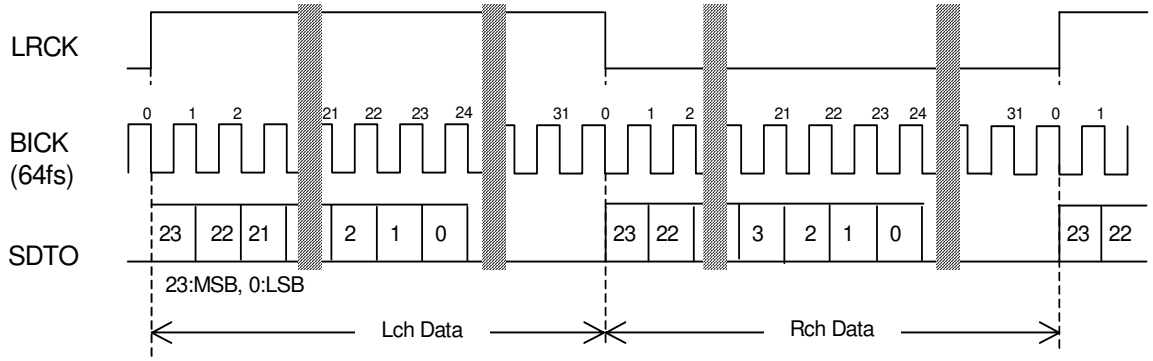


Figure 22. Mode 4 Timing

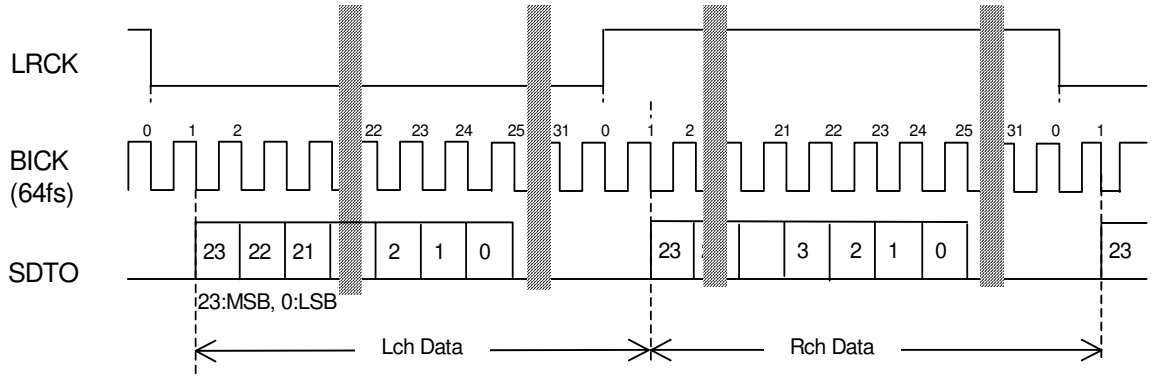
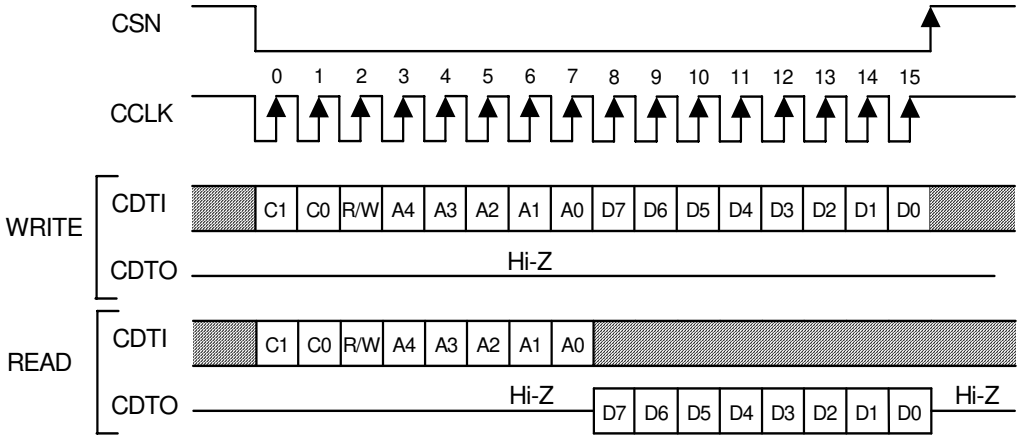


Figure 23. Mode 5 Timing

■ Serial Control Interface

The internal registers may be either written or read by the 4-wire µP interface pins: CSN, CCLK, CDTI & CDTO. The data on this interface consists of Chip address (2bits, C1-0 are fixed to "00"), Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data are clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CSN. For read operations, the CDTO output goes high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. PDN= "L" resets the registers to their default values.



C1,C0: Chip Address (Fixed to "00")
R/W: READ/WRITE (0:READ, 1:WRITE)
A4-A0: Register Address
D7-D0: Control Data

Figure 24. 4-wire Serial Control I/F Timing

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Down Control	0	0	0	EXCK	XTL1	XTL0	PWN	RSTN
01H	Clock Control	1	0	1	DIV	XCKS1	XCKS0	CM1	CM0
02H	Input/Output Control	0	0	CS12	EFH1	EFH0	DIF2	DIF1	DIF0
03H	INT0 MASK	MULK0	MPAR0	MAUT0	MV0	MAUD0	MSTC0	MCIT0	MQIT0
04H	INT1 MASK	MULK1	MPAR1	MAUT1	MV1	MAUD1	MSTC1	MCIT1	MQIT1
05H	Receiver status 0	UNLCK	PAR	AUTO	V	AUDION	STC	CINT	QINT
06H	Receiver status 1	0	DTSCD	NPCM	PEM	FS3	FS2	FS1	FS0
07H	Receiver status 2	0	0	0	0	0	0	CCRC	QCRC
08H	RX Channel Status Byte 0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
09H	RX Channel Status Byte 1	CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
0AH	RX Channel Status Byte 2	CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
0BH	RX Channel Status Byte 3	CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24
0CH	RX Channel Status Byte 4	CR39	CR38	CR37	CR36	CR35	CR34	CR33	CR32
0DH	Burst Preamble Pc Byte 0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
0EH	Burst Preamble Pc Byte 1	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
0FH	Burst Preamble Pd Byte 0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
10H	Burst Preamble Pd Byte 1	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
11H	Q-subcode Address / Control	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2
12H	Q-subcode Track	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
13H	Q-subcode Index	Q25	Q24	Q23	Q22	Q21	Q20	Q19	Q18
14H	Q-subcode Minute	Q33	Q32	Q31	Q30	Q29	Q28	Q27	Q26
15H	Q-subcode Second	Q41	Q40	Q39	Q38	Q37	Q36	Q35	Q34
16H	Q-subcode Frame	Q49	Q48	Q47	Q46	Q45	Q44	Q43	Q42
17H	Q-subcode Zero	Q57	Q56	Q55	Q54	Q53	Q52	Q51	Q50
18H	Q-subcode ABS Minute	Q65	Q64	Q63	Q62	Q61	Q60	Q59	Q58
19H	Q-subcode ABS Second	Q73	Q72	Q71	Q70	Q69	Q68	Q67	Q66
1AH	Q-subcode ABS Frame	Q81	Q80	Q79	Q78	Q77	Q76	Q75	Q74

Note: When PDN pin goes to “L”, the registers are initialized to their default values.
When RSTN bit goes to “0”, the internal timing is reset and all registers except RSTN, PWN, XTL1-0 and EXCK bits are initialized to their default values.
All data can be written to the registers even if PWN bit is “0”.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Down Control	0	0	0	EXCK	XTL1	XTL0	PWN	RSTN
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

RSTN: Timing Reset & Register Initialize
0: Reset & Initialize (except RSTN, PWN, XTL1-0 and EXCK bits)
1: Normal Operation (Default)
PWN: Power-Down for Clock Recovery Part
0: Power Down
1: Normal Operation (Default)
XTL1-0: Reference X'tal Frequency Select (Table 3; Default: 00)
EXCK: External Clock Mode Select
0: X'tal mode (Default)
1: External clock mode (Feedback resistor of X'tal oscillator circuit is open.)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Clock Control	1	0	1	DIV	XCKS1	XCKS0	CM1	CM0
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	0	0	1	0	0

CM1-0: Master Clock Operation Mode Select (Table 1; Default: 00)
XCKS1-0: Master Clock Frequency Select at X'tal Mode (Table 2; Default: 01)
DIV: Master Clock Output Select at X'tal Mode
0: Same frequency as X'tal (Default)
1: Half frequency of X'tal