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# AK4118A

## High Feature 192kHz 24bit Digital Audio I/F Transceiver

## GENERAL DESCRIPTION

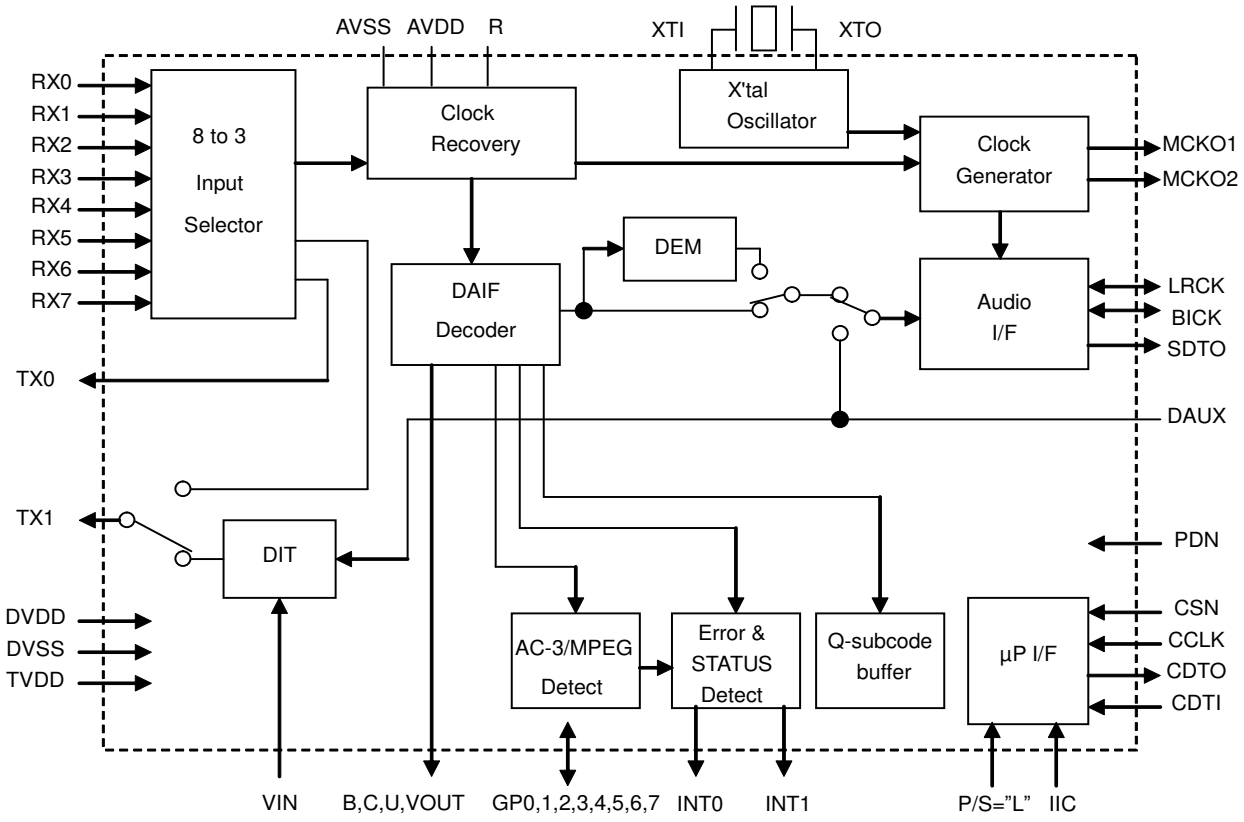
The AK4118A is a digital audio transceiver supporting 192kHz, 24bits. The channel status decoder supports both consumer and professional modes. The AK4118A can automatically detect a Non-PCM bit stream. When combined with the multi channel codec (AK4626A or AK4628A), the two chips provide a system solution for AC-3 applications. The dedicated pins or a serial µP I/F can control the mode setting. The small package, 48pin LQFP saves the system space.

*AC-3 is a trademark of Dolby Laboratories.

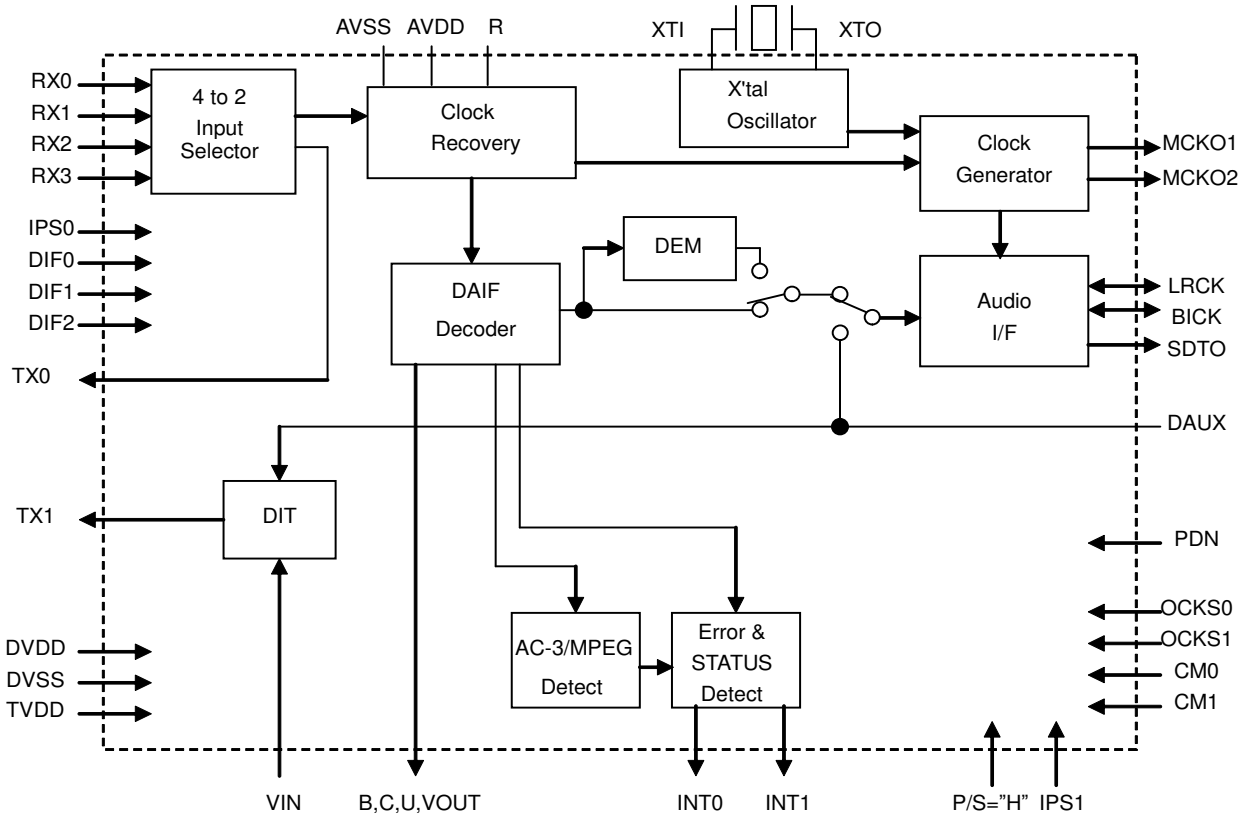
## FEATURES

- ☐ **AES3, IEC60958, S/PDIF, EIAJ CP1201 Compatible**
- ☐ **Low jitter Analog PLL**
- ☐ **PLL Lock Range: 8kHz ~ 192kHz**
- ☐ **Clock Source: PLL or X'tal**
- ☐ **8-channel Receiver input**
- ☐ **2-channel Transmission output (Through output or DIT)**
- ☐ **Auxiliary digital input**
- ☐ **De-emphasis for 32kHz, 44.1kHz, 48kHz and 96kHz**
- ☐ **Detection Functions**
  - **Non-PCM Bit Stream Detection**
  - **DTS-CD Bit Stream Detection**
  - **Sampling Frequency Detection (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, 192kHz)**
  - **Unlock & Parity Error Detection**
  - **Validity Flag Detection**
  - **DAT Start ID Detection**
- ☐ **Up to 24bit Audio Data Format**
- ☐ **Audio I/F: Master or Slave Mode**
- ☐ **42-bit Channel Status Buffer**
- ☐ **Burst Preamble bit Pc and Pd Buffer for Non-PCM bit stream**
- ☐ **Q-subcode Buffer for CD bit stream**
- ☐ **Serial µP I/F ($I^2C$, SPI)**
- ☐ **Two Master Clock Outputs: 64fs/128fs/256fs/512fs**
- ☐ **Operating Voltage: 2.7 to 3.6V with 5V tolerance**
- ☐ **8GPIO Port**
- ☐ **RX Data Input Detection**
- ☐ **Small Package: 48pin LQFP**
- ☐ **Ta: -10 to 70°C**

## ■ Block Diagram




Serial Control Mode

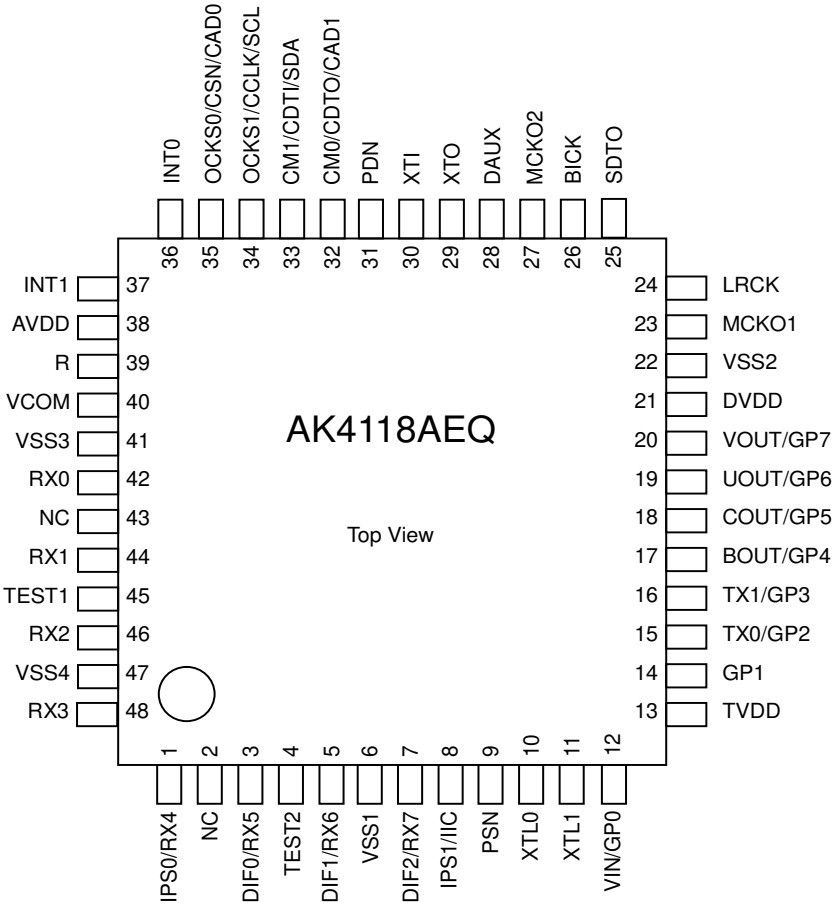



Parallel Control Mode

## ■ Ordering Guide

| | | |
|---|---|---|
| AK4118AEQ | -10 ~ +70 °C | 48pin LQFP (0.5mm pitch) |
| AKD4118A | Evaluation Board for AK4118A | |

## ■ Pin Layout



## ■ Compatibility with AK4118

### 1. Function and Characteristics

| Function | AK4118A | AK4118 |
|---|---|---|
| Master Clock | The MCKO2 pin outputs “L” when CM1-0 bit = “00”or “10” and UNLOCK bit = “0”. | The MCKO1 and MCKO2 pins output “256fs, 128fs, 64fs” clock according to OCKS1-0 bits setting, regardless of the clock source. |
| S/PDIF Receiver | Time deviation Jitter typ; 100ps RMS<br>Cycle-to-Cycle Jitter typ; 50ps RMS | No descriptions about Jitter. |

### 2. Register

| Addr | Bit | AK4118A | AK4118 |
|---|---|---|---|
| 28H | D6 | 1 | 0 |

## PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | IPS0 | I | Input Channel Select 0 Pin in Parallel Mode |
| | RX4 | I | Receiver Channel 4 Pin in Serial Mode (Internal biased pin) |
| 2 | NC | I | No Connect<br>No internal bonding. This pin should be connected to VSS3. |
| 3 | DIF0 | I | Audio Data Interface Format 0 Pin in Parallel Mode |
| | RX5 | I | Receiver Channel 5 Pin in Serial Mode (Internal biased pin) |
| 4 | TEST2 | I | TEST 2 pin<br>This pin should be connect to VSS3. |
| 5 | DIF1 | I | Audio Data Interface Format 1 Pin in Parallel Mode |
| | RX6 | I | Receiver Channel 6 Pin in Serial Mode (Internal biased pin) |
| 6 | VSS1 | I | Ground Pin |
| 7 | DIF2 | I | Audio Data Interface Format 2 Pin in Parallel Mode |
| | RX7 | I | Receiver Channel 7 Pin in Serial Mode (Internal biased pin) |
| 8 | IPS1 | I | Input Channel Select 1 Pin in Parallel Mode |
| | IIC | I | IIC Select Pin in Serial Mode.<br>"L": 4-wire Serial, "H": IIC |
| 9 | PSN | I | Parallel/Serial Select Pin<br>"L": Serial Mode, "H": Parallel Mode |
| 10 | XTL0 | I | X'tal Frequency Select 0 Pin |
| 11 | XTL1 | I | X'tal Frequency Select 1 Pin |
| 12 | VIN | I | V-bit Input Pin for Transmitter Output |
| | GP0 | I/O | GPIO0 pin in Serial Mode |
| 13 | TVDD | I | Input Buffer Power Supply Pin, DVDD ~5.5V |
| 14 | GP1 | I/O | GPIO1 pin1in Serial Mode |
| 15 | TX0 | O | Transmit Channel (Through Data) Output 0 Pin |
| | GP2 | I/O | GPIO2 pin in Serial Mode |
| 16 | TX1 | O | When TX bit = "0", Transmit Channel (Through Data) Output 1 Pin.<br>When TX bit = "1", Transmit Channel (DAUX Data) Output Pin (Default). (TX bit= "1": Default) |
| | GP3 | I/O | GPIO3 pin in Serial Mode |
| 17 | BOUT | O | Block-Start Output Pin for Receiver Input<br>"H" during first 40 flames. |
| | GP4 | I/O | GPIO4 pin in Serial Mode |
| 18 | COUT | O | C-bit Output Pin for Receiver Input |
| | GP5 | I/O | GPIO5 pin in Serial Mode |
| 19 | UOUT | O | U-bit Output Pin for Receiver Input |
| | GP6 | I/O | GPIO6 pin in Serial Mode |
| 20 | VOUT | O | V-bit Output Pin for Receiver Input |
| | GP7 | I/O | GPIO7 pin in Serial Mode |
| 21 | DVDD | I | Digital Power Supply Pin, 2.7V ~ 3.6V |
| 22 | VSS2 | I | Ground Pin |
| 23 | MCKO1 | O | Master Clock Output 1 Pin |
| 24 | LRCK | I/O | Channel Clock Pin |

## PIN/FUNCTION (Continued)

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 25 | SDTO | O | Audio Serial Data Output Pin |
| 26 | BICK | I/O | Audio Serial Data Clock Pin |
| 27 | MCKO2 | O | Master Clock Output 2 Pin |
| 28 | DAUX | I | Auxiliary Audio Data Input Pin |
| 29 | XTO | O | X'tal Output Pin |
| 30 | XTI | I | X'tal Input Pin |
| 31 | PDN | I | Power-Down Mode Pin<br>When "L", the AK4118A is powered-down, and all output pins go to "L" and registers are initialized. |
| 32 | CM0 | I | Master Clock Operation Mode 1 Pin in Parallel Mode |
| | CDTO | O | Control Data Input Pin in Serial Mode, IIC= "L". |
| | CAD1 | I | Control Data Pin in Serial Mode, IIC= "H". |
| 33 | CM1 | I | Master Clock Operation Mode 1 Pin in Parallel Mode |
| | CDTI | I | Control Data Input Pin in Serial Mode, IIC= "L". |
| | SDA | I/O | Control Data Pin in Serial Mode, IIC= "H". |
| 34 | OCKS1 | I | Output Clock Select 1 Pin in Parallel Mode |
| | CCLK | I | Control Data Clock Pin in Serial Mode, IIC= "L" |
| | SCL | I | Control Data Clock Pin in Serial Mode, IIC= "H" |
| 35 | OCKS0 | I | Output Clock Select 0 Pin in Parallel Mode |
| | CSN | I | Chip Select Pin in Serial Mode, IIC="L". |
| | CAD0 | I | Chip Address 0 Pin in Serial Mode, IIC= "H". |
| 36 | INT0 | O | Interrupt 0 Pin |
| 37 | INT1 | O | Interrupt 1 Pin |
| 38 | AVDD | I | Analog Power Supply Pin, 2.7V ~ 3.6V |
| 39 | R | - | External Resistor Pin<br>10kΩ +/-1% resistor should be connected to VSS3 externally. |
| 40 | VCOM | - | Common Voltage Output Pin<br>0.47μF capacitor should be connected to VSS3 externally. |
| 41 | VSS3 | I | Ground Pin |
| 42 | RX0 | I | Receiver Channel 0 Pin (Internal biased pin)<br>This channel is default in serial mode. |
| 43 | NC | I | No Connect<br>No internal bonding. This pin should be connected to VSS3. |
| 44 | RX1 | I | Receiver Channel 1 Pin (Internal biased pin) |
| 45 | TEST1 | I | TEST 1 pin.<br>This pin should be connected to VSS3. |
| 46 | RX2 | I | Receiver Channel 2 Pin (Internal biased pin) |
| 47 | VSS4 | I | Ground Pin |
| 48 | RX3 | I | Receiver Channel 3 Pin (Internal biased pin) |

Note 1. All input pins except internal biased pins (RX0-7 pins)should not be left floating.

## ABSOLUTE MAXIMUM RATINGS

(VSS1-4=0V; Note 2, Note 3)

| Parameter | | Symbol | min | max | Units |
|---|---|---|---|---|---|
| Power Supplies: | Analog | AVDD | -0.3 | 4.6 | V |
| | Digital | DVDD | -0.3 | 4.6 | V |
| | Input Buffer | TVDD | -0.3 | 6.0 | V |
| Input Current (Any pins except supplies) | | IIN | - | ±10 | mA |
| Input Voltage (Except XTI pin) | | VIN | -0.3 | TVDD+0.3 | V |
| Input Voltage (XTI pin) | | VINX | -0.3 | DVDD+0.3 | V |
| Ambient Temperature (Power applied) | | Ta | -10 | 70 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |

Note 2. All voltages with respect to ground.
Note 3. VSS1-4 must be connected to the same ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(VSS1-4=0V; Note 2)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| Power Supplies: | Analog | AVDD | 2.7 | 3.3 | 3.6 | V |
| | Digital | DVDD | 2.7 | 3.3 | AVDD | V |
| | Input Buffer | TVDD | DVDD | 5.0 | 5.5 | V |

Note 2. All voltages with respect to ground. There is no level shifter.

## S/PDIF RECEIVER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=2.7~3.6V; TVDD=2.7~5.5V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| Input Resistance | Zin | | 10 | | kΩ |
| Input Voltage | VTH | 200 | | | mVpp |
| Input Hysteresis | VHY | - | 50 | | mV |
| Input Sample Frequency | fs | 8 | - | 192 | kHz |
| Time deviation Jitter (Note 4) | | - | 100 | - | ps RMS |
| Cycle - to - Cycle Jitter (Note 4) | | - | 50 | - | ps RMS |

Note 4. AVDD=DVDD=3.3V, TVDD=5.0V, fs=48kHz

## DC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=2.7~3.6V; TVDD=2.7~5.5V; unless otherwise specified)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| Power Supply Current | | | | | |
| Normal operation: PDN = "H" (Note 5) | | | 32 | 53 | mA |
| Power down: PDN = "L" (Note 6) | | | 10 | 100 | μA |
| High-Level Input Voltage | VIH | 70%DVDD | - | TVDD | V |
| Low-Level Input Voltage | VIL | VSS2-0.3 | - | 30%DVDD | V |
| High-Level Output Voltage (Iout=-400μA) | VOH | DVDD-0.4 | - | - | V |
| Low-Level Output Voltage | | | | | |
| (Except SDA pin: Iout=400μA) | VOL | - | - | 0.4 | V |
| ( SDA pin: Iout= 3mA) | VOL | - | - | 0.4 | V |
| Input Leakage Current | Iin | - | - | ± 10 | μA |

Note 5. AVDD=DVDD=3.3V, TVDD=5.0V, $C_L$=20pF, fs=192kHz, X'tal=24.576MHz, Clock Operation Mode 2, OCKS1=1, OCKS0=1. AVDD=7mA (typ), DVDD=25mA (typ), TVDD=10μA (typ). DVDD=36mA (typ) when the circuit of Figure 23 is attached to both TX0 and TX1 pins.

Note 6. RX inputs are open and all digital input pins are held DVDD or VSS2.

## SWITCHING CHARACTERISTICS

(Ta=25°C; DVDD=AVDD2.7~3.6V, TVDD=2.7~5.5V; $C_L$=20pF)

| Parameter | | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|---|
| **Master Clock Timing** | | | | | | | |
| Crystal Resonator | Frequency | | fXTAL | 11.2896 | | 24.576 | MHz |
| External Clock | Frequency | (Note 7) | fECLK | 8.192 | | 24.576 | MHz |
| | Duty | | dECLK | 40 | 50 | 60 | % |
| MCKO1 Output | Frequency | | fMCK1 | 4.096 | | 24.576 | MHz |
| | Duty | | dMCK1 | 40 | 50 | 60 | % |
| MCKO2 Output | Frequency | | fMCK2 | 2.048 | | 24.576 | MHz |
| | Duty | | dMCK2 | 40 | 50 | 60 | % |
| PLL Clock Recover Frequency (RX0-7) | | | Fpll | 8 | - | 192 | kHz |
| LRCK Frequency | | | fs | 8 | | 192 | kHz |
| Duty Cycle | | | dLCK | 45 | | 55 | % |
| **Audio Interface Timing** | | | | | | | |
| **Slave Mode** | | | | | | | |
| BICK Period | | | tBCK | 80 | | | ns |
| BICK Pulse Width Low | | | tBCKL | 30 | | | ns |
| Pulse Width High | | | tBCKH | 30 | | | ns |
| LRCK Edge to BICK "↑" | | (Note 8) | tLRB | 20 | | | ns |
| BICK "↑" to LRCK Edge | | (Note 8) | tBLR | 20 | | | ns |
| LRCK to SDTO (MSB) | | | tLRM | | | 30 | ns |
| BICK "↓" to SDTO | | | tBSD | | | 30 | ns |
| DAUX Hold Time | | | tDXH | 20 | | | ns |
| DAUX Setup Time | | | tDXS | 20 | | | ns |
| **Master Mode** | | | | | | | |
| BICK Frequency | | | fBCK | | 64fs | | Hz |
| BICK Duty | | | dBCK | | 50 | | % |
| BICK "↓" to LRCK | | | tMBLR | -20 | | 20 | ns |
| BICK "↓" to SDTO | | | tBSD | -15 | | 15 | ns |
| DAUX Hold Time | | | tDXH | 20 | | | ns |
| DAUX Setup Time | | | tDXS | 20 | | | ns |
| **Control Interface Timing (4-wire serial mode)** | | | | | | | |
| CCLK Period | | | tCCK | 200 | | | ns |
| CCLK Pulse Width Low | | | tCCKL | 80 | | | ns |
| Pulse Width High | | | tCCKH | 80 | | | ns |
| CDTI Setup Time | | | tCDS | 50 | | | ns |
| CDTI Hold Time | | | tCDH | 50 | | | ns |
| CSN "H" Time | | | tCSW | 150 | | | ns |
| CSN "↓" to CCLK "↑" | | | tCSS | 50 | | | ns |
| CCLK "↑" to CSN "↑" | | | tCSH | 50 | | | ns |
| CDTO Delay | | | tDCD | | | 45 | ns |
| CSN "↑" to CDTO Hi-Z | | | tCCZ | | | 70 | ns |

Note 7. When fECLK=8.192MHz, sampling frequency detect function (page16) is disable.
Note 8. BICK rising edge must not occur at the same time as LRCK edge.

## SWITCHING CHARACTERISTICS (Continued)

(Ta=25°C; DVDD=AVDD2.7~3.6V, TVDD=2.7~5.5V; $C_L$=20pF)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Control Interface Timing ($I^2C$ Bus mode):** | | | | | |
| SCL Clock Frequency | fSCL | - | | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | | - | μs |
| Start Condition Hold Time (prior to first clock pulse) | tHD:STA | 0.6 | | - | μs |
| Clock Low Time | tLOW | 1.3 | | - | μs |
| Clock High Time | tHIGH | 0.6 | | - | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | | - | μs |
| SDA Hold Time from SCL Falling (Note 9) | tHD:DAT | 0 | | - | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 100 | | - | ns |
| Rise Time of Both SDA and SCL Lines | tR | - | | 300 | ns |
| Fall Time of Both SDA and SCL Lines | tF | - | | 300 | ns |
| Setup Time for Stop Condition | tSU:STO | 0.6 | | - | μs |
| Capacitive load on bus | Cb | - | | 400 | pF |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | | 50 | ns |
| **Reset Timing** | | | | | |
| PDN Pulse Width | tPW | 150 | | | ns |

Note 9. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 10. $I^2C$-bus is a trademark of NXP B.V.

## ■ Timing Diagram

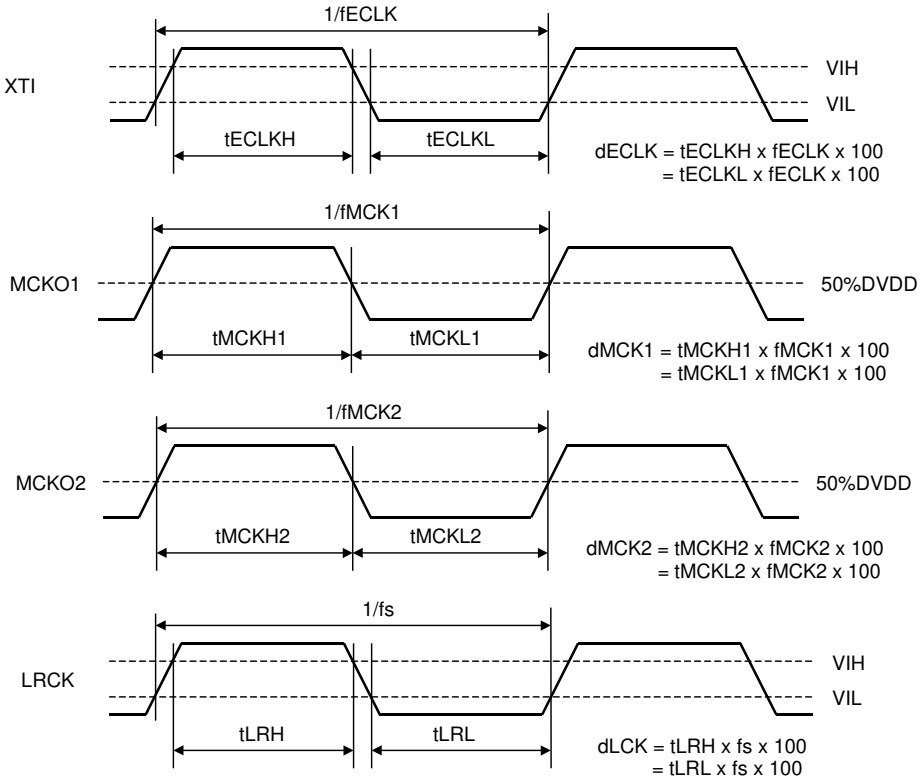



Figure 1. Clock Timing

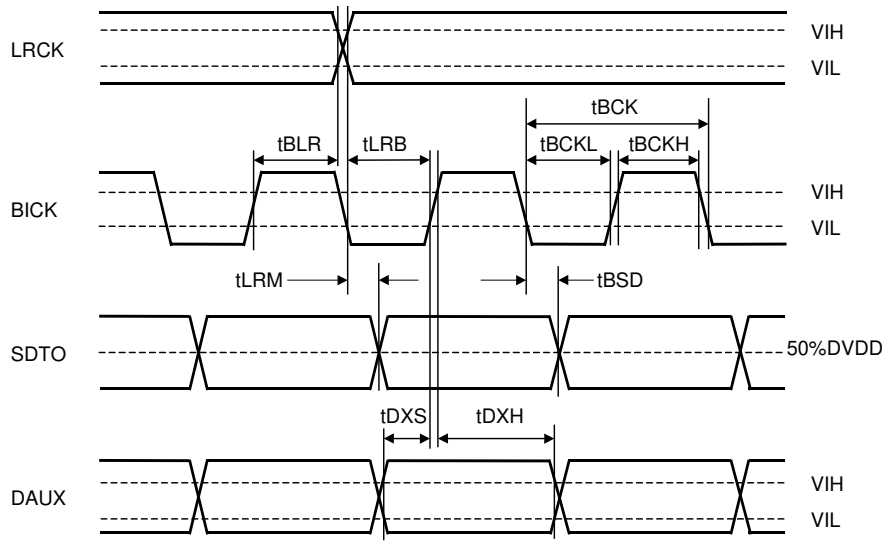



Figure 2. Serial Interface Timing (Slave Mode)

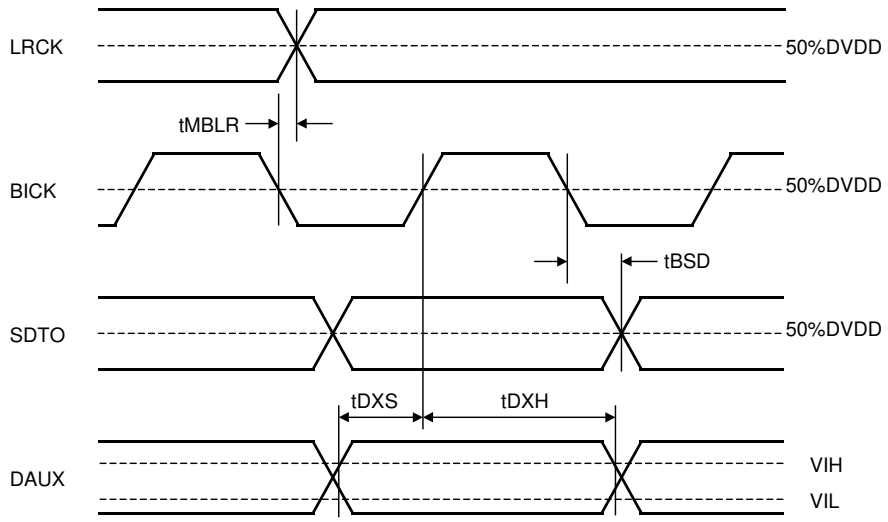



Figure 3. Serial Interface Timing (Master Mode)

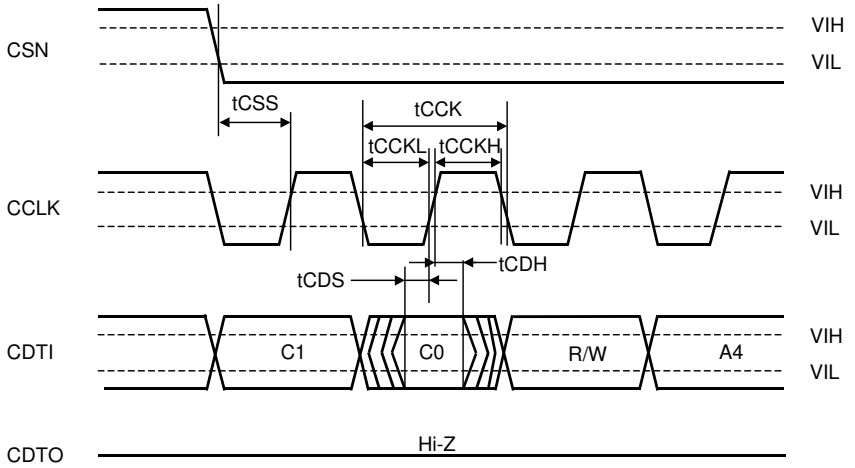



Figure 4. WRITE/READ Command Input Timing in 4-wire serial mode

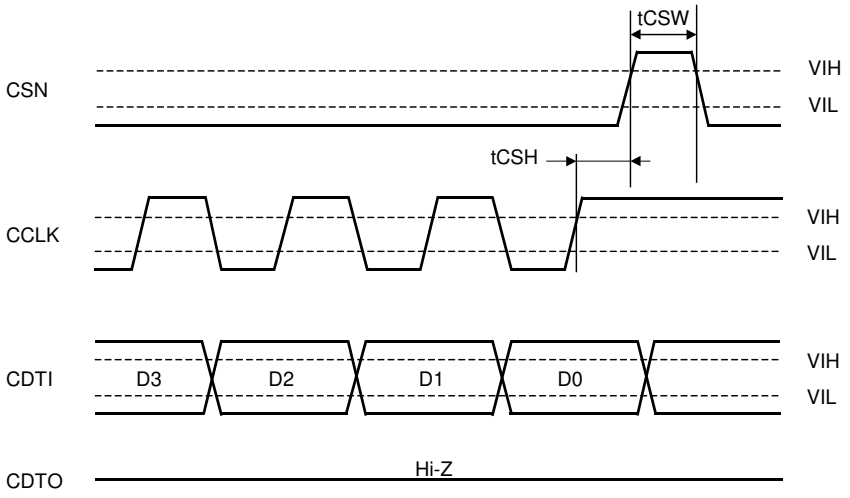



Figure 5. WRITE Data Input Timing in 4-wire serial mode

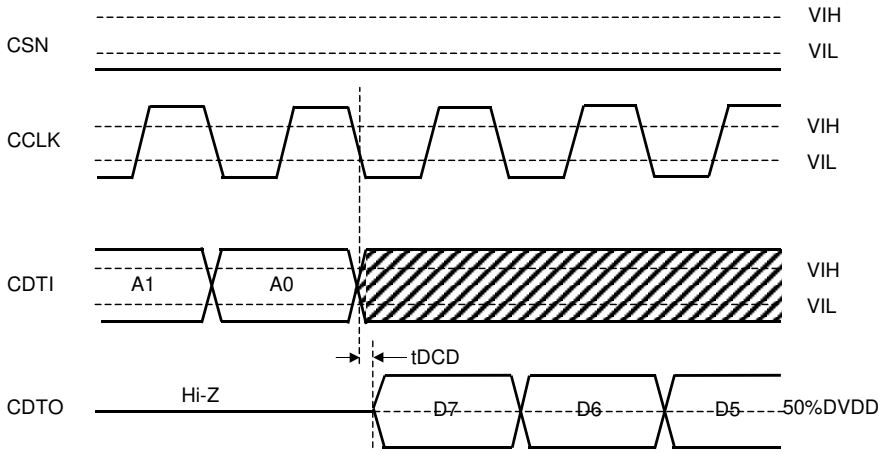



Figure 6. READ Data Output Timing 1 in 4-wire serial mode

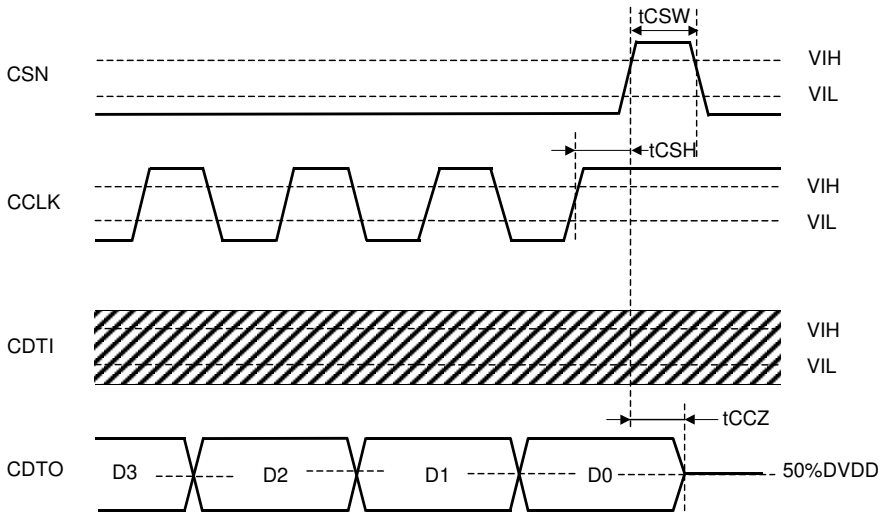



Figure 7. READ Data Input Timing 2 in 4-wire serial mode

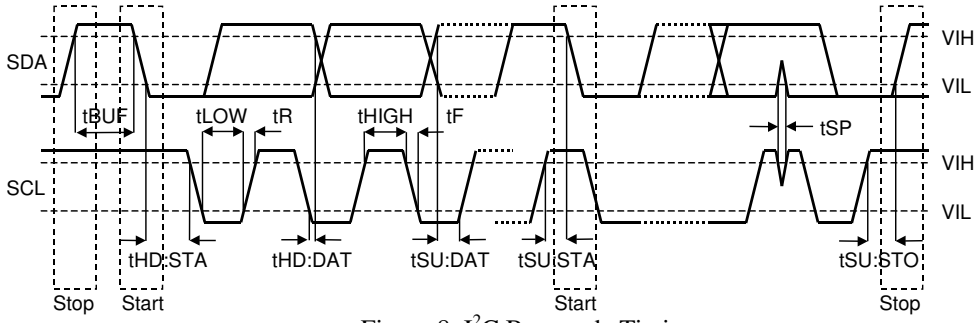



Figure 8. I$^2$C Bus mode Timing

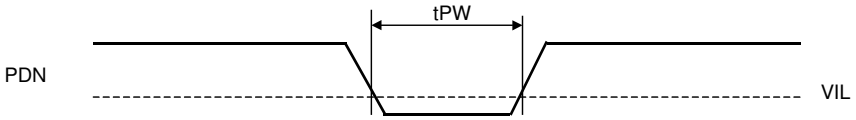



Figure 9. Power Down & Reset Timing

## OPERATION OVERVIEW

### ■ Non-PCM (AC-3, MPEG, etc.) and DTS-CD Bitstream Detection

The AK4118A has a Non-PCM steam auto-detection function. When the 32bit mode Non-PCM preamble based on Dolby "AC-3 Data Stream in IEC60958 Interface" is detected, the AUTO bit goes "1". The 96bit sync code consists of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872 and 0x4E1F. Detection of this pattern will set the AUTO bit "1". Once the AUTO is set "1", it will remain "1" until 4096 frames pass through the chip without additional sync pattern being detected. When those preambles are detected, the burst preambles Pc and Pd that follow those sync codes are stored to registers. The AK4118A also has the DTS-CD bitstream auto-detection function. When AK4118A detects DTS-CD bitstreams, DTSCD bit goes to "1". When the next sync code does not come within 4096 flames, DTSCD bit goes to "0" until when AK4118A detects the stream again. The AK4118A detects 14bit Sync Word and 16bit Sync Word of DTS-CD bitstream. In Serial control mode this detect function can be ON/OFF by DTS14 bit and DTS16 bit.

### ■ 192kHz Clock Recovery

The integrated low jitter PLL has a wide lock range from 8kHz to 192kHz and the lock time is dependent on the sampling frequency and FAST bit setting (Table 1). FAST bit is useful at lower sampling frequency and is fixed to "1" in parallel control mode. In serial control mode, the AK4118A has a sampling frequency detection function (8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz, 176.4kHz, 192kHz) that uses either a clock comparison against the X'tal oscillator or the channel status information from the setting of XTL1-0 bits. In parallel control mode, the sampling frequency is detected by using the reference frequency, 24.576MHz. When the sampling frequency is more than 64kHz, the FS96 pin goes to "H". When the sampling frequency is less than 54kHz, the FS96 pin goes to "L". The PLL loses lock when the received sync interval is incorrect.

| FAST bit | PLL Lock Time | |
|---|---|---|
| 0 | ≤ (15 ms + 384/fs) | (default) |
| 1 | ≤ (15 ms + 1/fs) | |

Table 1. PLL Lock Time (fs: Sampling Frequency)

### ■ Master Clock

The AK4118A has two clock outputs, MCKO1 and MCKO2. The MCKO2 pin output mode is selected by XMCK bit.

1) XMCK bit = "0"

The AK4118A has two clock outputs, MCKO1 and MCKO2. These clocks are derived from either the recovered clock or from the X'tal oscillator. The frequencies of the master clock outputs (MCKO1 and MCKO2) are set by OCKS0 and OCKS1 as shown in Table 2. The 512fs clock will not output when 96kHz and 192kHz. The 256fs clock will not output when 192kHz. The MCKO2 pin outputs "L" when PLL is the clock source.

| No. | OCKS1 | OCKS0 | MCKO1 | MCKO2 | X'tal | fs (max) | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 256fs | "L" | 256fs | 96 kHz | (default) |
| 1 | 0 | 1 | 256fs | "L" | 256fs | 96 kHz | |
| 2 | 1 | 0 | 512fs | "L" | 512fs | 48 kHz | |
| 3 | 1 | 1 | 128fs | "L" | 128fs | 192 kHz | |

When CM1-0 bits = "00" or "10" and UNLOCK bit= "0"

Table 2. Master Clock Frequency Select (Stereo mode)

When X'tal signal is the clock source, the clock can be output from the MCKO1 and MCKo2 pins. (Table 3)

| No. | OCKS1 | OCKS0 | MCKO1 | MCKO2 | X'tal | fs (max) | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 256fs | 256fs | 256fs | 96 kHz | (default) |
| 1 | 0 | 1 | 256fs | 128fs | 256fs | 96 kHz | |
| 2 | 1 | 0 | 512fs | 256fs | 512fs | 48 kHz | |
| 3 | 1 | 1 | 128fs | 64fs | 128fs | 192 kHz | |

When CM1-0 bits = "01", "11" or "10" and UNLOCK bit= "1"

Table 3. Master Clock Frequency Select (Stereo mode)

2) XMCK bit = "1"

The MCKO2 pin outputs the input clock of the XTI pin regardless of OCKS1-0 bit settings. DIV bit can set the output frequency. The MCKO1 pin outputs the clock according to the CM1-0 and OCKS1-0 bit settings.

| XMCK bit | DIV bit | MCKO2 Clock Source | MCKO2 Frequency |
|---|---|---|---|
| 1 | 0 | X'tal | x 1 |
| 1 | 1 | X'tal | x 1/2 |

Table 4. MCKO2 pin Output Frequency Setting

## ■ Clock Operation Mode

The CM0/CM1 pins (or bits) select the clock source and the data source of SDTO. In Mode 2, the clock source is switched from PLL to X'tal when PLL goes unlock state. In Mode3, the clock source is fixed to X'tal, but PLL is also operating and the recovered data such as C bits can be monitored. For Mode2 and Mode3, it is recommended that the frequency of X'tal is different from the recovered frequency from PLL.

| Mode | CM1 | CM0 | UNLOCK | PLL | X'tal | Clock source | MCKO1 | MCKO2 | SDTO | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | - | ON | ON(Note) | PLL | PLL | "L" | RX | (default) |
| 1 | 0 | 1 | - | OFF | ON | X'tal | X'tal | X'tal | DAUX | |
| 2 | 1 | 0 | 0 | ON | ON | PLL | PLL | "L" | RX | |
| | | | 1 | ON | ON | X'tal | X'tal | X'tal | DAUX | |
| 3 | 1 | 1 | - | ON | ON | X'tal | X'tal | X'tal | DAUX | |

ON: Oscillation (Power-up), OFF: STOP (Power-Down)

Note: When the X'tal is not used as clock comparison for fs detection (i.e. XTL1/0 pins= "H"), the X'tal is off.
When the clock source is PLL in Mode 0 and Mode 2, the MCKO2 pin is fixed to "L".

Table 5. Clock Operation Mode select

## ■ Clock Source

The clock for the XTI pin can be generated by the following methods:

1) X'tal

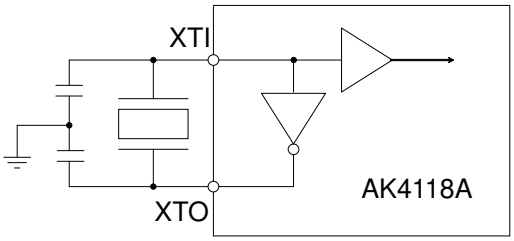



Figure 10. X'tal Mode
Note: External capacitance depends on the crystal oscillator (Max. 30pF)

2) External clock

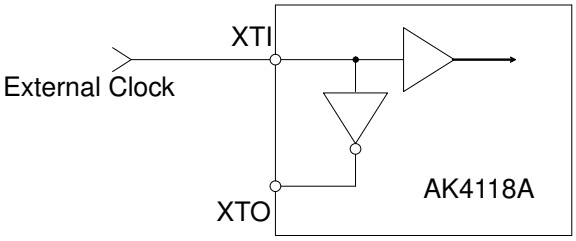



Figure 11. External clock mode
Note: Input clock must not exceed DVDD.

3) Fixed to the Clock Operation Mode 0

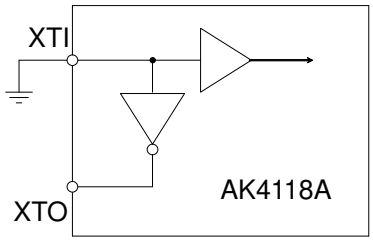



Figure 12. OFF Mode

## ■ Sampling Frequency and Pre-emphasis Detection

The AK4118A has two methods for detecting the sampling frequency as follows.

1. Clock comparison between recovered clock and X'tal oscillator
2. Sampling frequency information on channel status

Those could be selected by XTL1/0 pins. And the detected frequency is reported on FS3-0 and PEM bits.

| XTL1 | XTL0 | X'tal Frequency | |
|---|---|---|---|
| L | L | 11.2896MHz | (default) |
| L | H | 12.288MHz | |
| H | L | 24.576MHz | |
| H | H | (Use channel status) | |

Table 6. Reference X'tal frequency

| Register output | | | | fs | XTL1-0 bit ≠ "11" | XTL1-0 bit = "11" | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | Clock comparison (Note 11) | Consumer mode (Note 12) | Professional mode (Note 13) | |
| FS3 | FS2 | FS1 | FS0 | | | Byte3 Bit3,2,1,0 | Byte0 Bit7,6 | Byte4 Bit6,5,4,3 |
| 0 | 0 | 0 | 0 | 44.1kHz | 44.1kHz ± 3% | 0 0 0 0 | 0 1 | 0 0 0 0 |
| 0 | 0 | 0 | 1 | Reserved | - | 0 0 0 1 | (Others) | |
| 0 | 0 | 1 | 0 | 48kHz | 48kHz ± 3% | 0 0 1 0 | 1 0 | 0 0 0 0 |
| 0 | 0 | 1 | 1 | 32kHz | 32kHz ± 3% | 0 0 1 1 | 1 1 | 0 0 0 0 |
| 0 | 1 | 0 | 0 | 22.05kHz | 22.05kHz ± 3% | 0 1 0 0 | 0 0 | 1 0 0 1 |
| 0 | 1 | 0 | 1 | 11.025kHz | 11.025kHz ± 3% | | | |
| 0 | 1 | 1 | 0 | 24kHz | 24kHz ± 3% | 0 1 1 0 | 0 0 | 0 0 0 1 |
| 0 | 1 | 1 | 1 | 16kHz | 16kHz ± 3% | | | |
| 1 | 0 | 0 | 0 | 88.2kHz | 88.2kHz ± 3% | 1 0 0 0 | 0 0 | 1 0 1 0 |
| 1 | 0 | 0 | 1 | 8kHz | 8kHz ± 3% | | | |
| 1 | 0 | 1 | 0 | 96kHz | 96kHz ± 3% | 1 0 1 0 | 0 0 | 0 0 1 0 |
| 1 | 0 | 1 | 1 | 64kHz | 64kHz ± 3% | | | |
| 1 | 1 | 0 | 0 | 176.4kHz | 176.4kHz ± 3% | 1 1 0 0 | 0 0 | 1 0 1 1 |
| 1 | 1 | 1 | 0 | 192kHz | 192kHz ± 3% | 1 1 1 0 | 0 0 | 0 0 1 1 |

Note 11. At least ±3% frequency range is identified as the values in the Table 7. FS3-0 bits indicate nearer frequency for the intermediate frequency of two values. When the frequency is over the range of 32kHz to 192kHz, FS3-0 bits may indicate "0001".

Note 12. When consumer mode, Byte3 Bit3-0 are copied to FS3-0.

Note 13. In professional mode, FS3-0 bits are always "0001" except for the frequencies listed in the table.

Table 7. Sampling Frequency Information

The pre-emphasis information is detected and reported on PEM bit. This information is extracted from channel 1 at default. It can be switched to channel 2 by CS12 bit in control register.

| PEM | Pre-emphasis | Byte 0, Bits 3-5 |
|---|---|---|
| 0 | OFF | ≠ 0X100 |
| 1 | ON | 0X100 |

Table 8. PEM in Consumer Mode

| PEM | Pre-emphasis | Byte 0, Bits 2-4 |
|---|---|---|
| 0 | OFF | ≠110 |
| 1 | ON | 110 |

Table 9. PEM in Professional Mode

## ■ De-emphasis Filter Control

The AK4118A has a digital de-emphasis filter (tc=50/15μs) which corresponds to four sampling frequencies (32kHz, 44.1kHz, 48kHz and 96kHz) by IIR filter. When DEAU bit="1", the de-emphasis filter is enabled automatically by sampling frequency and pre-emphasis information in the channel status. The AK4118A is in this mode as default. Therefore, in Parallel Mode, the AK4118A is always placed in this mode and the status bits in channel 1 control the de-emphasis filter. In Serial Mode, DEM0/1 and DFS bits can control the de-emphasis filter when DEAU bit is "0". The internal de-emphasis filter is bypassed and the recovered data is output without any change if either pre-emphasis or de-emphasis Mode is OFF.

| PEM | FS3 | FS2 | FS1 | FS0 | Mode |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 44.1kHz |
| 1 | 0 | 0 | 1 | 0 | 48kHz |
| 1 | 0 | 0 | 1 | 1 | 32kHz |
| 1 | 1 | 0 | 1 | 0 | 96kHz |
| 1 | (Others) | | | | OFF |
| 0 | x | x | x | x | OFF |

Table 10. De-emphasis Auto Control at DEAU = "1" (default)

| PEM | DFS | DEM1 | DEM0 | Mode | |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 44.1kHz | |
| 1 | 0 | 0 | 1 | OFF | (default) |
| 1 | 0 | 1 | 0 | 48kHz | |
| 1 | 0 | 1 | 1 | 32kHz | |
| 1 | 1 | 0 | 0 | OFF | |
| 1 | 1 | 0 | 1 | OFF | |
| 1 | 1 | 1 | 0 | 96kHz | |
| 1 | 1 | 1 | 1 | OFF | |
| 0 | x | x | x | OFF | |

Table 11. De-emphasis Manual Control at DEAU = "0"

## ■ System Reset and Power-Down

The AK4118A has a power-down mode for all circuits by the PDN pin, and can be partially powerd-down by PWN bit. The RSTN bit initializes the register and resets the internal timing. In Parallel Mode, only the control by the PDN pin is enabled. The AK4118A should be reset once by bringing the PDN pin = "L" upon power-up.

PDN Pin:

All analog and digital circuit are placed in the power-down and reset mode by bringing the PDN pin= "L". All the registers are initialized, and clocks are stopped. Reading/Witting to the register are disabled.

RSTN Bit (Address 00H; D0):

All the registers except PWN and RSTN are initialized by bringing RSTN bit = "0". The internal timings are also initialized. Writing to the register is not available except PWN and RSTN bits. Reading to the register is disabled.

PWN Bit (Address 00H; D1):

The clock recovery part is initialized by bringing PWN bit = "0". In this case, clocks are stopped. The registers are not initialized and the mode settings are kept. Writing and Reading to the registers are enabled.

## ■ Biphase Input and Through Output

Eight receiver inputs (RX0-7) are available in Serial Control Mode. Each input includes amplifier corresponding to unbalance mode and can accept the signal of 200mV or more. IPS2-0 selects the receiver channel. When BCUV bit = "1", the Block start signal, C bit and U bit can output from each pins. RXDE7-0 bits indicate the input signal status at the RX pin. When the signal is input to the RX pin, RXDE bit = "1".

| IPS2 | IPS1 | IPS0 | INPUT Data | |
|---|---|---|---|---|
| 0 | 0 | 0 | RX0 | (default) |
| 0 | 0 | 1 | RX1 | |
| 0 | 1 | 0 | RX2 | |
| 0 | 1 | 1 | RX3 | |
| 1 | 0 | 0 | RX4 | |
| 1 | 0 | 1 | RX5 | |
| 1 | 1 | 0 | RX6 | |
| 1 | 1 | 1 | RX7 | |

Table 12. Recovery Data Select

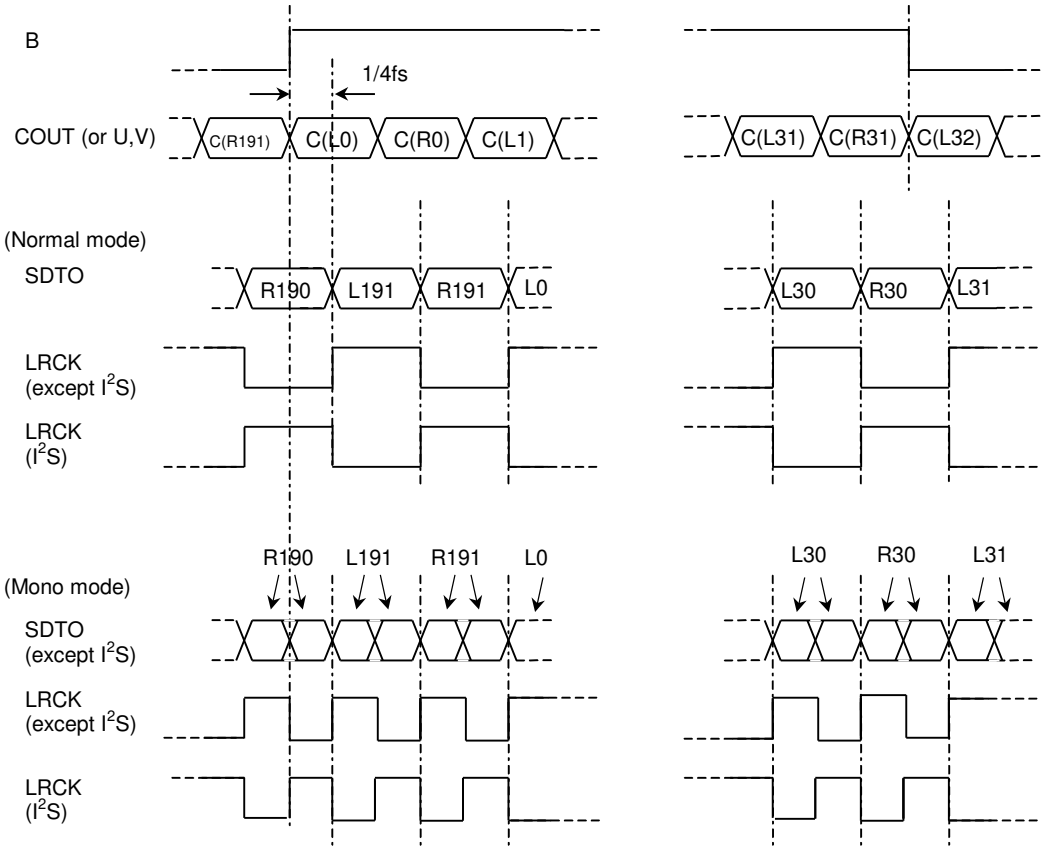



Figure 13. B, C, U, V output timings

## ■ Biphase Output

The AK4118A outputs the data either through output (from DIR) or transmitted output (DIT; the data from DAUX is transformed to IEC60958 format.) from TX1/0 pins. It is selected by DIT bit. The source of the data through output from the TX0 pin is selected among RX0-8 by OPS00, 01 and 02 bits, and selected by OPS10, 11 and 12 bits for the TX1 pin respectively. When the AK4118A outputs DAUX data, V bit is controlled by the VIN pin and first 5 bytes of C bit can be controlled by CT39-CT0 bits in control registers (Figure 14). When bit0= "0"(consumer mode), bit20-23(Audio channel) can not be controlled directly but can be controlled by CT20 bit. When the CT20 bit is "1", the AK4118A outputs "1000" at C20-23 for sub frame 1(left channel) and output "0100" at C20-23 for sub frame 2 (right channel) automatically. When CT20 bit is "0", the AK4118A outputs "0000". U bits are controlled by UDIT bit as follows; When UDIT bit is "0", U bits are always "0". When UDIT bit is "1", the recovered U bits are used for DIT( DIR-DIT loop mode of U bit). This mode is only available when PLL is locked in the master mode.

| OPS02 | OPS01 | OPS00 | Output Data | |
|---|---|---|---|---|
| 0 | 0 | 0 | RX0 | (default) |
| 0 | 0 | 1 | RX1 | |
| 0 | 1 | 0 | RX2 | |
| 0 | 1 | 1 | RX3 | |
| 1 | 0 | 0 | RX4 | |
| 1 | 0 | 1 | RX5 | |
| 1 | 1 | 0 | RX6 | |
| 1 | 1 | 1 | RX7 | |

Table 13. Output Data Select for TX0

| DIT | OPS12 | OPS11 | OPS10 | Output Data | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | RX0 | |
| 0 | 0 | 0 | 1 | RX1 | |
| 0 | 0 | 1 | 0 | RX2 | |
| 0 | 0 | 1 | 1 | RX3 | |
| 0 | 1 | 0 | 0 | RX4 | |
| 0 | 1 | 0 | 1 | RX5 | |
| 0 | 1 | 1 | 0 | RX6 | |
| 0 | 1 | 1 | 1 | RX7 | |
| 1 | x | x | x | DAUX | (default) |

(x: Don't care)

Table 14. Output Data Select for TX1

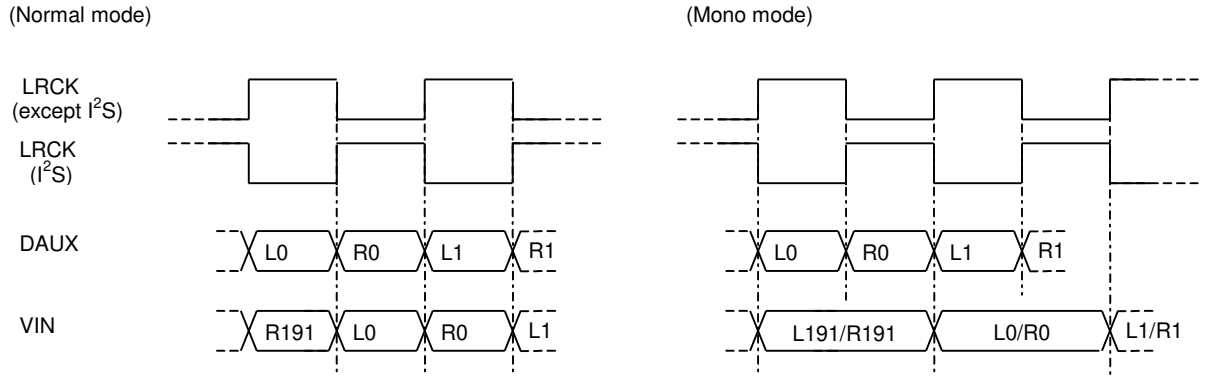



Figure 14. DAUX and VIN input timings

## ■ Double Sampling Frequency Mode

When MONO bit = "1", the AK4118A outputs data in double speed according to "Single channel double sampling frequency mode" of AES3. For example, when 192kHz mono data is transmitted or received, L/R channels of 96kHz biphase data are used. In this case, one frame is 96kHz and LRCK frequency is 192kHz.

1) RX

When MONO bit = "1", the AK4118A outputs mono data from SDTO as follows.

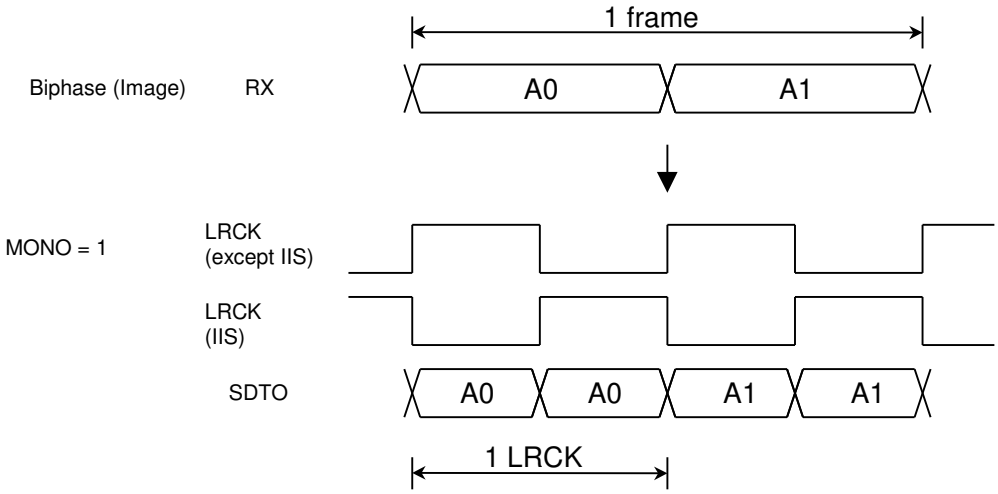



Figure 15. MONO Mode (RX)

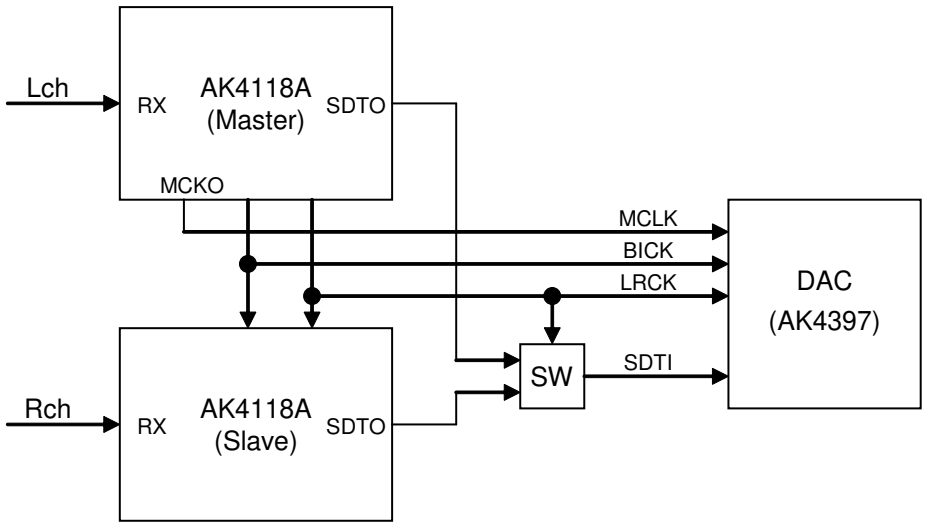



Figure 16. MONO mode Connection Example (RX)

2) TX

When MONO bit = "1" and TLR bit = "0", the AK4118A outputs Lch data through TX1 as biphase signal. When MONO bit = "1" and TLR bit = "1", then Rch data is output.

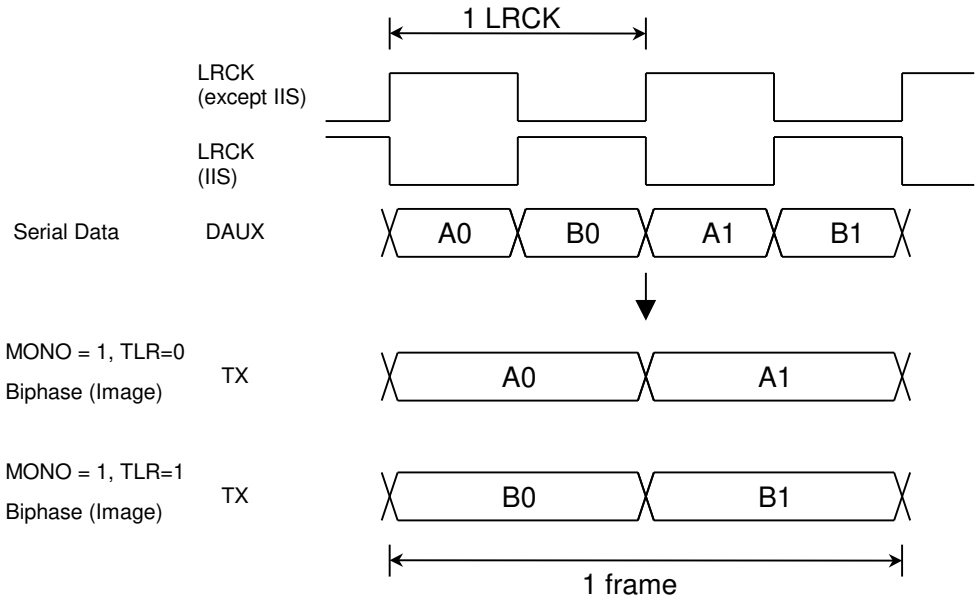



Figure 17. MONO Mode (TX)

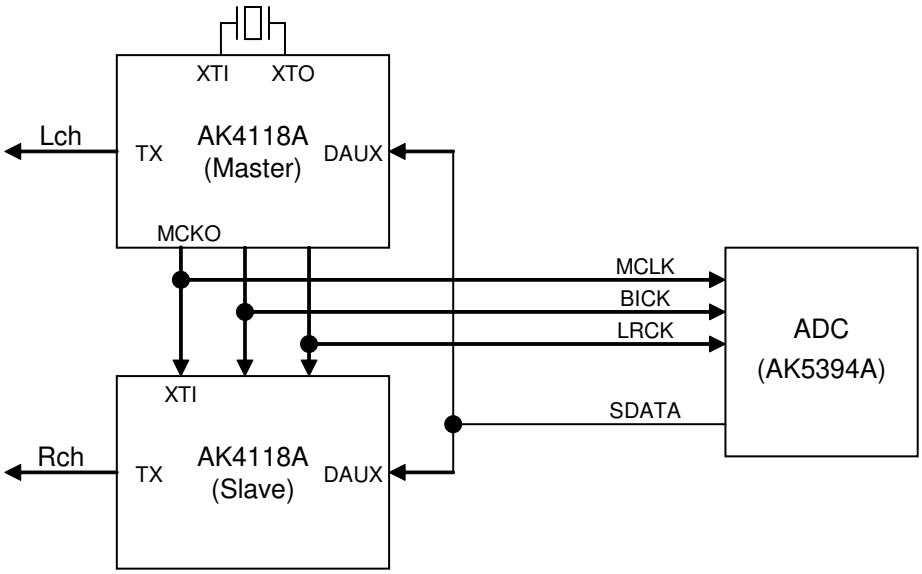
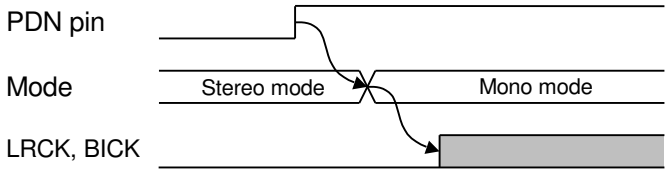


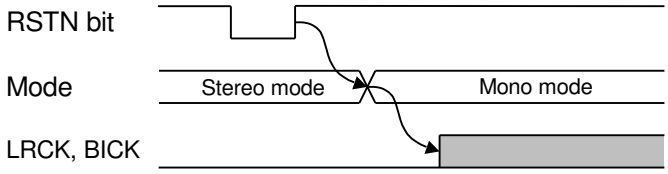

Figure 18. MONO Mode Connection Example (TX)

Note: In case of the connection example (Figure 18) or when more than one AK4118A's are used, LRCK and BICK should be input after reset so that the phase of TX outputs is aligned. The AK4118A's should be set by following sequence (Figure 19).

When Powered ON




During Operation




(1) Reset all the AK4118A's by the PDN pin = "L" → "H" or RSTN bit = "0" → "1".
(2) Set all the AK4118A's to MONO mode while they are still in slave mode.
(3) Set one of the AK4118A to master mode so that LRCK is input to all other AK4118A's at the same time, or Input LRCK externally to all the AK4118A's at the same time.

Figure 19. MONO Mode Setup Sequence (TX)

## ■ Biphase Signal Input/Output Circuit

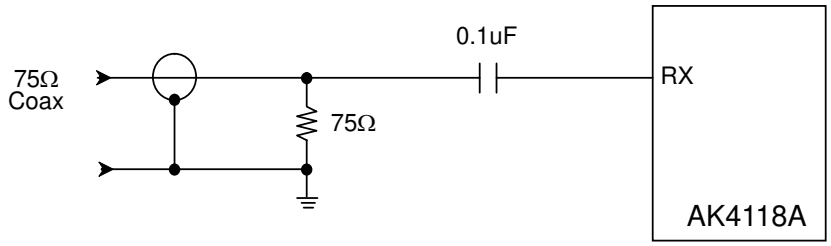



Figure 20. Consumer Input Circuit (Coaxial Input)

Note: In case of coaxial input, if a coupling level to this input from the next RX input line pattern exceeds 50mV, there is a possibility to occur an incorrect operation is occured. In this case, it is possible to lower the coupling level by adding this decoupling capacitor.

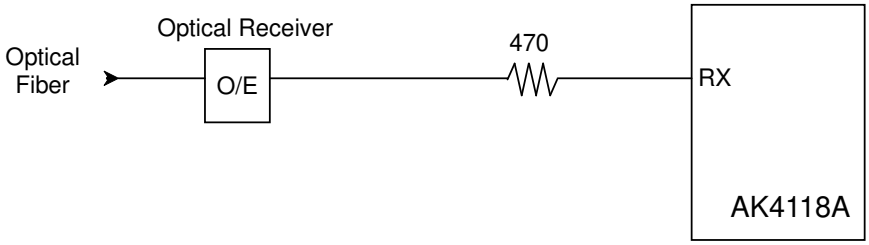
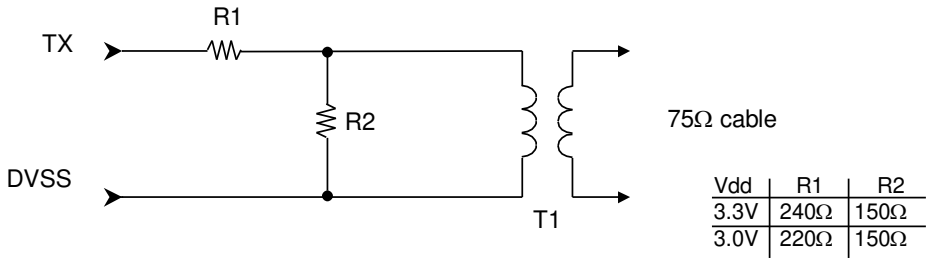



Figure 21. Consumer Input Circuit (Optical Input)

For coaxial input, as the input level of RX line is small in Serial Mode, cross-talking among RX input lines have to be avoided. For example, inserting the shield pattern among them is effective. In Parallel Mode, four channel inputs (RX0/1/2/3) are available and RX4-7 change to other pins for audio format control. Those pins must be fixed to "H" or "L".

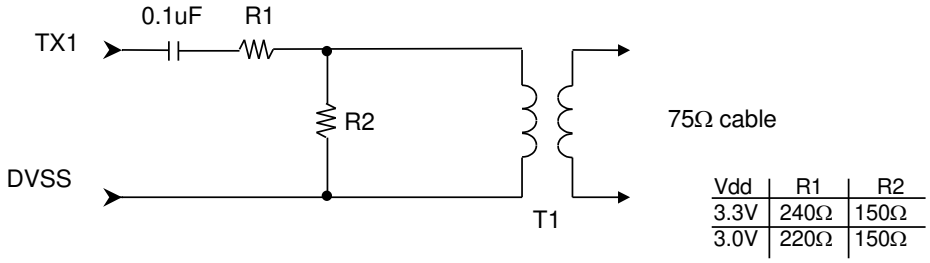
The AK4118A includes the TX output buffer. The output level meets 0.5V+/-20% using the external resistors. The T1 in the Figure 22 is a transformer of 1:1.




| Vdd | R1 | R2 |
|---|---|---|
| 3.3V | 240Ω | 150Ω |
| 3.0V | 220Ω | 150Ω |

Figure 22. TX External Resistor Network

Note: When the AK4118A is in the power-down mode (PDN pin= "L"), power supply current can be suppressed by using AC couple capacitor as following figure since the TX1 pin output becomes uncertain at power-down mode.




| Vdd | R1 | R2 |
|---|---|---|
| 3.3V | 240Ω | 150Ω |
| 3.0V | 220Ω | 150Ω |