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AK4122A
24-Bit 96kHz SRC with DIR

GENERAL DESCRIPTION

The AK4122A is a digital sample rate converter (SRC) with the digital audio receiver (DIR). The input sample rate ranges from 8kHz to 96kHz. The output sample rate is 32kHz, 44.1kHz, 48kHz or 96kHz. By using the AK4122A, the system can take very simple configuration because the AK4122A has an internal PLL and does not need any master clock at slave mode. Then the AK4122A is suitable for the application interfacing to different sample rates like Car Audio, DVD recorder, etc.

FEATURES

1. SRC
- **Asynchronous Sample Rate Converter**
- **Input Sample Rate Range (fsi) : 8kHz ~ 96kHz**
- **Output Sample Rate (fso) : 32kHz, 44.1kHz, 48kHz, 96kHz**
- **Input to Output Sample Rate Ratio : 0.33 to 6**
- **THD+N : –113dB**
- **I/F format : MSB justified, LSB justified (16/24bit) and I^2S compatible**
- **Clock for Master mode : 256/384/512/768fs**
- **SRC Bypass mode**
- **Soft Mute Function**

2. DIR
- **4-Channel Inputs Selector & 1-Channel Through Output**
- **AES3, IEC60958, S/PDIF, EIAJ CP1201 Compatible**
- **Low Jitter Analog PLL**
- **PLL Lock Range : 32kHz ~ 96kHz**
- **Auto detection**
  - **Non-PCM Bit Stream**
  - **DTS-CD Bit Stream**
  - **Validity Flag**
  - **Sampling Frequency (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz)**
  - **Unlock & Parity Error**
  - **DAT Start ID**
- **40-bit Channel Status Buffer**
- **Burst Preamble bit Pc, Pd Buffer for Non-PCM bit streams**
- **Q-subcode Buffer for CD bit streams**

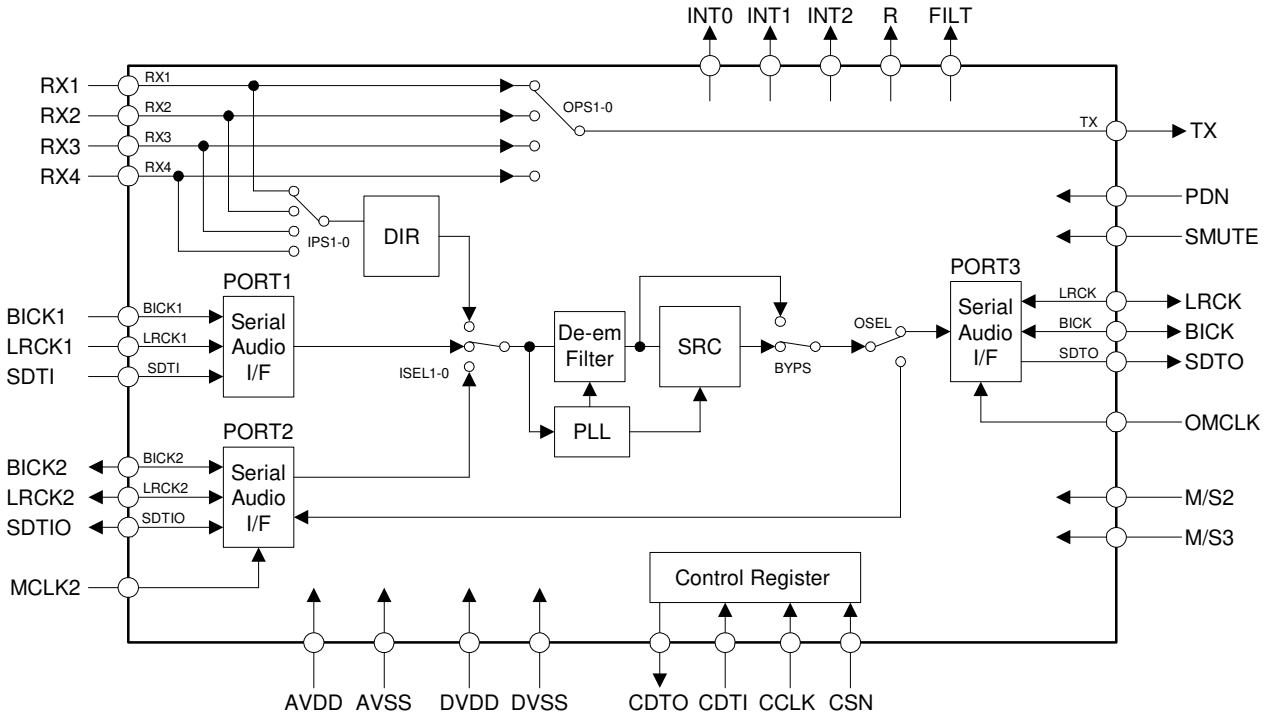
3. 4-wire Serial μP Interface

4. Power Supply
- **AVDD: 3.0 ~ 3.6V (typ. 3.3V)**
- **DVDD: 3.0 ~ 3.6V (typ. 3.3V)**

5. Ta = –10 ~ 70°C

6. Package : 48pin LQFP

■ Block Diagram

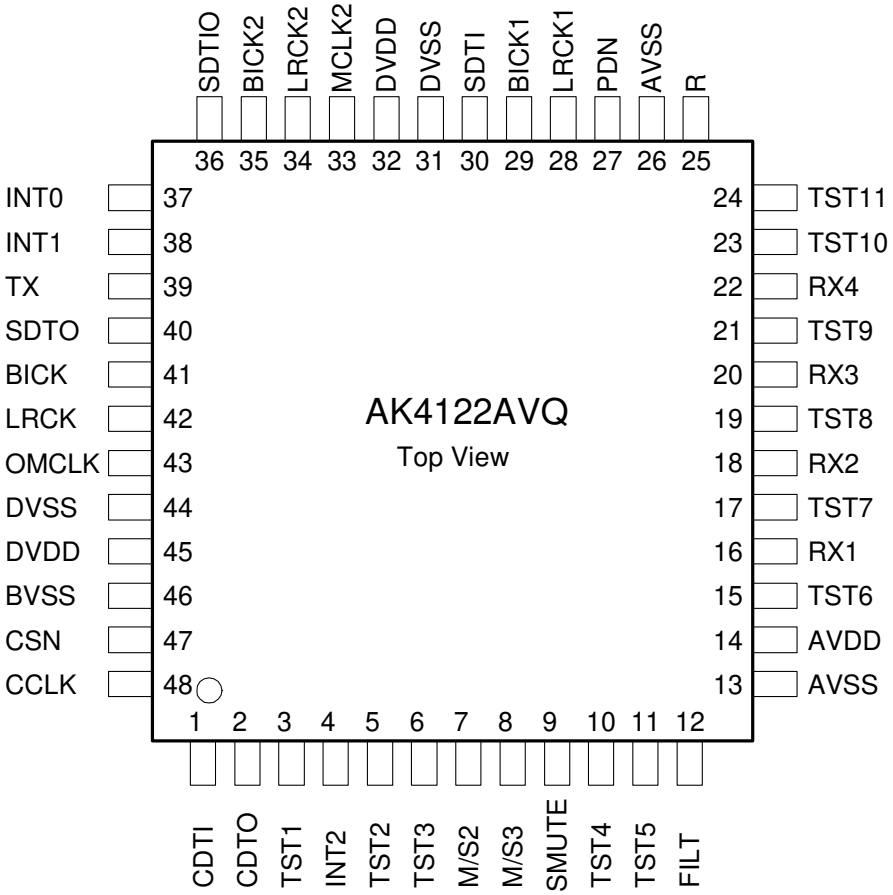


Block diagram

■ Ordering Guide

AK4122AVQ	−10 ~ +70°C	48pin LQFP (0.5mm pitch)
AKD4122A	Evaluation Board for AK4122A	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	CDTI	I	Control Data Input Pin
2	CDTO	O	Control Data Output Pin
3	TST1	O	Test 1 Pin
4	INT2	O	Interrupt 2 Pin
5	TST2	O	Test 2 Pin
6	TST3	I	Test 3 Pin This pin should be connected to DVSS.
7	M/S2	I	Master / Slave Mode Pin for PORT2 "H" : Master mode, "L" : Slave Mode
8	M/S3	I	Master / Slave Mode Pin for PORT3 "H" : Master mode, "L" : Slave Mode
9	SMUTE	I	Soft Mute Pin "H" : Soft Mute, "L" : Normal Operation
10	TST4	I	Test 4 Pin This pin should be connected to AVSS.
11	TST5	I	Test 5 Pin This pin should be connected to AVSS.
12	FILT	O	PLL Loop Filter Pin 470Ω±5% resistor and 2.2μF±50% ceramic capacitor in parallel with a 2.2nF±50% ceramic capacitor should be connected to AVSS externally.
13	AVSS	-	Analog Ground Pin
14	AVDD	-	Analog Power Supply Pin, 3.0 ~ 3.6V
15	TST6	I	Test 6 Pin This pin should be connected to AVSS.
16	RX1	I	Receiver Input 1 Pin with Amp for 0.2Vpp (Internal Biased Pin)
17	TST7	I	Test 7 Pin This pin should be connected to AVSS.
18	RX2	I	Receiver Input 2 Pin with Amp for 0.2Vpp (Internal Biased Pin)
19	TST8	I	Test 8 Pin This pin should be connected to AVSS.
20	RX3	I	Receiver Input 3 Pin with Amp for 0.2Vpp (Internal Biased Pin)
21	TST9	I	Test 9 Pin This pin should be connected to AVSS.
22	RX4	I	Receiver Input 4 Pin with Amp for 0.2Vpp (Internal Biased Pin)
23	TST10	I	Test 10 Pin This pin should be connected to AVSS.
24	TST11	O	Test 11 Pin

Note: All input pins except internal biased pins should not be left floating.

25	R	-	External Resistor Pin 12kΩ±5% resistor should be connected to AVSS externally.
26	AVSS	-	Analog Ground Pin
27	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initializes the control register.
28	LRCK1	I	Input Channel Clock Pin
29	BICK1	I	Audio Serial Data Clock Pin
30	SDTI	I	Audio Serial Data Input Pin
31	DVSS	-	Digital Ground Pin
32	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V
33	MCLK2	I	Master Clock Input Pin
34	LRCK2	I/O	Input / Output Channel Clock Pin
35	BICK2	I/O	Audio Serial Data Clock Pin
36	SDTIO	I/O	Audio Serial Data Input / Output Pin
37	INT0	O	Interrupt 0 Pin
38	INT1	O	Interrupt 1 Pin
39	TX	O	Transmitter Output Pin
40	SDTO	O	Audio Serial Data Output Pin
41	BICK	I/O	Audio Serial Data Clock Pin
42	LRCK	I/O	Output Channel Clock Pin
43	OMCLK	I	Master Clock Input Pin
44	DVSS	-	Digital Ground Pin
45	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V
46	BVSS	-	Substrate Ground Pin This pin should be connected to AVSS.
47	CSN	I	Chip Select Pin
48	CCLK	I	Control Data Clock Pin

Note: All input pins except internal biased pins should not be left floating.

■ Handling of Unused pins

The unused digital I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
PORT1	BICK1, LRCK1, SDTI	These pins should be connected to DVSS.
PORT2	MCLK2	This pin should be connected to DVSS.
	BICK2, LRCK2	These pins should be connected to DVSS in slave mode or open in master mode.
	SDTIO	This pin should be connected to DVSS.
	M/S2	This pin should be connected to DVDD or DVSS.
PORT3	OMCLK	This pin should be connected to DVSS.
	BICK, LRCK	These pins should be connected to DVSS in slave mode or open in master mode.
	SDTO	This pin should be open.
	M/S3	This pin should be connected to DVDD or DVSS.
DIR	RX1, RX2, RX3, RX4	These pins should be open.
	INT0, INT1, INT2, TX	These pins should be open.
Control PORT	CCLK, CDTI, CSN	These pins should be connected to DVSS.
	CDTO	This pin should be open.
Other	SMUTE	This pin should be connected to DVSS.
TEST	TST1, TST2, TST11	These pins should be open.
	TST3	This pin should be connected to DVSS.
	TST4, TST5, TST6, TST7, TST8, TST9, TST10	These pins should be connected to AVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS=BVSS=DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	|BVSS – DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage 1 (Except RX1-4 pins)		VIND1	–0.3	DVDD+0.3	V
Digital Input Voltage 2 (RX1-4 pins)		VIND2	–0.3	AVDD+0.3	V
Ambient Temperature (Power applied)		Ta	–10	70	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, BVSS and DVSS must be connected to the same ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS=BVSS=DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 3)	Analog	AVDD	3.0	3.3	3.6	V
	Digital	DVDD	3.0	3.3	AVDD	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD and DVDD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

SRC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.3V; AVSS=BVSS=DVSS=0V; data = 24bit; measurement bandwidth = 20Hz ~ FSO/2; unless otherwise specified.)

Parameter	Symbol	min	typ	max	Units
SRC Characteristics:					
Resolution (Note 4)				24	Bits
Input Sample Rate	FSI	8		96	kHz
Output Sample Rate	FSO	32		96	kHz
THD+N (Input = 1kHz, 0dBFS, Note 5)					
FSO/FSI = 44.1kHz/48kHz		-	−113	-	dB
FSO/FSI = 48kHz/44.1kHz		-	−113	-	dB
FSO/FSI = 32kHz/48kHz		-	−114	-	dB
FSO/FSI = 96kHz/32kHz		-	−111	-	dB
Worst Case (FSO/FSI = 48kHz/8kHz)		-	-	−103	dB
Dynamic Range (Input = 1kHz, −60dBFS, Note 5)					
FSO/FSI = 44.1kHz/48kHz		-	114	-	dB
FSO/FSI = 48kHz/44.1kHz		-	115	-	dB
FSO/FSI = 32kHz/48kHz		-	115	-	dB
FSO/FSI = 96kHz/32kHz		-	116	-	dB
Worst Case (FSO/FSI = 32kHz/44.1kHz)		112	-	-	dB
Dynamic Range (Input = 1kHz, −60dBFS, A-weighted, Note 5)					
FSO/FSI = 44.1kHz/48kHz		-	117	-	dB
Ratio between Input and Output Sample Rate (Note 6)	FSO/FSI	0.33		6	-

Note 4. Input data for SRC corresponds to 24bit data. When LSB 4bit data is input, the AK4122A calculates the data as "0" because SRC is 20bit calculation. Therefore, SRC outputs "0" data.

Note 5. Measured by ROHDE & SCHWARZ UPD04, Rejection Filter = wide, 8192point FFT.

Note 6. The "0.33" is the ratio of FSO/FSI when FSI is 96kHz and FSO is 32kHz. The "6" is the ratio of FSO/FSI when FSI is 8kHz and FSO is 48kHz.

S/PDIF RECEIVER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
Input Resistance	Zin	-	10	-	kΩ
Input Voltage	VTH	200			mVpp
Input Sample Frequency	fs	32	-	96	kHz

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband –0.001dB	0.985 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	0.905 ≤ FSO/FSI < 0.985	PB	0		0.4167FSI	kHz
	0.714 ≤ FSO/FSI < 0.905	PB	0		0.3195FSI	kHz
	0.656 ≤ FSO/FSI < 0.714	PB	0		0.2852FSI	kHz
	0.536 ≤ FSO/FSI < 0.656	PB	0		0.2245FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0		0.2003FSI	kHz
	0.452 ≤ FSO/FSI < 0.492	PB	0		0.1781FSI	kHz
	0.333 ≤ FSO/FSI < 0.452	PB	0		0.1092FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
	0.905 ≤ FSO/FSI < 0.985	SB	0.5021FSI			kHz
	0.714 ≤ FSO/FSI < 0.905	SB	0.3965FSI			kHz
	0.656 ≤ FSO/FSI < 0.714	SB	0.3643FSI			kHz
	0.536 ≤ FSO/FSI < 0.656	SB	0.2974FSI			kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2732FSI			kHz
	0.452 ≤ FSO/FSI < 0.492	SB	0.2510FSI			kHz
	0.333 ≤ FSO/FSI < 0.452	SB	0.1822FSI			kHz
Passband Ripple		PR			±0.01	dB
Stopband Attenuation		SA	96			dB
Group Delay (Note 7)		GD	-	58.5	-	1/fs

Note 7. This value is the time from the rising edge of LRCK after data is input to rising edge of LRCK after data is output, when LRCK for Output data corresponds with LRCK for Input.

DC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=–400μA)	VOH	DVDD–0.4	-	-	V
Low-Level Output Voltage (Iout=400μA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

Parameter	min	typ	max	Units
Power Supply Current				
Normal operation (PDN pin = "H") (Note 8)				
FSI=FSO=48kHz at Slave Mode: AVDD=DVDD=3.3V		15	-	mA
FSI=FSO=96kHz at Master Mode: AVDD=DVDD=3.3V		29	-	mA
FSI=FSO=96kHz at Master Mode: AVDD=DVDD=3.6V		-	45	mA
Power down (PDN pin = "L") (Note 9)				
AVDD+DVDD		10	100	μA

Note 8. Typ and max values are the value of AVDD+DVDD in each power supply voltage.
Power supply current of each path@Slave Mode, AVDD=DVDD=3.3V, FSI=FSO=48kHz
1. PORT1 → SRC → PORT3: AVDD=5mA(typ), DVDD=10mA(typ)
2. PORT2 → SRC → PORT3: AVDD=5mA(typ), DVDD=10mA(typ)
3. DIR → SRC → PORT3: AVDD=6mA(typ), DVDD=9mA(typ)

Note 9. All digital input pins are held DVSS.

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Frequency	fCLK	8.192		36.864	MHz
Pulse Width Low	tCLKL	0.4/fCLK			ns
Pulse Width High	tCLKH	0.4/fCLK			ns
LRCK for Input data (LRCK1, LRCK2)					
Frequency	fs	8		96	kHz
Duty Cycle	Duty	48	50	52	%
LRCK for Output data (LRCK, LRCK2)					
Frequency (Note 10)	fs	32		96	kHz
Duty Cycle Slave Mode	Duty	48	50	52	%
Master Mode	Duty		50		%
S/PDIF Clock Recover Frequency	fPLL	32		96	kHz
Audio Interface Timing					
Input for PORT1					
BICK1 Period	tBCK	1/64fs			ns
BICK1 Pulse Width Low	tBCKL	65			ns
Pulse Width High	tBCKH	65			ns
LRCK1 Edge to BICK1 "↑" (Note 11)	tLRB	30			ns
BICK1 "↑" to LRCK1 Edge (Note 11)	tBLR	30			ns
SDTI Hold Time from BICK1 "↑"	tSDH	30			ns
SDTI Setup Time to BICK1 "↑"	tSDS	30			ns
Input for PORT2 (Slave mode)					
BICK2 Period	tBCK	1/64fs			ns
BICK2 Pulse Width Low	tBCKL	65			ns
Pulse Width High	tBCKH	65			ns
LRCK2 Edge to BICK2 "↑" (Note 11)	tLRB	30			ns
BICK2 "↑" to LRCK2 Edge (Note 11)	tBLR	30			ns
SDTIO Hold Time from BICK2 "↑"	tSDH	30			ns
SDTIO Setup Time to BICK2 "↑"	tSDS	30			ns
Output for PORT2 (Slave mode)					
BICK2 Period	tBCK	1/64fs			ns
BICK2 Pulse Width Low	tBCKL	65			ns
Pulse Width High	tBCKH	65			ns
LRCK2 Edge to BICK2 "↑" (Note 11)	tLRB	30			ns
BICK2 "↑" to LRCK2 Edge (Note 11)	tBLR	30			ns
LRCK2 to SDTIO (MSB) (Except I^2S mode)	tLRS			30	ns
BICK2 "↓" to SDTIO	tBSD			30	ns

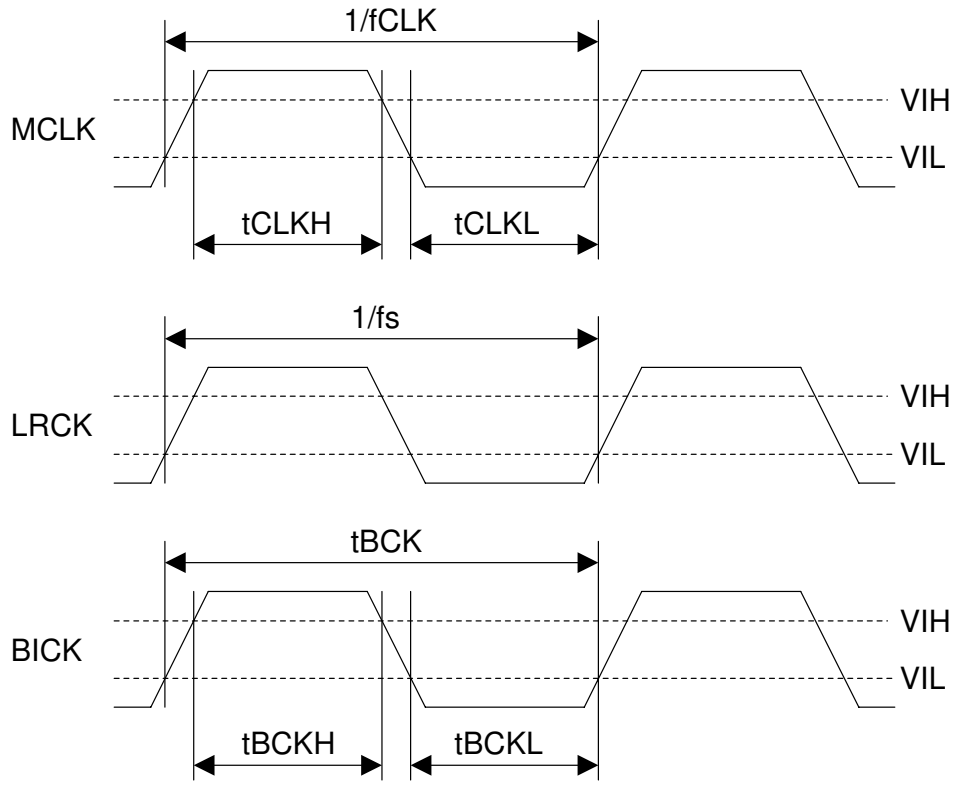
Note 10. Min value is 8kHz at BYPASS mode.

Note 11. BICK1 rising edge must not occur at the same time as LRCK1 edge.
BICK2 rising edge must not occur at the same time as LRCK2 edge.

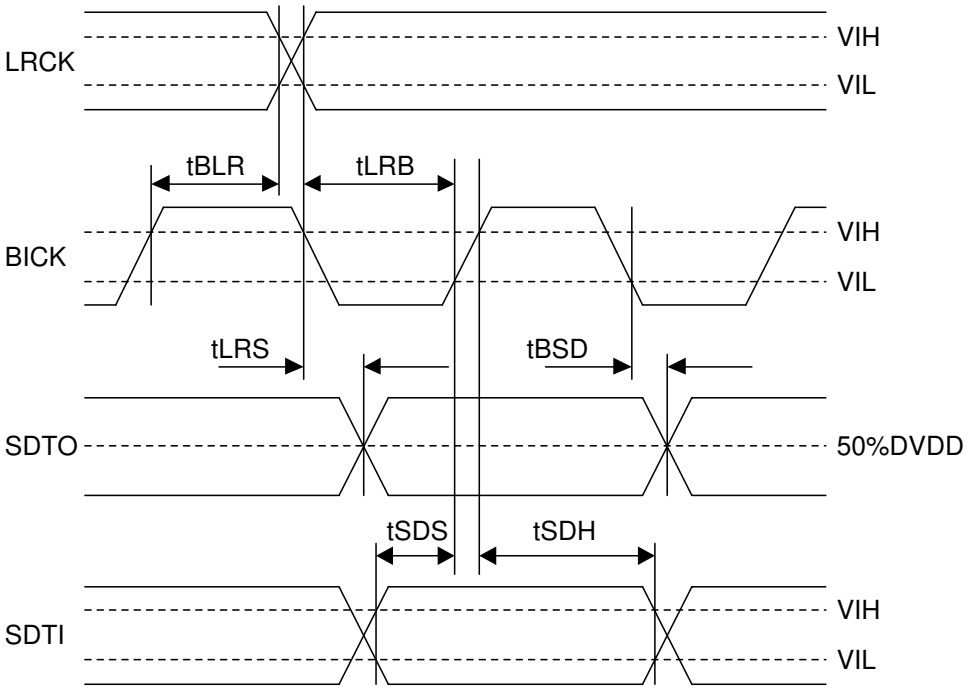
Parameter		Symbol	min	typ	max	Units
	Output for PORT3 (Slave mode)					
	BICK Period	tBCK	1/64fs			ns
	BICK Pulse Width Low	tBCKL	65			ns
	Pulse Width High	tBCKH	65			ns
	LRCK Edge to BICK "↑" (Note 11)	tLRB	30			ns
	BICK "↑" to LRCK Edge (Note 11)	tBLR	30			ns
	LRCK to SDTO (MSB) (Except I^2S mode)	tLRS			30	ns
	BICK "↓" to SDTO	tBSD			30	ns
	Output for PORT2 (Master mode)					
	BICK2 Frequency	fBCK		64fs		Hz
	BICK2 Duty	dBCK		50		%
	BICK2 "↓" to LRCK2	tMBLR	–20		20	ns
	BICK2 "↓" to SDTIO	tBSD	–20		30	ns
	Output for PORT3 (Master mode)					
	BICK Frequency	fBCK		64fs		Hz
	BICK Duty	dBCK		50		%
	BICK "↓" to LRCK	tMBLR	–20		20	ns
	BICK "↓" to SDTO	tBSD	–20		30	ns
Control Interface Timing						
	CCLK Period (Note 12)	tCCK	200		1000	ns
	CCLK Pulse Width Low	tCCKL	80			ns
	Pulse Width High	tCCKH	80			ns
	CDTI Setup Time	tCDS	40			ns
	CDTI Hold Time	tCDH	40			ns
	CSN "H" Time	tCSW	150			ns
	CSN "↓" to CCLK "↑"	tCSS	50			ns
	CCLK "↑" to CSN "↑"	tCSH	50			ns
	CDTO Delay	tDCD			45	ns
	CSN "↑" to CDTO Hi-Z	tCCZ			70	ns
Reset Timing						
	PDN Pulse Width (Note 13)	tPD	150			ns

Note 11. BICK rising edge must not occur at the same time as LRCK edge.
Note 12. In case of using INT2. When INT2 is not used, the max value is not limited.
Note 13. The AK4122A can be reset by bringing the PDN pin = "L".

■ Timing Diagram

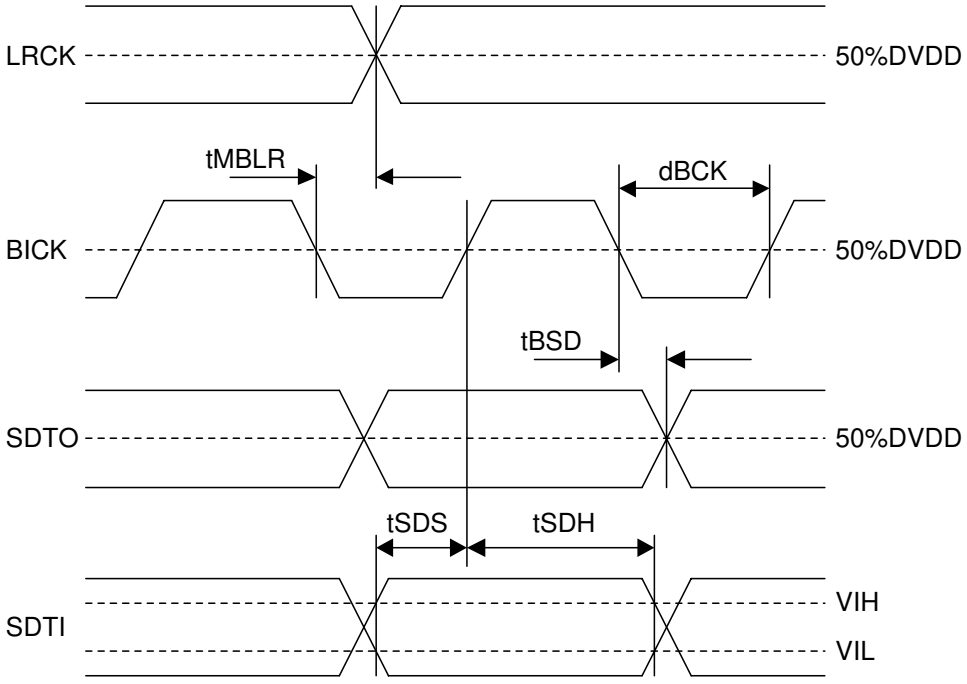


Clock Timing



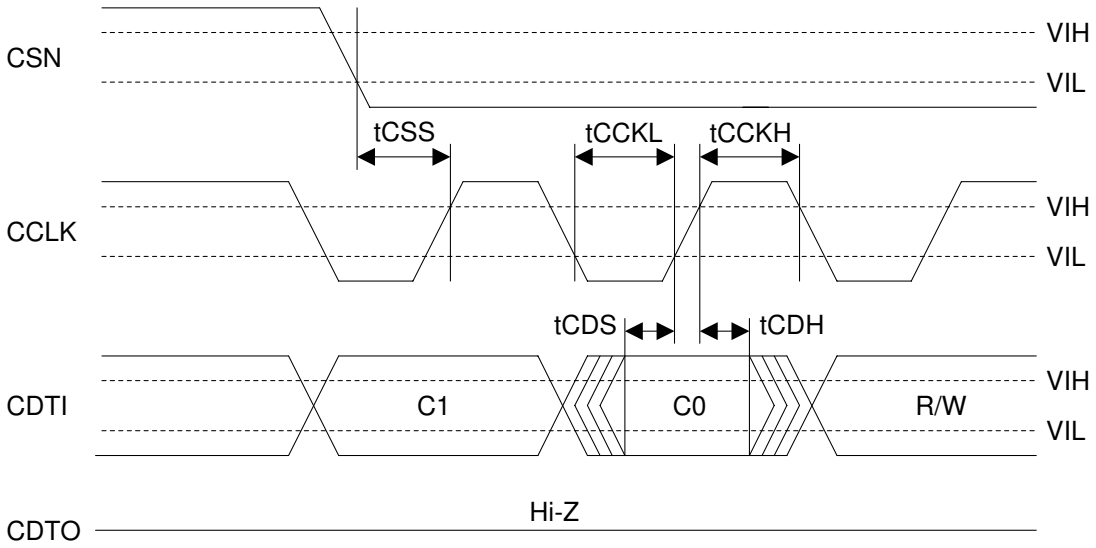
Audio Interface Timing (Slave mode)

Note : BICK shows BICK1 of PORT1, BICK2 of PORT2 and BICK of PORT3. LRCK shows LRCK1 of PORT1, LRCK2 of PORT2 and LRCK of PORT3. SDTI shows SDTI of PORT1 or SDTIO of PORT2 that is used as input port. SDTO shows SDTO of PORT3 or SDTIO of PORT2 that is used as output port.

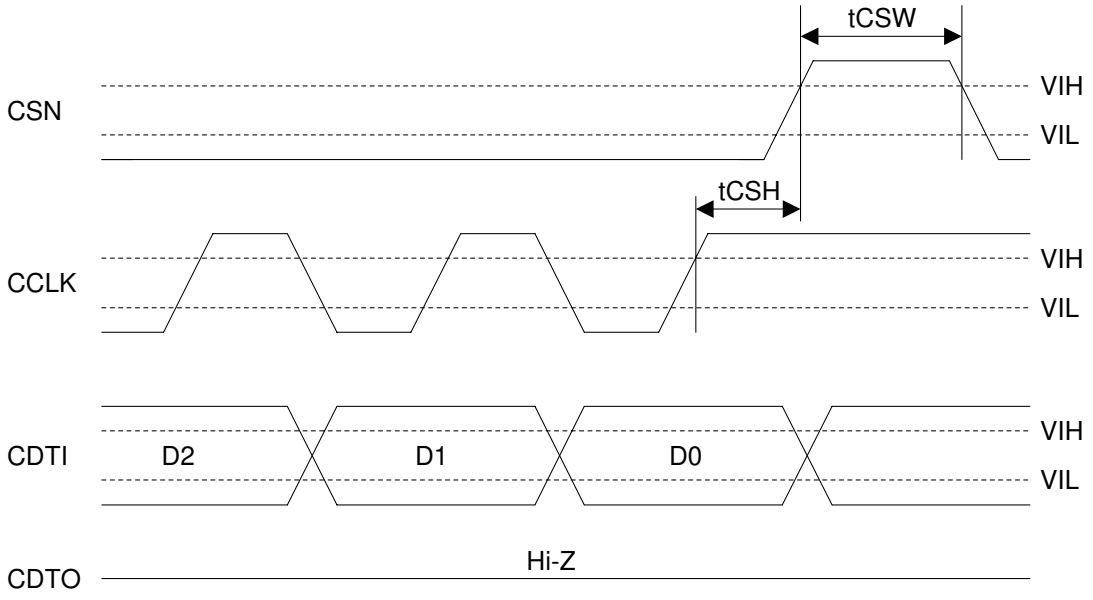


Audio Interface Timing (Master mode)

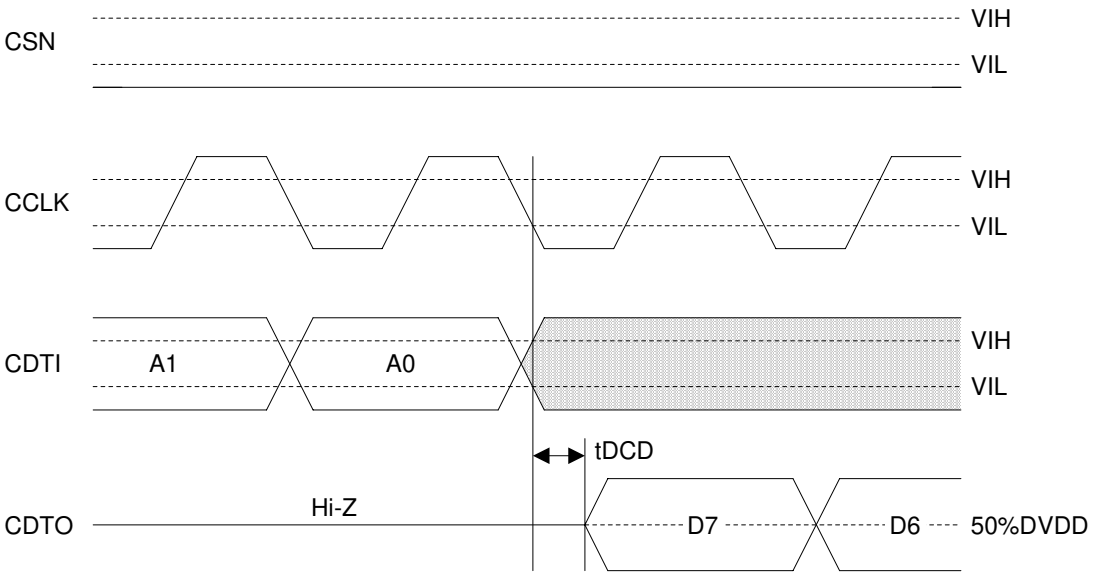
Note : BICK shows BICK1 of PORT1, BICK2 of PORT2 and BICK of PORT3. LRCK shows LRCK1 of PORT1, LRCK2 of PORT2 and LRCK of PORT3. SDTI shows SDTI of PORT1 or SDTIO of PORT2 that is used as input port. SDTO shows SDTO of PORT3 or SDTIO of PORT2 that is used as output port.



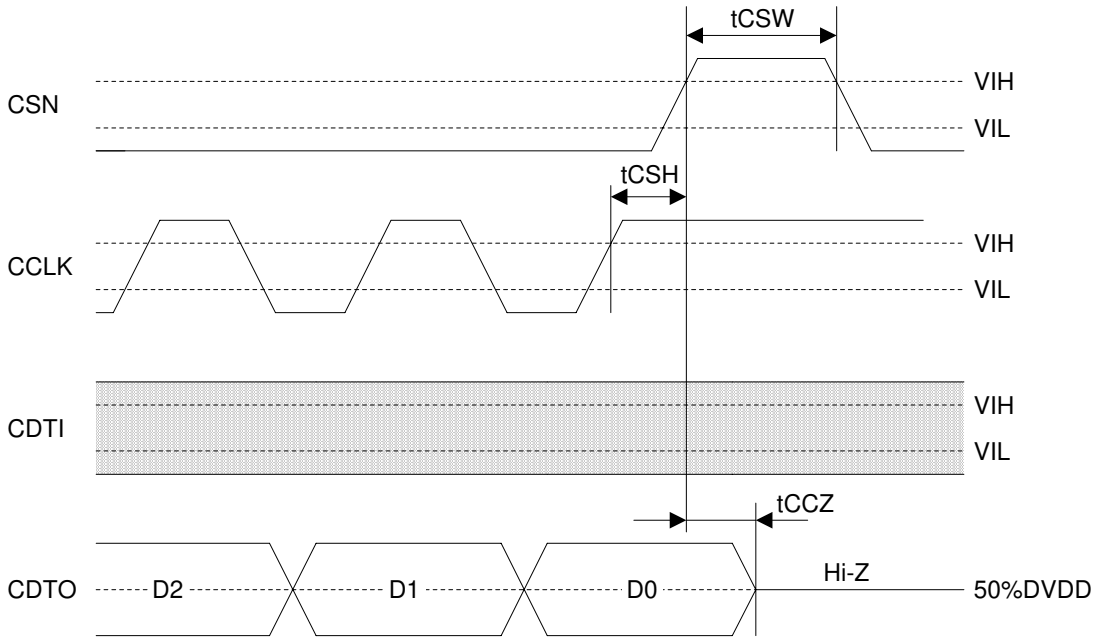
WRITE/READ Command Input Timing



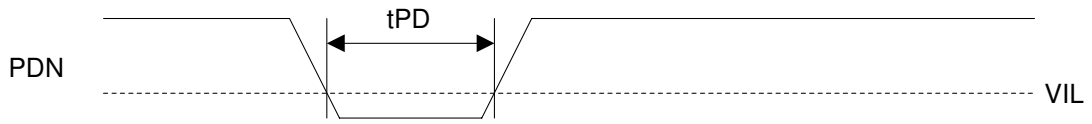
WRITE Data Input Timing



READ Data Output Timing 1



READ Data Output Timing 2



Power Down & Reset Timing

OPERATION OVERVIEW

■ Internal Signal Path

The input source of the SRC can be switched between the outputs of the DIR, PORT1 or PORT2. The input source of the PORT2 and PORT3 can be switched between the outputs of the SRC or BYPASS. When PORT2 is used as an input port, PORT2 cannot be used as an output port. The signal path should be controlled during PWN bit = "0". The Switch Names (ISEL1-0, BYPS and OSEL) in Figure 1 correspond to the register bits that control the switch function. Refer to Table 1.

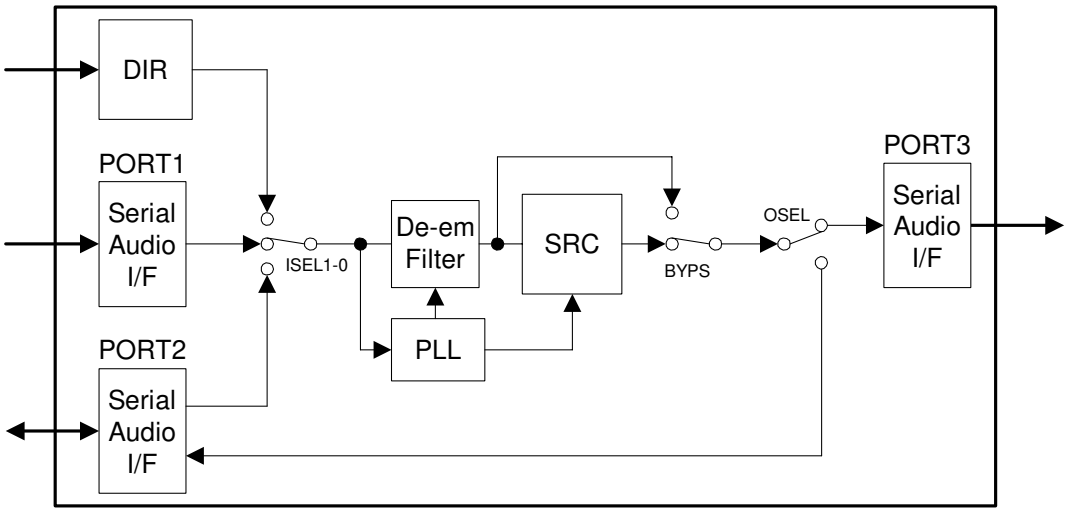


Figure 1. Connection Input Source & Output Source

Mode	Input PORT ISEL1-0 bit	SRC / Bypass BYPS bit	Output PORT OSEL bit	Path
0	00: PORT1	0: SRC	0: PORT3 (Note 14)	PORT1 → SRC → PORT3
1	01: PORT2			PORT2 → SRC → PORT3
2	10: DIR			DIR → SRC → PORT3
3	00: PORT1	1: Bypass		PORT1 → PORT3
4	01: PORT2			PORT2 → PORT3
5	10: DIR			DIR → PORT3
6	00: PORT1	0: SRC	1: PORT2 (Note 15)	PORT1 → SRC → PORT2
7	10: DIR			DIR → SRC → PORT2
8	00: PORT1	1: Bypass		PORT1 → PORT2
9	10: DIR			DIR → PORT2

Table 1. Path Select

Default is Mode 0. (Path : PORT1 → SRC → PORT3)
After PDN pin = "L" → "H", SDTIO pin of PORT2 is the input pin.
The DIF1-0 bits of the PORT1 should be set a value except "10" (I^2S Compatible) when the DIR is selected as an input port.

Refer to Table 6 and Table 7 for Master/Slave mode setting.

Note 14. In this case, PORT2 is input port. If PORT2 is unused, the digital I/O pins should be processed appropriately as shown in Table 2.

M/S2 pin	Mode	Unused pin	Pin I/O	Setting
L	Slave	MCLK2	I	This pin should be connected to DVSS.
		BICK2	I	This pin should be connected to DVSS.
		LRCK2	I	This pin should be connected to DVSS.
		SDTIO	I	This pin should be connected to DVSS.
H	Master	MCLK2	I	This pin should be connected to DVSS.
		BICK2	O	This pin should be open.
		LRCK2	O	This pin should be open.
		SDTIO	I	This pin should be connected to DVSS.

Table 2. Pin Setting for PORT2

Note 15. In this case, PORT3 is output port. If PORT3 is unused, the digital I/O pins should be processed appropriately as shown in Table 3.

M/S3 pin	Mode	Unused pin	Pin I/O	Setting
L	Slave	OMCLK	I	This pin should be connected to DVSS.
		BICK	I	This pin should be connected to DVSS.
		LRCK	I	This pin should be connected to DVSS.
		SDTO	O	This pin should be open.
H	Master	OMCLK	I	This pin should be connected to DVSS.
		BICK	O	This pin should be open.
		LRCK	O	This pin should be open.
		SDTO	O	This pin should be open.

Table 3. Pin Setting for PORT3

■ System Clock

PORT1 can be operated in slave mode only. PORT2 and PORT3 work in master mode and slave mode. Internal system clock is created by internal PLL using LRCK1, LRCK2 or LRCK of DIR. The MCLK is not needed when PORT2 and PORT3 are in slave mode. Set the MCLK2 pin and OMCLK pin to DVSS. When PORT2 and PORT3 are used in master mode, the MCLK2 pin and OMCLK pin should be supplied MCLK. The M/S2 pin and M/S3 pin control master and slave mode switching. Table 4 and Table 5 show setting of MCLK frequency when PORT2 and PORT3 are master mode. In case of detecting the sampling frequency by MCLK when DIR is used, MCLK (MCLK2 or OMCLK) of selected output port (PORT2 or PORT3) should be input.

ICKS1	ICKS0	MCLK2		
		32kHz ≤ fs ≤ 48kHz	48kHz < fs ≤ 96kHz	
0	0	256fs	256fs	
0	1	384fs	384fs	
1	0	512fs	N/A	(default)
1	1	768fs	N/A	

Table 4. MCLK2 frequency select for Master mode

OCKS1	OCKS0	OMCLK		
		32kHz ≤ fs ≤ 48kHz	48kHz < fs ≤ 96kHz	
0	0	256fs	256fs	
0	1	384fs	384fs	
1	0	512fs	N/A	(default)
1	1	768fs	N/A	

Table 5. OMCLK frequency select for Master mode

■ Master Mode and Slave Mode

When PORT2 and PORT3 are used as output port, the M/S2 pin and M/S3 pin select either master or slave mode for each port. “H” is for master mode, and “L” is for slave mode. MCLK should be supplied to the port which is in master mode, and the AK4122A outputs BICK and LRCK. BICK and LRCK should be supplied externally to the port which is in slave mode, and MCLK is not needed fro this ports. When PORT2 is used as an input port, the M/S2 pin should be set “H” or “L”.

M/S2 pin	BYPS bit	Data I/O	Mode	BICK, LRCK
L	0	I/O	Slave, SRC	Input
L	1	Input	Slave, Bypass	
		Output	Not Available	
H	0	I/O	Master, SRC	Output
H	1	I/O	Master, Bypass	

Table 6. Master mode/Slave mode for PORT2

M/S3 pin	BYPS bit	Data I/O	Mode	BICK, LRCK
L	0	Output	Slave, SRC	Input
L	1	Output	Not Available	
H	0	Output	Master, SRC	Output
H	1	Output	Master, Bypass	

Table 7. Master mode/Slave mode for PORT3

■ Audio Interface Format

The audio interface should be controlled during PWN bit = “0”. When in BYPASS mode, BICK1, BICK2 and BICK are fixed to 64fs.

(1) PORT1

Four types of data formats are available and are selected by setting the DIF1-0 bits. (Table 8) In all modes, the serial data is in MSB first, 2’s compliment format. The SDTI is latched on the rising edge of BICK1. PORT1 corresponds to slave mode only.

Mode	DIF1	DIF0	Input Format	LRCK	BICK	
0	0	0	16bit, LSB justified	H/L	≥ 32fs	
1	0	1	24bit, MSB justified	H/L	≥ 48fs	(default)
2	1	0	24bit, I^2S Compatible	L/H	≥ 48fs	
3	1	1	24bit, LSB justified	H/L	≥ 48fs	

Table 8. Audio Interface Format for PORT1

Note: The DIF1-0 bits of the PORT1 must not be set “10” (I^2S Compatible) when the DIR is selected as an input port.

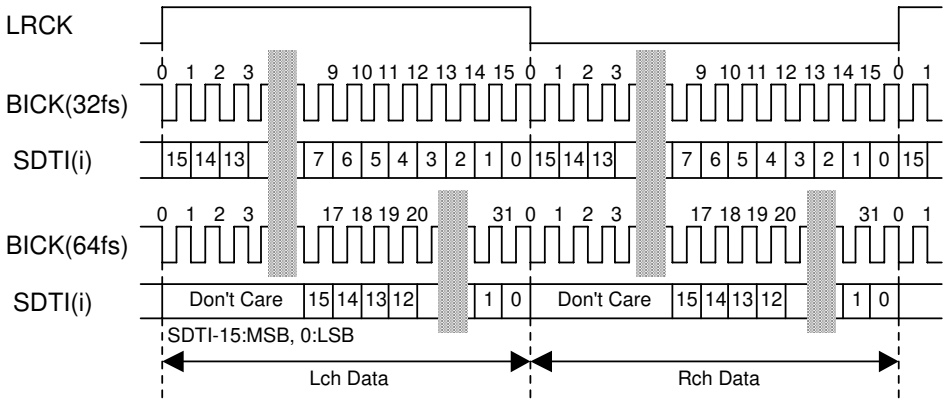


Figure 2. Mode 0 Timing

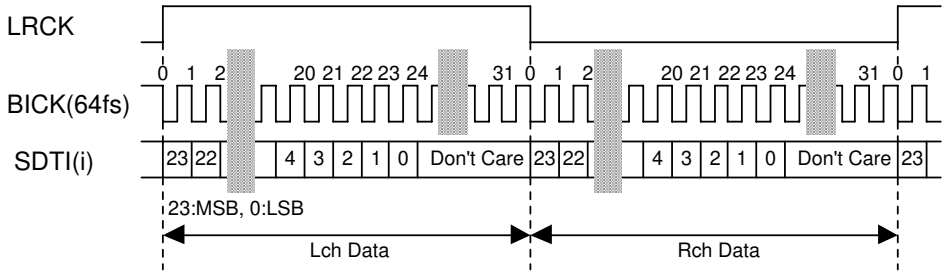


Figure 3. Mode 1 Timing

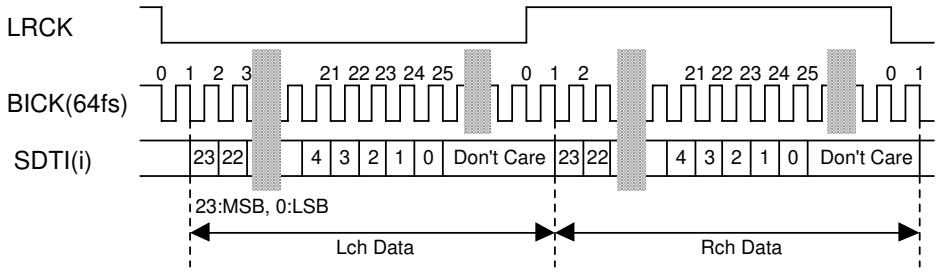


Figure 4. Mode 2 Timing

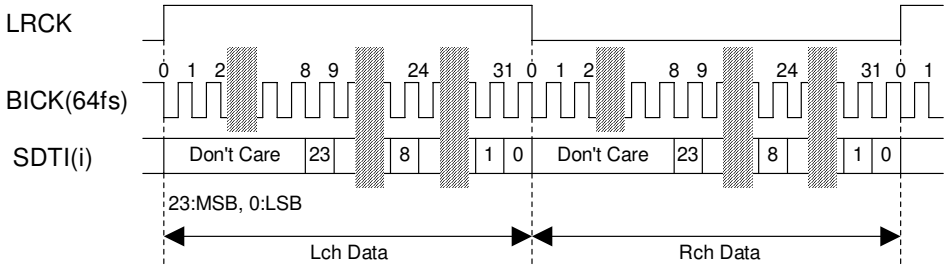


Figure 5. Mode 3 Timing

(2) PORT2

Four kinds of data formats are available and are selected by setting IDIF1-0 bits (Table 9). In all modes, the serial data is in MSB first, 2's compliment format. If PORT2 is selected as an output port, the SDTIO is clocked out on the falling edge of BICK2, and if PORT2 is selected as an input port, the SDTIO is latched on the rising edge of BICK2. The audio interface supports both master and slave modes. In master mode, BICK2 output is fixed to 64fs and the LRCK2 output fixed to 1fs.

Mode	IDIF1	IDIF0	Output Format	Input Format	LRCK	BICK	
0	0	0	24bit, MSB justified	16bit, LSB justified	H/L	≥ 32fs	
1	0	1	24bit, MSB justified	24bit, MSB justified	H/L	≥ 48fs	(default)
2	1	0	24bit, I^2S Compatible	24bit, I^2S Compatible	L/H	≥ 48fs	
3	1	1	24bit, MSB justified	24bit, LSB justified	H/L	≥ 48fs	

Table 9. Audio Interface Format for PORT2

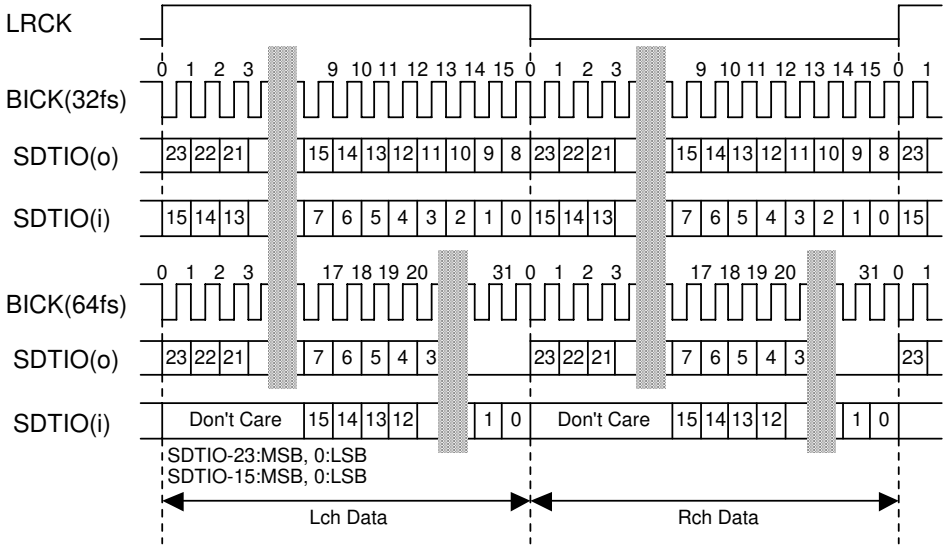


Figure 6. Mode 0 Timing

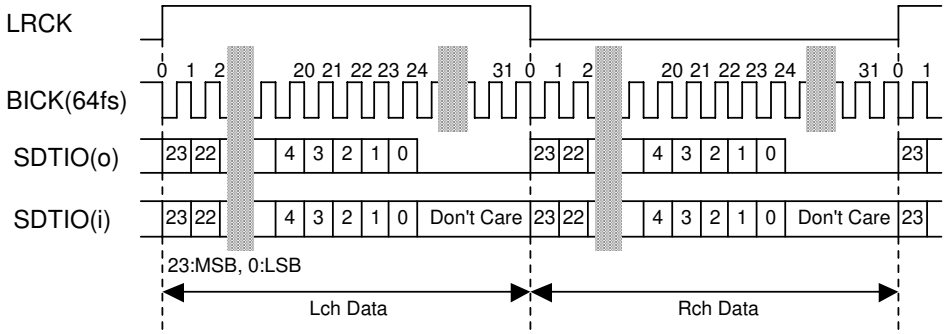


Figure 7. Mode 1 Timing

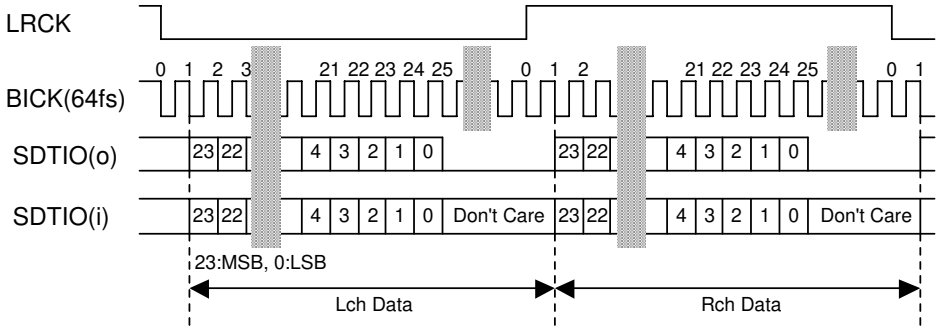


Figure 8. Mode 2 Timing

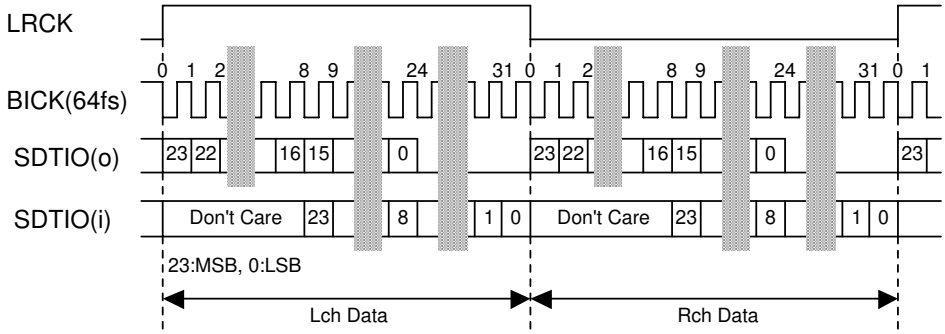


Figure 9. Mode 3 Timing

(3) PORT3

Two kinds of data formats are available and are selected by setting the ODIF bit (Table 10). In both modes, the serial data is in MSB first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK. The audio interface supports both master and slave modes. In master mode, BICK output is fixed to 64fs and LRCK output is fixed to 1fs.

Mode	ODIF	Output Format	LRCK	BICK	
0	0	24bit, MSB justified	H/L	≥ 48fs	(default)
1	1	24bit, I^{2}S Compatible	L/H	≥ 48fs	

Table 10. Audio Interface Format for PORT3

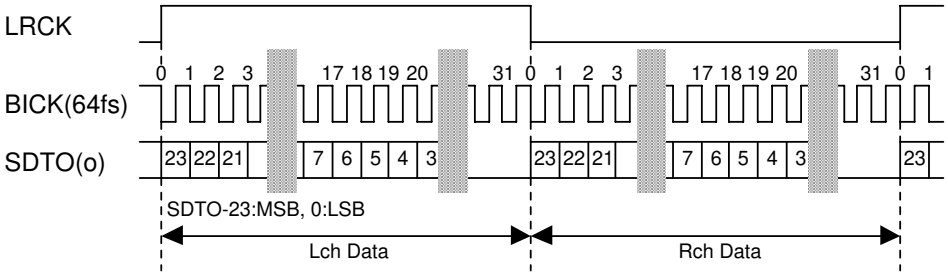


Figure 10. Mode 0 Timing

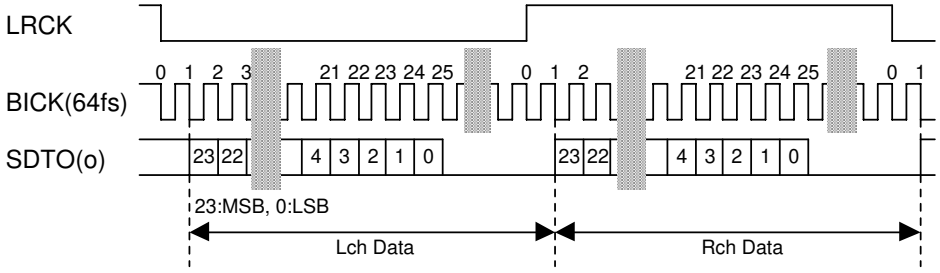


Figure 11. Mode 1 Timing

■ Soft Mute Operation

Soft mute operation is performed in the digital domain of the SRC output. Soft mute can be controlled by SMUTE bit or SMUTE pin. The SMUTE bit setting is logically ORed with the SMUTE pin setting. When SMUTE bit goes "1" or SMUTE pin goes "H", the SRC output data is attenuated by –∞ within 1024 LRCK cycles. When the SMUTE bit returned "0" and SMUTE pin goes "L" the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled before mute state, the attenuation is discontinued and returned to 0dB in the same cycles. The soft mute is effective for changing the signal source without stopping the signal transmission.

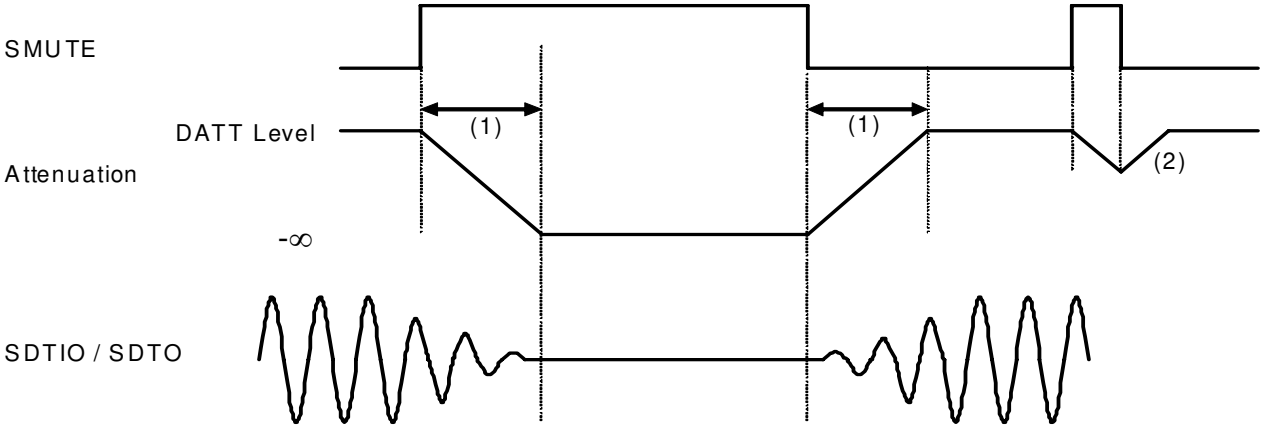


Figure 12. Soft Mute Function

(1) The output data is attenuated by –∞ during 1024 LRCK cycles (1024/fs).
(2) If the soft mute is cancelled before attenuating to –∞, the attenuation is discontinued and returned to 0dB in the same clock cycles.

■ De-emphasis Filter Control

The AK4122A includes a digital de-emphasis filter (tc=50/15μs) by IIR filter corresponding to three sampling frequencies (32kHz, 44.1kHz and 48kHz).

(1) When input port is DIR

When the input port is DIR and DEAU bit = "1", the de-emphasis filter is enabled automatically by sampling frequency (FS3-0 bit) and pre-emphasis information in the channel status. DEM1-0 bits can control the de-emphasis filter when DEAU bit = "0". When the de-emphasis filter is OFF, the internal de-emphasis filter is bypassed. When PEM bit = "0", the internal de-emphasis filter is always bypassed.

PEM	FS3	FS2	FS1	FS0	Mode
1	0	0	0	0	44.1kHz
1	0	0	1	0	48kHz
1	0	0	1	1	32kHz
1	(Others)				OFF
0	x	x	x	x	OFF

Table 11. De-emphasis Auto Control (DEAU bit = "1")

PEM	DEM1	DEM0	Mode	
1	0	0	44.1kHz	
1	0	1	OFF	(default)
1	1	0	48kHz	
1	1	1	32kHz	

Table 12. De-emphasis Manual Control (DEAU bit = "0")

(2) When input port is PORT1 or PORT2

When PORT1 or PORT2 is selected as an input port, DEM1-0 bits can control the de-emphasis filter regardless of the DEAU bit setting. In this case, the de-emphasis filter can not be enabled automatically. When the de-emphasis setting is OFF, the internal de-emphasis filter is bypassed.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 13. De-emphasis Manual Control

■ System Reset and Power-Down

The AK4122A has a full power-down mode for all circuits that is activated by the PDN pin, and a partial power-down mode activated by the PWN bit. The AK4122A should be reset once at power-up by bringing the PDN pin = "L".

PDN pin:

All analog and digital circuits are placed in power-down and reset modes by bringing the PDN pin = "L". All the registers are initialized and clocks are stopped. Read/Write operations to the registers are disabled.

PWN bit (Address 00H; D0):

Unlike the PDN pin operation described above, internal registers and mode settings are not initialized. Read/Write operations to the registers are enabled.

■ System Reset

Bringing the PDN pin = "L" sets the AK4122A in power-down mode and initializes digital filters. When the PDN pin = "L", the SDTO output is "L". The AK4122A should be reset once by bringing the PDN pin = "L" upon power-up. The SDTO becomes valid in less than 100ms from the rising edge of PDN after a reset release by clock supply. Until the SDTO becomes valid, it outputs "L". After the rising of PDN pin, the SDTIO pin is an input pin.

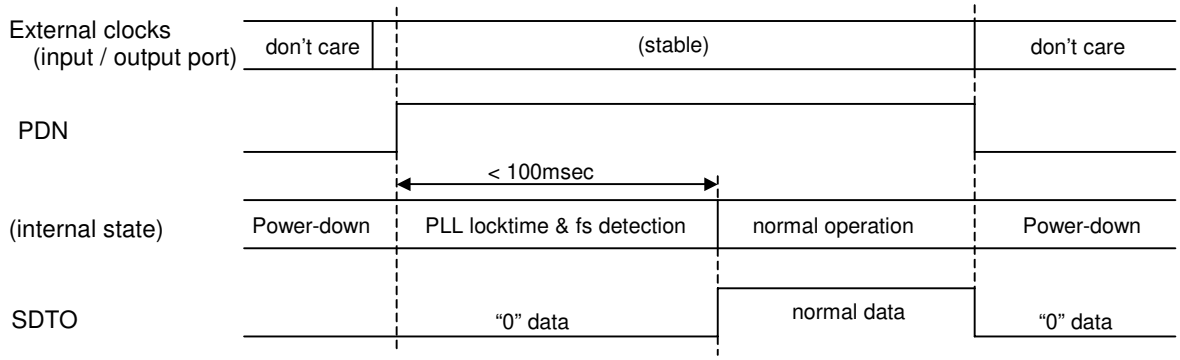


Figure 13. System Reset

■ Sequence of Changing Clocks

A clock change sequence is shown in Figure 14. An internal reset is executed when the input or the output clocks are changed. The SDTO data is placed "0" during the reset. Within 100ms, the SDTO outputs normal data after the reset. When the frequency transition occurs gradually without phase change or when the output clock is changed while fso/fsi > 4, the output data may have large distortion for several seconds. A reset should be made by bringing the PDN pin = "L" or PWN bit = "0" to obtain normal data within 100ms when clocks are changed.

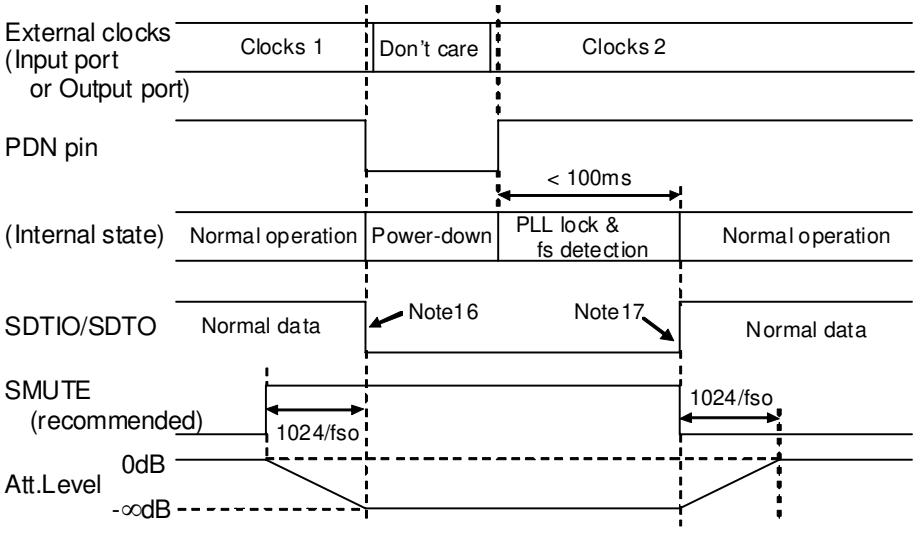


Figure 14. Sequence of Changing Clocks

Note 16. The data on SDTO may cause a clicking noise. To prevent this, set SDTI or SDTIO to "0" from GD before the PDN pin changes to "L", which will cause the data on SDTO to remain "0". SMUTE can also remove this clicking noise.

Note 17. The data on SDTO may cause a clicking noise. To prevent this, set SDTI to "0" for 1024/fso+100ms or more from the timing when the PDN pin changes to "H" while the SMUTE pin = "H".

Note 18. The data on SDTO may cause a clicking noise. To prevent this, set SDTI to "0" for 1024/fso+100ms or more from the timing when the PDN pin changes to "H" while the SMUTE pin = "H".

■ 96kHz Clock Recovery

An integrated low jitter PLL of the DIR has a wide lock range of 32kHz to 96kHz and its lock time is less than 20ms. The AK4122A has a sampling frequency detect function (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz) that uses either clock comparison against the MCLK2 or OMCLK frequency or the channel status information. The PLL loses synchronization when receiving preambles in incorrect interval.

■ Biphase Input

Four inputs (RX1-4) are available for DIR. Each input includes an amplifier for unbalance loads that can accept 200mVpp or greater signal. The IPS1-0 bits select the receiver channel (Table 14).

IPS1	IPS0	Input Data	
0	0	RX1	(default)
0	1	RX2	
1	0	RX3	
1	1	RX4	

Table 14. Recovery Data Select

■ Biphase Output

The AK4122A can output through data from the digital receiver inputs (RX1-4) to the TX pin. The OPS1-0 bits can select the source of the TX pin output. TX output can be stopped by TXE bit. The AK4122A does not have a TX output buffer (Line Driver), therefore the TX pin cannot drive the 75Ω coaxial cable directly.

OPS1	OPS0	Output Data	
0	0	RX1	(default)
0	1	RX2	
1	0	RX3	
1	1	RX4	

Table 15. Output Data Select for TX