Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AK4128A

8ch 216kHz / 24-Bit Asynchronous SRC

GENERAL DESCRIPTION

The AK4128A is an 8ch digital sample rate converter (SRC). The input sample rate ranges from 8kHz to 216kHz. The output sample rate is from 8kHz to 216kHz. The AK4128A has an internal Oscillator and does not need any external master clocks. It contributes simplifying a system configuration. The AK4128A supports master mode and TDM data interface, enabling simultaneous input of asynchronous stereo data. The AK4128A is suitable for the application interfacing to different sample rates such as multi-channel high-end Car Audio Systems and DVD recorders.

FEATURES

- **8 channels input/output**
- **Asynchronous Sample Rate Converter**
- **Input Sample Rate Range (FSI): 8kHz ~ 216kHz**
- **Output Sample Rate Range (FSO): 8kHz ~ 216kHz**
- **Input to Output Sample Rate Ratio: 1/6 to 6**
- **THD+N: –130dB**
- **Dynamic Range: 140dB (A-weighted)**
- **I/F format: MSB justified, LSB justified and I^2S compatible and TDM**
- **Oscillator for Internal Operation Clock**
- **Clock for Master mode: 128/256/384/512/768fso**
- **On-chip X'tal oscillator**
- **Digital De-emphasis Filter (32kHz, 44.1kHz and 48kHz)**
- **Soft Mute Function**
- **SRC Bypass mode (Master/Slave)**
- **µP Interface: I²C bus**
- **Power Supply: AVDD, DVDD1-4: 3.0 ~ 3.6V (typ. 3.3V)**
- **Ta = –20 ~ 85°C (AK4128AEQ), –40 ~ 85°C (AK4128AVQ)**
- **Package: 64LQFP**

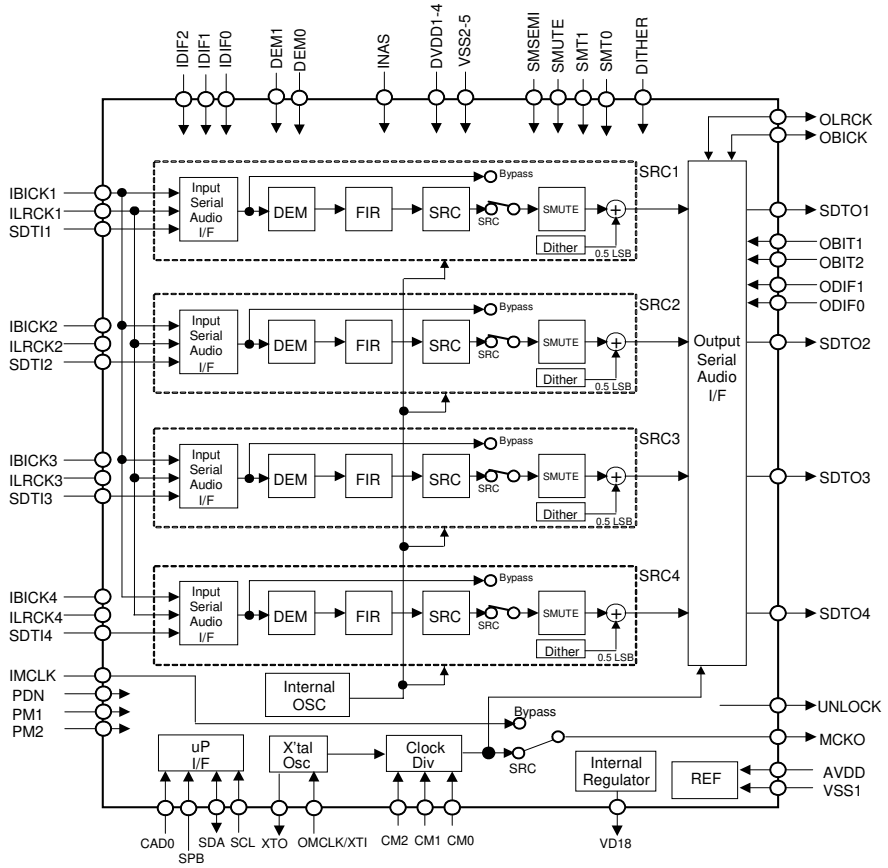


Figure 1. AK4128A Block Diagram (Synchronous mode INAS pin = "L")

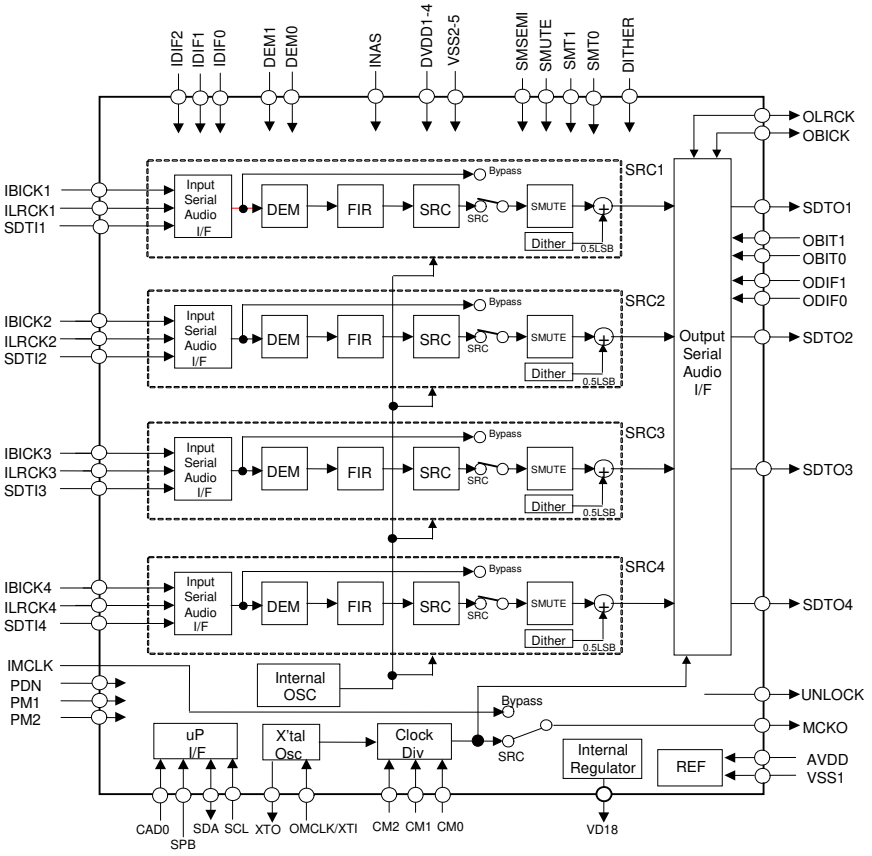


Figure 2. AK4128A Block Diagram (Asynchronous mode INAS pin = "H")

■ Compatibility with AK4126

(1) Specifications

Parameter	AK4126	AK4128A
Stereo Inputs Asynchronous Mode	Not Available Synchronous Mode Only	Available The INAS pin controls synchronous and asynchronous modes.
Internal Clock	Internal PLL The PLL2-0 pins must be set according to the PLL reference clock. #61 pin: A pin for external devices of PLL filter.	Internal Regulator + Internal Oscillator PLL reference clock select is not needed since internal oscillator generates the clock. #61 pin: A capacitor pin for the internal regulator.
Bypass Mode	Not Available	Available Controlled by CM2-0 pins or BYPS bit.
Master Mode for Output Ports	Not Available	Available Controlled by CM2-0 pins
Maximum FSI and FSO	192kHz	216kHz
Maximum IBICK and OBICK Frequency	64fs	256fs
X'tal Oscillator	Not Available	Available
Master Clock Output	Not Available	Available
TDM Mode	Not Available	Available Controlled by IDIF2-0 pins or IDIF2-0 bits (Input) Controlled by TDM pin (Output)
Soft Mute	All channels are controlled together.	Individual Setting Available Individual setting is available by setting SMUTE4-1 bits in serial control mode.
De-emphasis Filter	All channels are controlled together.	Individual Setting Available Individual setting is available by DEM41-40, 31-30, 21-20, 11-10 bits in serial control mode.
Audio Format for Input port.	All channels are controlled together.	Individual Setting Available Individual setting is available by IDIF42-40, 32-30, 22-20, 12-10 bits in serial control mode.
I2C	Not Available	Available Parallel and Serial control modes are selected by the SPB pin.
UNLOCK pin	Detects PLL unlock.	FSI:FSO Ratio Change Detect Detects over-current/voltage of the 1.8V outputs.

(2) Pins

Pin#	AK4126	AK4128A	
		AK4128A pin	6ch mode AK4126 compatible (PM2/1 pin = "LL")
1	NC	IBICK2	L
2	TEST0	IMCLK	L
7	TST0	SDTI4	L
14	TST1	ILRCK3	L
15	TST2	IBICK3	L
16	NC	ILRCK4	L
17	TST3	IBICK4	L
18	TST4	INAS	L
32	TST5	PM2	L
33	NC	TDM	L
42	TST6	SDTO4	L
47	TEST4	OMCLK/XTI	L
48	NC	XTO	L
49	NC	MCKO	L
51	TST8	CAD0	L
54	PLL2	TST1	L or H
55	PLL1	SMSEMI	L or H
56	PLL0	TST2	L or H
57	TST9	SCL	L
58	TST10	SDA	L
59	NC	SPB	L
61	FILT	VD18	*
63	TST11	TST3	AK4126: "Open" AK4128A: "L"
64	NC	ILRCK2	L

*: An external device is needed for the No 61 pin.

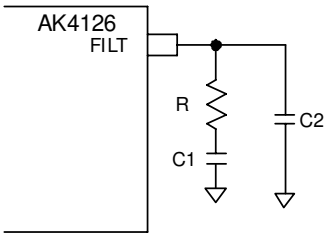


Figure 3. AK4126

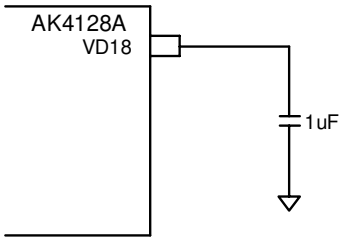


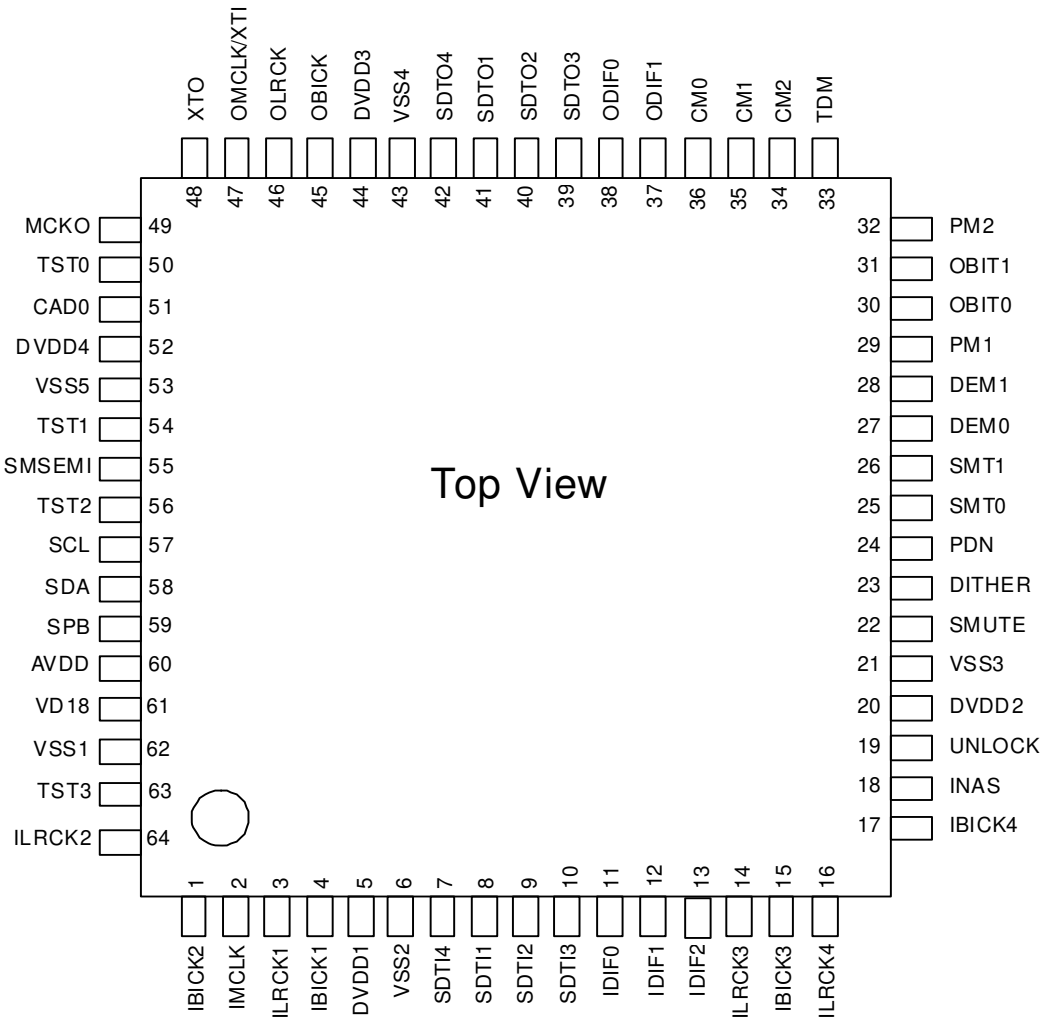
Figure 4. AK4128A

(Please refer to the AK4126 datasheet about external devices.)

■ Ordering Guide

AK4128AEQ	–20 ~ +85°C	64pin LQFP (0.5mm pitch)
AK4128AVQ	–40 ~ +85°C	64pin LQFP (0.5mm pitch)
AKD4128A	Evaluation Board for AK4128A	

■ Pin Layout



PIN / FUNCTION

No.	Pin Name	I/O	Function
1	IBICK2	I	Audio Serial Data Clock #2 Pin When the INAS pin = "L", this pin should be connected to VSS2-5.
2	IMCLK	I	Master Clock Input Pin for Input PORT
3	ILRCK1	I	Input Channel Clock #1 Pin
4	IBICK1	I	Audio Serial Data Clock #1 Pin
5	DVDD1	-	Digital Power Supply Pin, 3.0 ~ 3.6V
6	VSS2	-	Digital Ground Pin
7	SDTI4	I	Audio Serial Data Input #4 Pin
8	SDTI1	I	Audio Serial Data Input #1 Pin
9	SDTI2	I	Audio Serial Data Input #2 Pin
10	SDTI3	I	Audio Serial Data Input #3 Pin
11	IDIF0	I	Audio Interface Format #0 Pin for Input PORT (Note 2)
12	IDIF1	I	Audio Interface Format #1 Pin for Input PORT (Note 2)
13	IDIF2	I	Audio Interface Format #2 Pin for Input PORT (Note 2)
14	ILRCK3	I	Input Channel Clock #3 Pin When the INAS pin = "L", this pin should be connected to VSS2-5.
15	IBICK3	I	Audio Serial Data Clock #3 Pin When the INAS pin = "L", this pin should be connected to VSS2-5.
16	ILRCK4	I	Input Channel Clock #4 Pin When the INAS pin = "L", this pin should be connected toVSS2-5.
17	IBICK4	I	Audio Serial Data Clock #4 Pin When the INAS pin = "L", this pin should be connected to VSS2-5.
18	INAS	I	Asynchronous Mode Select Pin. "L"(connected to the ground): Synchronous mode. "H"(connected to DVDD1-4) : Asynchronous mode.
19	UNLOCK	O	Unlock Status Pin When the PDN pin= "L", this pin outputs "H".
20	DVDD2	-	Digital Power Supply Pin, 3.0 ~ 3.6V
21	VSS3	-	Digital Ground Pin
22	SMUTE	I	Soft Mute Pin (Note 3) "H": Soft Mute, "L": Normal Operation
23	DITHER	I	Dither Enable Pin "H": Dither ON, "L": Dither OFF
24	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initializes the control register. The AK4128A should be reset once by bringing PDN pin = "L" upon power-up.
25	SMT0	I	Soft Mute Timer Select #0 Pin
26	SMT1	I	Soft Mute Timer Select #1 Pin
27	DEM0	I	De-emphasis Control #0 Pin (Note 4)
28	DEM1	I	De-emphasis Control #1 Pin (Note 4)
29	PM1	I	Channel Mode Select #1 Pin
30	OBIT0	I	Bit Length Select #0 Pin for Output Data
31	OBIT1	I	Bit Length Select #1 Pin for Output Data
32	PM2	I	Channel Mode Select #2 Pin
33	TDM	I	TDM Format Select Pin. "L"(connected to the ground): Stereo mode. "H"(connected to DVDD1-4) : TDM mode.

No.	Pin Name	I/O	Function
34	CM2	I	Clock Select or Mode Select #2 Pin for Output PORT
35	CM1	I	Clock Select or Mode Select #1 Pin for Output PORT
36	CM0	I	Clock Select or Mode Select #0 Pin for Output PORT
37	ODIF1	I	Audio Interface Format #1 Pin for Output PORT
38	ODIF0	I	Audio Interface Format #0 Pin for Output PORT
39	SDTO3	O	Audio Serial Data Output #3 Pin for Output PORT When the PDN pin = "L", the SDRO3 pin outputs "L".
40	SDTO2	O	Audio Serial Data Output #2 Pin for Output PORT When the PDN pin = "L", the SDTO2 pin outputs "L".
41	SDTO1	O	Audio Serial Data Output #1 Pin for Output PORT When the PDN pin = "L", the SDTO1 pin outputs "L".
42	SDTO4	O	Audio Serial Data Output #4 Pin for Output PORT When the PDN pin = "L", the SDRO4 pin outputs "L".
43	VSS4	-	Digital Ground Pin
44	DVDD3	-	Digital Power Supply Pin, 3.0 ~ 3.6V
45	OBICK	I/ O	Audio Serial Data Clock Pin for Output PORT When the PDN pin = "L" in master mode, the OBOCK pin outputs "L".
46	OLRCK	I/ O	Output Channel Clock Pin for Output PORT When the PDN pin = "L" in master mode, the OBOCK pin outputs "L".
47	OMCLK/XTI	I	External Master Clock Input / X'tal Input Pin
48	XTO	O	X'tal Output Pin When the PDN pin = "L", XTO outputs Hi-z.
49	MCKO	O	Master Clock Output Pin When the PM2 pin = "H" and PDN pin = "L", the MCKO pin outputs "L". When the PM2 pin = "L" and PDN pin = "L", the MCKO pin outputs Hi-z.
50	TST0	I	Test Pin. This pin should be connected to VSS2-5.
51	CAD0	I	Chip Address 0 pin This pin must be connected to VSS2-5 in parallel control mode (SPB pin = "L").
52	DVDD4	-	Digital Power Supply Pin, 3.0 ~ 3.6V
53	VSS5	-	Digital Ground Pin
54	TST1	I	Test Pin. This pin should be connected to VSS2-5.
55	SMSEMI	I	Soft Mute Semi-auto Mode Setting Pin "H": Semi-auto, "L": Manual Mode
56	TST2	I	Test Pin. This pin should be connected to VSS2-5.
57	SCL	I	I^2C Control Data Clock Pin, (when the SPB pin= "H") Since there is a protection diode between this pin and DVDD1-4, connect pulled-up resister to DVDD1-4 + 0.3V or less. This pin must be connected to the VSS2-5 in parallel control mode (PSB pin= "L").
58	SDA	I/ O	I^2C Control Data In/Out put Pin, (when the SPB pin= "H") Since there is a protection diode between this pin and DVDD1-4, connect pulled-up resister to DVDD1-4 + 0.3V or less. This pin must be connected to the VSS2-5 in parallel control mode (PSB pin= "L").
59	SPB	I	Parallel/Serial Control Mode Select Pin "H": Serial Control Mode, "L": Parallel Control Mode

No.	Pin Name	I/O	Function
60	AVDD	-	Analog Power Supply Pin, 3.0 ~ 3.6V
61	VD18	O	Digital Power Output Pin, Typ 1.8V When the PDN pin= "L", the DV18 pin outputs "L". Current must not be taken from this pin. A 1μF (±30%; including the temperature characteristics) capacitor should be connected between this pin and DVSS. When this capacitor is polarized, the positive polarity pin should be connected to the VD18 pin.
62	VSS1	-	Analog Ground Pin
63	TST3	I	Test Pin. This pin should be connected to VSS2-5.
64	ILRCK2	I	Input Channel Clock #2 Pin When INAS pin = "L", this pin should be connected to VSS2-5.

Note: All input pins should not be left floating. DVDD1-4 must be connected to the same power supply.

Note 1. SPB, CM2-0, INAS, PM2-1, OBIT1-0, TDM, ODIF1-0, IDIF2-0 and CAD0 pin must be changed when the PDN pin= "L".

Note 2. In parallel control mode (SPB pin = "L"), IDIF2-0 pins control all SRC1~4 audio interface input formats.
In serial control mode (SPB pin = "H"), the setting of IDIF2-0 pins is ignored. The IDIF[12:10] bits setting is reflected to SRC1, the IDIF[22:20] bits setting is reflected to SRC2, the IDIF[32:30] bits setting is reflected to SRC3, and the IDIF[42:40] bits setting is reflected to SRC4.

Note 3. In parallel control mode (SPB pin = "L"), the SMUTE pin controls all SRC1~4 soft mute.
In serial control mode (SPB pin = "H"), the SUMUTE pin setting is ignored. The SMUTE1 bit setting is reflected to SRC1, the SMUTE2 bit setting is reflected to SRC2, the SMUTE3 bit setting is reflected to SRC3, and the SMUTE4 bit setting is reflected to SRC4.

Note 4. In parallel control mode (SPB pin= "L"), DEM1-0 pins control all SRC1~4 de-emphasis settings.
In serial control mode (SPB pin= "H"), setting of DEM1-0 pins is ignored. DEM[11:10] bits setting is reflected to SRC1, DEM[21:20] bits setting is reflected to SRC2, DEM[31:30] bits setting is reflected to SRC3, and DEM[41:40] bits setting is reflected to SRC4.

■ Handling of Unused Pins

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Digital	IBICK2, IMCLK, SDTI3-4, ILRCK3, IBICK3, ILRCK4, IBICK4, SMUTE, DITHER, OMCLK/XTI, ILRCK2, SDA, SCL, CAD0, TST0-3	These pins must be connected to VSS2-5.
	UNLOCK, SDTO1-4, MCKO, XTO	These pins must be open.

ABSOLUTE MAXIMUM RATINGS

(VSS1-5=0V; Note 5)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	4.2	V
	Digital	DVDD1-4	–0.3	4.2	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 6)		VIND	–0.3	DVDD1-4+0.3	V
Ambient Temperature (Power applied) (Note 7)	AK4128AEQ	Ta	–20	85	°C
	AK4128AVQ	Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 5. All voltages with respect to ground. VSS1-5 must be connected to the same ground.

Note 6. IMCLK, IBICK4-1, ILRCK4-1, IDIF2-0, INAS, SUMTE, DITHER, PDN, SMT1-0, DEM1-0, PM2-1, OBIT1-0, TDM, CM2-0, ODIF1-0, SDTO4-1, OBICK, OLRCK, OMCLK/XTI, CAD0, SMSEMI, SCL, SDA and SPB pins.

Note 7. In case that wiring density is 100%.

Note 8. DVDD1-4 pins must be connected to the same power supply.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1-5=0V; Note 5)

Parameter		Symbol	min	typ	max	Units
Power Supplies: (Note 9)	Analog	AVDD	3.0	3.3	3.6	V
	Digital	DVDD1-4	3.0	3.3	3.6	V
	Difference	AVDD - DVDD1-4	-0.3	0	+0.3	V

Note 5. All voltages with respect to ground. VSS1-5 must be connected to the same ground.

Note 8. DVDD1-4 pins must be connected to the same power supply.

Note 9. The power up sequence between AVDD and DVDD1-4 is not critical but the PDN pin must be “L” until all power supplies are ON, then put the PDN pin to “H”.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

SRC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD1-4=3.3V; VSS1-5=0V; Signal Frequency = 1kHz; data = 24bit;
Measurement bandwidth = 20Hz ~ FSO/2; unless otherwise specified.)

Parameter	Symbol	min	typ	max	Units
SRC Characteristics:					
Resolution				24	Bits
Input Sample Rate	FSI	8		216	kHz
Output Sample Rate	FSO	8		216	kHz
THD+N (Input = 1kHz, 0dBFS, Note 10)					
FSO/FSI = 44.1kHz/48kHz		-	–130	-	dB
FSO/FSI = 48kHz/44.1kHz		-	–124	-	dB
FSO/FSI = 48kHz/192kHz		-	–133	-	dB
FSO/FSI = 192kHz/48kHz		-	–124	-	dB
Worst Case (FSO/FSI = 32kHz/176.4kHz)		-	-	-91	dB
Dynamic Range (Input = 1kHz, –60dBFS, Note 10)					
FSO/FSI = 44.1kHz/48kHz		-	136	-	dB
FSO/FSI = 48kHz/44.1kHz		-	136	-	dB
FSO/FSI = 48kHz/192kHz		-	136	-	dB
FSO/FSI = 192kHz/48kHz		-	132	-	dB
Worst Case (FSO/FSI = 48kHz/32kHz)		132	-	-	dB
Dynamic Range (Input = 1kHz, –60dBFS, A-weighted, Note 10)					
FSO/FSI = 44.1kHz/48kHz		-	140	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1/6		6	-

Note 10. Measured by Audio Precision System Two Cascade.

POWER CONSUMPTION

(Ta= 25°C; AVDD=DVDD1-4=3.0~3.6V; VSS1-5=0V; Signal Frequency=1kHz; data=24bit; Asynchronous Input mode (INAS pin = "H"), Output PORT: Master mode, OMCLK/XTI are input via a X'tal. PM2/1 pin = "H/L" 8ch mode, unless otherwise specified.)

Parameter	min	typ	max	Units
Power Supplies				
Power Supply Current				
Normal operation (PDN pin = "H")				
AVDD+DVDD1-4				
FSI=FSO=48kHz: AVDD=DVDD1-4=3.3V (Note 12)		42	-	mA
FSI=FSO=192kHz: AVDD=DVDD1-4=3.3V (Note 13)		108	-	mA
: AVDD=DVDD1-4=3.6V (Note 14)		109	164	mA
Power down (PDN pin = "L") (Note 11)				
AVDD+DVDD1-4		10	100	μA

Note 11. All digital input pins are held to VSS2-5.
Note 12. It is 41 [mA] (typ) when the OMCLK/XTI pin is supplied a 24.576MHz external clock and the output port is in slave mode.
Note 13. It is 105 [mA] (typ) when the OMCLK/XTI pin is supplied a 24.576MHz external clock and the output port is in slave mode.
Note 14. It is 106 [mA] (typ) when the OMCLK/XTI pin is supplied a 24.576MHz external clock and the output port is in slave mode.

FILTER CHARACTERISTICS

(Ta= 25°C; AVDD=DVDD1-4=3.0 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband –0.01dB	0.985 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	0.905 ≤ FSO/FSI < 0.985	PB	0		0.4167FSI	kHz
	0.714 ≤ FSO/FSI < 0.905	PB	0		0.3195FSI	kHz
	0.656 ≤ FSO/FSI < 0.714	PB	0		0.2852FSI	kHz
	0.536 ≤ FSO/FSI < 0.656	PB	0		0.2182FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0		0.2177FSI	kHz
	0.452 ≤ FSO/FSI < 0.492	PB	0		0.1948FSI	kHz
	0.357 ≤ FSO/FSI < 0.452	PB	0		0.1458FSI	kHz
	0.324 ≤ FSO/FSI < 0.357	PB	0		0.1302FSI	kHz
	0.246 ≤ FSO/FSI < 0.324	PB	0		0.0917FSI	kHz
	0.226 ≤ FSO/FSI < 0.246	PB	0		0.0826FSI	kHz
	0.1667 ≤ FSO/FSI < 0.226	PB	0		0.0583FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
	0.905 ≤ FSO/FSI < 0.985	SB	0.5021FSI			kHz
	0.714 ≤ FSO/FSI < 0.905	SB	0.3965FSI			kHz
	0.656 ≤ FSO/FSI < 0.714	SB	0.3643FSI			kHz
	0.536 ≤ FSO/FSI < 0.656	SB	0.2974FSI			kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2813FSI			kHz
	0.452 ≤ FSO/FSI < 0.492	SB	0.2604FSI			kHz
	0.357 ≤ FSO/FSI < 0.452	SB	0.2116FSI			kHz
	0.324 ≤ FSO/FSI < 0.357	SB	0.1969FSI			kHz
	0.246 ≤ FSO/FSI < 0.324	SB	0.1573FSI			kHz
	0.226 ≤ FSO/FSI < 0.246	SB	0.1471FSI			kHz
	0.1667 ≤ FSO/FSI < 0.226	SB	0.1020FSI			kHz
Passband Ripple		PR			±0.01	dB
Stopband Attenuation	0.985 ≤ FSO/FSI ≤ 6.000	SA	121.2			dB
	0.905 ≤ FSO/FSI < 0.985	SA	121.4			dB
	0.714 ≤ FSO/FSI < 0.905	SA	115.3			dB
	0.656 ≤ FSO/FSI < 0.714	SA	116.9			dB
	0.536 ≤ FSO/FSI < 0.656	SA	114.6			dB
	0.492 ≤ FSO/FSI < 0.536	SA	100.2			dB
	0.452 ≤ FSO/FSI < 0.492	SA	103.3			dB
	0.357 ≤ FSO/FSI < 0.452	SA	102.0			dB
	0.324 ≤ FSO/FSI < 0.357	SA	103.6			dB
	0.246 ≤ FSO/FSI < 0.324	SA	103.3			dB
	0.226 ≤ FSO/FSI < 0.246	SA	101.5			dB
	0.1667 ≤ FSO/FSI < 0.226	SA	73.2			dB
Group Delay	(Note 15)	GD	-	64	-	1/fs

Note 15. This value is the time from the rising edge of ILRCK after SDTI data is input to rising edge of OLRCK after the SDTI data is output, when OLRCK data corresponds with ILRCK data.

DC CHARACTERISTICS

(Ta= 25°C; AVDD=DVDD1-4=3.0 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%DVDD1-4	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD1-4	V
High-Level Output Voltage					
Except the SDA pin (Iout=–400μA)	VOH	DVDD1-4 – 0.4	-	-	V
Low-Level Output Voltage					
Except the SDA pin (Iout=400μA)	VOL	-	-	0.4	V
SDA pin (Iout=3mA)	VOL			0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta= 25°C; AVDD=DVDD1-4=3.0 ~ 3.6V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Crystal Oscillator Frequency	fXTAL	11.2896		24.576	MHz
IMCLK Input					
Frequency	fECLK	1.024		36.864	MHz
Duty	dECLK	40	50	60	%
OMCLK Input					
128 FSO :	fCLK	1.024		27.648	MHz
Pulse Width Low	tCLKL	13			ns
Pulse Width High	tCLKH	13			ns
256 FSO :	fCLK	2.048		27.648	MHz
Pulse Width Low	tCLKL	13			ns
Pulse Width High	tCLKH	13			ns
384 FSO :	fCLK	3.072		36.864	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns
512 FSO :	fCLK	4.096		27.648	MHz
Pulse Width Low	tCLKL	13			ns
Pulse Width High	tCLKH	13			ns
768 FSO :	fCLK	6.144		36.864	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns
MCKO Output					
Frequency	fMCK	1.024		36.864	MHz
Duty (Note 16)	dMCLK	40	50	60	%

Note 16. This is a value of MCKO output duty when the master clock for output ports is supplied by a crystal oscillator.

Input PORT LRCK for Stereo Mode (ILRCK1-4)					
Frequency	FSI	8		216	kHz
Duty Cycle Slave Mode	Duty	48	50	52	%
Output PORT LRCK for Stereo Mode (OLRCK)					
Frequency					
Slave mode	FSO	8		216	kHz
Master mode OMCLK Input 128FSO mode	FSO	8		216	kHz
Master mode OMCLK Input 256FSO mode	FSO	8		108	kHz
Master mode OMCLK Input 384FSO mode	FSO	8		96	kHz
Master mode OMCLK Input 512FSO mode	FSO	8		54	kHz
Master mode OMCLK Input 768FSO mode	FSO	8		48	kHz
Duty Cycle Slave Mode	Duty	48	50	52	%
Master Mode	Duty		50		%
Input PORT LRCK for TDM256 Mode (ILRCK1)					
Asynchronous Inputs Mode (INAS pin = "L")					
Frequency	FSI	8		48	kHz
"H" time (slave mode)	tLRH	1/256FSI			ns
"L" time (slave mode)	tLRL	1/256 FSI			ns
Output PORT LRCK for TDM256 Mode (OLRCK)					
Frequency	FSO	8		48	kHz
"H" time (slave mode)	tLRH	1/256 FSO			ns
"L" time (slave mode)	tLRL	1/256 FSO			ns
"H" time (Master mode, TDM256 24bit MSB justified)	tLRH	-	1/8 FSO	-	ns
"L" time (Master mode, TDM256 24bit I^2S)	tLRL	-	1/8 FSO	-	ns
Audio Interface Timing					
Input PORT (Stereo Slave mode)					
IBICK1-4 Period (FSI= 8kHz ~ 54kHz)	tBCK	1/256 FSI			ns
(FSI=54kHz ~ 108kHz)	tBCK	1/128 FSI			ns
(FSI=108kHz ~ 216kHz)	tBCK	1/64 FSI			ns
IBICK1-4 Pulse Width Low	tBCKL	27			ns
Pulse Width High	tBCKH	27			ns
ILRCK1-4 Edge to IBICK1-4 "↑"(Note 17)	tLRB	15			ns
IBICK1-4 "↑" to ILRCK1-4 Edge (Note 17)	tBLR	15			ns
SDTI1-4 Hold Time from IBICK1-4 "↑"	tSDH	15			ns
SDTI1-4 Setup Time to IBICK1-4 "↑"	tSDS	15			ns
Input PORT (TDM256 slave mode)					
IBICK1 Period	tBCK	81			ns
IBICK1 Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
ILRCK1 Edge to IBICK1 "↑" (Note 17)	tLRB	20			ns
IBICK1 "↑" to ILRCK1 Edge (Note 17)	tBLR	20			ns
SDTI1 Hold Time from IBICK1 "↑"	tSDH	20			ns
SDTI1 Setup Time to IBICK1 "↑"	tSDS	10			ns
Output PORT (Stereo Slave mode)					
OBICK Period (FSO= 8kHz ~ 54kHz)	tBCK	1/256 FSO			ns
(FSO= 54kHz ~ 108kHz)	tBCK	1/128 FSO			ns
(FSO=108kHz ~ 216kHz)	tBCK	1/64 FSO			ns
OBICK Pulse Width Low	tBCKL	27			ns
Pulse Width High	tBCKH	27			ns
OLRCK Edge to OBICK "↑" (Note 17)	tLRB	20			ns
OBICK "↑" to OLRCK Edge (Note 17)	tBLR	20			ns
OLRCK to SDTO1-4 (MSB) (Except I^2S mode)	tLRS			20	ns
OBICK "↓" to SDTO1-4	tBSD			20	ns

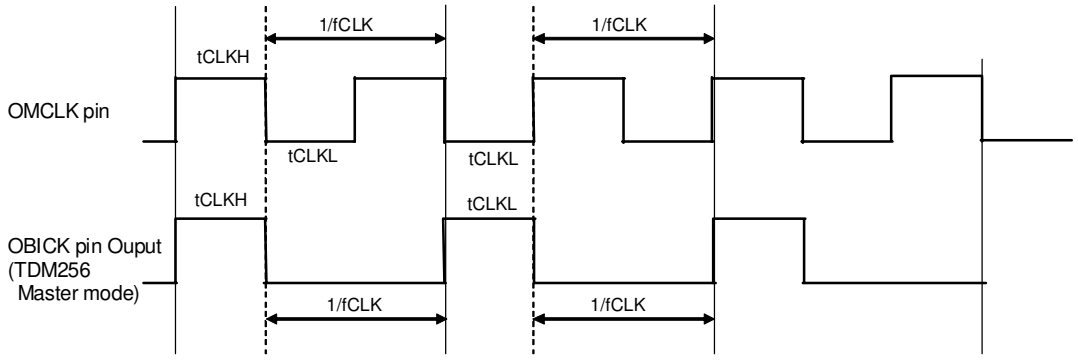
Output PORT (TDM256 slave mode)						
OBICK Period		tBCK	81			ns
OBICK Pulse Width Low		tBCKL	32			ns
Pulse Width High		tBCKH	32			ns
OLRCK Edge to OBICK "↑"	(Note 17)	tLRB	20			ns
OBICK "↑" to OLRCK Edge	(Note 17)	tBLR	20			ns
OBICK "↓" to SDTO1		tBSD			20	ns
Output PORT (Stereo Master mode)						
OBICK Frequency		fBCK		64 FSO		Hz
OBICK Duty		dBCK		50		%
OBICK "↓" to OLRCK Edge		tMBLR	–20		20	ns
OBICK "↓" to SDTO1-4		tBSD	–20		20	ns
Output PORT (TDM256 master mode)						
OBICK Frequency		fBCK	-	256 FSO	-	Hz
OBICK Duty		dBCK	-	50(Note 19)	-	%
OBICK "↓" to OLRCK Edge		tMBLR	–10	-	10	ns
OBICK "↓" to SDTO1		tBSD	–20		20	ns
Reset Timing						
PDN Pulse Width	(Note 18)	tPD	150			ns

Note 17. BICK rising edge must not occur at the same time as LRCK edge.

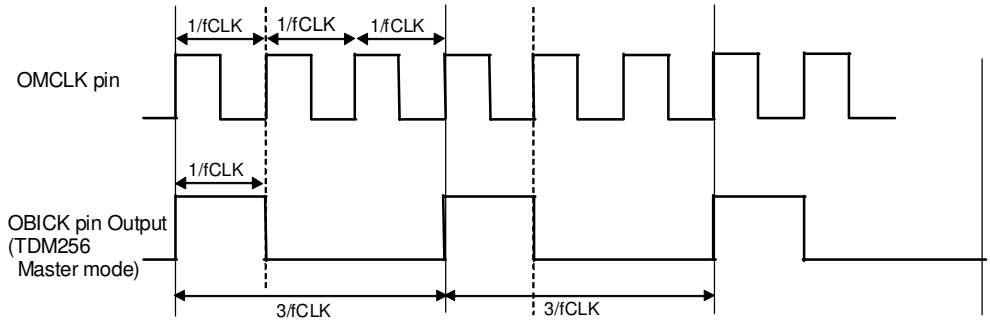
Note 18. The AK4128A can be reset by bringing the PDN pin = "L".

Note 19. When OMCLK=512FSO. If the OMCLK=256FSO, OMCLK clock is though and output from the OBICK pin. When OMCLK = 384FSO, dBCK= (tCLKH)/(tCLKH+1/fCLK) x100 [%] or (tCLKL)/(tCLKL+1/fCLK) x100 [%]. When OMCLK=768FSO, dBCK= (1/fCLK)/(3/fCLK) x100 [%].

OMCLK=384FSO



OMCLK=768FSO



Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 20)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF

Note 20. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

■ Timing Diagram

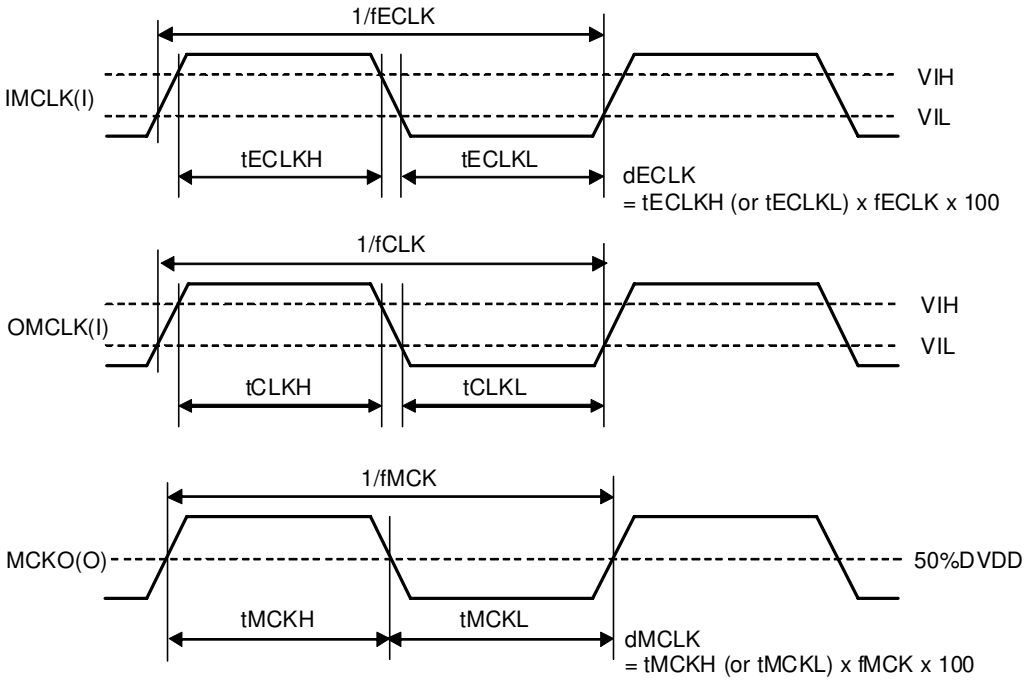


Figure 5. IMCLK, OMCLK, MCKO Clock Timing

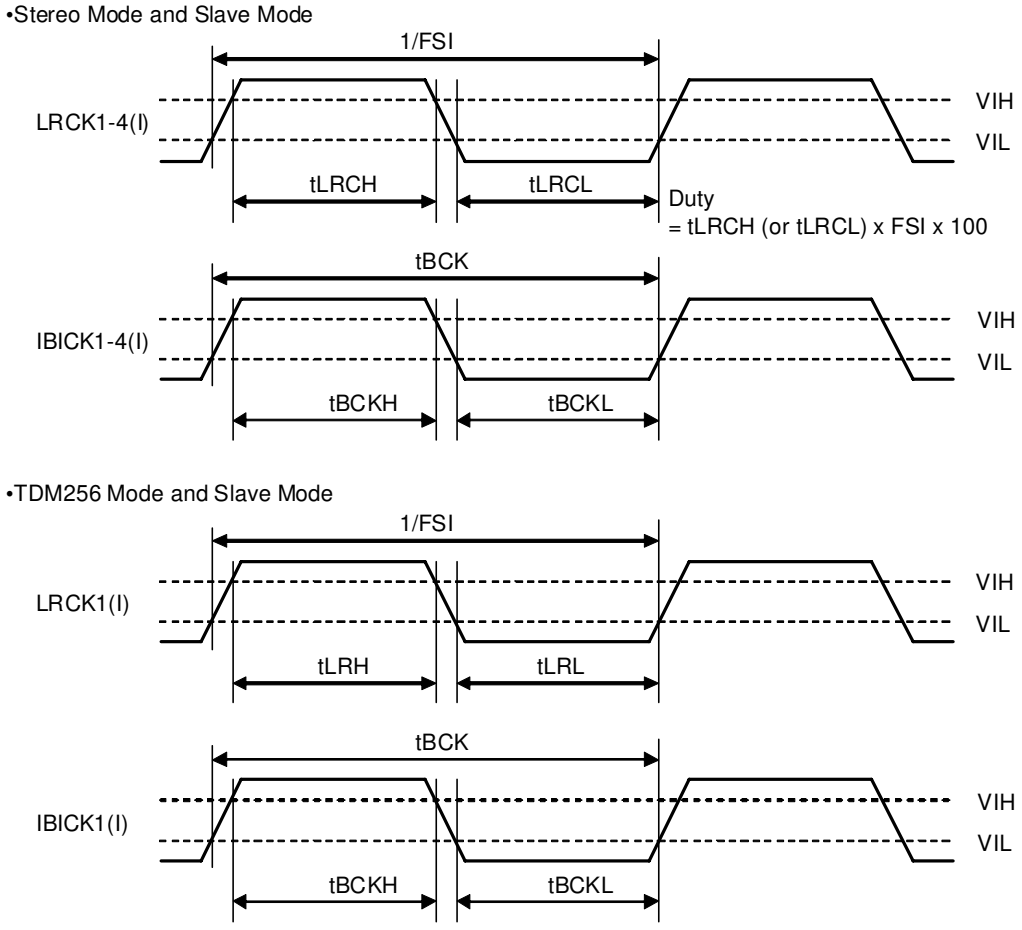


Figure 6. ILRCK1-4, IBICK1-4 Clock Timing

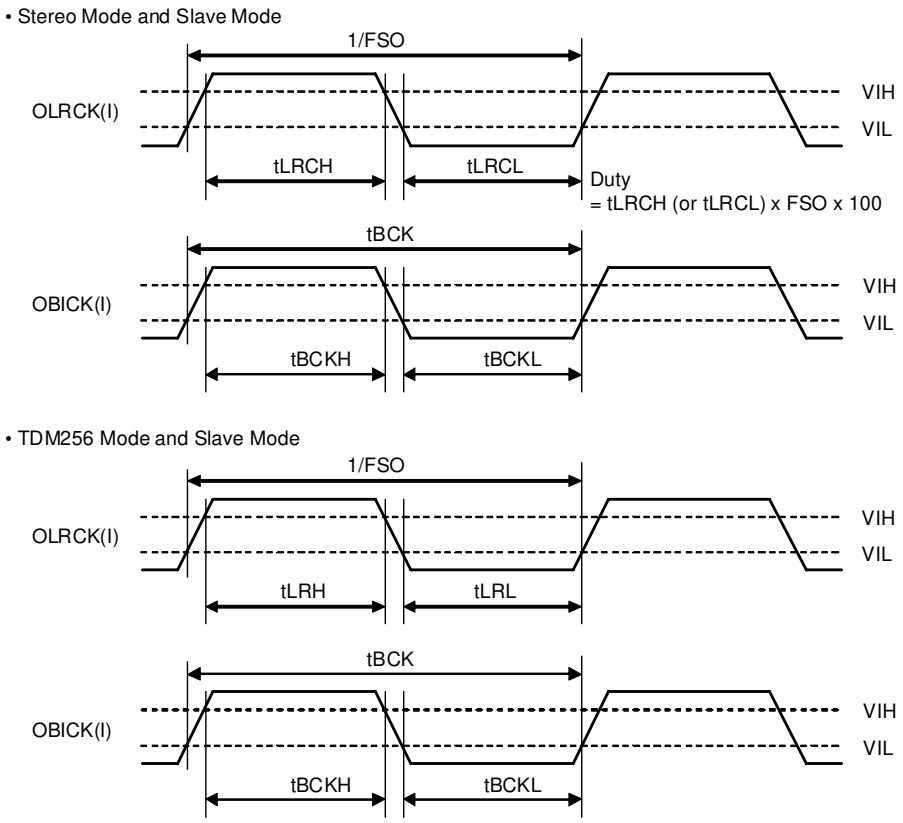


Figure 7. OLRCK, OBICK, Clock Timing (Slave Mode)

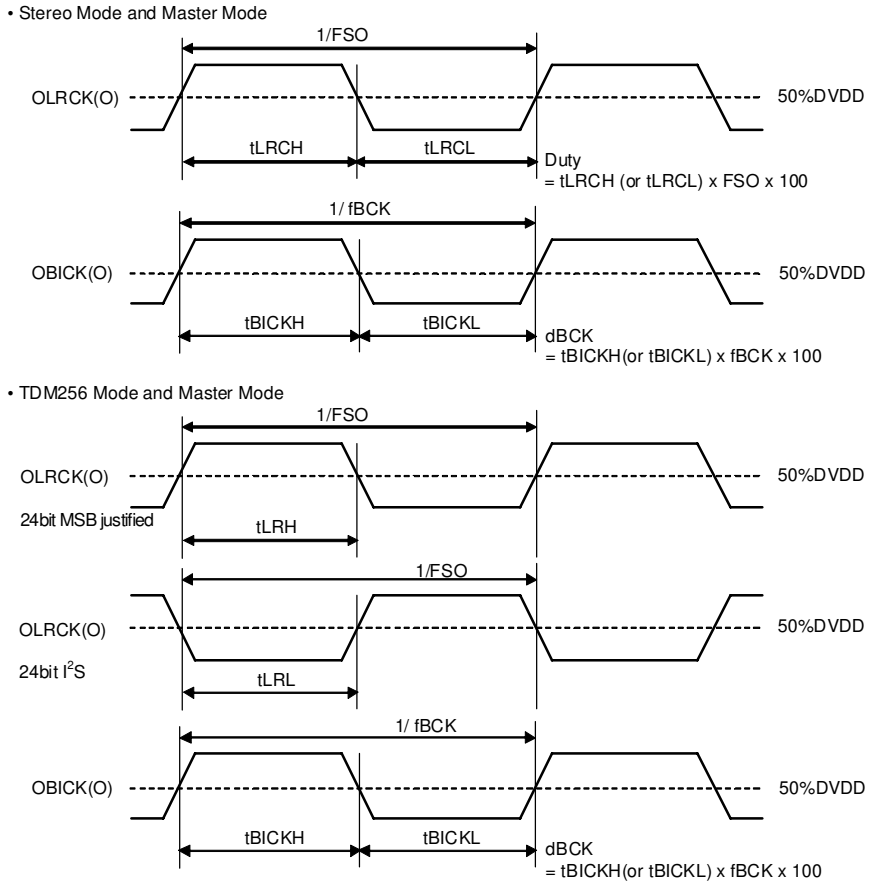


Figure 8. OLRCK, OBICK, Clock Timing (Master Mode)

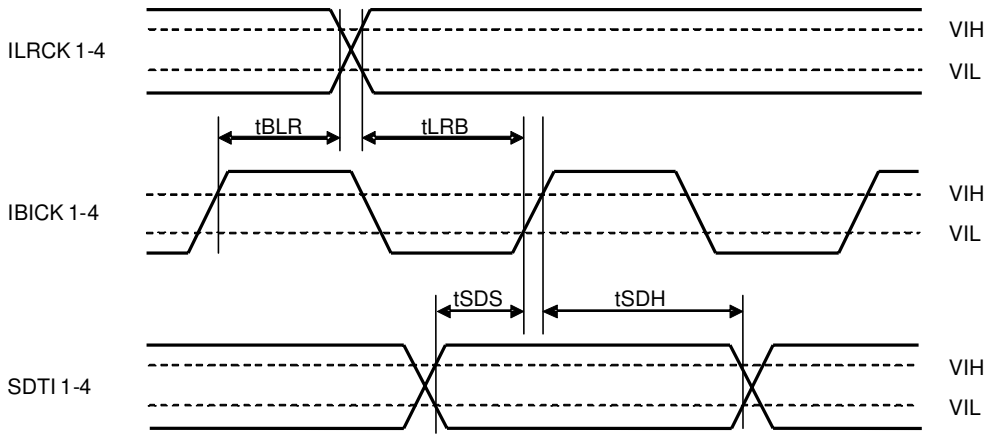


Figure 9. Input PORT Audio Interface Timing (Stereo Slave mode and TDM256 Slave Mode)

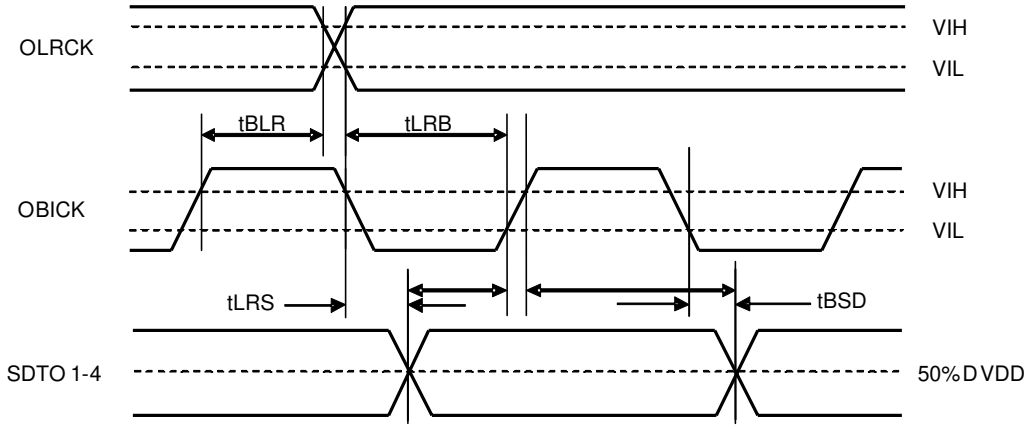


Figure 10. Output PORT Audio Interface Timing (TDM256 Slave mode & Stereo Slave mode)

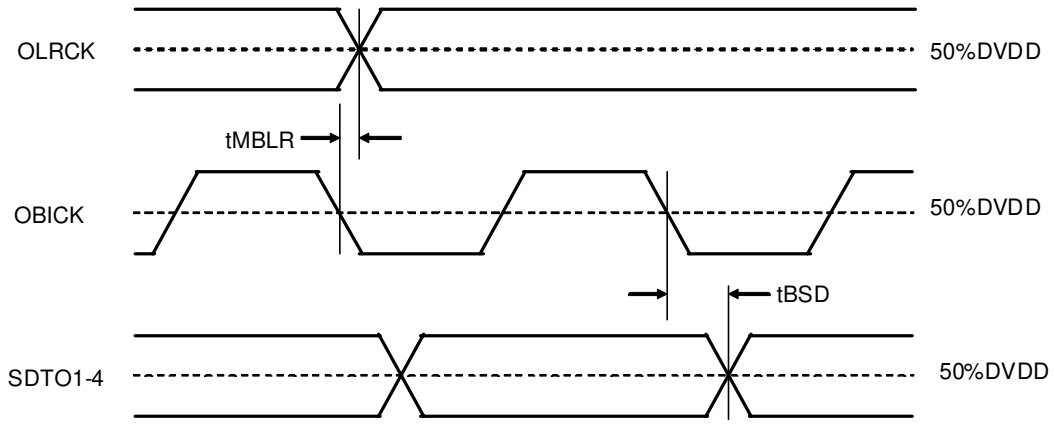


Figure 11. Output PORT Audio Interface Timing (TDM256 Master mode & Stereo Master mode)

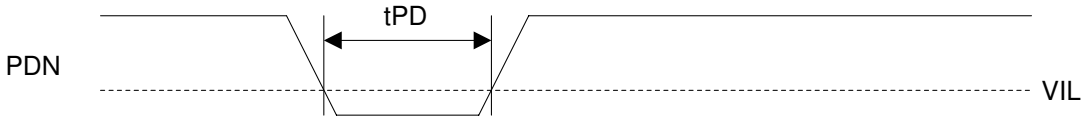


Figure 12. Power Down Timing

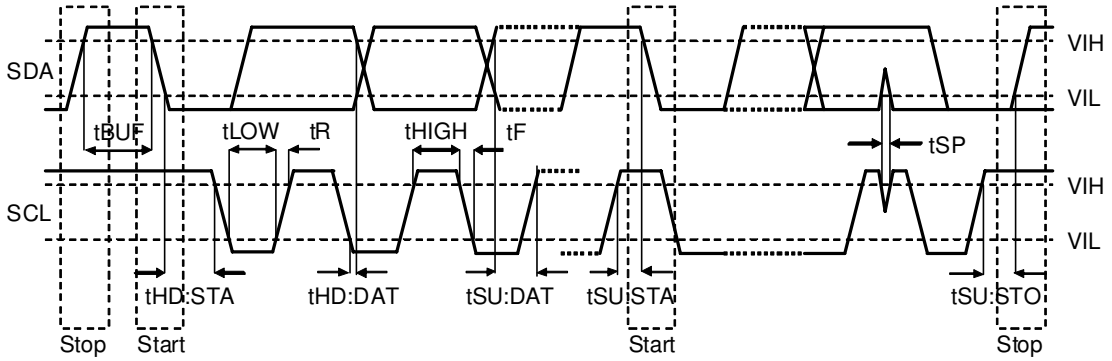


Figure 13. I^2C Bus Timing

OPERATION OVERVIEW

■ Synchronous and Asynchronous Modes Setting

There are two modes of operation: asynchronous and synchronous modes. The AK4128A is set to Synchronous mode when the INAS pin is "L" and it is set to Asynchronous mode when the INAS pin is "H".

FSI pin	Mode	Data	LRCK	BICK
L	Synchronous	SDTI1	ILRCK1 (Note 21)	IBICK1 (Note 22)
		SDTI2		
		SDTI3		
		SDTI4		
H	Asynchronous	SDTI1	ILRCK1	IBICK1
		SDTI2	ILRCK2	IBICK 2
		SDTI3	ILRCK3	IBICK 3
		SDTI4	ILRCK4	IBICK 4

Note 21. ILRCK2-4 pins must be connected to VSS2-5.
Note 22. IBICK2-4 pins must be connected to VSS2-5.

Table 1. Input Data Synchronous/Asynchronous Mode Setting

■ Audio Interface Format for Input PORT

The audio data format of input port is MSB first, 2's complement format. The SDTI1, SDTI2, SDTI3 and SDTI4 are latched on the rising edge of IBICK1, IBICK2, IBIXK3 and IBICK4 respectively.

In parallel control mode (SPB pin= "L"), IDIF2-0 pins control all audio interface formats of SRC1~4. IDIF2-0 pins must be set during the PDN pin= "L".

In serial control mode (SPB pin = "H"), setting of IDIF2-0 pins is ignored. IDIF[12:10] bits setting is reflected to SRC1, IDIF[22:20] bits setting is reflected to SRC2, IDIF[32:30] bits setting is reflected to SRC3, and IDIF[42:40] bits setting is reflected to SRC4.

IDIF[12:10] bits should be changed after all SDTO1 output codes become zero during soft mute by SMUTE1 bit = "1" or the SMUTE pin = "H". IDIF[22:20] bits should be changed after all SDTO2 output codes become zero during soft mute by SMUTE2 bit = "1" or the SMUTE pin = "H". IDIF[32:30] bits should be changed after all SDTO3 output codes become zero during soft mute by SMUTE3 bit = "1" or the SMUTE pin = "H". IDIF[42:40] bits should be changed after all SDTO4 output codes become zero during soft mute by SMUTE4 bit = "1" or the SMUTE pin = "H".

TDM mode (Mode 5/6) can be set in Synchronous Inputs mode (INAS pin = "L"). Serial data for 8channels should be input from the SDTI1 pin. In this mode, connect SDTI2-4 pins to VDD2-5 because there pins are ignored.

Asynchronous Inputs mode (INAS pin = "H") does not support TDM mode. The AK4128A is not able to operate correctly because of SDTI1-4 data inputs are incorrect. TDM mode is must be OFF, when using the AK4128A in asynchronous inputs mode (INAS pin = "H"). The maximum input frequency of IBICK1-4 is 256FSI.

Mode	IDIF2 Pin (Note 23)	IDIF1 Pin (Note 23)	IDIF0 Pin (Note 23)	SDTI1-4 Format	ILRCK 1-4	IBICK 1-4	IBICK1-4 Freq
0	L	L	L	16bit, LSB justified	Input	Input	≥ 32FSI
1	L	L	H	20bit, LSB justified			≥ 40FSI
2	L	H	L	24bit, MSB justified			≥ 48FSI
3	L	H	H	24 or 16bit, I²S Compatible			≥ 48FSI
				16bit, I²S Compatible			32FSI
4	H	L	L	24bit, LSB justified			≥ 48FSI
5	H	L	H	TDM 24bit, MSB justified			256FSI
6	H	H	X	TDM 24bit, I²S Compatible			256FSI

Table 2. Input PORT Audio Interface Format (Parallel Control Mode, SPB pin= "L") (X= Don't care)

Note 23. In serial control mode (SPB pin = "H"), setting of IDIF2-0 pins is ignored. IDIF[12:10] bits setting is reflected to SRC1, IDIF[22:20] bits setting is reflected to SRC2, IDIF[32:30] bits setting is reflected to SRC3, and IDIF[42:40] bits setting is reflected to SRC4.

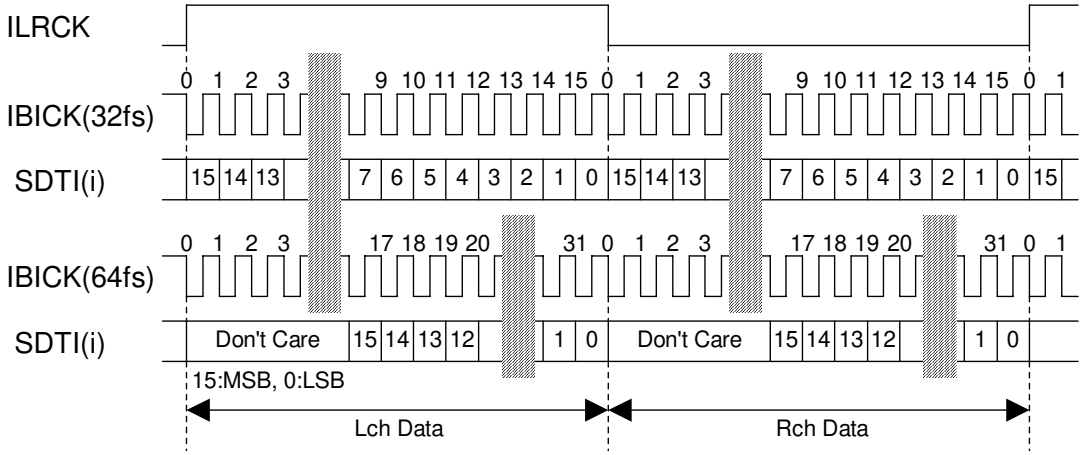


Figure 14. Mode 0 Timing (16bit, LSB justified)

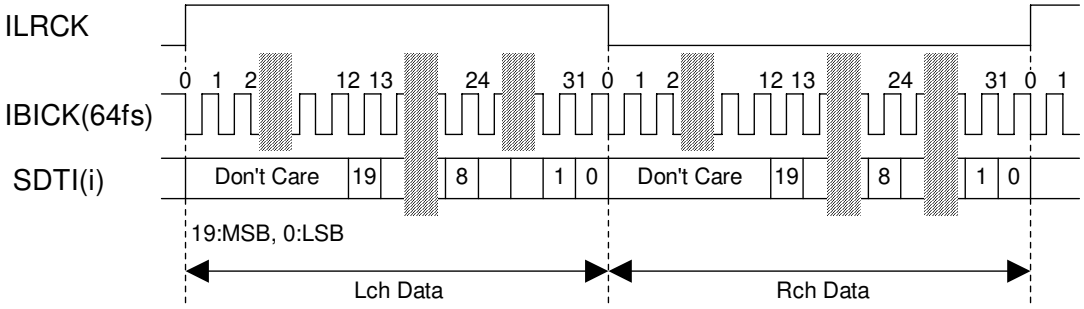


Figure 15. Mode 1 Timing (20bit, LSB justified)

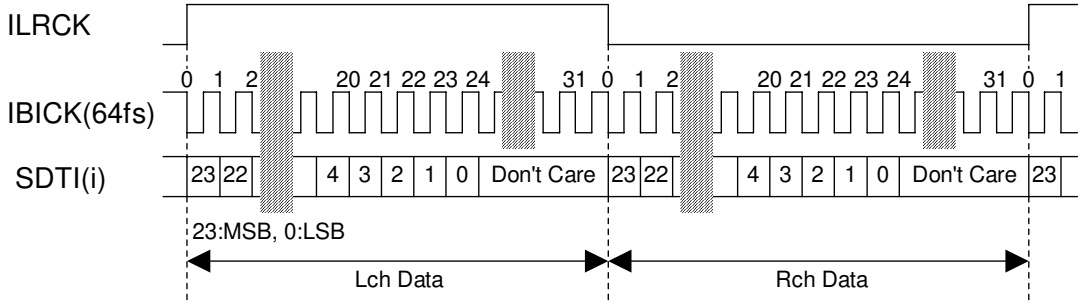


Figure 16. Mode 2 Timing (24bit, MSB justified)

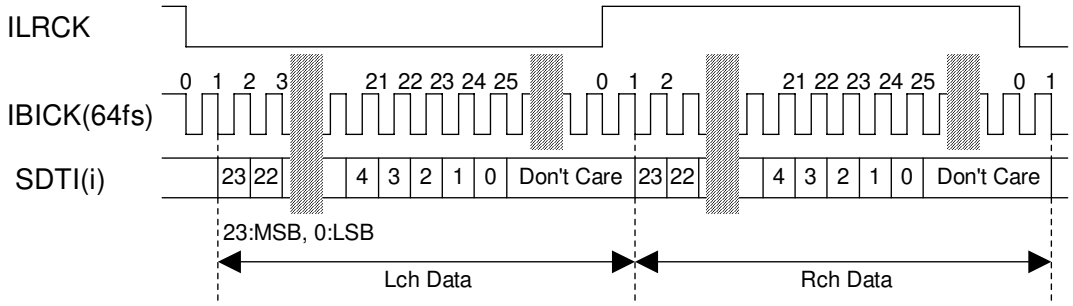


Figure 17. Mode 3 Timing (24bit I^2S)

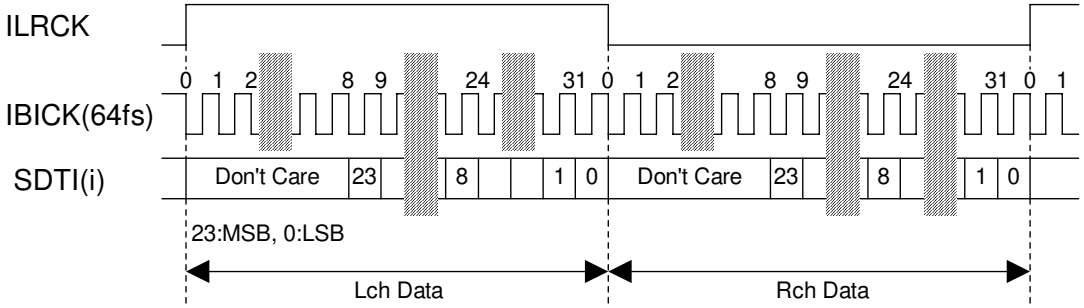


Figure 18. Mode 4 Timing (24bit, LSB justified)

Note: SDTI is identified as SDTI1, SDTI2, SDTI3 and SDTI4, ILRCK is identified as ILRCK1, ILRCK2, ILRCK3 and ILRCK4, IBICK is identified as IBICK1, IBICK2, IBICK3 and IBICK4.

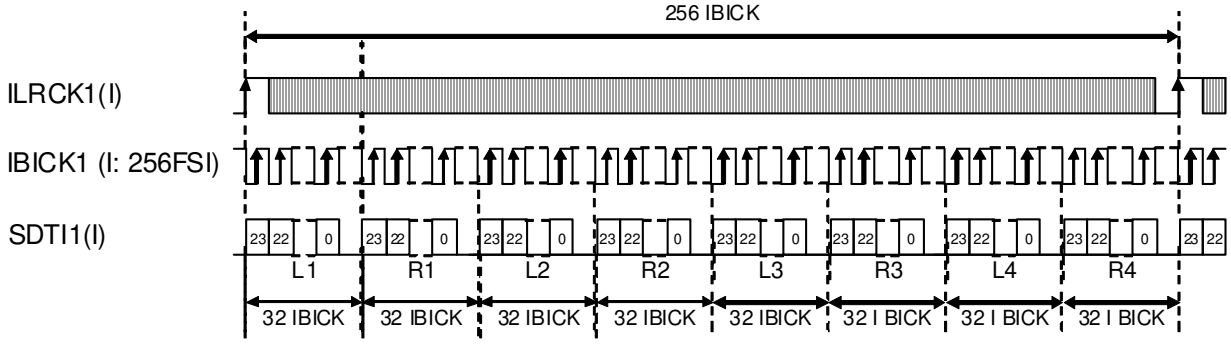


Figure 19. Mode 5 Timing (TDM, 24bit, MSB justified, SDTI2-4: Don't care)

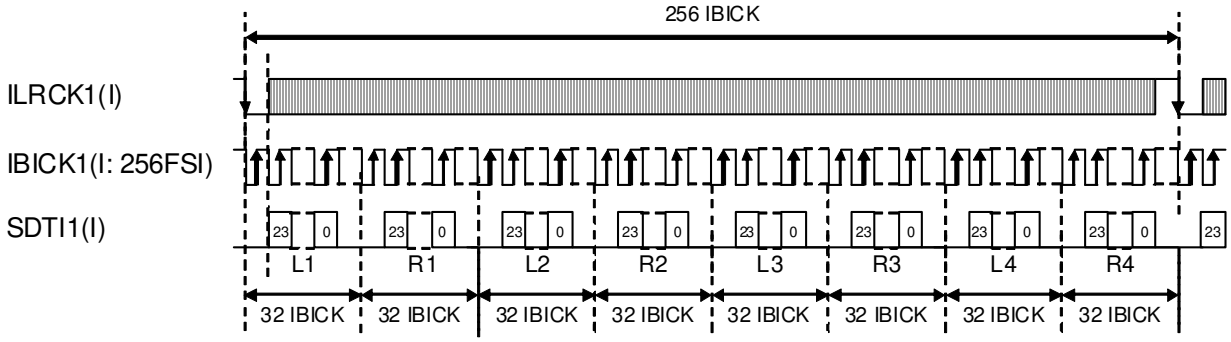


Figure 20. Mode 6 Timing (TDM, I^2S, SDTI2-4: Don't care)

■ System Clock for Output PORT

The output ports work in master mode and slave mode. The CM2-0 pins select the master/slave mode.

Mode	CM2 pin	CM1 pin	CM0 pin	Master / Slave	OMCLK/XTI Input	MCKO Output	FSO	FSO with X'tal
0	L	L	L	Master	256FSO	256FSO	8k~108kHz	44.1~96kHz
1	L	L	H	Master	384FSO	384FSO	8k~96kHz	29.4~64kHz
2	L	H	L	Master	512FSO	512FSO	8k~54kHz	22.05~48kHz
3	L	H	H	Master	768FSO	768FSO	8k~48kHz	14.7~32kHz
4	H	L	L	Slave	Not used. (Note 24)	OMCLK Input Clock	8k~216kHz	-
5	H	L	H	Master	128FSO (Note 25)	128FSO	8k~216kHz	88.2~192kHz
6	H	H	L	Slave(Bypass)	Not used. (Note 24)	IMCLK Input Clock	8k~216kHz	-
7	H	H	H	Master(Bypass)				

Note 24. Use for a clock input or connect to VSS2-5 pin. In Mode 4, the MCKO pin outputs "L" if the OMCLK/XTI pin is connected to VSS2-5. When a clock is input to the OMCLK/XTI pin, the clock is through and output from the MCKO pin. In Mode 6-7, OMCLK/XTI input is ignored internally.

Note 25. Output ports do not support TDM mode in this mode.

Table 3. Output PORT Master/Slave/ Bypass Mode Control (SPB pin = "L")

In serial control mode (SPB pin = "H"), the BYPS bit selects SRC bypass mode and SRC mode.
The default value of the BYPS bit is "0" (SRC mode).

Mode	CM2 pin	CM1 pin	CM0 pin	BYPS bit	Master / Slave	OMCLK/XTI Input	MCKO Output	FSO	FSO with X'tal
0	L	L	L	0	Master	256FSO	256FSO	8~108kHz	44.1~96kHz
1	L	L	H	0	Master	384FSO	384FSO	8~96kHz	29.4~64kHz
2	L	H	L	0	Master	512FSO	512FSO	8~54kHz	22.05~48kHz
3	L	H	H	0	Master	768FSO	768FSO	8k~48kHz	14.7~32kHz
4	H	L	L	0	Slave	Not used. (Note 26)	OMCLK Input Clock	8~216kHz	-
5	H	L	H	0	Master	128FSO (Note 25)	128FSO	8~216kHz	88.2~192kHz
6	H	H	L	0	Slave (Bypass)	Not used. (Note 26)	IMCLK Input Clock	8~216kHz	-
7	H	H	H	0	Master (Bypass)				
8	L	L	L	1	Master (Bypass)				
9	L	L	H	1	Master (Bypass)				
10	L	H	L	1	Master (Bypass)				
11	L	H	H	1	Master (Bypass)				
12	H	L	L	1	Slave (Bypass)				
13	H	L	H	1	Master (Bypass)				
14	H	H	L	1	Slave (Bypass)				
15	H	H	H	1	Master (Bypass)				

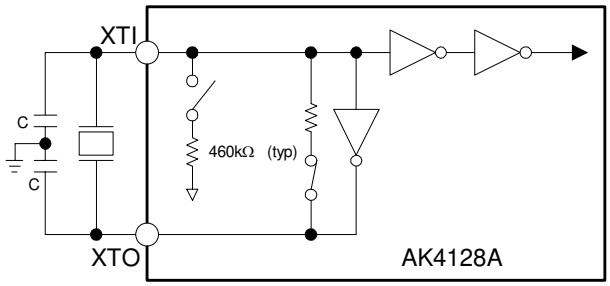
Note 26. Use for a clock input or connect to VSS2-5 pin. In Mode 4, the MCKO pin outputs "L" if the OMCLK/XTI pin is connected to VSS2-5. When a clock is input to the OMCLK/XTI pin, the clock is through and output from the MCKO pin. In Mode 6-15, OMCLK/XTI input is ignored internally.

Table 4. Output PORT Master/Slave/ Bypass Mode Control (SPB pin = "H")

(1) Master Mode

The OLRCK pin and OBICK pin are output pins in master mode. Master clock is supplied from the OMCLK/XTI pin. The clock for the OMCLK/XTI pin can be generated by the following methods: Connect a crystal oscillator between the OMCLK/XTI and XTO pins, or input a clock to the OMCLK/XTI pin. In bypass mode, the MCKO pin outputs IMCLK data.

a. X'tal



The OMCLK/XTI pin is pulled down when the PDN pin= "L".

Note: Refer to Table 5 for the capacitor and resistor values of the X'tal oscillator.

Figure 21. X'tal Mode

Nominal Frequency [MHz]	11.2896	12.288	24.576
Equivalent Series Resistance R1[Ω] max	60		
External Capacitance C[pF] max	15		

Table 5. Equivalent Series Resistor and External Capacitor for External X'tal Oscillator

In X'tal mode at 256FSO OMCLK input, FSO ranges from 44.1kHz to 96kHz.
In X'tal mode at 384FSO OMCLK input, FSO ranges from 29.4kHz to 64kHz.
In X'tal mode at 512FSO OMCLK input, FSO ranges from 22.05kHz to 48kHz.
In X'tal mode at 768FSO OMCLK input, FSO ranges from 14.7kHz to 32kHz.
In X'tal mode at 128FSO OMCLK input, FSO ranges from 88.2kHz to 192kHz.

b. External Clcok

- Note: Do not input the clock over DVDD1-4.

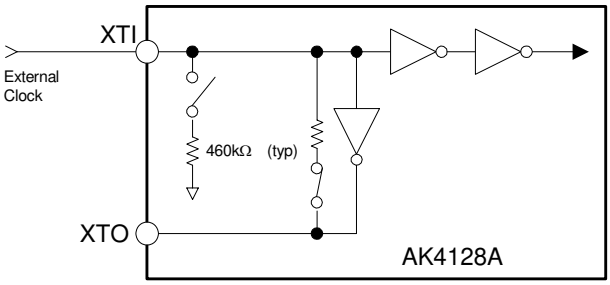


Figure 22. External Clock (OMCLK) mode

(2) Slave Mode

The OLRCK pin and OBICK pin are input pins in slave mode.

(3) SRC Bypass Mode

SRC bypass mode can be set in Synchronous inputs mode (INAS pin = "L"). Asynchronous inputs mode (INAS pin = "H") does not supports SRC bypass mode, so that the data is not transferred correctly on SDTI1→SDTO1, SDTI2→SDTO2, SDTI3→SDTO3 and SDTI4→SDTO4 lines. In Asynchronous inputs mode (INAS pin = "H"), the AK4128A should be used in SRC mode.

When the AK4128A is in slave mode, SDTI1-4 data are input by the ILRCK1 and IBICK1 clocks in SRC bypass mode (Table 2). The SDTI1-4 data are output from the OLRCK and OBICK pins in a format shown in Table 6 and Table 7. IBICK and OBICK must be synchronized but the phase is not critical. ILRCK and OLRCK must be synchronized but the phase is not critical.

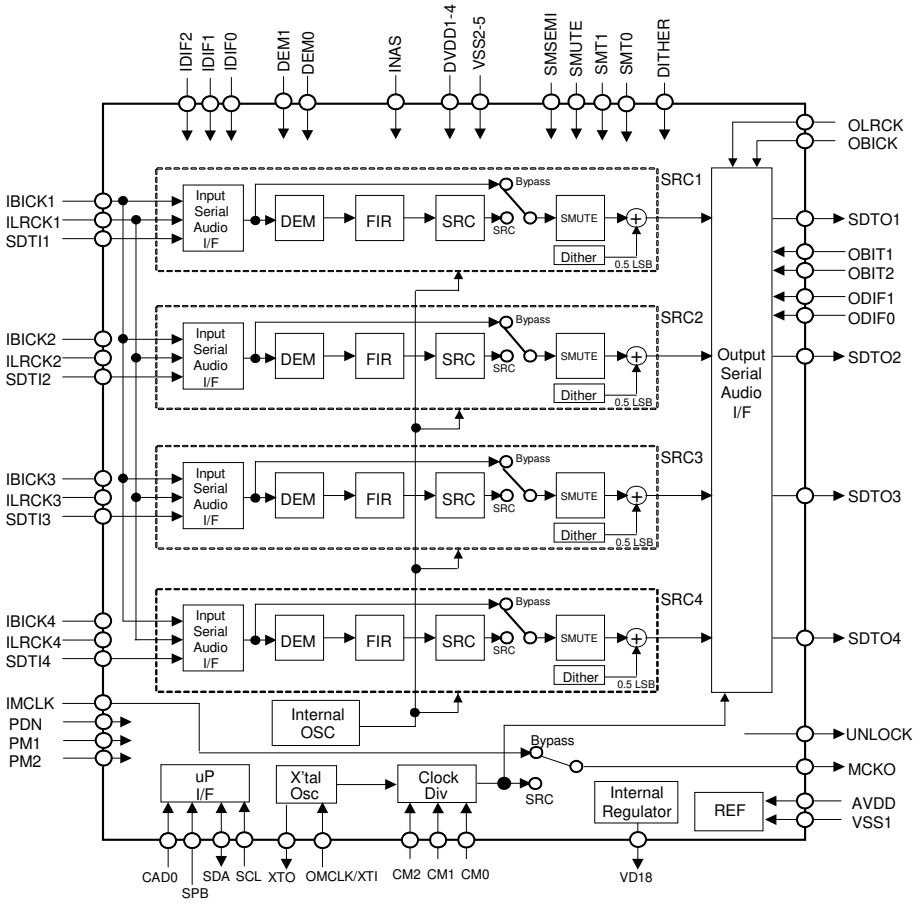


Figure 23. Bypass Mode in Slave Mode (Synchronous mode INAS pin = "L")