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AK4136
32bit 384kHz SRC

1. General Description

The AK4136 is a 2ch digital sample rate converter (SRC). The input sample rate ranges from 8kHz to 384kHz. The output sample rate is from 8kHz to 384kHz. The AK4136 has an internal Oscillator. Therefore it does not need any external master clocks and simplifies system configuration. The AK4136 is suitable for a high-resolution audio application interfacing to different sample rates such as Network Audios, USB DACs and Car Audios.

Application: AV Receivers, CD/SACD Players, Network Audios, USB DACs, USB Headphones, Sound Plate/Bars, Car Audios, Automotive External Amplifiers, Measuring Instruments, Control Systems, Public Audios (PA), IC-Recorders, Bluetooth Headphones, HD Audio/Voice Conference Systems

2. Features

- ☐ 2 channels input/output
- ☐ Asynchronous Sample Rate Converter
- ☐ PCM
  - Input Sample Rate Range (FSI): 8kHz ~ 384kHz
  - Output Sample Rate Range (FSO): 8kHz ~ 384kHz
- ☐ Input to Output Sample Rate Ratio: FSO/FSI = 1/6 ~ 12
- ☐ THD+N: Up to -140dB
- ☐ Dynamic Range: 176dB (A-weighted)
- ☐ I/F format: MSB justified, LSB justified, I2S compatible and TDM
- ☐ Oscillator for Internal Operation Clock
- ☐ Clock for Master mode: 128/192/256/384/512/768fso
- ☐ On-chip X'tal oscillator
- ☐ Digital De-emphasis Filter (32kHz, 44.1kHz, 48kHz) (Serial Mode Only)
- ☐ Soft Mute Function
- ☐ SRC Bypass mode (Master/Slave, PCM)
- ☐ uP Interface：I2C bus/SPI 4-wire
- ☐ Power Supply
  - DVDD: 3.0~3.6V (internal LDO enabled)
  - DVDD: 1.7~1.9V (internal LDO disabled)
- ☐ Ta: -40 ~ +105°C
- ☐ Package: 48-pin LQFP (0.5mm pitch)

3. Table of Contents

	AK4137	AK4136
bit	32	←
DR（A-Weighted）	186	176
THD+N	150	140
fsi	8 ~ 768kHz	8 ~ 384kHz
fso	8 ~ 768kHz	8 ~ 384kHz
Ratio I/O	1/6 ~ 24	1/6 ~ 12
Output Clock (Master Mode Operation)	64/128/256/384/512/768fso	128/256/384/512/768fso
SRC Conversion	PCM → PCM, DSD → DSD DSD → PCM, PCM → DSD DoP → DSD, DoP → PCM	PCM → PCM conversion only
SRC Bypass Function	Available (Master, Slave)	←
Soft Mute	Available Semi-Auto Mode Mute Time Setting Adjustment	Available Semi-Auto Mode and Mute Time Adjustment are only available by register settings.
DITHER	Available	Available (only by register settings)
De-emphasis	Available	Available (only by register settings)
Internal Regulator	3V→1.8V	←
External 1.8V Input	Available	←
Crystal Oscillator	Available	←
Pop Noise reduction on Rate Switching	Available	←
Micro Controller I/F	I2C, 4-wire	←

4. Block Diagram

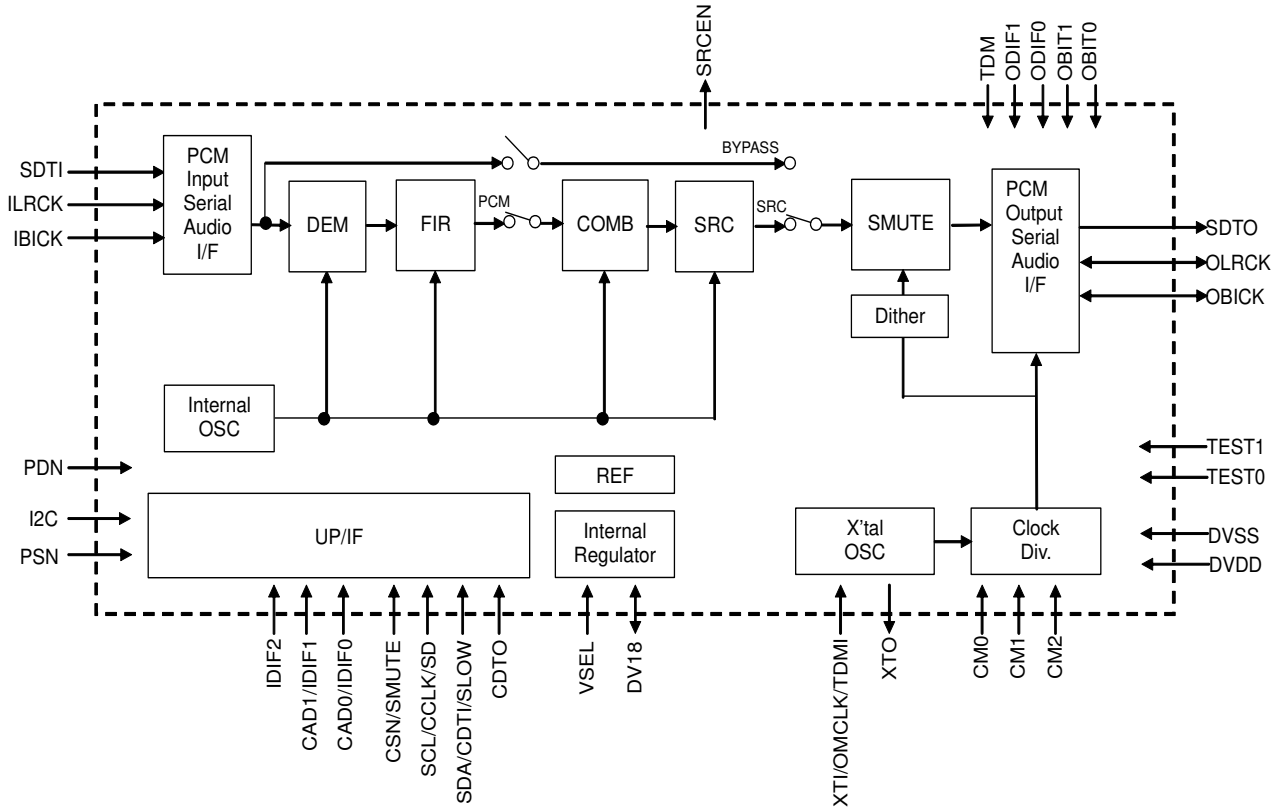


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations

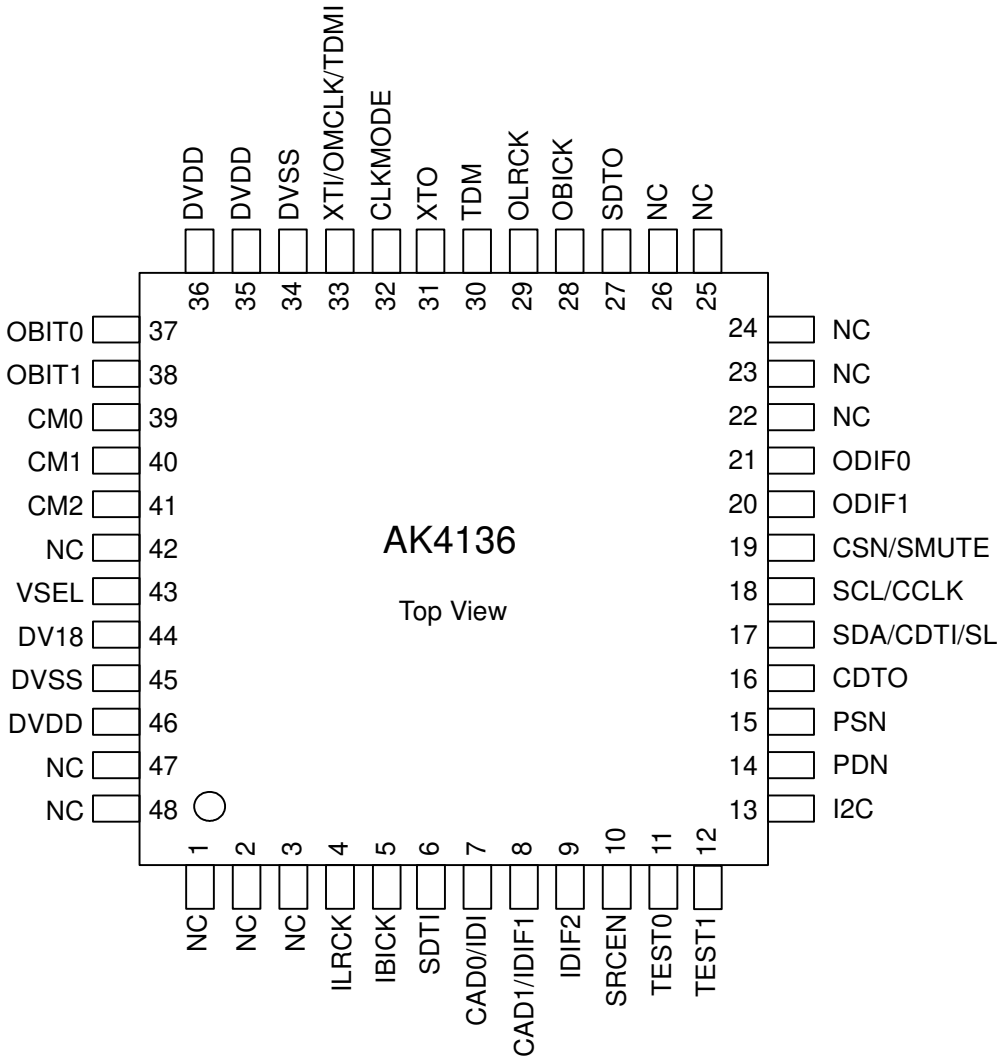


Figure 2. Pin Layout

■ **Pin Functions**

No.	Pin Name	I/O	Function
1	NC	-	This pin must be connected to DVSS.
2	NC	-	This pin must be connected to DVSS.
3	NC	-	This pin must be connected to DVSS.
4	ILRCK	I	L/R Clock Pin in PCM Mode
5	IBICK	I	Audio Serial Data Clock Pin in PCM Mode
6	SDTI	I	Audio Serial Data Input Pin in PCM Mode
7	CAD0	I	Chip Address 0 Pin in Serial Control Mode
	IDIF0	I	Digital Input Format 0 Pin in Parallel Control Mode
8	CAD1	I	Chip Address 1 Pin in Serial Control Mode
	IDIF1	I	Digital Input Format 1 Pin in Parallel Control Mode
9	IDIF2	I	Digital Input Format 2 Pin in Parallel Control Mode
10	SRCEN	O	Unlock Status Pin When the PDN pin= "L", this pin outputs "H".
11	TEST0	I	Test pin 0. Must be connected to DVSS in normal use.
12	TEST1	I	Test pin 1. Must be connected to DVSS in normal use.
13	I2C	I	Select serial mode "L": 4-wire serial Mode ,"H": I2C Mode
14	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initializes the control register. The AK4136 should be reset once by bringing PDN pin = "L" upon power-up.
15	PSN	I	Parallel/Serial Mode Select "L": Serial Mode , "H": Parallel Mode
16	CDTO	O	I2C= "L": Control Data Output Pin in Serial Control Mode
17	SDA	I/O	I2C= "H": Control Data In/Out Pin in Serial Control Mode
	CDTI	I	I2C= "L": Control Data Input Pin in Serial Control Mode
	SLOW	I	Digital Filter Select Pin in Parallel Control Mode
18	SCL	I	I2C= "H": Control Data Clock Input Pin in Serial Control Mode
	CCLK	I	I2C= "L": Control Data Clock Pin in Serial Control Mode
	SD	I	Digital Filter Select Pin in Parallel Control Mode
19	CSN	I	Chip Select Pin in Serial Control Mode, I2C= "L"
	SMUTE	I	Soft Mute Pin in Parallel Control Mode When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.
20	ODIF1	I	Audio Interface Format #1 Pin for Output PORT
21	ODIF0	I	Audio Interface Format #0 Pin for Output PORT
22	NC	-	This pin must be connected to DVSS.
23	NC	-	This pin must be connected to DVSS.
24	NC	-	This pin must be connected to DVSS.
25	NC	-	This pin must be connected to DVSS.
26	NC	-	This pin must be connected to DVSS.

Note 1. All input pins must not be allowed to float. DVDD must be connected to the same power supply.
Note 2. PSN, CM2-0, OBIT1-0, TDM, ODIF1-0, IDIF2-0 and CAD1-0 pins must be changed when the PDN pin = "L".

No.	Pin Name	I/O	Function
27	SDTO	O	Audio Serial Data Output Pin for Output PORT When the PDN pin = “L”, the SDTO pin outputs “L”.
28	OBICK	I/O	Audio Serial Data Clock Pin for Output PORT When the PDN pin = “L” in master mode, the OBICK pin outputs “L”.
29	OLRCK	I/O	Output Channel Clock Pin for Output PORT When the PDN pin = “L” in master mode, the OLRCK pin outputs “L”.
30	TDM	I	TDM Format Select Pin “L”(connected to DVSS): Stereo Mode “H”(connected to DVDD): TDM mode for Output
31	XTO	O	X’tal Output Pin When the PDN pin = “L” or CM2-0 pins = “HHL” or “HHH”, XTO outputs “L”.
32	CLKMODE	I	Master Clock Select Pin “L”(connected to DVSS): X'tal Mode “H”(connected to DVDD): External Master Clock or TDM pin = “H”
33	XTI	I	X’tal Input Pin
	OMCLK	I	External Master Clock Input
	TDMI	I	TDMI Daisy-Chain Input Pin
34	DVSS	-	Digital Ground Pin
35	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V or 1.7 ~ 1.9V
36	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V or 1.7 ~ 1.9V
37	OBIT0	I	Bit Length Select #0 Pin for Output Data
38	OBIT1	I	Bit Length Select #1 Pin for Output Data
39	CM0	I	Clock Select or Mode Select #0 Pin for Output PORT
40	CM1	I	Clock Select or Mode Select #1 Pin for Output PORT
41	CM2	I	Clock Select or Mode Select #2 Pin for Output PORT
42	NC	-	This pin must be connected to DVSS.
43	VSEL	I	Digital Power select “L”: DV18 is Output pin, “H”: DV18 is Power Supply Pin
44	DV18	I/O	Digital Power Pin, Typ 1.8V VSEL= “L”, Output When the PDN pin= “L”, the DV18 pin outputs “L”. Current must not be taken from this pin. A 10μF (±30%; including the temperature characteristics) capacitor should be connected between this pin and DVSS. When this capacitor is polarized, the positive polarity pin should be connected to the DV18 pin. VSEL= “H”, Input
45	DVSS	-	Digital Ground Pin
46	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V or 1.7 ~ 1.9V
47	NC	-	This pin must be connected to DVSS.
48	NC	-	This pin must be connected to DVSS.

Note 1. All input pins must not be allowed to float. DVDD must be connected to the same power supply.
Note 2. PSN, CM2-0, OBIT1-0, TDM, ODIF1-0, IDIF2-0 and CAD1-0 pins must be changed when the PDN pin = “L”.

*Unused Input/Output Pins

Classification	Pin Name	Setting
Digital	CSN/SMUTE	Connect to DVSS
	XTI/OMCLK/TDMI	Connect to DVSS (Slave Mode)
	SRCEN, XTO, CDTO	Open

* The status of OLRCK and OBICK pins, when the PDN pin = “L”, are shown below. (“L” output in Master mode)

Setting Pins			OLRCK, OBICK
CM2	CM1	CM0	
L	L	L	“L” Output
L	L	H	
L	H	L	
L	H	H	
H	L	L	Input
H	L	H	“L” Output
H	H	L	
H	H	H	

* The output pin status when the PDN pin = “L” is shown below.

Output Pin	Status
SDTO	“L” Output
SRCEN	“H” Output
XTO	“L” Output
CDTO	Hi-z

6. Absolute Maximum Ratings

(DVSS=0V; Note 3)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Digital	DVDD	-0.3	4.3	V
	(Internal Digital) (Note 4)	DV18	-0.3	2.5	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 5)		VDIN	-0.3	(DVDD+0.3) or 4.3	V
Ambient Temperature (Power applied) (Note 6)		Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 3. All voltages are with respect to ground.
Note 4. DVSS must be connected to the same ground.
Note 5. ILRCK,IBICK, SDTI, IDIF0/CAD0, IDIF1/CAD1, IDIF2, PDN, PSN, I2C, SLOW/CDTI/SDA, SD/CCLK/SCL, SMUTE/CSN, OBIT1-0, ODIF1-0,CM2-0, VSEL, TEST1-0 pin
Note 6. In the case that the PCB wiring density is more than 100%

WARING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(DVSS=0V; Note 3; VSEL= "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Digital	DVDD	3.0	3.3	3.6	V

(DVSS=0V; Note 3; VSEL= "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies:	Digital	DVDD	1.7	1.8	1.9	V
(Note 7)	Digital	DV18	1.7	1.8	1.9	V
	Difference	DVDD- DV18	-	0	-	V

Note 3. All voltages are with respect to ground.
Note 7. DVDD and DV18 should be connected externally.

The PDN pin must be "L" when power up the AK4136. Set the PDN pin to "H" after all power supplies are ON. Writing by a microcontroller should be executed with a 5ms interval after the PDN pin = "H".

8. SRC Characteristics

■ **PCMIN → PCMOUT**

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V; DVSS=0V; Signal Frequency = 1kHz; data = 32bit; measurement bandwidth = 20Hz~FSO/2; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Resolution				32	Bits
Input Sample Rate	FSI	8		384	kHz
Output Sample Rate	FSO	8		384	kHz
THD+N (Input = 1kHz, 0dBFS)					
FSO/FSI = 48kHz/48kHz		-	-140	-	dB
FSO/FSI = 48kHz/44.1kHz		-	-133	-	dB
FSO/FSI = 48kHz/192kHz		-	-143	-	dB
FSO/FSI = 192kHz/48kHz		-	-134	-	dB
Worst Case (FSO/FSI=32kHz/176.4kHz)		-	-	-100	dB
Dynamic Range (Input = 1kHz, -60dBFS)					
FSO/FSI = 48kHz/44.1kHz		-	170	-	dB
FSO/FSI = 48kHz/192kHz		-	174	-	dB
FSO/FSI = 192kHz/48kHz		-	170	-	dB
FSO/FSI = 32kHz/176.4kHz		-	170	-	dB
Worst Case (FSO/FSI = 48kHz/48kHz)		168	-	-	dB
Dynamic Range (Input = 1kHz, -60dBFS, A-weighted)					
FSO/FSI = 8kHz/48kHz		-	176	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1/6		12	-

9. Power Consumptions

■ Internal LDO Mode

(Ta=-40~ +105°C; DVDD=3.0~3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Current					
Normal operation: (PDN = "H")					
FSI=FSO=48kHz at Master Mode : DVDD=3.3V		-	11	-	mA
FSI=FSO=192kHz at Master Mode: DVDD=3.3V		-	33	-	mA
FSI=FSO=384kHz at Master Mode: DVDD=3.3V		-	40	-	mA
: DVDD=3.6V		-	-	60	mA
Power down: PDN pin = "L" (Note 8)					
DVDD=3.6V			10	100	μA

Note 8. All digital inputs including clock pins are held to DVSS.

■ DV18 External Supply Mode

(Ta=-40~ +105°C; DVDD=DV18=1.7~1.9V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Current					
Normal operation:					
FSI=FSO=48kHz at Master Mode : DVDD＝DV18=1.8V		-	11	-	mA
FSI=FSO=192kHz at Master Mode: DVDD＝DV18=1.8V		-	28	-	mA
FSI=FSO=384kHz at Master Mode: DVDD＝DV18=1.8V		-	32	-	mA
: DVDD＝DV18=1.9V		-	-	50	mA
Power down: PDN pin = "L" (Note 8)					
DVDD=DV18=1.9V			10	100	μA

Note 8. All digital inputs including clock pins are held to DVSS.

10. Filter Characteristics

■ Sharp Roll-Off Filter Characteristics

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V, DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband −0.01dB	0.985 ≤ FSO/FSI ≤ 12.000	PB	0	-	0.4583FSI	kHz
	0.905 ≤ FSO/FSI < 0.985	PB	0	-	0.4167FSI	kHz
	0.714 ≤ FSO/FSI < 0.905	PB	0	-	0.3195FSI	kHz
	0.656 ≤ FSO/FSI < 0.714	PB	0	-	0.2852FSI	kHz
	0.536 ≤ FSO/FSI < 0.656	PB	0	-	0.2182FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0	-	0.2177FSI	kHz
	0.452 ≤ FSO/FSI < 0.492	PB	0	-	0.1948FSI	kHz
	0.357 ≤ FSO/FSI < 0.452	PB	0	-	0.1458FSI	kHz
	0.324 ≤ FSO/FSI < 0.357	PB	0	-	0.1302FSI	kHz
	0.246 ≤ FSO/FSI < 0.324	PB	0	-	0.0917FSI	kHz
	0.226 ≤ FSO/FSI < 0.246	PB	0	-	0.0826FSI	kHz
	0.1667 ≤ FSO/FSI < 0.226	PB	0	-	0.0583FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 12.000	SB	0.5417FSI	-	-	kHz
	0.905 ≤ FSO/FSI < 0.985	SB	0.5021FSI	-	-	kHz
	0.714 ≤ FSO/FSI < 0.905	SB	0.3965FSI	-	-	kHz
	0.656 ≤ FSO/FSI < 0.714	SB	0.3643FSI	-	-	kHz
	0.536 ≤ FSO/FSI < 0.656	SB	0.2974FSI	-	-	kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2813FSI	-	-	kHz
	0.452 ≤ FSO/FSI < 0.492	SB	0.2604FSI	-	-	kHz
	0.357 ≤ FSO/FSI < 0.452	SB	0.2116FSI	-	-	kHz
	0.324 ≤ FSO/FSI < 0.357	SB	0.1969FSI	-	-	kHz
	0.246 ≤ FSO/FSI < 0.324	SB	0.1573FSI	-	-	kHz
	0.226 ≤ FSO/FSI < 0.246	SB	0.1471FSI	-	-	kHz
	0.1667 ≤ FSO/FSI < 0.226	SB	0.1020FSI	-	-	kHz
Passband Ripple	0.226 ≤ FSO/FSI ≤12.000	PR	-	-	±0.01	dB
	0.1667 ≤ FSO/FSI < 0.226	PR	-	-	±0.03	dB
Stopband Attenuation	0.985 ≤ FSO/FSI ≤ 12.000	SA	140.2	-	-	dB
	0.905 ≤ FSO/FSI < 0.985	SA	140.9	-	-	dB
	0.714 ≤ FSO/FSI < 0.905	SA	135.2	-	-	dB
	0.656 ≤ FSO/FSI < 0.714	SA	135.1	-	-	dB
	0.536 ≤ FSO/FSI < 0.656	SA	133.5	-	-	dB
	0.492 ≤ FSO/FSI < 0.536	SA	115.3	-	-	dB
	0.452 ≤ FSO/FSI < 0.492	SA	118.2	-	-	dB
	0.357 ≤ FSO/FSI < 0.452	SA	123.3	-	-	dB
	0.324 ≤ FSO/FSI < 0.357	SA	122.9	-	-	dB
	0.246 ≤ FSO/FSI < 0.324	SA	117.9	-	-	dB
	0.226 ≤ FSO/FSI < 0.246	SA	119.7	-	-	dB
	0.1667 ≤ FSO/FSI < 0.226	SA	90.3	-	-	dB
Group Delay (Note 9)		GD	-	64	-	1/fs

Note 9. This is the time from a rising edge of ILRCK after L and R channels data is input to a rising edge of OLRCK before the L and R channels data is output, when there is no phase difference between input and output data.

■ **Slow Roll-Off Filter Characteristics**

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V, DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband −0.01dB	0.1667 ≤ FSO/FSI < 12.000	PB	0	-	0.0417FSI	kHz
Stopband	0.1667 ≤ FSO/FSI < 12.000	SB	0.4167FSI	-		kHz
Passband Ripple		PR	-	-	±0.01	dB
Stopband Attenuation		SA	-	108.1	-	dB
Group Delay (Note 9)		GD	-	64	-	1/fs

Note 9. This is the time from a rising edge of ILRCK after L and R channels data is input to a rising edge of OLRCK before the L and R channels data is output, when there is no phase difference between input and output data.

■ **Short Delay Sharp Roll-Off Filter Characteristics**

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V, DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband −0.01dB	0.985 ≤ FSO/FSI ≤ 12.000	PB	0	-	0.4583FSI	kHz
	0.905 ≤ FSO/FSI < 0.985	PB	0	-	0.4167FSI	kHz
	0.714 ≤ FSO/FSI < 0.905	PB	0	-	0.3195FSI	kHz
	0.656 ≤ FSO/FSI < 0.714	PB	0	-	0.2852FSI	kHz
	0.536 ≤ FSO/FSI < 0.656	PB	0	-	0.2182FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0	-	0.2177FSI	kHz
	0.452 ≤ FSO/FSI < 0.492	PB	0	-	0.1948FSI	kHz
	0.357 ≤ FSO/FSI < 0.452	PB	0	-	0.1458FSI	kHz
	0.324 ≤ FSO/FSI < 0.357	PB	0	-	0.1302FSI	kHz
	0.246 ≤ FSO/FSI < 0.324	PB	0	-	0.0917FSI	kHz
	0.226 ≤ FSO/FSI < 0.246	PB	0	-	0.0826FSI	kHz
	0.1667 ≤ FSO/FSI < 0.226	PB	0	-	0.0583FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 12.000	SB	0.5417FSI	-	-	kHz
	0.905 ≤ FSO/FSI < 0.985	SB	0.5021FSI	-	-	kHz
	0.714 ≤ FSO/FSI < 0.905	SB	0.3965FSI	-	-	kHz
	0.656 ≤ FSO/FSI < 0.714	SB	0.3643FSI	-	-	kHz
	0.536 ≤ FSO/FSI < 0.656	SB	0.2974FSI	-	-	kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2813FSI	-	-	kHz
	0.452 ≤ FSO/FSI < 0.492	SB	0.2604FSI	-	-	kHz
	0.357 ≤ FSO/FSI < 0.452	SB	0.2116FSI	-	-	kHz
	0.324 ≤ FSO/FSI < 0.357	SB	0.1969FSI	-	-	kHz
	0.246 ≤ FSO/FSI < 0.324	SB	0.1573FSI	-	-	kHz
	0.226 ≤ FSO/FSI < 0.246	SB	0.1471FSI	-	-	kHz
	0.1667 ≤ FSO/FSI < 0.226	SB	0.1020FSI	-	-	kHz
Passband Ripple	0.226 ≤ FSO/FSI ≤ 12.000	PR	-	-	±0.01	dB
	0.1667 ≤ FSO/FSI < 0.226	PR	-	-	±0.03	dB
Stopband Attenuation	0.985 ≤ FSO/FSI ≤ 24.000	SA	140.2	-	-	dB
	0.905 ≤ FSO/FSI < 0.985	SA	140.9	-	-	dB
	0.714 ≤ FSO/FSI < 0.905	SA	135.2	-	-	dB
	0.656 ≤ FSO/FSI < 0.714	SA	135.1	-	-	dB
	0.536 ≤ FSO/FSI < 0.656	SA	133.5	-	-	dB
	0.492 ≤ FSO/FSI < 0.536	SA	115.3	-	-	dB
	0.452 ≤ FSO/FSI < 0.492	SA	118.2	-	-	dB
	0.357 ≤ FSO/FSI < 0.452	SA	123.3	-	-	dB
	0.324 ≤ FSO/FSI < 0.357	SA	122.9	-	-	dB
	0.246 ≤ FSO/FSI < 0.324	SA	117.9	-	-	dB
	0.226 ≤ FSO/FSI < 0.246	SA	119.7	-	-	dB
	0.1667 ≤ FSO/FSI < 0.226	SA	90.3	-	-	dB
Group Delay (Note 9)	0.905 ≤ FSO/FSI ≤ 12.000	GD	-	20	-	1/fs
	0.656 ≤ FSO/FSI < 0.905	GD	-	22	-	1/fs
	0.536 ≤ FSO/FSI < 0.656	GD	-	26	-	1/fs
	0.492 ≤ FSO/FSI < 0.536	GD	-	23	-	1/fs
	0.452 ≤ FSO/FSI < 0.492	GD	-	24	-	1/fs
	0.324 ≤ FSO/FSI < 0.452	GD	-	26	-	1/fs
	0.246 ≤ FSO/FSI < 0.324	GD	-	29	-	1/fs
	0.226 ≤ FSO/FSI < 0.246	GD	-	30	-	1/fs
	0.1667 ≤ FSO/FSI < 0.226	GD	-	32	-	1/fs

Note 9. This is the time from a rising edge of ILRCK after L and R channels data is input to a rising edge of OLRCK before the L and R channels data is output, when there is no phase difference between input and output data.

■ **Short Delay Slow Roll-Off Filter Characteristics**

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V, DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband −0.01dB	0.1667≤FSO/FSI < 12.000	PB	0	-	0.0417FSI	kHz
Stopband	0.1667≤FSO/FSI < 12.000	SB	0.4167FSI	-		kHz
Passband Ripple		PR	-	-	±0.01	dB
Stopband Attenuation		SA	-	108.1	-	dB
Group Delay (Note 9)		GD	-	21	-	1/fs

Note 9. This is the time from a rising edge of ILRCK after L and R channels data is input to a rising edge of OLRCK before the L and R channels data is output, when there is no phase difference between input and output data.

11. Input and Output Examples

Possible Input and Output data combinations are shown below.
Fsi is the sampling rate of input data, and Fso is the sampling rate of output data.

Fsi[kHz]	Fso[kHz]	
PCM	PCM	
	min	max
8	8	96
11.025	8	132.3
16	8	192
32	8	384
44.1	8	384
48	8	384
88.2	14.7	384
96	16	384
176.4	29.6	384
192	32	384

When the input data is 384 kHz and down converted, THD+N may degrade to 80dB.

12. DC Characteristics

(Ta=-40~ +105°C; DVDD=3.0~3.6V: VSEL pin = "L" or DVDD=DV18=1.7V~1.9V: VSEL pin = "H")

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage					
Except SDA pin (Iout=−400μA)	VOH	DVDD−0.4	-	-	V
Low-Level Output Voltage					
Except SDA pin (Iout=400μA)	VOL	-	-	0.4	V
SDA pin (Iout=3mA)	VOL			0.4	V
Input Leakage Current	Iin	-	-	±10	μA

13.Switching Characteristics

(Ta=-40~ +105°C; DVDD=3.0~3.6V: VSEL pin = "L" or DVDD=DV18=1.7V~1.9V: VSEL pin = "H"; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
Crystal Oscillator Frequency (256 times of 44.1, 48, 88.2 or 96kHz)	fXTAL	11.2896	-	24.576	MHz
OMCLK Input					
128 FSO:	fCLK	1.024		49.152	MHz
Pulse Width Low	tCLKL	7			ns
Pulse Width High	tCLKH	7			ns
256 FSO:	fCLK	2.048		49.152	MHz
Pulse Width Low	tCLKL	7			ns
Pulse Width High	tCLKH	7			ns
384 FSO:	fCLK	3.072		36.864	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns
512 FSO:	fCLK	4.096		49.152	MHz
Pulse Width Low	tCLKL	7			ns
Pulse Width High	tCLKH	7			ns
768 FSO:	fCLK	6.144		36.864	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input PORT ILRCK					
Frequency					kHz
Normal speed mode	FSIN	8		54	kHz
Double speed mode	FSID	54		108	kHz
Quad speed mode	FSIQ	108		216	kHz
Oct speed mode	FSIO		384		kHz
Duty Cycle Slave Mode	Duty	48	50	52	%
Output PORT OLRCK					
Frequency					
Slave mode					
Normal speed mode	FSON	8		54	kHz
Double speed mode	FSOD	54		108	kHz
Quad speed mode	FSOQ	108		216	kHz
Oct speed mode	FSOO		384		kHz
Master mode					
OMCLK Input, 128FSO mode	FSO	8		384	kHz
OMCLK Input, 256FSO mode	FSO	8		192	kHz
OMCLK Input, 384FSO mode	FSO	8		96	kHz
OMCLK Input, 512FSO mode	FSO	8		96	kHz
OMCLK Input, 768FSO mode	FSO	8		48	kHz
Duty Cycle					
Slave Mode	Duty	48	50	52	%
Master Mode	Duty		50		%
Input PORT ILRCK for TDM256 Mode					
Frequency	FSI	8		96	kHz
“H” time (slave mode)	tLRH	1/256FSI			ns
“L” time (slave mode)	tLRL	1/256FSI			ns
Input PORT ILRCK for TDM512 Mode					
Frequency	FSI	8		48	kHz
“H” time (slave mode)	tLRH	1/512FSI			ns
“L” time (slave mode)	tLRL	1/512FSI			ns
Output PORT OLRCK for TDM256 Mode					
Frequency	FSO	8		96	kHz
“H” time (slave mode)	tLRH	1/256 FSO			ns
“L” time (slave mode)	tLRL	1/256 FSO			ns
Output PORT OLRCK for TDM512 Mode					
Frequency	FSO	8		48	kHz
“H” time (slave mode)	tLRH	1/512 FSO			ns
“L” time (slave mode)	tLRL	1/512 FSO			ns

Parameter		Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing						
Input PORT (Slave mode)						
IBICK Period						
Normal speed mode		tBCK	1/256 FSIN			ns
Double speed mode		tBCK	1/128 FSID			ns
Quad speed mode		tBCK	1/64 FSIQ			ns
Oct speed mode		tBCK	1/64 FSIO			ns
IBICK Pulse Width Low		tBCKL	16			ns
IBICK Pulse Width High		tBCKH	16			ns
ILRCK Edge to IBICK "↑"	(Note 10)	tLRB	10			ns
IBICK "↑" to ILRCK Edge	(Note 10)	tBLR	10			ns
SDTI Hold Time from IBICK "↑"		tSDH	10			ns
SDTI Setup Time to IBICK "↑"		tSDS	6			ns
Input PORT (TDM256 slave mode)						
IBICK Period		tBCK	40			ns
IBICK Pulse Width Low		tBCKL	16			ns
IBICK Pulse Width High		tBCKH	16			ns
ILRCK Edge to IBICK "↑"	(Note 10)	tLRB	10			ns
IBICK "↑" to ILRCK Edge	(Note 10)	tBLR	10			ns
SDTI Hold Time from IBICK "↑"		tSDH	10			ns
SDTI Setup Time to IBICK "↑"		tSDS	6			ns
Input PORT (TDM512 slave mode)						
IBICK Period		tBCK	40			ns
IBICK Pulse Width Low		tBCKL	16			ns
IBICK Pulse Width High		tBCKH	16			ns
ILRCK Edge to IBICK "↑"	(Note 10)	tLRB	10			ns
IBICK "↑" to ILRCK Edge	(Note 10)	tBLR	10			ns
SDTI Hold Time from IBICK "↑"		tSDH	10			ns
SDTI Setup Time to IBICK "↑"		tSDS	6			ns

Note 10. IBICK rising edge must not occur at the same time as ILRCK edge.
Note 11. Maximum frequency of IBICK and OBICK is 24.576MHz.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing					
Output PORT (Slave mode)					
OBICK Period					
Normal speed mode	tBCK	1/256 FSON			
Double speed mode	tBCK	1/128 FSOD			
Quad speed mode	tBCK	1/64 FSOQ			
Oct speed mode	tBCK	1/64 FSOO			
OBICK Pulse Width Low	tBCKL	16			ns
OBICK Pulse Width High	tBCKH	16			ns
OLRCK Edge to OBICK "↑" (Note 10)	tLRB	10			ns
OBICK "↑" to OLRCK Edge (Note 10)	tBLR	10			ns
DVDD=3.0V~3.6V (VSEL pin= "L")					
OLRCK to SDTO(MSB) (Except I^2S mode)	tLRS			10	ns
OBICK "↓" to SDTO	tBSD			10	ns
DVDD=1.7V~1.9V (VSEL pin= "H") (Except fso=384kHz)					
OLRCK to SDTO(MSB) (Except I^2S mode)	tLRS			20	ns
OBICK "↓" to SDTO	tBSD			20	ns

Note 10. IBICK rising edge must not occur at the same time as ILRCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing					
Output PORT (TDM256 slave mode)					
DVDD=3.0V～3.6V (VSEL pin= "L")					
OBICK Period	tBCK	40			ns
OBICK Pulse Width Low	tBCKL	16			ns
OBICK Pulse Width High	tBCKH	16			ns
OLRCK Edge to OBICK "↑" (Note 10)	tLRB	10			ns
OBICK "↑" to OLRCK Edge (Note 10)	tBLR	10			ns
OBICK "↓" to SDTO	tBSD			10	ns
DVDD=1.7V～1.9V (VSEL pin= "H")					
OBICK Period	tBCK	80			ns
OBICK Pulse Width Low	tBCKL	32			ns
OBICK Pulse Width High	tBCKH	32			ns
OLRCK Edge to OBICK "↑" (Note 10)	tLRB	20			ns
OBICK "↑" to OLRCK Edge (Note 10)	tBLR	20			ns
OBICK "↓" to SDTO	tBSD			20	sn
Output PORT (TDM512 slave mode)					
DVDD=3.0V～3.6V(VSEL pin= "L")					
OBICK Period	tBCK	40			ns
OBICK Pulse Width Low	tBCKL	16			ns
OBICK Pulse Width High	tBCKH	16			ns
OLRCK Edge to OBICK "↑" (Note 10)	tLRB	10			ns
OBICK "↑" to OLRCK Edge (Note 10)	tBLR	10			ns
OBICK "↓" to SDTO	tBSD			10	ns
Output PORT (Master mode)					
OBICK Frequency	fBCK		64 FSO		Hz
OBICK Duty	dBCK		50		%
OBICK "↓" to OLRCK Edge	tMBLR	−5		5	ns
OBICK "↓" to SDTO	tBSD	−5		5	ns
Reset Timing					
PDN "L" Width after DVDD is on. (Note 13)	tAPD1	150			ns
PDN Accept Pulse Width (Note 13)	tAPD2	700			ms
PDN pin Pulse Width of Spike Noise Suppressed by Input Filter (Note 14)	tPDS	0		50	ns

Note 10. IBICK rising edge must not occur at the same time as ILRCK edge.
Note 12. TDM modes are only supported in slave mode.
Note 13. The AK4136 can be reset by bringing the PDN pin = "L".
Note 14. "L" pulse width of spike noise suppressed by input filter of the PDN pin.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing					
CCLK Period	tCCK	200		-	ns
CCLK Pulse Width High	tCCKH	80		-	ns
CCLK Pulse Width Low	tCCKL	80		-	ns
CDTI Setup Time	tCDS	50		-	ns
CDTI Hold Time	tCDH	50		-	ns
CSN High Time	tCSW	150		-	ns
CSN "↓" to CCLK "↑"	tCSS	50		-	ns
CCLK "↑" to CSN "↑"	tCSH	50		-	ns
CCLK "↓" to CDTO	tDCD			45	ns
CSN "↑" to CDTO "Hi-Z"	tCCZ			70	ns
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	μs
Clock Low Time	tLOW	1.3		-	μs
Clock High Time	tHIGH	0.6		-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	μs
SDA Hold Time from SCL Falling (Note 15)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	μs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6		-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF

Note 15. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

■ Timing Diagrams

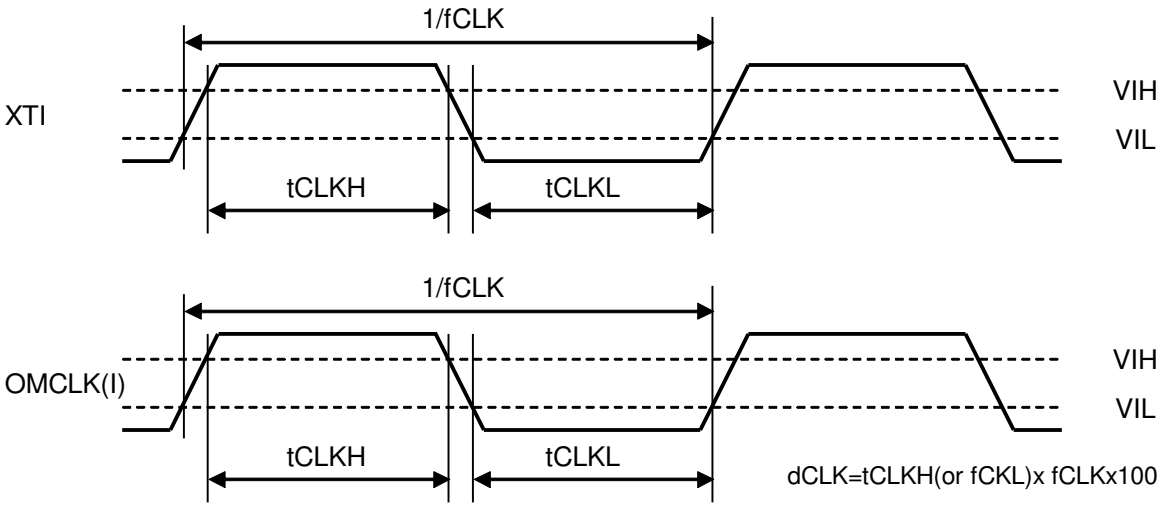
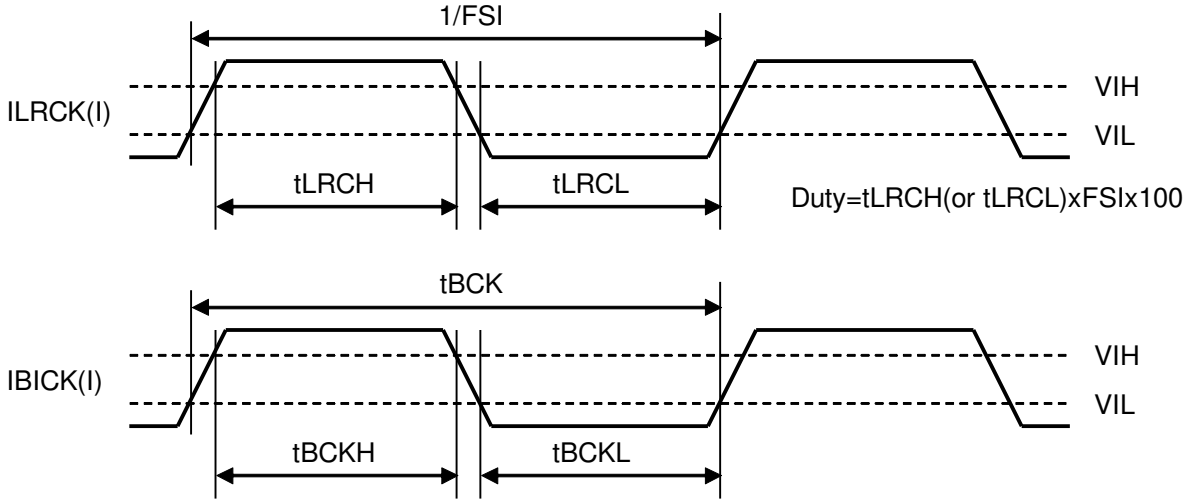


Figure 3. OMCLK, Clock Timing

Slave Mode



TDM256 or TDM512 Mode and Slave Mode

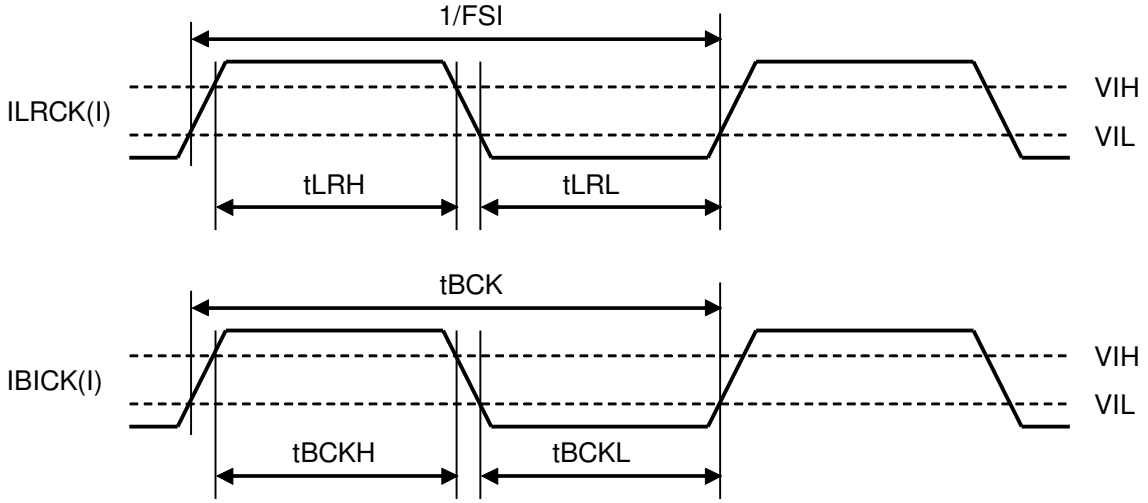
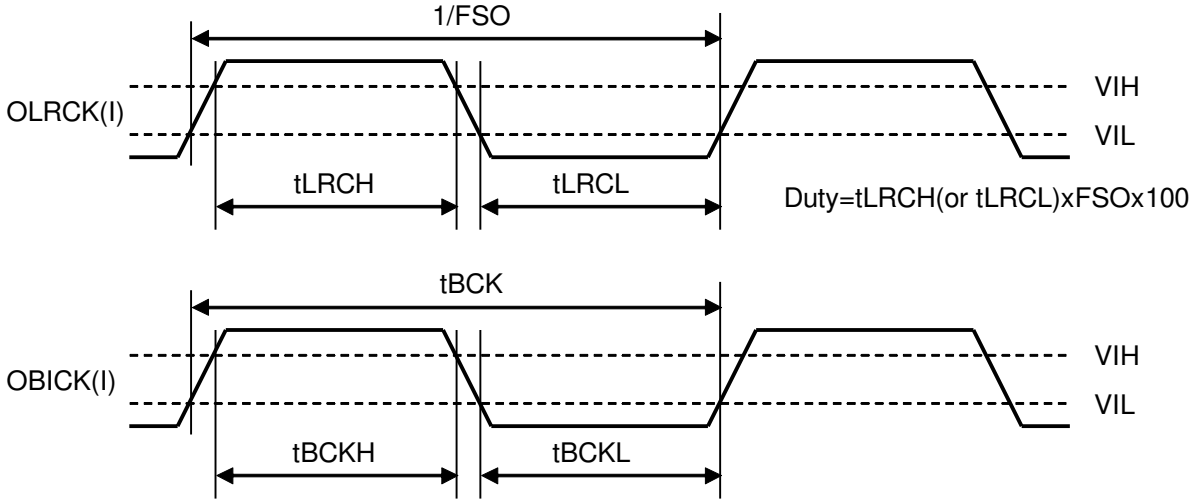


Figure 4. ILRCK, IBICK Clock Timing

Slave Mode



TDM256 or TDM512 Mode and Slave Mode

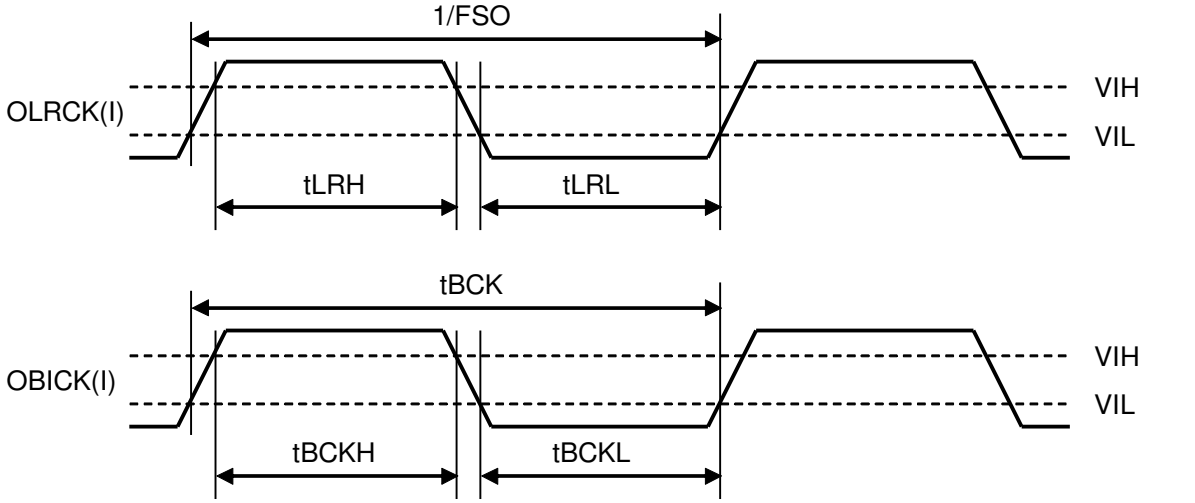


Figure 5. OLRCK, OBICK Clock Timing (Slave Mode)

Master Mode

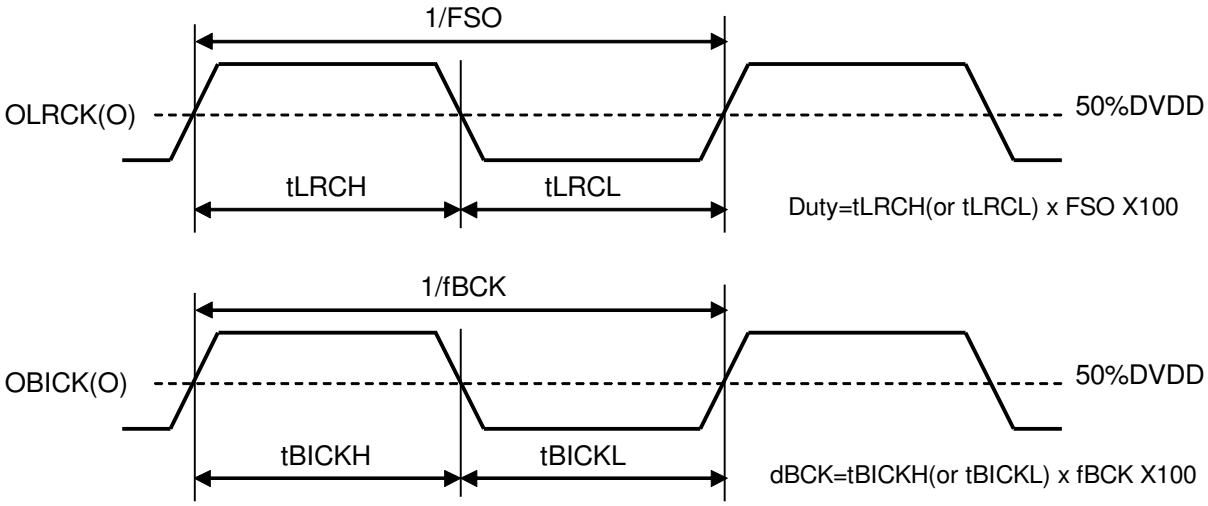


Figure 6. OLRCK, OBICK Clock Timing (Master Mode)