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AK4137

32bit SRC with PCM/DSD conversion

1. General Description

The AK4137 is a 2ch digital sample rate converter (SRC). The input sample rate ranges from 8kHz to 768kHz. The output sample rate is from 8kHz to 768kHz. The AK4137 has an internal Oscillator. Therefore it does not need any external master clocks and simplifies a system configuration. The AK4137 is suitable for the application interfacing to different sample rates such as high-end Audio Systems and USB-DACs. It is capable of playing back various audio formats with PCM-DSD data conversion function.

2. Features

- **2 channels input/output**
- **Asynchronous Sample Rate Converter**
- **PCM**
  - **Input Sample Rate Range (FSI): 8kHz~768kHz**
  - **Output Sample Rate Range (FSO): 8kHz~768kHz**
- **Input to Output Sample Rate Ratio: FSO/FSI = 1/6 ~ 24**
- **DSD**
  - **Input Sample Rate Range (FSI): 2.8224MHz~12.288MHz**
  - **Output Sample Rate Range (FSO): 2.8224MHz~12.288MHz**
- **Input to Output Sample Rate Ratio: FSO/FSI = 1/6 ~ 24**
- **THD+N: Up to −150dB**
- **Dynamic Range: 186dB (A-weighted)**
- **I/F format: MSB justified, LSB justified, I^2S compatible and TDM**
- **PCM/DSD converter**
- **DoP I/F**
- **Oscillator for Internal Operation Clock**
- **Clock for Master mode: 64/128/192/256/384/512/768fso**
- **On-chip X'tal oscillator**
- **Digital De-emphasis Filter (32kHz, 44.1kHz, 48kHz)**
- **Soft Mute Function**
- **SRC Bypass mode (Master/Slave, PCM, DSD)**
- **uP Interface: I2C bus/SPI 4-wire**
- **Power Supply**
  - **DVDD: 3.0~3.6V (internal LDO enabled)**
  - **DVDD: 1.7~1.9V (internal LDO disabled)**
- **Operating Temperature: Ta= −40 ~ +105°C**
- **Package**
  - **48-pin LQFP (0.5mm pitch)**

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	AK4137	AK4136
Bit	32	←
DR（A-Weighted）	186	176
THD+N	150	140
fsi	8~768KHz	8~384KHz
fso	8~768KHz	8~384KHz
Ratio I/O	1/6~24	1/6~12
Output Clock (Master Mode Operation)	64/128/256/384/512/768fso	128/256/384/512/768fso
SRC Conversion	PCM→PCM, DSD→DSD DSD→PCM, PCM→DSD DoP→DSD, DoP→PCM	PCM→PCM conversion only
SRC Bypass Function	Available (Master, Slave)	←
Soft Mute	Available Semi-Auto Mode Mute Time Setting Adjustment	Available Semi-Auto Mode and Mute Time Adjustment are only available by register settings.
DITHER	Available	Available (only by register settings)
Internal Regulator	3V→1.8V	←
External 1.8V Input	Available	←
Crystal Oscillator	Available	←
Pop Noise reduction on Rate Switching	Available	←
Micro Controller I/F	I2C, 4-Wire	←

4. Block Diagram

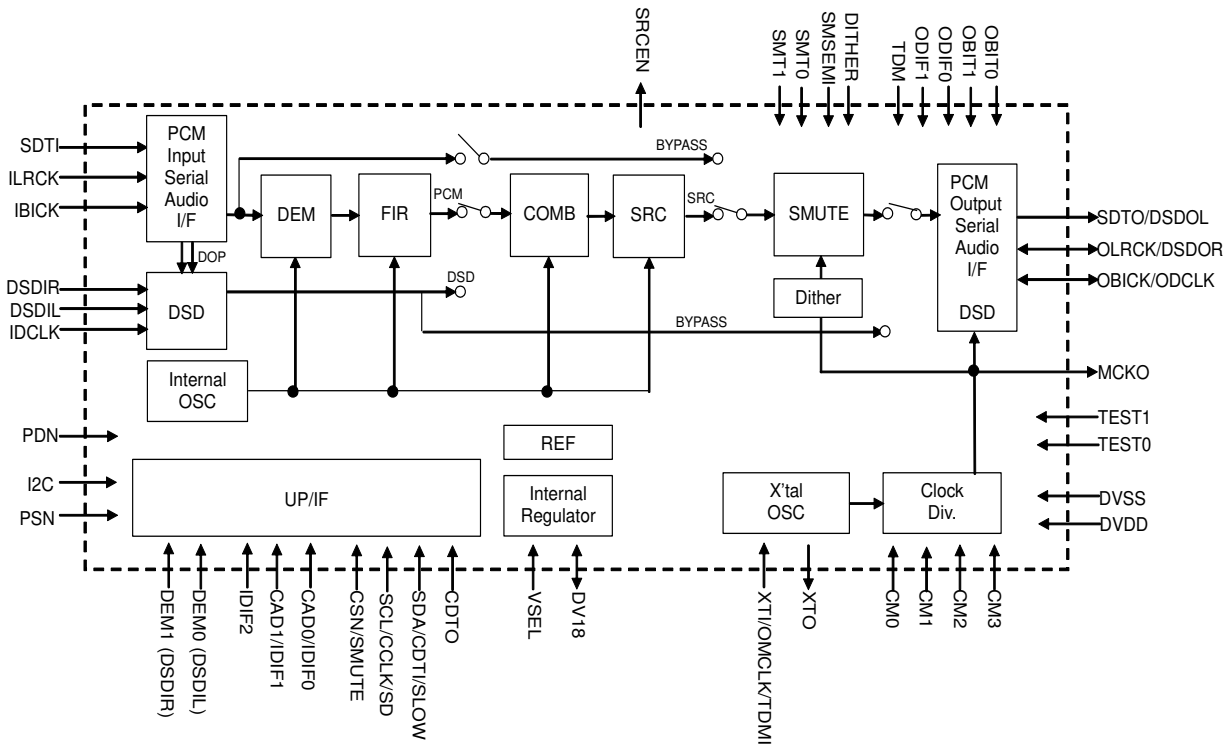

Figure 1. Block Diagram

5. Pin Configurations and Functions

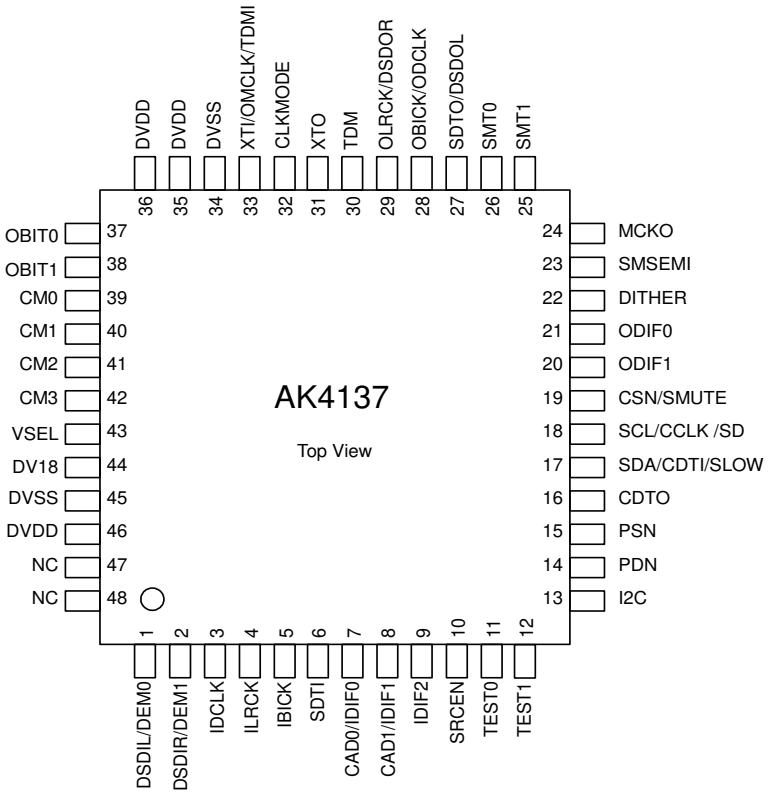

Figure 2. Pin Layout

■ **Pin Functions**

No.	Pin Name	I/O	Function
1	DSDIL	I	DSD Data Pin in DSD Mode
	DEM0	I	De-emphasis Control #0 Pin
2	DSDIR	I	DSD Data Pin in DSD Mode
	DEM1	I	De-emphasis Control #1 Pin
3	IDCLK	I	DSD Clock Pin in DSD Mode
4	ILRCK	I	L/R Clock Pin in PCM Mode
5	IBICK	I	Audio Serial Data Clock Pin in PCM Mode
6	SDTI	I	Audio Serial Data Input Pin in PCM Mode
7	CAD0	I	Chip Address 0 Pin in Serial Control Mode
	IDIF0	I	Digital Input Format 0 Pin in Parallel Control Mode
8	CAD1	I	Chip Address 1 Pin in Serial Control Mode
	IDIF1	I	Digital Input Format 1 Pin in Parallel Control Mode
9	IDIF2	I	Digital Input Format 2 Pin in Parallel Control Mode
10	SRCEN	O	Unlock Status Pin When the PDN pin= “L”, this pin outputs “H”.
11	TEST0	I	Test pin 0. Must be connected to DVSS in normal use.
12	TEST1	I	Test pin 1. Must be connected to DVSS in normal use.
13	I2C	I	Select serial mode “L”: 4-wire serial Mode ,“H”: I2C Mode
14	PDN	I	Power-Down Mode Pin “H”: Power up, “L”: Power down reset and initializes the control register. The AK4137 should be reset once by bringing PDN pin = “L” upon power-up.
15	PSN	I	Parallel/Serial Mode Select. “L”: Serial Mode , “H”: Parallel Mode

Note 1. All input pins must not be allowed to float. DVDD must be connected to the same power supply.
Note 2. PSN, CM3-0, OBIT1-0, TDM, ODIF1-0, IDIF2-0 and CAD1-0 pin must be changed when the PDN pin = “L”.

No.	Pin Name	I/O	Function
16	CDTO	O	I2C= “L”: Control Data Output Pin in Serial Control Mode
17	SDA	I/O	I2C= “H”: Control Data In/Out Pin in Serial Control Mode
	CDTI	I	I2C= “L”: Control Data Input Pin in Serial Control Mode
	SLOW	I	Digital Filter Select Pin in Parallel Control Mode
18	SCL	I	I2C= “H”: Control Data Clock Input Pin in Serial Control Mode
	CCLK	I	I2C= “L”: Control Data Clock Pin in Serial Control Mode
	SD	I	Digital Filter Select Pin in Parallel Control Mode
19	CSN	I	Chip Select Pin in Serial Control Mode , I2C= “L”
	SMUTE	I	Soft Mute Pin in Parallel Control Mode When this pin is changed to “H”, soft mute cycle is initiated. When returning “L”, the output mute releases.
20	ODIF1	I	Audio Interface Format #1 Pin for Output PORT
21	ODIF0	I	Audio Interface Format #0 Pin for Output PORT
22	DITHER	I	Dither Enable Pin “H”: Dither ON, “L”: Dither OFF
23	SMSEMI	I	Soft Mute Semi Auto Mode “L”: Manual Mode , “H”: Semi Auto Mode
24	MCKO	O	Master Clock Output Pin
25	SMT1	I	Soft Mute Timer select #1 Pin
26	SMT0	I	Soft Mute Timer select #0 Pin
27	SDTO	O	Audio Serial Data Output Pin for Output PORT When the PDN pin = “L”, the SDTO pin outputs “L”.
	DSDOL	O	DSD Data Pin in DSD Mode
28	OBICK	I/O	Audio Serial Data Clock Pin for Output PORT When the PDN pin = “L” in master mode, the OBICK pin outputs “L”.
	ODCLK	I/O	DSD Clock Pin in DSD Mode
29	OLRCK	I/O	Output Channel Clock Pin for Output PORT When the PDN pin = “L” in master mode, the OLRCK pin outputs “L”.
	DSDOR	O	DSD Data Pin in DSD Mode
30	TDM	I	TDM Format Select Pin “L”(connected to DVSS): Stereo Mode “H”(connected to DVDD): TDM mode for Output
31	XTO	O	X’tal Output Pin When the PDN pin = “L” or CM3-0 = “LHHL” or “LHHH” or “Hxxx” XTO outputs “L”.
32	CLKMODE	I	Master Clock Select Pin “L”(connected to DVSS): X'tal Mode “H”(connected to DVDD): External Master Clock or TDM=”H”

Note 1. All input pins must not be allowed to float. DVDD must be connected to the same power supply.
Note 2. PSN, CM3-0, OBIT1-0, TDM, ODIF1-0, IDIF2-0 and CAD1-0 pin must be changed when the PDN pin = “L”.

No.	Pin Name	I/O	Function
33	XTI	I	X'tal Input Pin
	OMCLK	I	External Master Clock Input
	TDMI	I	TDMI Daisy-Chain Input Pin
34	DVSS	-	Digital Ground Pin
35	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V or 1.7 ~ 1.9V
36	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V or 1.7 ~ 1.9V
37	OBIT0	I	Bit Length Select #0 Pin for Output Data
38	OBIT1	I	Bit Length Select #1 Pin for Output Data
39	CM0	I	Clock Select or Mode Select #0 Pin for Output PORT
40	CM1	I	Clock Select or Mode Select #1 Pin for Output PORT
41	CM2	I	Clock Select or Mode Select #2 Pin for Output PORT
42	CM3	I	Clock Select or Mode Select #3 Pin for Output PORT
43	VSEL	I	Digital Power select "L": DV18 is Output pin, "H": DV18 is Power Supply Pin
44	DV18	I/O	Digital Power Pin, Typ 1.8V VSEL= "L", Output When the PDN pin= "L", the DV18 pin outputs "L". Current must not be taken from this pin. A 10µF (±30%; including the temperature characteristics) capacitor should be connected between this pin and DVSS. When this capacitor is polarized, the positive polarity pin should be connected to the DV18 pin. VSEL= "H", Input
45	DVSS	-	Digital Ground Pin
46	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V or 1.7 ~ 1.9V
47	NC	-	This pin must be connected to DVSS.
48	NC	-	This pin must be connected to DVSS.

Note 1. All input pins must not be allowed to float. DVDD must be connected to the same power supply.
Note 2. PSN, CM3-0, OBIT1-0, TDM, ODIF1-0, IDIF2-0 and CAD1-0 pin must be changed when the PDN pin = "L".

*Unused Input/Output Pins

Classification	Pin Name	Setting
Digital	SMSEMI, DITHER, CSN/SMUTE	Connect to DVSS
	XTI/OMCLK/TDMI	Connect to DVSS (Slave Mode)
	SRCEN, MCKO, XTO, CDTO	Open

*The status of OLRCK and OBICK pins, when the PDN pin = “L”, are shown below. (“L” output in Master mode) When the CM3 pin = “H”, the AK4137 is always in output mode.

Setting Pins				OLRCK, OBICK
CM3	CM2	CM1	CM0	
L	L	L	L	“L” Output
L	L	L	H	
L	L	H	L	
L	L	H	H	
L	H	L	L	Input
L	H	L	H	“L” Output
L	H	H	L	
L	H	H	H	
H	-	-	-	

* The output pin status when the PDN pin = “L” is shown below.

Output Pin	Status
SDTO	“L” Output
SRCEN	“H” Output
MCKO	“L” Output
XTO	“L” Output
CDTO	Hi-z

6. Absolute Maximum Ratings

(DVSS=0V; Note 3)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Digital	DVDD	-0.3	4.3	V
	(Internal Digital) (Note 4)	DV18	-0.3	2.5	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 5)		VDIN	-0.3	DVDD+0.3	V
Ambient Temperature (Power applied) (Note 6)		Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 3. All voltages are with respect to ground.
Note 4. DVSS must be connected to the same ground.
Note 5. DSDIL/DEM0, DSDIR/DEM1, ILRCK, IBICK, DCLK, SDTI, IDIF0/CAD0, IDIF1/CAD1, IDIF2, PDN, PSN, I2C, SLOW/CDTI/SDA, SD/CCLK/SCL, SMUTE/CSN, SMSEMI, SMT1-0, OBIT1-0, ODIF1-0, CM3-0, DITHER, VSEL and TEST1-0 pins
Note 6. In the case that the PCB wiring density is more than 100%

WARING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(DVSS=0V; Note 3; VSEL= “L”)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Digital	DVDD	3.0	3.3	3.6	V

(DVSS=0V; Note 3; VSEL= “H”)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Digital	DVDD	1.7	1.8	1.9	V
(Note 7)	Digital	DV18	1.7	1.8	1.9	V
	Difference	DVDD- DV18	-	0	-	V

Note 3. All voltages are with respect to ground.
Note 7. DVDD and DV18 should be connected externally.

The PDN pin must be “L” when power up the AK4137. Set the PDN pin to “H” after all power supplies are ON. Writing by a microcontroller should be executed with a 5ms interval after the PDN pin = “H”.

8. SRC Characteristics

■ PCMIN → PCMOUT

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V; DVSS=0V; Signal Frequency=1KHz; data = 32bit; measurement bandwidth = 20Hz~ FSO/2; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Resolution				32	Bits
Input Sample Rate	FSI	8		768	kHz
Output Sample Rate	FSO	8		768	kHz
THD+N (Input= 1kHz, 0dBFS)					
FSO/FSI=44.1kHz/48kHz		-	-150	-	dB
FSO/FSI=48kHz/44.1kHz		-	-133	-	dB
FSO/FSI=48kHz/192kHz		-	-153	-	dB
FSO/FSI=192kHz/48kHz		-	-144	-	dB
Worst Case (FSO/FSI=32kHz/176.4kHz)		-	-	-111	dB
Dynamic Range (Input= 1kHz, -60dBFS)					
FSO/FSI=44.1kHz/48kHz		-	184	-	dB
FSO/FSI=48kHz/44.1kHz		-	183	-	dB
FSO/FSI=48kHz/192kHz		-	184	-	dB
FSO/FSI=192kHz/48kHz		-	184	-	dB
Worst Case (FSO/FSI= 48kHz/32kHz)		176	-	-	dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted)					
FSO/FSI=44.1kHz/48kHz		-	186	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1/6		24	-

■ PCMIN → DSDOUT

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=VD18=1.7~1.9V; DVSS=0V; Signal Frequency=1KHz; data = 32bit; measurement bandwidth = 20Hz~ FSO/2; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Resolution				32	Bits
Input Sample Rate	FSI	8		768	kHz
Output Sample Rate	FSO	44.1		48	kHz
THD+N (Input= 1kHz, 0dBFS, Note 8)					
64FSO/FSI=2.822MHz/44.1kHz		-	-115	-	dB
128FSO/FSI=5.6448MHz/44.1kHz		-	-119	-	dB
256FSO/FSI=11.2896MHz/176.4kHz		-	-123	-	dB
Dynamic Range (Input= 1kHz, -60dBFS, Note 8)					
64FSO/FSI=2.822MHz /44.1kHz		-	116	-	dB
128FSO/FSI=5.6448MHz/44.1kHz		-	119	-	dB
256FSO/FSI=11.2896MHz/176.4kHz		-	123	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1/16		1	-

Note 8. OGAINM6 bit = “1”

■ **DSDIN → PCMOUT**

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=VD18=1.7~1.9V; DVSS=0V; Signal Frequency=1KHz; data = 32bit; measurement bandwidth = 20Hz~ FSO/2; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Resolution				32	Bits
Input Sample Rate	FSI	44.1		48	kHz
Output Sample Rate	FSO	44.1		768	kHz
THD+N (Input= 1kHz, -6dBFS, Note 9)					
FSO/64FSI =44.1kHz/2.8224MHz		-	-98	-	dB
FSO/128FSI =44.1kHz/5.6448MHz		-	-115	-	dB
FSO/256FSI = 44.1kHz/11.2896MHz		-	-115	-	dB
Dynamic Range (Input= 1kHz, -60dBFS, Note 9)					
FSO/64FSI =44.1kHz/2.8224MHz		-	108	-	dB
FSO/128FSI =44.1kHz/5.6448MHz		-	140	-	dB
FSO/256FSI =44.1kHz/11.2896MHz		-	132	-	dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted, Note 9)					dB
FSO/128FSI =44.1kHz/5.6448MHz		-	142	-	
Ratio between Input and Output Sample Rate	FSO/FSI	1		17.4	-

Note 9. IGAINM6 bit = “1”. It is defined that DSD outputs of the AK4137 are source.

■ **DSDIN → DSDOUT**

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=VD18=1.7~1.9V; DVSS=0V; Signal Frequency=1KHz; data = 32bit; measurement bandwidth = 20Hz~ FSO/2; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Resolution				32	Bits
Input Sample Rate	FSI	44.1		48	kHz
Output Sample Rate	FSO	44.1		48	kHz
THD+N (Input= 1kHz, -6dBFS, Note 10)					
64FSO/64FSI =2.8224MHz/2.8224MHz		-	-111	-	dB
128FSO/128FSI =5.6448MHz/5.6448MHz		-	-115	-	dB
256FSO/256FSI =11.2896MHz/11.2896MHz		-	-115	-	dB
Dynamic Range (Input= 1kHz, -60dBFS, Note 10)					
64FSO/64FSI =2.8224MHz/2.8224MHz		-	116	-	dB
128FSO/128FSI =5.6448MHz/5.6448MHz		-	119	-	dB
256FSO/256FSI =11.2896MHz/11.2896MHz		-	123	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1		1	-

Note 10. *IGAINM6 bit = “1”, OGAINM6 bit = “1”

9. Power Consumptions

■ Internal LDO Mode

(Ta=-40~ +105°C; DVDD=3.0~3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Current					
Normal operation: （PDN = “H”）					
FSI=FSO=48kHz at Master Mode : DVDD=3.3V			11		mA
FSI=FSO=192kHz at Master Mode: DVDD=3.3V			33	-	mA
FSI=FSO=768kHz at Master Mode: DVDD=3.3V			40	-	mA
: DVDD=3.6V				60	mA
Power down: PDN = “L” (Note 11)					
DVDD=3.6V			10	100	μA

Note 11. All digital inputs including clock pins are held to DVSS.

■ DV18 External Supply Mode

(Ta=-40~ +105°C; DVDD=DV18=1.7~1.9V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Current					
Normal operation:					
FSI=FSO=48kHz at Master Mode: DVDD＝DV18=1.8V			11		mA
FSI=FSO=192kHz at Master Mode: DVDD＝DV18=1.8V			28	-	mA
FSI=FSO=768kHz at Master Mode: DVDD＝DV18=1.8V			32	-	mA
: DVDD＝DV18=1.9V				50	mA
Power down: PDN = “L” (Note 11)					
DVDD=DV18=1.9V			10	100	μA

Note 11. All digital inputs including clock pins are held to DVSS.

10. Filter Characteristics

■ Sharp Roll-Off Filter Characteristics

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V, DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband −0.01dB	0.985 ≤ FSO/FSI ≤ 24.000	PB	0	-	0.4583FSI	kHz
	0.905 ≤ FSO/FSI < 0.985	PB	0	-	0.4167FSI	kHz
	0.714 ≤ FSO/FSI < 0.905	PB	0	-	0.3195FSI	kHz
	0.656 ≤ FSO/FSI < 0.714	PB	0	-	0.2852FSI	kHz
	0.536 ≤ FSO/FSI < 0.656	PB	0	-	0.2182FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0	-	0.2177FSI	kHz
	0.452 ≤ FSO/FSI < 0.492	PB	0	-	0.1948FSI	kHz
	0.357 ≤ FSO/FSI < 0.452	PB	0	-	0.1458FSI	kHz
	0.324 ≤ FSO/FSI < 0.357	PB	0	-	0.1302FSI	kHz
	0.246 ≤ FSO/FSI < 0.324	PB	0	-	0.0917FSI	kHz
	0.226 ≤ FSO/FSI < 0.246	PB	0	-	0.0826FSI	kHz
	0.1667 ≤ FSO/FSI < 0.226	PB	0	-	0.0583FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 24.000	SB	0.5417FSI	-	-	kHz
	0.905 ≤ FSO/FSI < 0.985	SB	0.5021FSI	-	-	kHz
	0.714 ≤ FSO/FSI < 0.905	SB	0.3965FSI	-	-	kHz
	0.656 ≤ FSO/FSI < 0.714	SB	0.3643FSI	-	-	kHz
	0.536 ≤ FSO/FSI < 0.656	SB	0.2974FSI	-	-	kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2813FSI	-	-	kHz
	0.452 ≤ FSO/FSI < 0.492	SB	0.2604FSI	-	-	kHz
	0.357 ≤ FSO/FSI < 0.452	SB	0.2116FSI	-	-	kHz
	0.324 ≤ FSO/FSI < 0.357	SB	0.1969FSI	-	-	kHz
	0.246 ≤ FSO/FSI < 0.324	SB	0.1573FSI	-	-	kHz
	0.226 ≤ FSO/FSI < 0.246	SB	0.1471FSI	-	-	kHz
	0.1667 ≤ FSO/FSI < 0.226	SB	0.1020FSI	-	-	kHz
Passband Ripple	0.226 ≤ FSO/FSI ≤24.000	PR		-	±0.01	dB
	0.1667 ≤ FSO/FSI < 0.226	PR		-	±0.03	dB
Stopband Attenuation	0.985 ≤ FSO/FSI ≤ 24.000	SA	140.2	-	-	dB
	0.905 ≤ FSO/FSI < 0.985	SA	140.9	-	-	dB
	0.714 ≤ FSO/FSI < 0.905	SA	135.2	-	-	dB
	0.656 ≤ FSO/FSI < 0.714	SA	135.1	-	-	dB
	0.536 ≤ FSO/FSI < 0.656	SA	133.5	-	-	dB
	0.492 ≤ FSO/FSI < 0.536	SA	115.3	-	-	dB
	0.452 ≤ FSO/FSI < 0.492	SA	118.2	-	-	dB
	0.357 ≤ FSO/FSI < 0.452	SA	123.3	-	-	dB
	0.324 ≤ FSO/FSI < 0.357	SA	122.9	-	-	dB
	0.246 ≤ FSO/FSI < 0.324	SA	117.9	-	-	dB
	0.226 ≤ FSO/FSI < 0.246	SA	119.7	-	-	dB
	0.1667 ≤ FSO/FSI < 0.226	SA	90.3	-	-	dB
Group Delay (Note 12)		GD	-	64	-	1/fs

Note 12. This is the time from a rising edge of ILRCK after L and R channels data is input to a rising edge of OLRCK before the L and R channels data is output, when there is no phase difference between input and output data.

■ **Slow Roll-Off Filter Characteristics**

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V, DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband −0.01dB	0.1667 ≤ FSO/FSI < 24.000	PB	0	-	0.0417FSI	kHz
Stopband	0.1667 ≤ FSO/FSI < 24.000	SB	0.4167FSI	-	-	kHz
Passband Ripple		PR	-	-	±0.01	dB
Stopband Attenuation		SA	-	108.1	-	dB
Group Delay (Note 12)		GD	-	64	-	1/fs

Note 12. This is the time from a rising edge of ILRCK after L and R channels data is input to a rising edge of OLRCK before the L and R channels data is output, when there is no phase difference between input and output data.

■ Short Delay Sharp Roll-Off Filter Characteristics

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V, DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband −0.01dB	0.985 ≤ FSO/FSI ≤ 24.000	PB	0	-	0.4583FSI	kHz
	0.905 ≤ FSO/FSI < 0.985	PB	0	-	0.4167FSI	kHz
	0.714 ≤ FSO/FSI < 0.905	PB	0	-	0.3195FSI	kHz
	0.656 ≤ FSO/FSI < 0.714	PB	0	-	0.2852FSI	kHz
	0.536 ≤ FSO/FSI < 0.656	PB	0	-	0.2182FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0	-	0.2177FSI	kHz
	0.452 ≤ FSO/FSI < 0.492	PB	0	-	0.1948FSI	kHz
	0.357 ≤ FSO/FSI < 0.452	PB	0	-	0.1458FSI	kHz
	0.324 ≤ FSO/FSI < 0.357	PB	0	-	0.1302FSI	kHz
	0.246 ≤ FSO/FSI < 0.324	PB	0	-	0.0917FSI	kHz
	0.226 ≤ FSO/FSI < 0.246	PB	0	-	0.0826FSI	kHz
	0.1667 ≤ FSO/FSI < 0.226	PB	0	-	0.0583FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 24.000	SB	0.5417FSI	-	-	kHz
	0.905 ≤ FSO/FSI < 0.985	SB	0.5021FSI	-	-	kHz
	0.714 ≤ FSO/FSI < 0.905	SB	0.3965FSI	-	-	kHz
	0.656 ≤ FSO/FSI < 0.714	SB	0.3643FSI	-	-	kHz
	0.536 ≤ FSO/FSI < 0.656	SB	0.2974FSI	-	-	kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2813FSI	-	-	kHz
	0.452 ≤ FSO/FSI < 0.492	SB	0.2604FSI	-	-	kHz
	0.357 ≤ FSO/FSI < 0.452	SB	0.2116FSI	-	-	kHz
	0.324 ≤ FSO/FSI < 0.357	SB	0.1969FSI	-	-	kHz
	0.246 ≤ FSO/FSI < 0.324	SB	0.1573FSI	-	-	kHz
	0.226 ≤ FSO/FSI < 0.246	SB	0.1471FSI	-	-	kHz
	0.1667 ≤ FSO/FSI < 0.226	SB	0.1020FSI	-	-	kHz
Passband Ripple	0.226 ≤ FSO/FSI ≤ 24.000	PR		-	±0.01	dB
	0.1667 ≤ FSO/FSI < 0.226	PR		-	±0.03	dB
Stopband Attenuation	0.985 ≤ FSO/FSI ≤ 24.000	SA	140.2	-	-	dB
	0.905 ≤ FSO/FSI < 0.985	SA	140.9	-	-	dB
	0.714 ≤ FSO/FSI < 0.905	SA	135.2	-	-	dB
	0.656 ≤ FSO/FSI < 0.714	SA	135.1	-	-	dB
	0.536 ≤ FSO/FSI < 0.656	SA	133.5	-	-	dB
	0.492 ≤ FSO/FSI < 0.536	SA	115.3	-	-	dB
	0.452 ≤ FSO/FSI < 0.492	SA	118.2	-	-	dB
	0.357 ≤ FSO/FSI < 0.452	SA	123.3	-	-	dB
	0.324 ≤ FSO/FSI < 0.357	SA	122.9	-	-	dB
	0.246 ≤ FSO/FSI < 0.324	SA	117.9	-	-	dB
	0.226 ≤ FSO/FSI < 0.246	SA	119.7	-	-	dB
	0.1667 ≤ FSO/FSI < 0.226	SA	90.3	-	-	dB
Group Delay (Note 12)	0.905 ≤ FSO/FSI ≤ 24.000	GD	-	20	-	1/fs
	0.656 ≤ FSO/FSI < 0.905	GD	-	22	-	1/fs
	0.536 ≤ FSO/FSI < 0.656	GD	-	26	-	1/fs
	0.492 ≤ FSO/FSI < 0.536	GD	-	23	-	1/fs
	0.452 ≤ FSO/FSI < 0.492	GD	-	24	-	1/fs
	0.324 ≤ FSO/FSI < 0.452	GD	-	26	-	1/fs
	0.246 ≤ FSO/FSI < 0.324	GD	-	29	-	1/fs
	0.226 ≤ FSO/FSI < 0.246	GD	-	30	-	1/fs
	0.1667 ≤ FSO/FSI < 0.226	GD	-	32	-	1/fs

Note 12. This is the time from a rising edge of ILRCK after L and R channels data is input to a rising edge of OLRCK before the L and R channels data is output, when there is no phase difference between input and output data.

■ **Short Delay Slow Roll-Off Filter Characteristics**

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V, DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband −0.01dB	0.1667≤ FSO/FSI< 24.000	PB	0	-	0.0417FSI	kHz
Stopband	0.1667≤ FSO/FSI< 24.000	SB	0.4167FSI	-	-	kHz
Passband Ripple		PR	-	-	±0.01	dB
Stopband Attenuation		SA	-	108.1	-	dB
Group Delay (Note 12)		GD	-	21	-	1/fs

Note 12. This is the time from a rising edge of ILRCK after L and R channels data is input to a rising edge of OLRCK before the L and R channels data is output, when there is no phase difference between input and output data.

11. DSD Mode Characteristics

■ Sharp Roll-Off Filter Characteristics

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V; DVSS=0V, ILRCK=48kHz)

Parameter				Symbol	Min.	Typ.	Max.	Unit
Digital Filter								
Passband	PCMFSO bit	"00"	-0.24dB	PB	0	-	20	kHz
	PCMFSO bit	"01"	-1.04dB	PB	0	-	40	kHz
	PCMFSO bit	"10"	-3.86dB	PB	0	-	80	kHz
	PCMFSO bit	"11"	-5.90dB	PB	0	-	100	kHz
Stopband	PCMFSO bit	"00"		SB	46	-	-	kHz
	PCMFSO bit	"01"		SB	66	-	-	kHz
	PCMFSO bit	"10"		SB	86	-	-	kHz
	PCMFSO bit	"11"		SB	126	-	-	kHz
Passband Ripple	PCMFSO bit	"00"		PR	-	-	±0.2	dB
	PCMFSO bit	"01"		PR	-	-	±0.5	dB
	PCMFSO bit	"10"		PR	-	-	±2.0	dB
	PCMFSO bit	"11"		PR	-	-	±3.0	dB
Stopband Attenuation				SA	-	112	-	dB
Group Delay (Note 15)				GD	-	15	-	1/fs

Note 13. In DSD mode, the signal level is ranging from 25% to 75%. Peak levels of DSD signal above this duty are not recommended by SACD format book (Scarlet Book).

Note 14. The output level is assumed as 0dB when 1kHz, 25 ~ 75% duty range sine wave is input.

Note 15. When PCM output is 44.1kHz or 48kHz.

■ Slow Roll-Off Filter Characteristics

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V; DVSS=0V, ILRCK=48kHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital Filter					
Passband −0.28dB	PB	0	-	10	kHz
Stopband	SB	156	-	-	kHz
Passband Ripple	PR	-	-	±0.15	dB
Stopband Attenuation	SA	-	112	-	dB
Group Delay (Note 15)	GD	-	15	-	1/fs

Note 13. In DSD mode, the signal level is ranging from 25% to 75%. Peak levels of DSD signal above this duty are not recommended by SACD format book (Scarlet Book).

Note 14. The output level is assumed as 0dB when 1kHz, 25 ~ 75% duty range sine wave is input.

Note 15. When PCM output is 44.1kHz or 48kHz.

■ Short Delay Sharp Roll-Off Filter Characteristics

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V; DVSS=0V, ILRCK=48kHz)

Parameter				Symbol	Min.	Typ.	Max.	Unit
Digital Filter								
Passband	PCMFSO bit	"00"	-0.24dB	PB	0	-	20	kHz
	PCMFSO bit	"01"	-1.04dB	PB	0	-	40	kHz
	PCMFSO bit	"10"	-3.86dB	PB	0	-	80	kHz
	PCMFSO bit	"11"	-5.90dB	PB	0	-	100	kHz
Stopband	PCMFSO bit	"00"		SB	46	-	-	kHz
	PCMFSO bit	"01"		SB	66	-	-	kHz
	PCMFSO bit	"10"		SB	86	-	-	kHz
	PCMFSO bit	"11"		SB	126	-	-	kHz
Passband Ripple	PCMFSO bit	"00"		PR	-	-	±0.2	dB
	PCMFSO bit	"01"		PR	-	-	±0.5	dB
	PCMFSO bit	"10"		PR	-	-	±2.0	dB
	PCMFSO bit	"11"		PR	-	-	±3.0	dB
Stopband Attenuation				SA	-	112	-	dB
Group Delay (Note 15)				GD	-	13	-	1/fs

Note 13. In DSD mode, the signal level is ranging from 25% to 75%. Peak levels of DSD signal above this duty are not recommended by SACD format book (Scarlet Book).

Note 14. The output level is assumed as 0dB when 1kHz, 25 ~ 75% duty range sine wave is input.

Note 15. When PCM output is 44.1kHz or 48kHz.

■ Short Delay Slow Roll-Off Filter Characteristics

(Ta=-40~ +105°C; DVDD=3.0~3.6V or DVDD=DV18=1.7V~1.9V; DVSS=0V, ILRCK=48kHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital Filter					
Passband −0.28dB	PB	0	-	10	kHz
Stopband	SB	156	-	-	kHz
Passband Ripple	PR	-	-	±0.15	dB
Stopband Attenuation	SA	-	112	-	dB
Group Delay (Note 15)	GD	-	13	-	1/fs

Note 13. In DSD mode, the signal level is ranging from 25% to 75%. Peak levels of DSD signal above this duty are not recommended by SACD format book (Scarlet Book).

Note 14. The output level is assumed as 0dB when 1kHz, 25 ~ 75% duty range sine wave is input.

Note 15. When PCM output is 44.1kHz or 48kHz.

12. Input and Output Examples

Possible Input and Output data combinations are shown below.
Fsi is the sampling rate of input data, and Fso is the sampling rate of output data.

Fsi[KHz]	Fso[KHz]		Fso[MHz]		
PCM	PCM		DSD		
	min	max			
8	8	192	-	-	-
11.025	8	264.6	-	-	-
16	8	384	-	-	-
32	8	768	-	-	-
44.1	8	768	2.8224	5.6448	-
48	8	768	2.8224	5.6448	-
88.2	14.7	768	2.8224	5.6448	-
96	16	768	2.8224	5.6448	-
176.4	29.6	768	2.8224	5.6448	11.2896
192	32	768	2.8224	5.6448	11.2896

Fsi[MHz]	Fso[KHz]		Fso[MHz]		
DSD	PCM		DSD		
	min	max			
2.8224	44.1	768	2.8224	5.6448	11.2896
5.6448	44.1	768	2.8224	5.6448	11.2896
11.2896	44.1	768	2.8224	5.6448	11.2896

Fsi[KHz]	Fso[KHz]		Fso[MHz]		
PCM	PCM		DSD		
	min	max			
8	8	192	-	-	-
12	8	288	-	-	-
16	8	384	-	-	-
32	8	768	-	-	-
44.1	8	768	3.072	6.144	-
48	8	768	3.072	6.144	-
88.2	14.7	768	3.072	6.144	-
96	16	768	3.072	6.144	-
176.4	29.6	768	3.072	6.144	-
192	32	768	3.072	6.144	12.288

Fsi[MHz]	Fso[KHz]		Fso[MHz]		
DSD	PCM		DSD		
	min	max			
3.072	48	768	3.072	6.144	12.288
6.144	48	768	3.072	6.144	12.288
12.288	48	768	3.072	6.144	12.288

With combinations shown below, in case down convert, THD+N will be degraded -80dB.

Fsi[KHz]	Fso[KHz]		Fso[MHz]		
PCM	PCM		DSD		
	min	max			
384	64～384	768	2.8224	5.6448	11.2896
768	128～768	768	2.8224	5.6448	11.2896

Fsi[KHz]	Fso[KHz]		Fso[MHz]		
PCM	PCM		DSD		
	min	max			
384	64～384	768	3.072	6.144	12.288
768	128～768	768	3.072	6.144	12.288

13. DC Characteristics

(Ta=-40~ +105°C; DVDD=3.0~3.6V: VSEL = "L" or DVDD=DV18=1.7V~1.9V: VSEL = "H")

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage Except SDA pin (Iout=−400μA)	VOH	DVDD−0.4	-	-	V
Low-Level Output Voltage Except SDA pin (Iout=400μA)	VOL	-	-	0.4	V
SDA pin (Iout=3mA)	VOL			0.4	V
Input Leakage Current	Iin	-	-	±10	μA

14. Switching Characteristics

(Ta=-40~ +105°C; DVDD=3.0~3.6V: VSEL = "L" or DVDD=DV18=1.7V~1.9V: VSEL = "H"; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
Crystal Oscillator Frequency (256 times of 44.1, 48, 88.2 or 96KHz)	fXTAL	11.2896		24.576	MHz
OMCLK Input					
64 FSO :	fCLK	0.512		49.152	MHz
Pulse Width Low	tCLKL	7			ns
Pulse Width High	tCLKH	7			ns
128 FSO :	fCLK	1.024		49.152	MHz
Pulse Width Low	tCLKL	7			ns
Pulse Width High	tCLKH	7			ns
256 FSO :	fCLK	2.048		49.152	MHz
Pulse Width Low	tCLKL	7			ns
Pulse Width High	tCLKH	7			ns
384 FSO :	fCLK	3.072		36.864	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns
512 FSO :	fCLK	4.096		49.152	MHz
Pulse Width Low	tCLKL	7			ns
Pulse Width High	tCLKH	7			ns
768 FSO :	fCLK	6.144		36.864	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns
MCKO Output					
Frequency	fMCK	0.512		49.152	MHz
Duty (Note 16)	dMCLK	40	50	60	%

Note 16. This is a value of MCKO output duty when the master clock for output ports is supplied by a crystal oscillator.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input PORT ILRCK					
Frequency					kHz
Normal speed mode	FSIN	8		54	kHz
Double speed mode	FSID	54		108	kHz
Quad speed mode	FSIQ	108		216	kHz
Oct speed mode	FSIO		384		kHz
Hex speed mode	FSIH		768		kHz
Duty Cycle Slave Mode	Duty	48	50	52	%
Output PORT OLRCK					
Frequency					
Slave mode					
Normal speed mode	FSON	8		54	kHz
Double speed mode	FSOD	54		108	kHz
Quad speed mode	FSOQ	108		216	kHz
Oct speed mode	FSOO		384		kHz
Hex speed mode	FSOH		768		kHz
Master mode, OMCLK Input, 64FSO mode	FSO	8		768	kHz
Master mode, OMCLK Input, 128FSO mode	FSO	8		384	kHz
Master mode, OMCLK Input, 256FSO mode	FSO	8		192	kHz
Master mode, OMCLK Input, 384FSO mode	FSO	8		96	kHz
Master mode, OMCLK Input, 512FSO mode	FSO	8		96	kHz
Master mode, OMCLK Input, 768FSO mode	FSO	8		48	kHz
Duty Cycle					
Slave Mode	Duty	48	50	52	%
Master Mode	Duty		50		%
Input PORT ILRCK for TDM256 Mode					
Frequency	FSI	8		96	kHz
“H” time (slave mode)	tLRH	1/256FSI			ns
“L” time (slave mode)	tLRL	1/256FSI			ns
Input PORT ILRCK for TDM512 Mode					
Frequency	FSI	8		48	kHz
“H” time (slave mode)	tLRH	1/512FSI			ns
“L” time (slave mode)	tLRL	1/512FSI			ns
Output PORT OLRCK for TDM256 Mode					
Frequency	FSO	8		96	kHz
“H” time (slave mode)	tLRH	1/256 FSO			ns
“L” time (slave mode)	tLRL	1/256 FSO			ns
Output PORT OLRCK for TDM512 Mode					
Frequency	FSO	8		48	kHz
“H” time (slave mode)	tLRH	1/512 FSO			ns
“L” time (slave mode)	tLRL	1/512 FSO			ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing					
Input PORT (Slave mode)					
IBICK Period Normal speed mode	tBCK	1/256 FSIN			ns
Double speed mode	tBCK	1/128 FSID			ns
Quad speed mode	tBCK	1/64 FSIQ			ns
Oct speed mode	tBCK	1/64 FSIO			ns
Hex speed mode	tBCK	1/64 FSIH			ns
IBICK Pulse Width Low	tBCKL	7			ns
Pulse Width High	tBCKH	7			ns
ILRCK Edge to IBICK "↑"(Note 17)	tLRB	5			ns
IBICK "↑" to ILRCK Edge (Note 17)	tBLR	5			ns
SDTI Hold Time from IBICK "↑"	tSDH	5			ns
SDTI Setup Time to IBICK "↑"	tSDS	5			ns
DSD Audio Interface Timing (64 mode)					
IDCLK Period	tDCK	-	1/64FSIN	-	ns
IDCLK Pulse Width Low	tDCKL	160			ns
IDCLK Pulse Width High	tDCKH	160			ns
IDCLK Edge to DSDL/R	tDDD	–20		20	ns
DSD Audio Interface Timing (128 mode)					
IDCLK Period	tDCK	-	1/128FSIN	-	ns
IDCLK Pulse Width Low	tDCKL	80			ns
IDCLK Pulse Width High	tDCKH	80			ns
IDCLK Edge to DSDL/R	tDDD	–10		10	ns
DSD Audio Interface Timing (256 mode)					
IDCLK Period	tDCK	-	1/256FSIN	-	ns
IDCLK Pulse Width Low	tDCKL	40			ns
IDCLK Pulse Width High	tDCKH	40			ns
IDCLK Edge to DSDL/R	tDDD	–5		5	ns
Input PORT (TDM256 slave mode)					
IBICK Period	tBCK	40			ns
IBICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
ILRCK Edge to IBICK "↑" (Note 17)	tLRB	10			ns
IBICK "↑" to ILRCK Edge (Note 17)	tBLR	10			ns
SDTI Hold Time from IBICK "↑"	tSDH	10			ns
SDTI Setup Time to IBICK "↑"	tSDS	6			ns
Input PORT (TDM512 slave mode)					
IBICK Period	tBCK	40			ns
IBICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
ILRCK Edge to IBICK "↑" (Note 17)	tLRB	10			ns
IBICK "↑" to ILRCK Edge (Note 17)	tBLR	10			ns
SDTI Hold Time from IBICK "↑"	tSDH	10			ns
SDTI Setup Time to IBICK "↑"	tSDS	6			ns

Note 17. IBICK rising edge must not occur at the same time as ILRCK edge.
Note 18. Maximum frequency of IBICK and OBICK is 49.152MHz.