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AK4141

NICAM/A2/EIA-J Digital Stereo Decoder

GENERAL DESCRIPTION

The AK4141 is a NICAM/A2/EIA-J stereo decoder, which is optimized for Digital TV application. The AK4141 achieves no alignment, few external components and high audio performance by digital stereo decoding architecture. The AK4141 integrates a stereo sample rate converter (SRC) for asynchronous digital audio sources such as digital tuners, digital switches and sound processing functions like 5-band equalizers. The AK4141 supports major audio data formats (MSB/LSB justified, I^2S and TDM) to interface with DSP, ADC, DAC. Therefore, the AK4141 is suitable for the AV systems such as Digital TV and DVR.

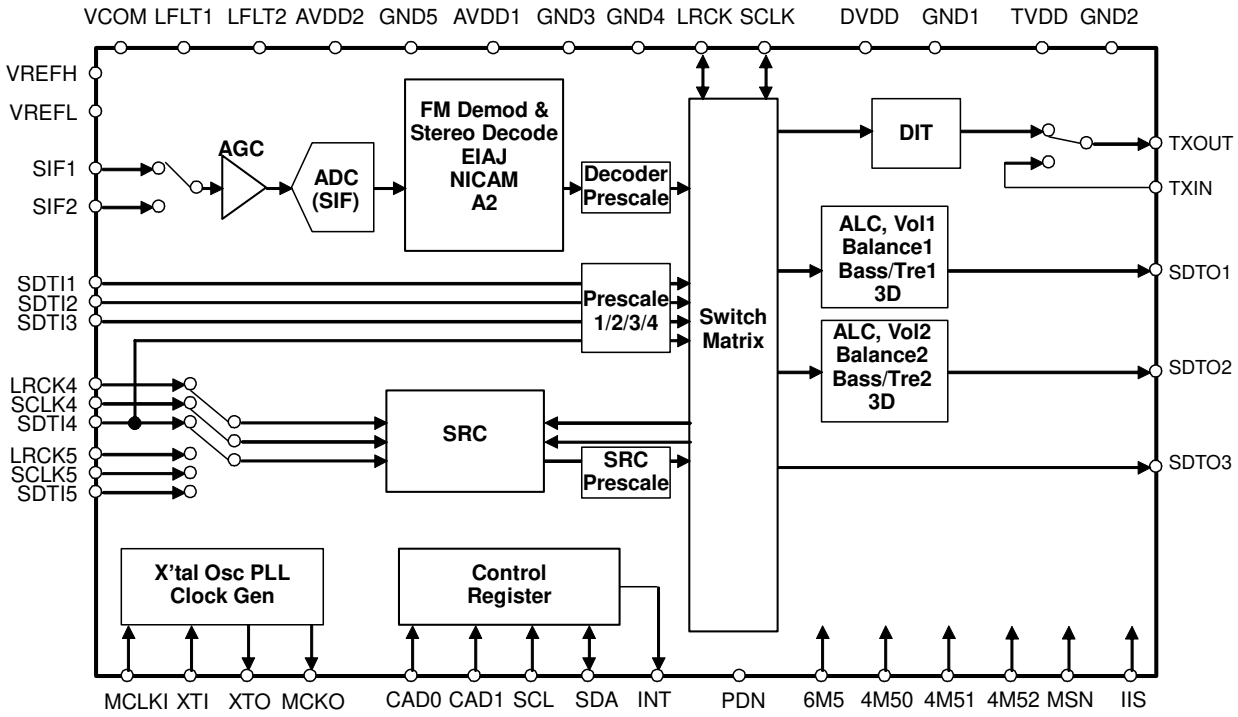
FEATURES

1. Stereo Decoding
- ☐ Capable of receiving Sound Intermediate Frequency (SIF) with Selector and FM Demodulation
- ☐ Automatic Gain Control (AGC: 100mVpp ~ 1Vpp) for SIF input
- ☐ Alignment Free Digital Stereo Decoding
  - EIA-J
  - NICAM: B/G, L, I, D/K with FM/AM Mono
  - A2: B/G, D/K1, D/K2, D/K3, M/N
- ☐ Automatic/Manual Stereo Decoding Standard Selection
- ☐ Automatic/Manual Audio Mode (Stereo/MONO/two sounds) Selection
- ☐ Signal Quality Detection for Auto Selection Mode
- ☐ High FM Deviation Option (max: 540kHz)
- ☐ I2S sampling rate (fs): 32k/44.1k/48kHz

2. Audio Processing (Two Stereos)
- ☐ Automatic Level Control (ALC)
- ☐ Balance
- ☐ 5-band Equalizer
- ☐ Stereo Separation Emphasis
- ☐ Digital Volume Control with Soft Mute (+12dB~-115dB, 0.5dB/step)
- ☐ Audio Data Interface:
  - I2S input x 5 (2 inputs: SRC available)
  - I2S output x 3
  - Master/Slave Mode
  - Audio Format: 24bit Left justified /Right justified / I^2S or TDM

3. Asynchronous Sample Rate Converter (SRC)
- ☐ Input Sample Rate: 8k~192kHz
- ☐ fso/fsi: 1/6~6

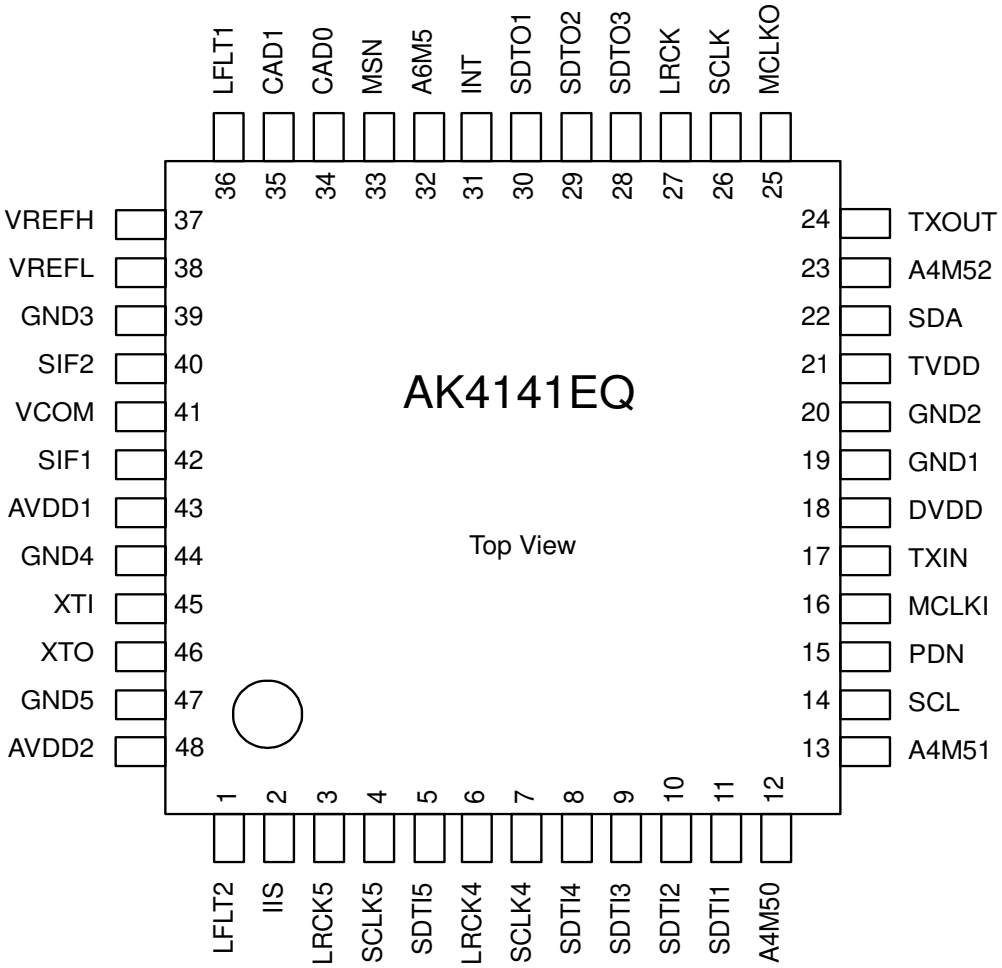
4. Digital Audio Interface Transmitter (DIT) with Through Mode
5. Integrated X'tal Oscillator
6. Master Clock: 256fs/384fs/512fs/768fs/1024fs
7. I2C-bus Control Interface
8. Power Supply: DVDD=1.8V±0.1V, AVDD=3.3V±0.3V, TVDD=1.7V~3.6V
9. Ta: -20 ~ 85°C
10. Package: 48pin LQFP


VCOM LFLT1 LFLT2 AVDD2 GND5 AVDD1 GND3 GND4 LRCK SCLK DVDD GND1 TVDD GND2
VREFH
VREFL
SIF1
SIF2
AGC
ADC (SIF)
FM Demod & Stereo Decode EIAJ NICAM A2
Decoder Prescale
DIT
TXOUT
TXIN
SDTI1
SDTI2
SDTI3
Prescale 1/2/3/4
Switch Matrix
ALC, Vol1 Balance1 Bass/Tre1 3D
SDTO1
ALC, Vol2 Balance2 Bass/Tre2 3D
SDTO2
LRCK4
SCLK4
SDTI4
LRCK5
SCLK5
SDTI5
SRC
SRC Prescale
SDTO3
X'tal Osc PLL Clock Gen
Control Register
MCLKI XTI XTO MCKO CAD0 CAD1 SCL SDA INT PDN 6M5 4M50 4M51 4M52 MSN IIS

■ Ordering Guide

AK4141EQ	-20 ~ +85°C 48pin LQFP (0.5mm pitch)
AKD4141	Evaluation Board for AK4141

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	FILT2	O	PLL Loop Filter 2 Pin A 0.68μF capacitor should be connected to GND5 externally. Hi-Z when PDN Pin = "L".
2	IIS	I	Audio Data Format Select Pin. ORed with ODIF bit, ORed with IDIF0 bit. "L": 24bit Left justified if IDIF0 bit = "0"(default) "H": 24/16 bit IIS
3	LRCK5	I	Input Channel Clock 5 Pin
4	SCLK5	I	Audio Serial Data Clock 5 Pin
5	SDTI5	I	Audio Serial Data Input 5 Pin
6	LRCK4	I	Input Channel Clock 4 Pin
7	SCLK4	I	Audio Serial Data Clock 4 Pin
8	SDTI4	I	Audio Serial Data Input 4 Pin Should be synchronized to LRCK and SCLK when SRC is not used.
9	SDTI3	I	Audio Serial Data Input 3 Pin
10	SDTI2	I	Audio Serial Data Input 2 Pin
11	SDTI1	I	Audio Serial Data Input 1 Pin
12	A4M50	I	Decoder Standard Preference Control 0 Pin for 4.5MHz Carrier This pin is internally XORed with A4M50 bit (default = "1").
13	A4M51	I	Decoder Standard Preference Control 1 Pin for 4.5MHz Carrier This pin is internally XORed with A4M51 bit (default = "1").
14	SCL	I	Control Data Clock Pin for I2C bus
15	PDN	I	Power-Down Mode & Reset Pin When "L", the AK4141 is powered-down, all registers are reset. And then all digital output pins go "L". The AK4141 must be reset once upon power-up.
16	MCKI	I	Master Clock Input Pin
17	TXIN	I	S/PDIF Input Pin For through output. No Input Amplifier integrated.
18	DVDD	-	Digital Power Supply Pin, 1.7V~1.9V
19	GND1	-	Ground Pin, 0V
20	GND2	-	Ground Pin, 0V
21	TVDD	-	I/O Buffer Power Supply Pin, 1.7V~3.6V
22	SDA	I/O	Control Data Pin for I2C bus
23	A4M52	I	Decoder Standard Preference Control 2 Pin for 4.5MHz Carrier This pin is internally ORed with A4M52 bit (default = "0").
24	TXOUT	O	S/PDIF Output pin. Outputs "L" when PDN Pin = "L".
25	MCKO	O	Master Clock Output Pin. Outputs "L" when PDN Pin = "L".
26	SCLK	I/O	Audio Serial Data Clock Pin. Outputs "L" when PDN Pin = "L" and MSN Pin = "H". Hi-Z when PDN Pin = "L" and MSN Pin = "L".
27	LRCK	I/O	Input Channel Clock Pin Outputs "L" when PDN Pin = "L" and MSN Pin = "H". Hi-Z when PDN Pin = "L" and MSN Pin = "L".
28	SDTO3	O	Audio Serial Data Output 3 Pin Outputs "L" when PDN Pin = "L".
29	SDTO2	O	Audio Serial Data Output 2 Pin Outputs "L" when PDN Pin = "L".
30	SDTO1	O	Audio Serial Data Output 1 Pin Outputs "L" when PDN Pin = "L".

PIN/FUNCTION

31	INT	O	Interrupt Pin Outputs “L” when PDN Pin = “L”.
32	A6M5	I	Decoder Standard Preference Control for 6.5MHz carrier. “L”: SECAM L NICAM “H”: D/K1, D/K2, D/K3 or D/K NICAM This Pin is internally ORed with A6M5 bit (default = “0”).
33	MSN	I	Master Mode Select Pin “L”: Slave mode if CKS[2:0] bits = “000”(default) “H”: Master mode of MCLK = 256fs if CKS2 bit = “0”(default)
34	CAD0	I	Chip Address 0 pin Should match CAD0 bit in I2C first byte.
35	CAD1	I	Chip Address 1 pin Should match CAD1 bit in I2C first byte.
36	FILT1	O	PLL Loop Filter 1 Pin A 4.7nF capacitor should be connected to GND3 externally. Hi-Z when PDN Pin = “L”.
37	VREFH	O	ADC Voltage Reference High Pin A 0.1μF capacitor should be connected to GND3, and another 0.1μF capacitor should be connected to VREFL Pin externally. Hi-Z when PDN Pin = “L”.
38	VREFL	O	ADC Voltage Reference Low Pin A 0.1μF capacitor should be connected to GND3 externally. Hi-Z when PDN Pin = “L”.
39	GND3	-	Ground Pin, 0V
40	SIF2	I	Sound Intermediate Frequency(SIF) Input 2 Pin
41	VCOM	O	ADC Common Voltage Output Pin. A 1μF capacitor should be connected to GND3 externally. Hi-Z when PDN Pin = “L”.
42	SIF1	I	Sound Intermediate Frequency(SIF) Input 1 Pin
43	AVDD1	-	Analog Power Supply Pin, 3.0V~3.6V
44	GND4	-	Ground Pin, 0V
45	XTI	I	X'tal Input Pin
46	XTO	O	X'tal Output Pin. Outputs “L” when PDN pin = “L”.
47	GND5	-	Ground Pin, 0V
48	AVDD2	-	Analog Power Supply Pin, 3.0V~3.6V

Note: All digital input pins should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	SIF1, SIF2	These pins should be connected to GND through 10nF capacitor.
Digital	TXOUT, MCLKO, SDTO1, SDTO2, SDTO3, INT, LRCK(master mode), SCLK(master mode)	These pins should be open.
	LRCK5, SCLK5, SDTI5, LRCK4, SCLK4, SDTI4, LRCK(slave mode), SCLK(slave mode), SDTI3, SDTI2, SDTI1, A4M50, A4M51, A4M52, A6M5, SCL, MCLKI, TXIN, SDA, IIS, MSN, CAD1, CAD0	These pins should be connected to GND.

ABSOLUTE MAXIMUM RATINGS

(GND1=GND2=GND3=GND4=GND5=0V; Note 1)

Parameter		Symbol	min	max	Unit
Power Supplies	Analog	AVDD	-0.3	4.3	V
	Digital	DVDD	-0.3	2.4	V
	Digital I/O	TVDD	-0.3	4.3	V
Input Current, Any Pin Except Supply		IIN	-	±10	mA
Analog Input Voltage (SIF1, SIF2 pin)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 2)		VIND	–0.3	TVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–20	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. LRCK5, SCLK5, SDTI5, LRCK4, SCLK4, SDTI4, LRCK(slave mode), SCLK(slave mode), SDTI3, SDTI2, SDTI1, A4M50, A4M51, A4M52, A6M5, SCL, MCLKI, TXIN, SDA, IIS, MSN, CAD1 and CAD0 pin.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(GND1=GND2=GND3=GND4=GND5=0V; Note 1)

Parameter		Symbol	min	typ	max	Unit
Power Supplies	AVDD	AVDD	3.0	3.3	3.6	V
	DVDD	DVDD	1.7	1.8	1.9	V
	TVDD	TVDD	DVDD	3.3	3.6	V

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

AUDIO CHARACTERISTICS

(Ta=25°C; AVDD=3.3V, DVDD=1.8V, TVDD=3.3V; GND1=GND2=GND3=GND4=GND5=0V; fs=48kHz; SCLK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=50Hz ~ 13kHz; unless otherwise specified)

SIF & Demodulator Parameter	**min**	**typ**	**max**	**Unit**
SIF Input Impedance				
GSEL bit = 0	4.05	4.50		kohm
GSEL bit = 1	5.09	5.66		kohm
SIF Separation (Note 3)	30	50		dB
AGC step width		0.64		dB
Input Voltage				
1 or 2 FM Carriers				
GSEL bit = "0"	0.1		1.4	Vpp
GSEL bit = "1"	0.1		1.0	Vpp
1 FM and 1 NICAM Carrier				
GSEL bit = "0"	0.1		1.4	Vpp
GSEL bit = "1"	0.1		1.0	Vpp
1 AM and 1 NICAM Carrier				
GSEL bit = "0"	0.1		0.8	Vpp
GSEL bit = "1"	0.1		0.8	Vpp
1 NICAM Only				
GSEL bit = "0"	0.05		1.0	Vpp
GSEL bit = "1"	0.05		1.0	Vpp
Max FM-deviation (approx.)				
Normal			+/-180	kHz
High deviation			+/-360	kHz
Very High Deviation			+/-540	kHz
NICAM Characteristics	**min**	**typ**	**max**	**Unit**
Output level (1kHz, 0dBr)	-1.5		+1.5	dB
S/N	74	80		dB
THD+N		0.05	0.15	%
NICAM Bit Error Rate (FM+ NICAM, normal condition)			1	10^{-7}
Frequency response (20 ~ 15kHz, -12dB, dual)	-1		+1	dB
NICAM Crosstalk attenuation (dual)	80			dB
Channel separation (stereo)	80			dB
FM Characteristics (Note 4)	**min**	**typ**	**max**	**Unit**
Output level (1kHz, 0dBr)	-1.5		+1.5	dB
S/N	67	73		dB
THD+N		0.1	0.3	%
Frequency response (20 ~ 12kHz, -12dB, dual)	-1		+1	dB
FM Crosstalk attenuation (dual)	75	85		dB
Channel separation (stereo)	30	40		dB
AM Characteristics	**min**	**typ**	**max**	**Unit**
S/N	47	62		dB
THD+N		1.2	3	%
Frequency response (20 ~ 12kHz, -12dB, dual)	-2.5		+1	dB

Note 3. Selected SIF pin is connected to GND through 10nF capacitor.
Note 4. 1 FM-Carrier, 5.5MHz.

AUDIO CHARACTERISTICS (Continued)

(Ta=25°C; AVDD=3.3V, DVDD=1.8V, TVDD=3.3V; GND1=GND2=GND3=GND4=GND5=0V; fs=48kHz; SCLK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=50Hz ~ 13kHz; unless otherwise specified)

EIAJ Characteristics	min	typ	max	Unit
S/N				
Stereo	54	60		dB
Sub	54	60		dB
THD+N (1kHz L or R or Sub 100%)				
Stereo		0.3	0.9	%
Sub		0.3	0.9	%
Frequency response				
Stereo (20 ~ 12kHz, 100%EIM)	-1		+1	dB
Sub (20 ~ 12kHz, 100%EIM)	-1		+1	dB
Channel separation (stereo)	30	40		dB

SRC CHARACTERISTICS

(Ta=25°C; AVDD=3.3V, DVDD=1.8V, TVDD=3.3V; GND1=GND2=GND3=GND4=GND5=0V; fs=48kHz; SCLK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ FSO/2; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
SRC Characteristics:					
Resolution				20	Bits
Input Sample Rate	FSI	8		216	kHz
Output Sample Rate	FSO	32		48	kHz
THD+N (Input = 1kHz, 0dBFS, Note 5)					
FSO/FSI = 48kHz/8kHz		-	-100	-	dB
FSO/FSI = 48kHz/32kHz		-	-100	-	dB
FSO/FSI = 48kHz/192kHz		-	-100	-	dB
Worst Case (FSO/FSI = 32kHz/176.4kHz)		-	-91	-81	dB
Dynamic Range (Input = 1kHz, –60dBFS, A-weighted, Note 5)					
FSO/FSI = 48kHz/8kHz		-	115	-	dB
FSO/FSI = 48kHz/32kHz		-	115	-	dB
FSO/FSI = 48kHz/192kHz		-	115	-	dB
Worst Case (FSO/FSI = 48kHz/32kHz)		111	115	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1/6		6	-

Note 5. Measured by Audio Precision System Two Cascade.

Power Supplies				
Parameter	**min**	**typ**	**max**	**Unit**
Power Supply Current				
Normal Operation (PDN pin = “H”)				
TVDD		5	8	mA
AVDD1+AVDD2		20	28	mA
DVDD		61	92	mA
Power-Down Mode (PDN pin = “L”; Note: 1)				
TVDD		10	100	μA
AVDD1+AVDD2		10	100	μA
DVDD		10	100	μA

Note: 1. All digital inputs including clock pins are held at DVDD or GND.

SRC FILTER CHARACTERISTICS

(Ta=25°C; AVDD=3.0 ~ 3.6V, DVDD=1.7V~ 1.9V, TVDD=1.7 ~ 3.6V; GND1=GND2=GND3=GND4=GND5=0V)

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband –0.01dB	0.985 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	0.905 ≤ FSO/FSI < 0.985	PB	0		0.4167FSI	kHz
	0.714 ≤ FSO/FSI < 0.905	PB	0		0.3195FSI	kHz
	0.656 ≤ FSO/FSI < 0.714	PB	0		0.2852FSI	kHz
	0.536 ≤ FSO/FSI < 0.656	PB	0		0.2182FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0		0.2177FSI	kHz
	0.452 ≤ FSO/FSI < 0.492	PB	0		0.1948FSI	kHz
	0.357 ≤ FSO/FSI < 0.452	PB	0		0.1458FSI	kHz
	0.324 ≤ FSO/FSI < 0.357	PB	0		0.1302FSI	kHz
	0.246 ≤ FSO/FSI < 0.324	PB	0		0.0917FSI	kHz
	0.226 ≤ FSO/FSI < 0.246	PB	0		0.0826FSI	kHz
	0.1667 ≤ FSO/FSI < 0.226	PB	0		0.0583FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
	0.905 ≤ FSO/FSI < 0.985	SB	0.5021FSI			kHz
	0.714 ≤ FSO/FSI < 0.905	SB	0.3965FSI			kHz
	0.656 ≤ FSO/FSI < 0.714	SB	0.3643FSI			kHz
	0.536 ≤ FSO/FSI < 0.656	SB	0.2974FSI			kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2813FSI			kHz
	0.452 ≤ FSO/FSI < 0.492	SB	0.2604FSI			kHz
	0.357 ≤ FSO/FSI < 0.452	SB	0.2116FSI			kHz
	0.324 ≤ FSO/FSI < 0.357	SB	0.1969FSI			kHz
	0.246 ≤ FSO/FSI < 0.324	SB	0.1573FSI			kHz
	0.226 ≤ FSO/FSI < 0.246	SB	0.1471FSI			kHz
	0.1667 ≤ FSO/FSI < 0.226	SB	0.1020FSI			kHz
Passband Ripple		PR			±0.01	dB
Stopband Attenuation	0.985 ≤ FSO/FSI ≤ 6.000	SA	102.2			dB
	0.905 ≤ FSO/FSI < 0.985	SA	100.4			dB
	0.714 ≤ FSO/FSI < 0.905	SA	99.0			dB
	0.656 ≤ FSO/FSI < 0.714	SA	101.6			dB
	0.536 ≤ FSO/FSI < 0.656	SA	99.5			dB
	0.492 ≤ FSO/FSI < 0.536	SA	95.2			dB
	0.452 ≤ FSO/FSI < 0.492	SA	96.6			dB
	0.357 ≤ FSO/FSI < 0.452	SA	97.0			dB
	0.324 ≤ FSO/FSI < 0.357	SA	94.4			dB
	0.246 ≤ FSO/FSI < 0.324	SA	95.8			dB
	0.226 ≤ FSO/FSI < 0.246	SA	95.0			dB
	0.1667 ≤ FSO/FSI < 0.226	SA	73.7			dB
Group Delay	(Note 6)	GD	-	56	-	1/fs

Note 6. This value is the time from the rising edge of LRCK after data is input to rising edge of LRCK after data is output, when LRCK for Output data corresponds with LRCK for Input.

DC CHARACTERISTICS

(Ta=25°C; AVDD=3.0 ~ 3.6V, DVDD=1.7V~ 1.9V, TVDD=1.7 ~ 3.6V; GND1=GND2=GND3=GND4=GND5=0V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage					
TVDD < 2.7V	VIH	80%TVDD	-	-	V
TVDD ≥ 2.7V	VIH	70%TVDD	-	-	V
Low-Level Input Voltage					
TVDD < 2.7V	VIL	-	-	20%TVDD	V
TVDD ≥ 2.7V	VIL	-	-	30%TVDD	V
High-Level Output Voltage (Iout=-400μA)	VOH	TVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= -400μA(except SDA pin), 3mA(SDA pin))	VOL	-		0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=-20~ 85°C; AVDD= 3.0~3.6V, DVDD=1.7~1.9V TVDD=1.7~3.6V; GND1=GND2=GND3=GND4=GND5=0V; C_L=20pF; unless otherwise specified)

Parameter		Symbol	min	typ	max	Unit
Crystal Resonator Frequency		fXTAL		256fs		
fs=32kHz				8.192		MHz
fs=44.1kHz				11.2896		MHz
fs=48kHz				12.288		MHz
Master Clock Timing						
Master Clock	128fs:	fCLK	4.096		6.144	MHz
	Pulse Width Low	tCLKL	65			ns
	Pulse Width High	tCLKH	65			ns
	192fs:	fCLK	6.144		9.216	MHz
	Pulse Width Low	tCLKL	43			ns
	Pulse Width High	tCLKH	43			ns
	256fs:	fCLK	8.192		12.288	MHz
	Pulse Width Low	tCLKL	27			ns
	Pulse Width High	tCLKH	27			ns
	384fs:	fCLK	12.288		18.432	MHz
	Pulse Width Low	tCLKL	20			ns
	Pulse Width High	tCLKH	20			ns
	512fs:	fCLK	16.384		24.576	MHz
	Pulse Width Low	tCLKL	16			ns
	Pulse Width High	tCLKH	16			ns
	768fs:	fCLK	24.576		36.864	MHz
	Pulse Width Low	tCLKL	11			ns
	Pulse Width High	tCLKH	11			ns
	1024fs:	fCLK	32.768		49.152	MHz
	Pulse Width Low	tCLKL	8			ns
	Pulse Width High	tCLKH	8			ns

SWITCHING CHARACTERISTICS (Continued)

(Ta=-20~ 85°C; AVDD= 3.0~3.6V, DVDD=1.7~1.9V TVDD=1.7~3.6V; GND1=GND2=GND3=GND4=GND5=0V; C_L=20pF; unless otherwise specified)

Parameter (Note 8)	Symbol	min	typ	max	Unit
LRCK Timing (Slave Mode)					
Normal mode (TDM="0")					
LRCK Frequency	fs	32		48	kHz
Duty Cycle	Duty	45		55	%
TDM256 mode (TDM="1")					
LRCK Frequency	fs	32		48	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
SRC Input					
LRCK Frequency	fs	8		192	KHz
Duty Cycle	Duty	45		55	%
LRCK Timing (Master Mode)					
Normal mode (TDM="0")					
LRCK Frequency	fs	32		48	kHz
Duty Cycle	Duty		50		%
TDM256 mode (TDM="1")					
LRCK Frequency	fs	32		48	kHz
"H" time (Note 7)	tLRH		1/8fs		ns
Audio Interface Timing (Slave mode)					
Normal mode (TDM="0")					
SCLK Period	tBCK	160			ns
SCLK Pulse Width Low	tBCKL	65			ns
Pulse Width High	tBCKH	65			ns
LRCK Edge to SCLK "↑" (Note 9)	tLRB	30			ns
SCLK "↑" to LRCK Edge (Note 9)	tBLR	30			ns
LRCK to SDTO(MSB) (Except I^2S mode)	tLRS			35	ns
SCLK "↓" to SDTO	tBSD			35	ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM256 mode (TDM="1")					
SCLK Period	tBCK	81			ns
SCLK Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCK Edge to SCLK "↑" (Note 9)	tLRB	20			ns
SCLK "↑" to LRCK Edge (Note 9)	tBLR	20			ns
SCLK "↓" to SDTO	tBSD			20	ns
TDMIN Hold Time	tSDH	10			ns
TDMIN Setup Time	tSDS	10			ns
SRC Input (Note 10)					
SCLK Period	tBCK	81			ns
SCLK Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCK Edge to SCLK "↑" (Note 9)	tLRB	20			ns
SCLK "↑" to LRCK Edge (Note 9)	tBLR	20			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns

SWITCHING CHARACTERISTICS (Continued)

(Ta=-20~ 85°C; AVDD= 3.0~3.6V, DVDD=1.7~1.9V TVDD=1.7~3.6V; GND1=GND2=GND3=GND4=GND5=0V; C_L=20pF; unless otherwise specified)

Parameter (Note 8)	Symbol	min	typ	max	Unit
Audio Interface Timing (Master mode)					
Normal mode (TDM="0")					
SCLK Frequency	fBCK		64fs		Hz
SCLK Duty	dBCK		50		%
SCLK "↓" to LRCK	tMBLR	–20		20	ns
SCLK "↓" to SDTO	tBSD	–40		40	ns
TDM256 mode (TDM="1")					
SCLK Frequency	fBCK		256fs		Hz
SCLK Duty (Note 11)	dBCK		50		%
SCLK "↓" to LRCK	tMBLR	–12		12	ns
SCLK "↓" to SDTO	tBSD	–20		20	ns
TDMIN Hold Time	tSDH	10			ns
TDMIN Setup Time	tSDS	10			ns
Power-Down & Reset Timing					
PDN Pulse Width (Note 12)	tPD	150			ns
PDN "↑" to SDTO valid (Note 13)	tPDV		TBD		1/fs

Note 7. "L" time at I^2S format.
Note 8. SCLK= SCLK/SCLK4/SCLK5, LRCK= SCLK/LRCK4/LRCK5 unless otherwise specified.
Note 9. SCLK rising edge must not occur at the same time as LRCK edge.
Note 10. SCLK= SCLK4/SCLK5, LRCK= LRCK4/LRCK5.
Note 11. This value is when fs=48kHz or 44.1kHz. When fs=32kHz, L=(5/9x100)% and H=(4/9x100)%.
Note 12. The AK4141 can be reset by bringing the PDN pin = "L".
Note 13. This cycle is the number of LRCK rising edges from the PDN pin = "H".

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 14)	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on SDA	Cb	0		400	pF

Note 14. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 15. I^2C is a registered trademark of Philips Semiconductors.

■ Timing Diagram

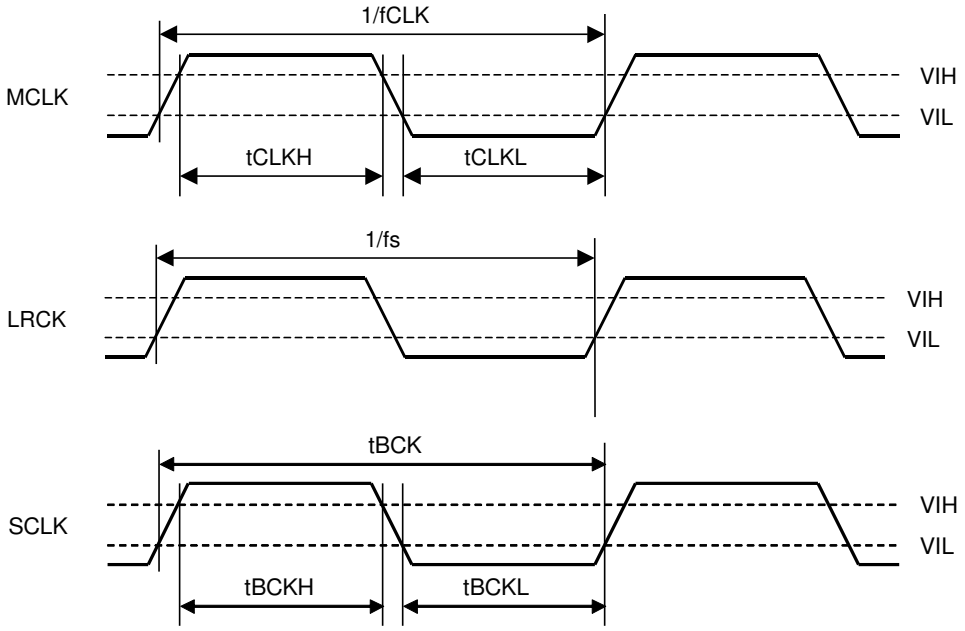


Figure 1. Clock Timing (TDM bit = "0")

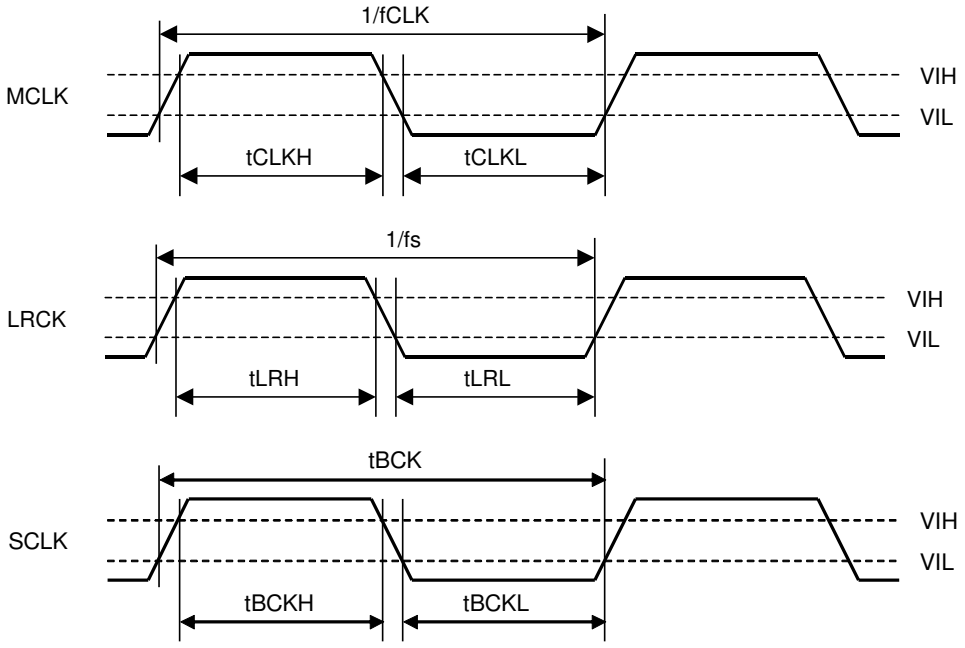


Figure 2. Clock Timing (TDM bit = "1")

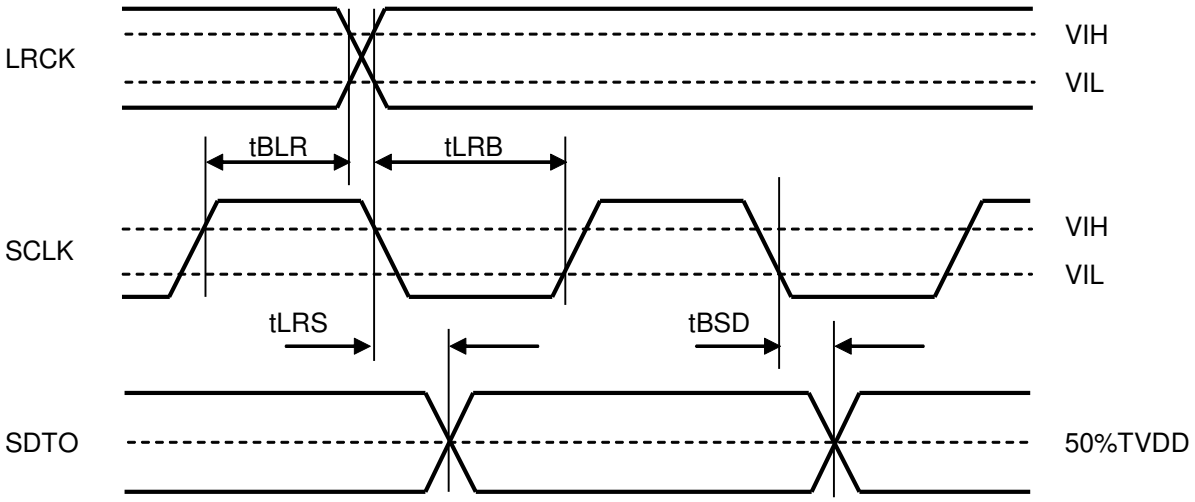


Figure 3. Audio Interface Timing (Slave mode, Normal Mode)

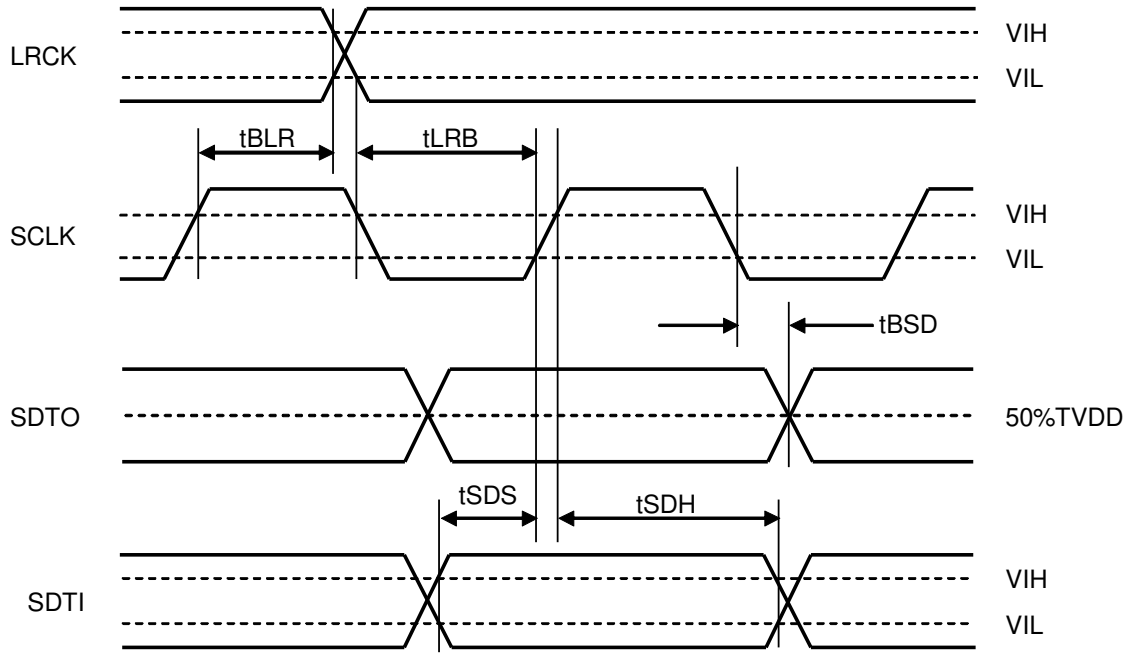


Figure 4. Audio Interface Timing (Slave mode, TDM Mode)

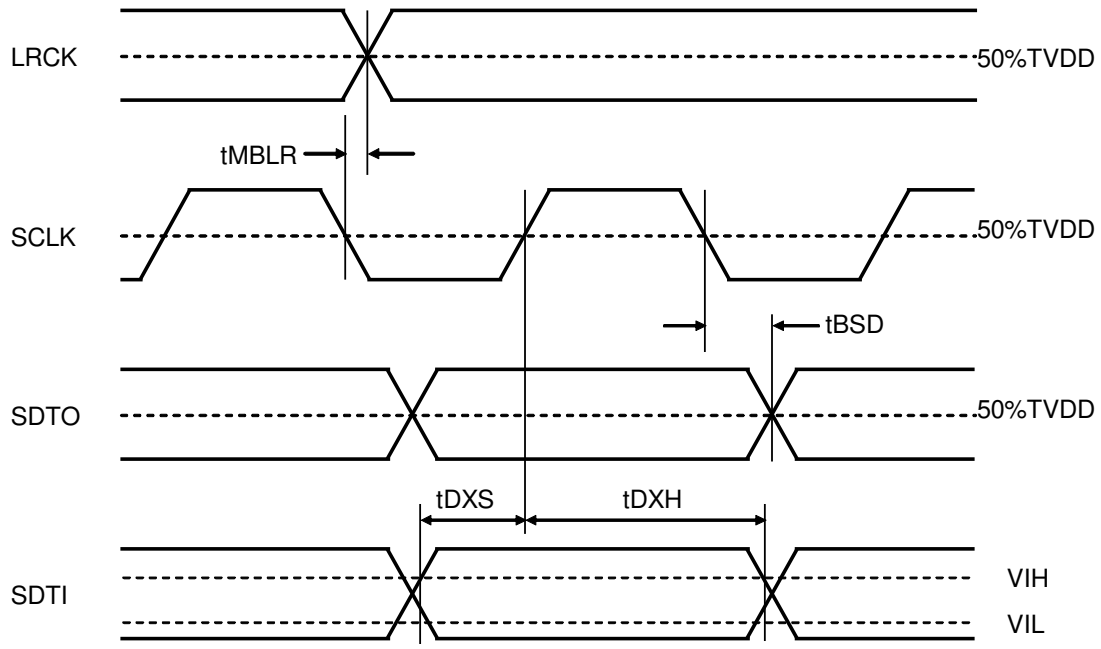


Figure 5. Audio Interface Timing (Master mode, Normal Mode)

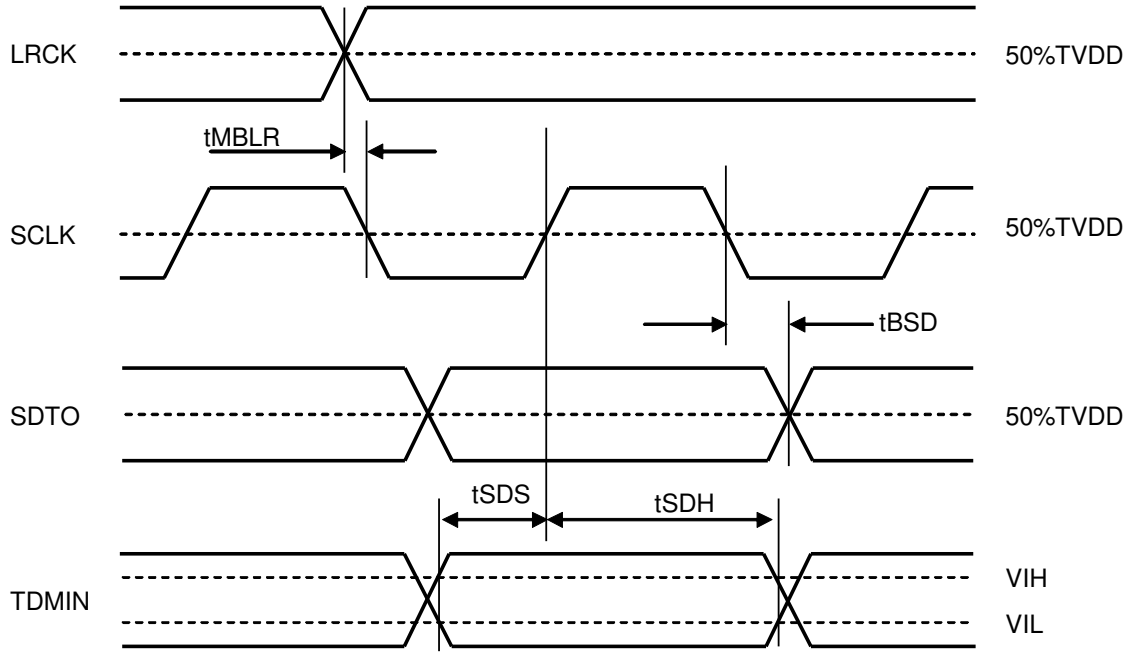


Figure 6. Audio Interface Timing (Master mode, TDM Mode)

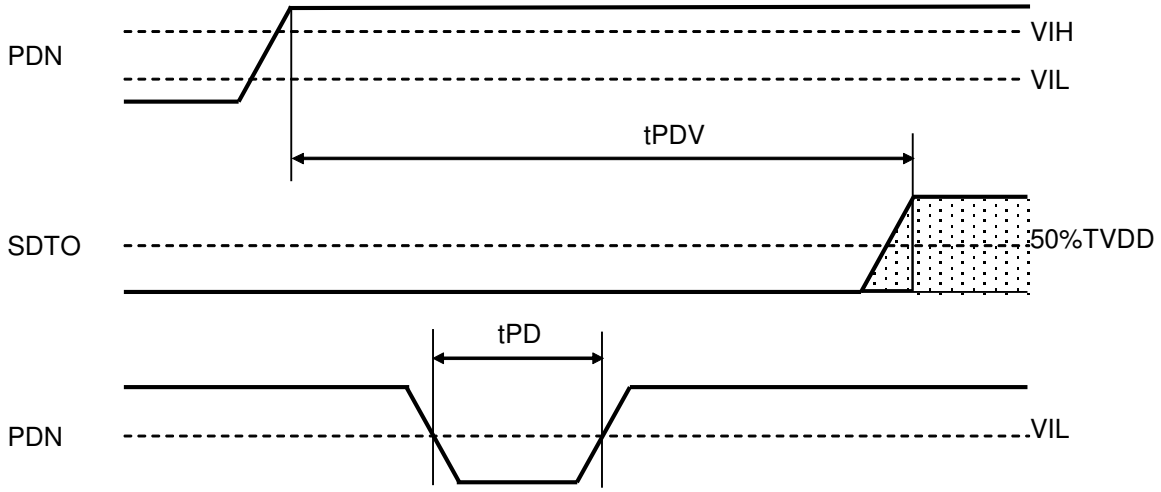


Figure 7. Power Down & Reset Timing

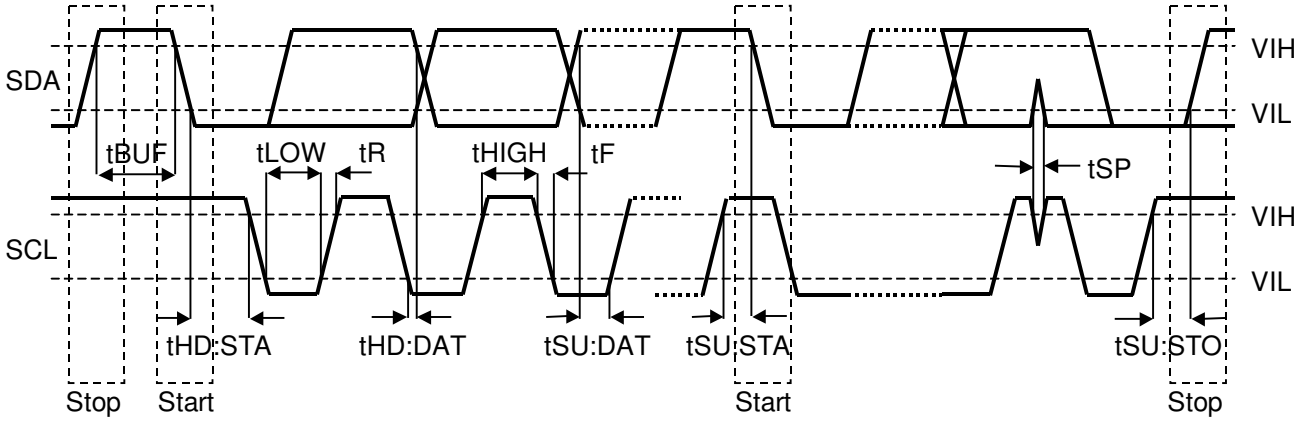


Figure 8. I^2C Bus mode Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4141, are MCLK(or XTI), LRCK and SCLK. The MCLK(or XTI) should always be present whenever the AK4141 is in normal operation, and should be synchronized with LRCK but the phase is not critical. The on-chip X'tal oscillator or external system clock through MCKI can be used for the AK4141 operation. If the external clocks are not present, the AK4141 should be in the power-down mode (PDN pin = "L") or in the reset mode (RSTN bit = "0"). After exiting reset at power-up etc., the AK4141 is in the power-down mode until MCLK(or XTI) and LRCK are input.

The AK4141 supports both master mode (SCLK, LRCK = output) and slave mode (SCLK, LRCK = input). The AK4141 is master mode when MSN pin = "H", slave mode when MSN pin = "L". SRC inputs (SCLK4/5, LRCK4/5) are always slave mode (input) and can operate asynchronously.

PDN pin	MSN pin	SCLK, LRCK	SCLK4/5, LRCK4/5
L	L	Input (slave mode)	Input (slave mode)
	H	Output "L" (master mode)	Input (slave mode)
H	L	Input (slave mode)	Input (slave mode)
	H	Output (master mode)	Input (slave mode)

note: when CKS2-0 bits are default.

Table 1. Master/Salve Mode

The MSN pin and the CKS2-0 bits select the clock frequency (Table 2). The external clock (X'tal or MCKI) should always be supplied except in the power-down mode. The AK4141 is in power-down mode until the clock is supplied.

MSN pin	CKS2 bit	CKS1 bit	CKS0 bit	Master /Slave	Master Clock Speed
L	0	0	0	Slave	128fs, 192fs, 256fs, 384fs, 512fs, 768fs, 1024fs (register default)
L	0	0	1	Master	128fs
L	0	1	0	Master	192fs
L	0	1	1	Master	256fs
L	1	0	0	Master	384fs
L	1	0	1	Master	512fs
L	1	1	0	Master	768fs
L	1	1	1	Master	1024fs
H	0	x	x	Master	256fs (register default)
H	1	x	x	Master	1024fs

(x: Don't care.)

Table 2. System clock control

LRCK	MCLK (MHz)						
fs	128fs	192fs	256fs	384fs	512fs	768fs	1024fs
32.0kHz	4.0960	6.1440	8.1920	12.2880	16.3840	24.5760	32.7680
44.1kHz	5.6448	7.5264	11.2896	16.9344	22.5792	33.8688	45.1584
48.0kHz	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640	49.1520

Table 3. System clock example

■ Multi-standard Stereo Decoding

The AK4141 receives the Sound IF(SIF) signal and demodulates/decodes according to NICAM/A2/EIA-J standards. The AK4141 can automatically select the stereo standard according to the actual input signal, the A4M5[2-0] pins(XORed with A4M5[2-0] bits, default = "011") and the A6M5 pin (XORed with A6M5 bit) setting.

A6M5 bit	A6M5 pin	Decoder Standard Preference1
0 (default)	L	SECAM L NICAM
0 (default)	H	D/K1, D/K2, D/K3 or D/K NICAM
1	L	D/K1, D/K2, D/K3 or D/K NICAM
1	H	SECAM L NICAM

Table 4. Decoder Standard Preference 1 (for 6.5MHz carrier)

A4M5[2-0] pins	Decoder Standard Preference2
LLL	PAL (Chroma Carrier)
LLH	M-Korea
LHL	EIAJ
LHH	Reserved
HLL	Reserved
HLH	Reserved
HHL	Reserved
HHH	Reserved

Table 5. Decoder Standard Preference 2 (for 4.5MHz carrier. Pin control. A4M5[2-0] bits = "011"(default))

A4M5[2-0] bits	Decoder Standard Preference2
00H	Reserved
01H	EIAJ
02H	M-Korea
03H	PAL (Chroma Carrier)
04H	Reserved
05H	Reserved
06H	Reserved
07H	Reserved

Table 6. Decoder Standard Preference 2 (for 4.5MHz carrier. Register control. A4M5[2-0] pins = "LLL")

■ Audio Serial Interface Format

The IDIF[1-0] and ODIF bit control the audio format for SCLK, SCLK4/5, LRCK, LRCK4/5, SDTI[1-5] and SDTO[1-3]. ODIF bit and IDIF0 bit are ORed with DIF pin. When the TDM bit = "1", the TDM mode is enabled. The SRC inputs (SDTI [4-5]) ignore the TDM bit and operate in normal mode. In all modes the serial data is MSB-first, 2's complement format. The SDTO1-3 pins are clocked out on the falling edge of SCLK pin and the SDTI[1-3] pins are latched on the rising edge of SCLK pin. The SDTI[4-5] pins are latched on the rising edge of SCLK[4-5] pins. In SRC bypass mode, The SCLK[4-5] and LRCK[4-5] should be synchronized to LRCK.

1. Normal mode: TDM bit = "0"
   The TDM bit = "0" sets the AK4141 audio serial interface format to the normal mode. The IIS pin, DIF1-0 bits and ODIF bit select following serial data format (Table 7, Table 8)

MSN pin	IIS pin	IDIF1 bit	IDIF0 bit	Mode	Input Audio Data Format	LRCK		BICK	
						L/R	I/O	speed	I/O
L	L	0	0	0	20bit Right Justified	H/L	I	≥ 16fs	I
			1	1	24bit Right Justified			≥ 48fs	
		1	0	2	24bit Left Justified (register default)			≥ 48fs	
			1	3	24/16bit I2S	L/H		32fs or ≥ 48fs	
	H	0	x	2	24bit Right Justified	H/L		≥ 48fs	
		1		3	24/16bit I2S (register default)	L/H		32fs or ≥ 48fs	
H	L	0	0	4	16bit Right Justified	H/L	O	64fs	O
			1	5	24bit Right Justified				
		1	0	6	24bit Left Justified (register default)				
			1	7	24/16bit I2S	L/H			
	H	0	x	6	24bit Right Justified	H/L			
		1		7	24/16bit I2S (register default)	L/H			

(x: Don't care.)

Table 7. Input Audio Data Format control

MSN pin	IIS pin	ODIF bit	Mode	Output Audio Data Format	LRCK		SCLK	
					L/R	I/O	speed	I/O
L	L	0	8	24bit Left Justified (register default)	H/L	I	≥ 48fs	I
		1	9	24/16bit I2S	L/H		32fs or ≥ 48fs	
	H	x	9	24/16bit I2S (register default)	L/H		32fs or ≥ 48fs	
H	L	0	10	24bit Left Justified (register default)	H/L	O	64fs	O
		1	11	24/16bit I2S	L/H			
	H	x	11	24/16bit I2S (register default)	L/H			

(x: Don't care.)

Table 8. Output Audio Data Format control

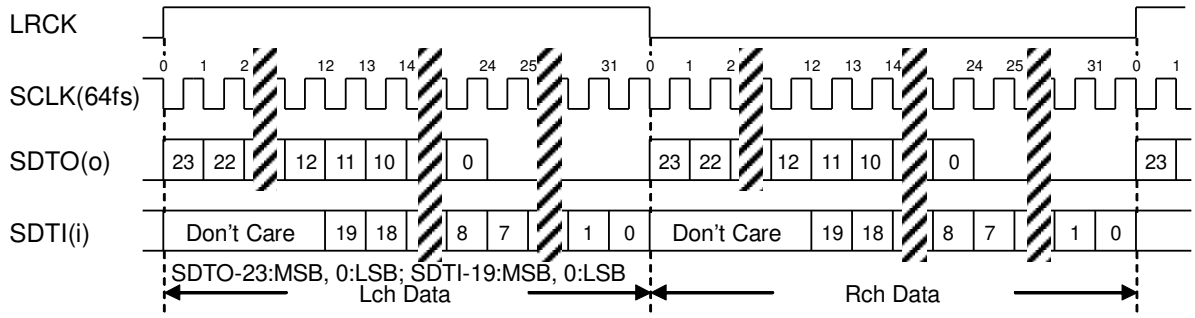


Figure 9. Mode 0/4/8/10 Timing

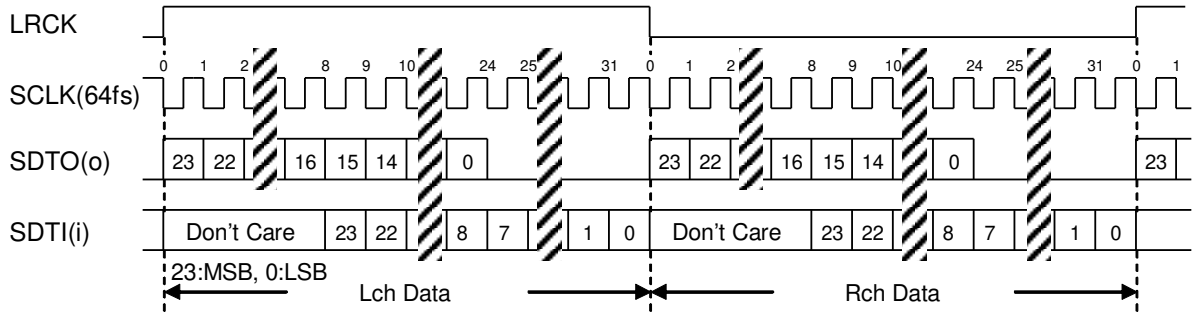


Figure 10. Mode 1/5 Timing

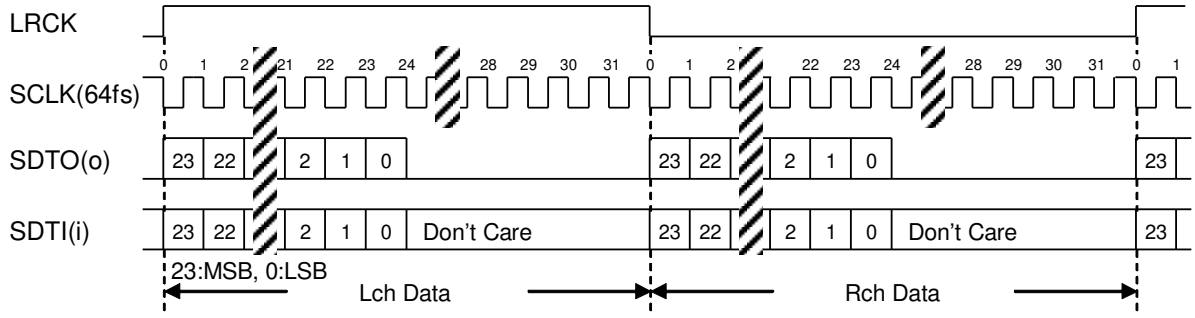


Figure 11. Mode 2/6 Timing

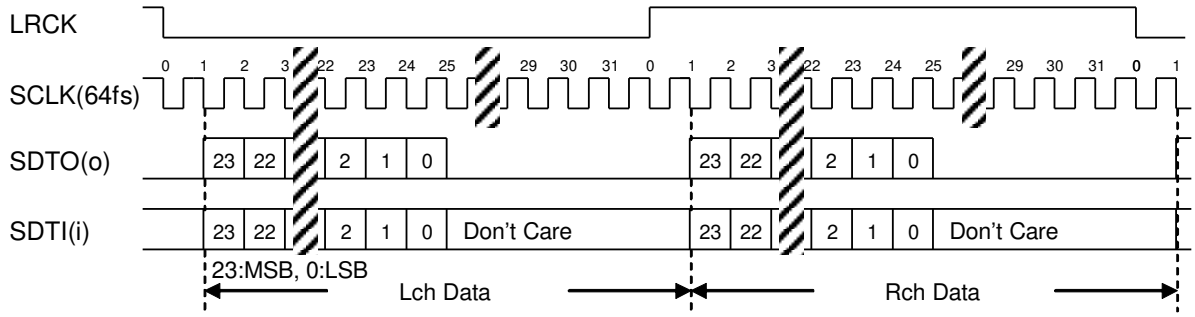


Figure 12. Mode 3/7/9/11 Timing

2. TDM mode: TDM bit = "1"

The TDM bits = "1" set the AK4141 audio serial interface format to the TDM mode. The eight channel serial data (SDTI1/2/3 and SDTI4 at non-SRC mode) is input through the SDTI1 pin. The six channel serial data is output through the SDTO1 pin. The SDTI2/3/4/5 pins are not used for TDM input and the SDTO2/3 pins outputs "L".

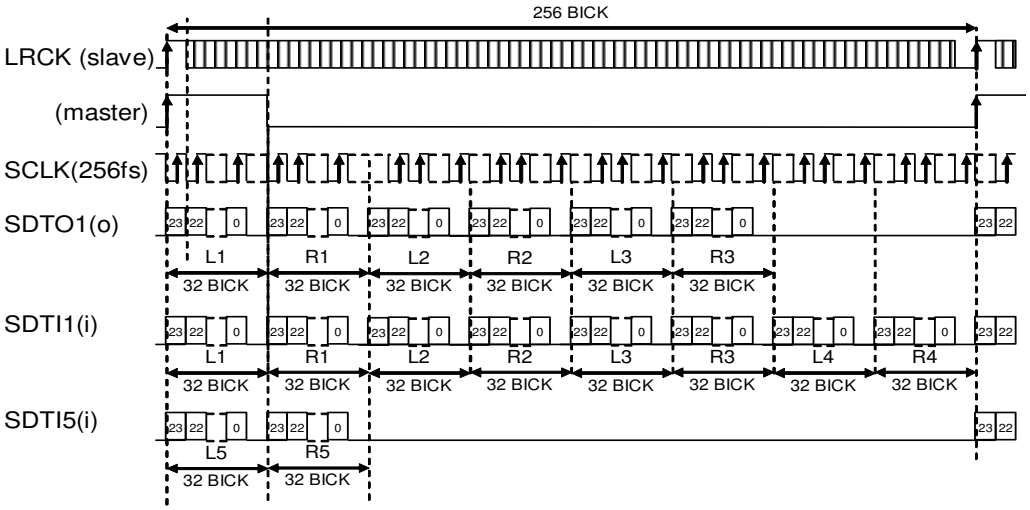


Figure 13. TDM MSB Justified Timing

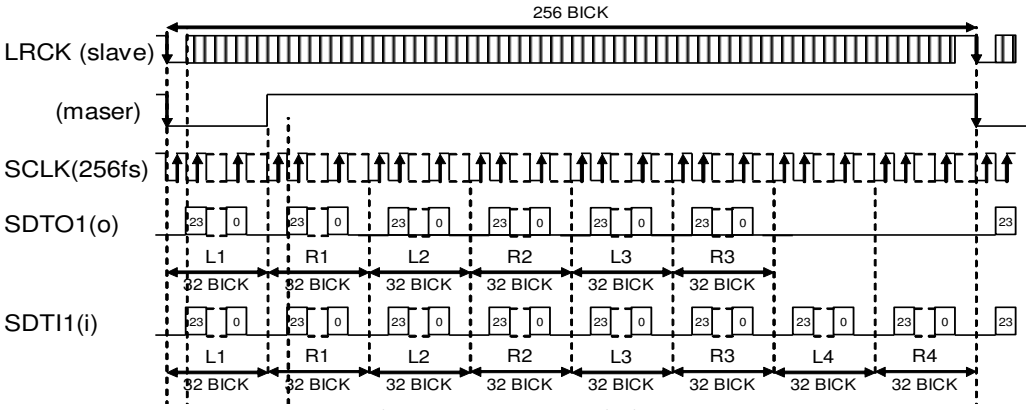
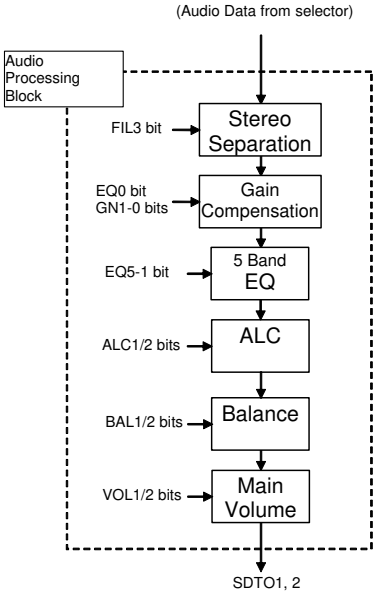


Figure 14. TDM IIS Timing

■ Digital Block

The digital block consists of block diagram as shown in Figure 15.



(1) Stereo Separation: Digital Separation Emphasis Filter (See “Digital Programmable Filter Circuit”)
(2) Gain Compensation: Composed of the Equalizer (EQ0) and the Gain (0bB/+12dB/+24dB). Compensate the frequency response and the gain after the Stereo Separation Emphasis Filter.
(3) 5-Band Notch: Applicable to use as Equalizer or Notch Filter. (See “Digital Programmable Filter”)
(4) ALC: Input Digital Volume with ALC function. (See “ALC Operation”)
(5) Balance: Stereo Balance Control.
(6) Main Volume: Stereo Main Volume Control.

Figure 15 Audio Processing Block

■ Digital Programmable Filter Circuit

(1) Stereo Separation Emphasis Filter (FIL3)

FIL3 is used to emphasize the stereo separation of stereo data. F3A1[13:0], F3A2[13:0] and F3B1[13:0], F3B1[13:0] bits set the filter coefficient of FIL3 for SDTO1/2 respectively. FIL3 becomes High Pass Filter (HPF) at F3AS1/2 bit = "1", and Low Pass Filter (LPF) at F3AS1/2 bit = "0". F3BP1/2 bit controls ON/OFF of FIL3. When Stereo Separation Emphasis Filter is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when F3BP1/2 bit = "0".

1) When FIL3 is set to "HPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ −10dB)

Register setting (Figure 15)
FIL3: F3AS1/2 bit = "1", F3A1[13:0], F3A1[13:0] bits =A, F3B1[13:0], F3B2[13:0] bits =B
(MSB=F3A113(F3A213), F3B13(F3B213); LSB=F3A10(F3A20), F3B10(F3B20))

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

2) When FIL3 is set to "LPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ −10dB)

Register setting (Figure 15)
FIL3: F3AS1/2 bit = "0", F3A1[13:0], F3A1[13:0] bits =A, F3B1[13:0], F3B2[13:0] bits =B
(MSB= F3A113(F3A213), F3B13(F3B213); LSB= F3A10(F3A20), F3B10(F3B20))

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

(2) Gain Compensation (EQ0)

Gain Compensation is used to compensate the frequency response and the gain that is changed by Stereo Separation Emphasis Filter. Gain Compensation is composed of the Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). E0A1[15:0], E0A215:0], E0B1[15:0] and E0B2[15:0] bits set the coefficient of EQ0. GN1[1:0], GN2[1:0] bits set the gain (Table 9).

fs: Sampling frequency
fc_1: Pole frequency
fc_2: Zero-point frequency
K: Filter gain [dB] (Maximum +12dB)

Register setting (Figure 15)
E0A1[15:0], E0A2[15:0] bits =A, E0B1[13:0], E0B2[13:0] bits =B, E0C1[15:0], E0C2[15:0] bits =C
(MSB=E0A115(E0A215),E0B113(E0B213), E0C115(E0C215); LSB=E0A10(E0A20), E0B10(E0B20), E0C10(E0C20))

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

Transfer function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

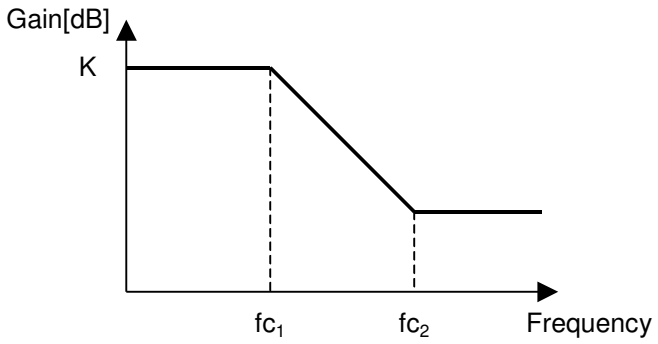


Figure 16. EQ0 Frequency Response

GN1	GN0	Gain	
0	0	0dB	(default)
0	1	+12dB	
1	x	+24dB	

Table 9. Gain select of gain block (x: Don't care)

(3) 5 Band Equalizer

The center frequencies and cut/boost amount are the followings.

- Center frequency: 100Hz, 250Hz, 1kHz, 3.5kHz, 10kHz (Note 16, Note 17)
- Cut/Boost amount: Minimum –10.5dB, Maximum +12dB, Step 1.5dB

Note 16: These are the frequencies when the sampling frequency is 44.1kHz. These frequencies are proportional to the sampling frequency.
Note 17: 100Hz is not center frequency but the frequency component lower than 100Hz is controlled.
Note 18: 10kHz is not center frequency but the frequency component higher than 10kHz is controlled.

EQ1/2 bits control ON/OFF of this Equalizer and these Boost amount are set by EQx3-0 bit as shown in Table 23.

EQA3-0: Select the boost level of 100Hz
EQB3-0: Select the boost level of 250Hz
EQC3-0: Select the boost level of 1kHz
EQD3-0: Select the boost level of 3.5kHz
EQE3-0: Select the boost level of 10kHz

EQx3-0	Boost amount	
0H	+12.0dB	
1H	+10.5dB	
2H	+9.0dB	
3H	+7.5dB	
:	:	
8H	0dB	(default)
:	:	
DH	–7.5dB	
EH	–9.0dB	
FH	–10.5dB	

Table 10. Boost amount of 5 Band Equalizer