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AK4331

Low-Power Advanced 32-bit DAC with HP/SRC

1. General Description

The AK4331 is an advanced 32-bit high sound quality stereo audio DAC with a built-in ground-referenced headphone amplifier. The AK4331 has four types of 32-bit digital filters for better sound quality, achieving low distortion characteristics and wide dynamic range. The AK4331 also has a jitter cleaner with a built-in SRC and a X'tal. The AK4331 is available in a 36-pin CSP package, utilizing less board space than competitive offerings.

2. Features

1. **High Sound Quality Low Power Advanced 32-bit Stereo DAC**
   - **4 types of Digital Filter for Sound Color Selection**
     - **Short Delay Sharp Roll-off, GD = 5.5 / fs**
     - **Short Delay Slow Roll-off, GD = 4.5 / fs**
     - **Sharp Roll-off**
     - **Slow Roll-off**
2. **Ground-referenced Class-G Stereo Headphone Amplifier**
   - **Output Power: 70 mW @ 8Ω**
   - **THD+N: –100 dB**
   - **S/N: 109 dB**
   - **Output Noise Level: –114 dBV (Analog Volume = –10 dB)**
   - **Analog Volume: +4 to –10 dB, 2 dB Step**
   - **Ground Loop Noise Cancellation**
3. **Low Power Consumption: 4.4 mW (Play back, fs = 48 kHz, External Slave Mode)**
   5.0 mW (Play back, fs = 48 kHz, PLL Slave Mode)
4. **Headphone Amplifier Output Pins Comply with IEC61000-4-2 ESD Protection**
   - **±8 kV Contact Discharge**
5. **Digital Audio interface**
   - **Master / Slave Mode**
   - **Sampling Frequency (Slave Mode / Master Mode):**
     8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 128 k, 176.4 k, 192 kHz
   - **Interface Format: 32/24/16-bit I^2S/MSB justified**
6. **Asynchronous Sample Rate Converter**
   - **Up sample: up to ×6.02**
7. **Stereo Digital Microphone Interface**
8. **Power Management**
9. **PLL**
10. **Jitter Cleaner with a built-in SRC and X'tal Oscillator**
11. **µP Interface: I^2C-bus (400 kHz)**
12. **Operation Temperature Range: Ta = –40 to 85 °C**
13. **Power Supply:**
    - **AVDD (DAC, PLL): 1.7 to 1.9 V**
    - **CVDD (Headphone Amplifier, Charge Pump): 1.7 to 1.9 V**
    - **LVDD (LDO2 for Digital Core): 1.7 to 1.9 V (built-in LDO)**
    - **TVDD (Digital Interface): 1.65 to 3.6 V**
14. **Pin Compatible and Register Backward Compatible with the AK4375A**
15. **Package: 36-pin CSP (2.533 × 2.371 mm, 0.4 mm pitch)**

3. Table of Contents

4. Block Diagram and Functions

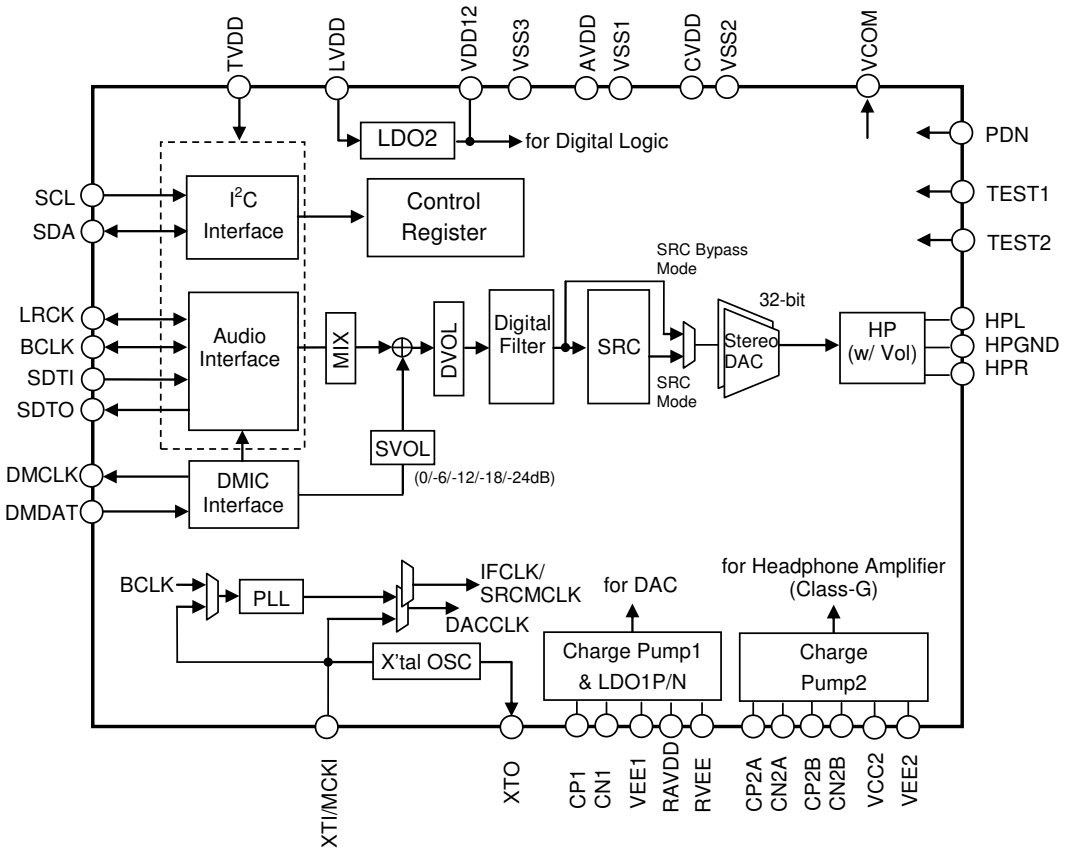
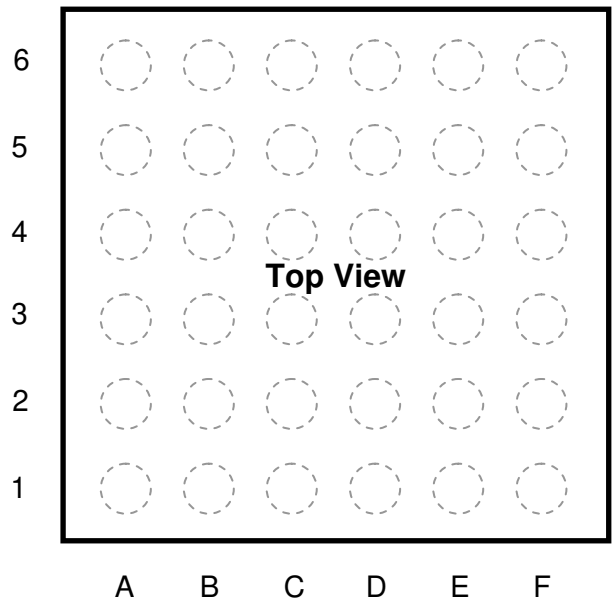


Figure 1. AK4331 Block Diagram

5. Pin Configurations and Functions

5-1. Pin Configurations

36-pin CSP



6	VDD12	LVDD	CN1	CP1	CVDD	CN2B
5	VSS3	SDTI	VEE1	VSS2	CP2B	CN2A
4	TVDD	LRCK	SDA	SCL	CP2A	VEE2
3	MCKI /XTI	BCLK	PDN	TEST1	VCC2	HPR
2	XTO	DMDAT	TEST2	VSS1	HPL	HPGND
1	SDTO	DMCLK	RVEE	RAVDD	AVDD	VCOM
	A	**B**	**C**	**D**	**E**	**F**

Top View

5-2. Pin Function Difference with AK4375A

Pin No.	AK4375A		AK4331	
	Pin Name	Function	Pin Name	Function
A1	XTI	X'tal Oscillator Input Pin Left floating when not in use.	SDTO	Audio Serial Data Output Pin Left floating when not in use.
A3	MCKI	External Master Clock Input Pin Connect to VSS3 when not in use.	MCKI/XTI	External Master Clock Input / X'tal Oscillator Input Pin Connect to VSS3 and set PMOSC bit to "0" when not in use.
B1	TESTO	Test Output Pin Left floating when not in use.	DMCLK	Digital MIC Clock Output Pin Left floating when not in use.
B2	LDO2E	LDO2 Enable pin This pin must be tied "H".	DMDAT	Digital MIC Data Input Pin Connect to VSS1 or AVDD when not in use.
C2	VSS4	Ground4 pin This pin must be tied "L".	TEST2	Test Input pin This pin must be tied "L".

5-3. Pin Functions

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Power Supply					
E1	AVDD	-	Analog Power Supply Pin	-	AVDD
D2	VSS1	-	Ground 1 Pin	-	-
E6	CVDD	-	Headphone Amplifier / Charge Pump Power Supply Pin	-	CVDD
D5	VSS2	-	Ground 2 Pin	-	-
B6	LVDD	-	Digital Core & LDO2 Power Supply Pin	-	LVDD
A5	VSS3	-	Ground 3 Pin	-	-
A4	TVDD	-	Digital Interface Power Supply Pin	-	TVDD
F1	VCOM	O	Common Voltage Output Pin Connect a 2.2 µF ±50% capacitor between this pin and the VSS1 pin. (Note 2)	AVDD / VSS1	-
A6	VDD12	-	LDO2 (1.2 V) Output Power Supply Pin (Note 1) Connect a capacitor between this pin to the VSS3 pin. (Note 2)	LVDD / VSS3	LVDD

Note 1. Capacitor value connected to the VDD12 pin should be selected from 2.2 µF ±50% to 4.7µF ±50%.

Note 2. Do not connect a load to the VCOM pin and the VDD12 pin.

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Charge Pump & LDO					
D6	CP1	O	Positive Charge Pump Capacitor Terminal 1 Pin Connect a 2.2 µF ±50% capacitor between this pin and the CN1 pin.	CVDD / VSS2	CVDD
C6	CN1	I	Negative Charge Pump Capacitor Terminal 1 Pin Connect a 2.2 µF ±50% capacitor between this pin and the CP1 pin.	CVDD	CVDD
C5	VEE1	O	Charge Pump Circuit Negative Voltage (−CVDD) Output 1 Pin Connect a 2.2 µF ±50% capacitor between this pin and the VSS2 pin. (Note 3)	CVDD / VSS2	-
D1	RAVDD	O	LDO1P (1.5 V) Output Pin (Note 4) Connect a capacitor between this pin and the VSS1 pin. (Note 3)	AVDD / VSS1	-
C1	RVEE	O	LDO1N (−1.5 V) Output Pin (Note 4) Connect a capacitor between this pin and the VSS1 pin. (Note 3)	AVDD / VSS1	-
E3	VCC2	O	Charge Pump Circuit Positive Voltage (CVDD or 1/2 × CVDD) Output Pin Connect a 2.2 µF ±50% capacitor between this pin and the VSS2 pin. (Note 3)	CVDD / VSS2	CVDD
E4	CP2A	O	Positive Charge Pump Capacitor Terminal 2A Pin Connect a 2.2 µF ±50% capacitor between this pin and the CN2A pin.	CVDD / VSS2	CVDD
F5	CN2A	I	Negative Charge Pump Capacitor Terminal 2A Pin Connect a 2.2 µF ±50% capacitor between this pin and the CP2A pin.	CVDD	CVDD
E5	CP2B	O	Positive Charge Pump Capacitor Terminal 2B Pin Connect a 2.2 µF ±50% capacitor between this pin and the CN2B pin.	CVDD / VSS2	CVDD
F6	CN2B	I	Negative Charge Pump Capacitor Terminal 2B Pin Connect a 2.2 µF ±50% capacitor between this pin and the CP2B pin.	CVDD	CVDD
F4	VEE2	O	Charge Pump Circuit Negative Voltage (−CVDD or −1/2 × CVDD) Output 2 Pin Connect a 2.2 µF ±50% capacitor between this pin and the VSS2 pin. (Note 3)	CVDD / VSS2	-

Note 3. Do not connect a load to the VEE1 pin, VCC2 pin, VEE2 pin, RAVDD pin and the RVEE pin.
Note 4. Capacitor value connected to the RAVDD pin and the RVEE pin should be selected from 1.0 µF ±50% to 4.7 µF ±50%.

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Control Interface					
D4	SCL	I	I^2C Serial Data Clock Pin	TVDD / VSS3	TVDD
C4	SDA	I/O	I^2C Serial Data Input/Output Pin	TVDD / VSS3	TVDD
Audio Interface					
A3	MCKI	I	External Master Clock Input Pin (PMOSC bit = "0")	TVDD / VSS3	TVDD
	XTI	I	X'tal Oscillator Input Pin (PMOSC bit = "1")		
A1	SDTO	O	Audio Serial Data Output Pin	TVDD / VSS3	TVDD
A2	XTO	O	X'tal Oscillator Output Pin	TVDD / VSS3	TVDD
B3	BCLK	I/O	Audio Serial Data Clock Pin	TVDD / VSS3	TVDD
B4	LRCK	I/O	Frame Sync Clock Pin	TVDD / VSS3	TVDD
B5	SDTI	I	Audio Serial Data Input Pin	TVDD / VSS3	TVDD
Analog Output					
E2	HPL	O	Lch Headphone Amplifier Output Pin	CVDD / VEE2	CVDD / VEE2
F3	HPR	O	Rch Headphone Amplifier Output Pin	CVDD / VEE2	CVDD / VEE2
F2	HPGND	I	Headphone Amplifier Ground Loop Noise Cancellation Pin	-	-
Digital MIC Interface					
B1	DMCLK	O	Digital MIC Clock Output Pin	AVDD / VSS1	AVDD
B2	DMDAT	I	Digital MIC Data Input Pin	AVDD / VSS1	AVDD
Others					
C3	PDN	I	Power down Pin "L": Power-Down, "H": Power-Up	TVDD / VSS3	TVDD
D3	TEST1	I	Test Input 1 Pin It must be tied "L".	TVDD VSS3	TVDD
C2	TEST2	I	Test Input 2 Pin It must be tied "L".	TVDD / VSS3	TVDD

Note 5. The SCL pin, SDA pin, MCKI/XTI pin, BCLK pin, LRCK pin, SDTI pin, HPGND pin, DMDAT pin, PDN pin, TEST1 pin and the TEST2 pin must not be allowed to float.

5-4. Handing of Unused Pins

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	HPL, HPR	Open
Digital	MCKI/XTI, TEST1, TEST2	Connect to VSS3
	DMCLK, SDTO, XTO	Open
	DMDAT	Connect to VSS1 or AVDD

6. Absolute Maximum Ratings

(VSS1 = VSS2 = VSS3 = 0 V; Note 7, Note 8)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies: (Note 6)	Analog	AVDD	−0.3	4.3	V
	Headphone Amplifier / Charge Pump	CVDD	−0.3	4.3	V
	LDO2 for Digital Core	LVDD	−0.3	4.3	V
	Digital Interface	TVDD	−0.3	4.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage 1 (Note 9)		VIND1	−0.3	AVDD+0.3 or 4.3	V
Digital Input Voltage 2 (Note 10)		VIND2	−0.3	TVDD+0.3 or 4.3	V
Ambient Temperature (powered applied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 6. Charge pump 1 & 2 are not in operation. In the case that charge pump 1 & 2 are in operation, the maximum values of AVDD and CVDD become 2.15 V.

Note 7. All voltages with respect to ground.

Note 8. VSS1, VSS2 and VSS3 must be connected to the same analog plane.

Note 9. DMDAT pin
The maximum value of input voltage is lower value between (AVDD+0.3) V and 4.3 V.

Note 10. MCKI/XTI, BCLK, LRCK, SDTI, SCL, SDA, PDN, TEST1, TEST2 pins
The maximum value of input voltage is lower value between (TVDD+0.3) V and 4.3 V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal Operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1 = VSS2 = VSS3 = 0 V; Note 11)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies: (Note 12)	Analog	AVDD	1.7	1.8	1.9	V
	Headphone Amplifier / Charge Pump	CVDD	1.7	1.8	1.9	V
	LDO2 for Digital Core	LVDD	1.7	1.8	1.9	V
	Digital Interface	TVDD	1.65	1.8	3.6	V

Note 11. All voltages with respect to ground.

Note 12. Each power up/down sequence is shown below.

<Power-Up>

1. PDN pin = “L”
2. TVDD, AVDD, LVDD and CVDD are powered up.
   (AVDD must be powered up before or at the same time of CVDD. The power-up sequence of TVDD and LVDD is not critical.)
3. The PDN pin is allowed to be “H” after all power supplies are applied and settled.

<Power-down>

1. PDN pin = “L”
2. TVDD, AVDD, LVDD and CVDD are powered down.
   (CVDD must be powered down before or at the same time of AVDD. The power-down sequence of TVDD and LVDD is not critical.)

8. Electrical Characteristics

8-1. DAC Analog Characteristics

(Ta = 25°C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; Signal Frequency = 1 kHz; 24-bit Data; fs = 48 kHz, BCLK = 64fs; Measurement Bandwidth = 20 Hz to 20 kHz, OVL/R = 0 dB, R_L = 32Ω, SELDAIN bit = "0"; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
Stereo DAC Characteristics:					
Resolution		-	-	32	Bits
Headphone Amplifier Characteristics: DAC (Stereo) → HPL/HPR pins					
Output Power					
0 dBFS, R_L = 32Ω, HPG = 0 dB		-	25	-	mW
0 dBFS, R_L = 32Ω, HPG = −4 dB		-	10	-	mW
R_L = 16Ω, HPG = 0 dB, THD+N < −60 dB		-	45	-	mW
R_L = 8Ω, HPG = +2 dB, THD+N < −20 dB		-	70	-	mW
Output Level (0 dBFS, R_L = 32Ω, HPG = −4 dB) (Note 13)		0.52	0.57	0.61	Vrms
THD+N					
0 dBFS, R_L = 32Ω, HPG = −4 dB (Po = 10 mW)	fs = 48 kHz BW = 20 kHz	-	−100	−90	dB
	fs = 96 kHz BW = 40 kHz	-	−97	-	dB
	fs = 192 kHz BW = 40 kHz	-	−97	-	dB
−60 dBFS, R_L = 32Ω, HPG = −4 dB	fs = 48 kHz BW = 20 kHz	-	−44	-	dB
	fs = 96 kHz BW = 40 kHz	-	−40	-	dB
	fs = 192 kHz BW = 40 kHz	-	−40	-	dB
Dynamic Range −60 dBFS, A-weighted, HPG = −4 dB		-	107	-	dB
S/N (A-weighted)					
Po = 25 mW, HPG = 0 dB (Data = 0 dBFS / "0" Data)		-	109	-	dB
Po = 10 mW, HPG = −4 dB (Data = 0 dBFS / "0" Data)		99	107	-	dB
Output Noise Level (A-weighted, HPG = −10 dB)		-	−114	−106	dBV

Note 13. Output level is proportional to AVDD. Typ. 0.57 Vrms × AVDD / 1.8 V @headphone amplifier gain = −4 dB.

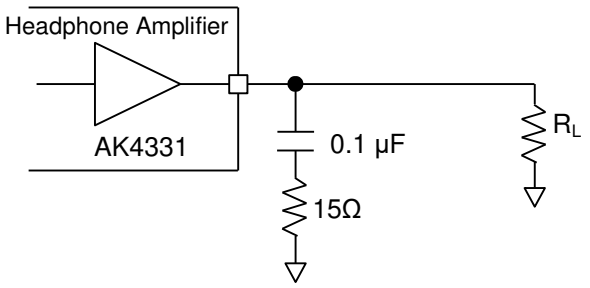


Figure 2. External Circuit for Headphone Amplifier

Parameter		Min.	Typ.	Max.	Unit
Interchannel Isolation 0 dBFS, HPG = −4 dB (Po = 10 mW) External Impedance = 0.09Ω (Note 14)		80	100	-	dB
Interchannel Gain Mismatch		-	0	0.8	dB
Load Resistance		7.2	32	-	Ω
Load Capacitance		-	-	500	pF
Load Inductance		-	-	0.375	µH
PSRR (HPG = −4 dB) (Note 15) 217 Hz 1 kHz		- -	85 85	- -	dB dB
DC-offset (Note 16) HPG = 0 dB HPG = All gain		−0.15 −0.2	0 0	+0.15 +0.2	mV mV
Headphone Output Volume Characteristics:					
Gain Setting		−10	-	+4	dB
Step Width	Gain: +4 to −10 dB	1	2	3	dB

Note 14. Impedance between the HPGND pin and the system ground.
Note 15. PSRR is referred to all power supplies with 100 mVpp sine wave.
Note 16. When there is no gain change and temperature drift after headphone amplifier is powered up.

Parameter	Value	Unit
ESD Immunity IEC61000-4-2 Level4, Contact (Note 17)	±8	kV

Note 17. It is measured at the HPL and HPR pins on an evaluation board (AKD4331-SA Rev.1).

8-2. PLL Characteristics

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; unless otherwise specified)

Parameter	Min.	Typ.	Max.	Unit
PLL Characteristics				
Reference Clock (Note 15)	76.8	-	768	kHz
PLLCLK Frequency (Note 15)				
44.1 kHz × 256fs × 2	-	22.5792	-	MHz
48.0 kHz × 256fs × 2	-	24.576	-	MHz
Lock Time	-	-	2	msec

8-3. Charge Pump & LDO Circuit Power-Up Time

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; unless otherwise specified)

Parameter	Capacitor	Min.	Typ.	Max.	Unit
Block Power-Up Time					
CP1 (Note 18)	-	-	-	6.5	msec
CP2 (Class-G) (Note 18, Note 19)	-	-	-	4.5	msec
LDO1P (Note 20)	1 µF @RAVDD	-	-	0.5	msec
LDO1N (Note 20)	1 µF @RVEE	-	-	0.5	msec
LDO2 (Note 18)	-	-	-	1	msec

Note 18. Power-up time is a fixed value that is not affected by a capacitor.

Note 19. Power-up time is a value to −1/2 × CVDD, since CP2 starts with 1/2VDD Mode as part of Class-G operation.

Note 20. Power-up time is proportional to a capacitor value. For instance, if a 2.2 µF capacitor is connected to the RAVDD pin, LDO1P power-up time is 1.1 msec at maximum.

8-4. Power Supply Current

(Ta = 25°C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; unless otherwise specified)

Parameter	Min.	Typ.	Max.	Unit
Power Supply Current:				
Power Up (PDN pin = "H", All Circuits Power-Up) (Note 21)				
AVDD + CVDD + LVDD + TVDD	-	4.1	6.1	mA
Power Down (PDN pin = "L") (Note 22)				
AVDD + CVDD + LVDD + TVDD	-	0	10	μA

Note 21. fso/fsi = 48 kHz/48 kHz, MCKI = 256fs, BCLK = 64fs; No data input, R_L = 32Ω, DAC, Headphone Amplifier, PLL & X'tal & SRC & DMIC Power-Up

Note 22. The DMDAT pin is fixed to AVDD or VSS1 and other digital input pins are fixed to TVDD or VSS3.

8-5. Power Consumptions for Each Operation Mode

(Ta = 25°C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; SRC Bypass Mode, MCKI = 256fs, BCLK = 64fs; No data input, R_L = 32Ω, X'tal & DMIC OFF)

Table 1. Power Consumption (Typ.) for Each Operation Mode

Mode	Typical Current [mA]				Total Power [mW]
	AVDD	CVDD	LVDD	TVDD	
DAC → Headphone (fs = 48 kHz), External Slave Mode	0.79	1.37	0.27	0.01	4.4
DAC → Headphone (fs = 96 kHz), External Slave Mode	0.87	1.69	0.36	0.01	5.3
DAC → Headphone (fs = 192 kHz), External Slave Mode, MCKI = 128fs	0.87	1.69	0.44	0.01	5.4
DAC → Headphone (fs = 48 kHz), External Slave Mode, DMIC enable	0.79	1.37	0.69	0.01	5.1
DAC → Headphone (fs = 96 kHz), External Slave Mode, DMIC enable	0.87	1.69	1.16	0.01	6.7
DAC → Headphone (fs = 48 kHz), PLL Slave Mode	1.06	1.37	0.31	0.01	5.0
DAC → Headphone (fs = 96 kHz), PLL Slave Mode	1.14	1.69	0.41	0.01	5.9
DAC → Headphone (fs = 192 kHz), PLL Slave Mode	1.14	1.69	0.49	0.01	6.0

8-6. SRC Characteristics

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = 0 V; unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Resolution		-	-	32	Bits
Input Sample Rate	FSI	8	-	192	kHz
Output Sample Rate	FSO	8	-	192	kHz
Ratio between Input and Output Sample Rate	FSO/FSI	0.98	-	6.02	-

8-7. DAC Sharp Roll-Off Filter Characteristics (SRC Bypass Mode)

8-7-1. Sharp Roll-Off Filter (SRC Bypass Mode, fs = 48 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 48 kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 23)	–0.006 to +0.23 dB	PB	0	-	22.42	kHz
	–6.0 dB		-	24.02	-	kHz
Stopband (Note 23)		SB	26.2	-	-	kHz
Passband Ripple		PR	–0.006	-	+0.23	dB
Stopband Attenuation (Note 24)		SA	69.8	-	-	dB
Group Delay (Note 25)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 20.0 kHz		FR	–0.12	-	+0.10	dB

Note 23. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.467 × fs (@–0.006/+0.23 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 24. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 25. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-7-2. Sharp Roll-Off Filter (SRC Bypass Mode, fs = 96 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 96 kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 26)	–0.003 to +0.24 dB	PB	0	-	44.85	kHz
	–6.0 dB		-	48.04	-	kHz
Stopband (Note 26)		SB	52.5	-	-	kHz
Passband Ripple		PR	–0.003	-	+0.24	dB
Stopband Attenuation (Note 27)		SA	69.8	-	-	dB
Group Delay (Note 28)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 40.0 kHz		FR	–1.69	-	+0.11	dB

Note 26. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4672 × fs (@–0.003/+0.24 dB), SB = 0.547 × fs. Each frequency response refers to that of 1 kHz.

Note 27. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 28. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-7-3. Sharp Roll-Off Filter (SRC Bypass Mode, fs = 192 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 192 kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 29)	−0.002 to +0.24 dB	PB	0	-	89.74	kHz
	−6.0 dB		-	96.08	-	kHz
Stopband (Note 29)		SB	104.9	-	-	kHz
Passband Ripple		PR	−0.002	-	+0.24	dB
Stopband Attenuation (Note 30)		SA	69.8	-	-	dB
Group Delay (Note 31)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 80.0 kHz		FR	−8.23	-	+0.35	dB

Note 29. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4674 × fs (@−0.002/+0.24 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 30. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 31. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-8. DAC Slow Roll-Off Filter Characteristics (SRC Bypass Mode)

8-8-1. Slow Roll-Off Filter (SRC Bypass Mode, fs = 48 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 48 kHz; DASD bit = "0", DASL bit = "1", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 32)	–0.07 to +0.005 dB	PB	0	-	8.49	kHz
	–3.0 dB		-	20.15	-	kHz
Stopband (Note 32)		SB	42.59	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.005	dB
Stopband Attenuation (Note 33)		SA	72.8	-	-	dB
Group Delay (Note 34)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 20.0 kHz		FR	–3.21	-	+0.03	dB

Note 32. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.1769 × fs (@–0.07/+0.005 dB), SB = 0.887 × fs. Each frequency response refers to that of 1 kHz.

Note 33. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 34. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-8-2. Slow Roll-Off Filter (SRC Bypass Mode, fs = 96 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 96 kHz; DASD bit = "0", DASL bit = "1", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 35)	–0.07 to +0.006 dB	PB	0	-	17.02	kHz
	–3.0 dB		-	40.3	-	kHz
Stopband (Note 35)		SB	85.15	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.006	dB
Stopband Attenuation (Note 36)		SA	72.8	-	-	dB
Group Delay (Note 37)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 40.0 kHz		FR	–4.84	-	+0.10	dB

Note 35. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.1773 × fs (@–0.07/+0.006 dB), SB = 0.887 × fs. Each frequency response refers to that of 1 kHz.

Note 36. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 37. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-8-3. Slow Roll-Off Filter (SRC Bypass Mode, fs = 192 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 192 kHz; DASD bit = "0", DASL bit = "1", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 38)	−0.07 to +0.006 dB	PB	0	-	34.17	kHz
	−3.0 dB		-	80.65	-	kHz
Stopband (Note 38)		SB	170.3	-	-	kHz
Passband Ripple		PR	−0.07	-	+0.006	dB
Stopband Attenuation (Note 39)		SA	72.8	-	-	dB
Group Delay (Note 40)		GD	-	25.8	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 80.0 kHz		FR	−11.38	-	+0.35	dB

Note 38. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.178 × fs (@−0.07/+0.006 dB), SB = 0.887 × fs. Each frequency response refers to that of 1 kHz.

Note 39. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 40. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-9. DAC Short Delay Sharp Roll-Off Filter Characteristics (SRC Bypass Mode)

8-9-1. Short Delay Sharp Roll-Off Filter (SRC Bypass Mode, fs = 48 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 48 kHz; DASD bit = "1", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 41)	–0.009 to +0.232 dB	PB	0	-	22.41	kHz
	–6.0 dB		-	24.15	-	kHz
Stopband (Note 41)		SB	26.23	-	-	kHz
Passband Ripple		PR	–0.009	-	+0.232	dB
Stopband Attenuation (Note 42)		SA	69.8	-	-	dB
Group Delay (Note 43)		GD	-	5.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 20.0 kHz		FR	–0.12	-	+0.10	dB

Note 41. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4669 × fs (@–0.009/+0.232 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 42. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 43. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-9-2. Short Delay Sharp Roll-Off Filter (SRC Bypass Mode, fs = 96 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 96 kHz; DASD bit = "1", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 44)	–0.004 to +0.238 dB	PB	0	-	44.82	kHz
	–6.0 dB		-	48.32	-	kHz
Stopband (Note 44)		SB	52.5	-	-	kHz
Passband Ripple		PR	–0.004	-	+0.238	dB
Stopband Attenuation (Note 45)		SA	69.8	-	-	dB
Group Delay (Note 46)		GD	-	5.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 40.0 kHz		FR	–1.69	-	+0.11	dB

Note 44. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4669 × fs (@–0.004/+0.238 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 45. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 46. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-9-3. Short Delay Sharp Roll-Off Filter (SRC Bypass Mode, fs = 192 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 192 kHz; DASD bit = "1", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 47)	−0.002 to +0.247 dB	PB	0	-	89.68	kHz
	−6.0 dB		-	96.64	-	kHz
Stopband (Note 47)		SB	104.9	-	-	kHz
Passband Ripple		PR	−0.002	-	+0.247	dB
Stopband Attenuation (Note 48)		SA	69.8	-	-	dB
Group Delay (Note 49)		GD	-	5.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 80.0 kHz		FR	−8.23	-	+0.36	dB

Note 47. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4671 × fs (@−0.002/+0.247 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 48. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 49. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-10. DAC Short Delay Slow Roll-Off Filter Characteristics (SRC Bypass Mode)

8-10-1. Short Delay Slow Roll-Off Filter (SRC Bypass Mode, fs = 48 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 48 kHz; DASD bit = "1", DASL bit = "1", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 50)	–0.07 to +0.025 dB	PB	0	-	9.82	kHz
	–3.0 dB		-	20.57	-	kHz
Stopband (Note 50)		SB	42.98	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.025	dB
Stopband Attenuation (Note 51)		SA	75.1	-	-	dB
Group Delay (Note 52)		GD	-	4.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 20.0 kHz		FR	–2.96	-	+0.04	dB

Note 50. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.2045 × fs (@–0.07/+0.025 dB), SB = 0.8955 × fs. Each frequency response refers to that of 1 kHz.

Note 51. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 52. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-10-2. Short Delay Slow Roll-Off Filter (SRC Bypass Mode, fs = 96 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 96 kHz; DASD bit = "1", DASL bit = "1", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 53)	–0.07 to +0.027 dB	PB	0	-	19.7	kHz
	–3.0 dB		-	41.16	-	kHz
Stopband (Note 53)		SB	85.97	-	-	kHz
Passband Ripple		PR	–0.07	-	+0.027	dB
Stopband Attenuation (Note 54)		SA	75.1	-	-	dB
Group Delay (Note 55)		GD	-	4.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 40.0 kHz		FR	–4.59	-	+0.10	dB

Note 53. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.2052 × fs (@–0.07/+0.027 dB), SB = 0.8955 × fs. Each frequency response refers to that of 1 kHz.

Note 54. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 55. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-10-3. Short Delay Slow Roll-Off Filter (SRC Bypass Mode, fs = 192 kHz)

(Ta = -40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 192 kHz; DASD bit = "1", DASL bit = "1", SELDAIN bit = "0", DADFSEL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 56)	−0.07 to +0.028 dB	PB	0	-	39.54	kHz
	−3.0 dB		-	82.37	-	kHz
Stopband (Note 56)		SB	172	-	-	kHz
Passband Ripple		PR	−0.07	-	+0.028	dB
Stopband Attenuation (Note 57)		SA	75.1	-	-	dB
Group Delay (Note 58)		GD	-	4.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 80.0 kHz		FR	−11.13	-	+0.35	dB

Note 56. The passband and stopband frequencies scale with fs (system sampling rate)
PB = 0.2059 × fs (@−0.07/+0.028 dB), SB = 0.8958 × fs. Each frequency response refers to that of 1 kHz.

Note 57. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 58. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-11. DAC Sharp Roll-Off Filter Characteristics (SRC Mode)

8-11-1. Sharp Roll-Off Filter (SRC Mode, fs = 48 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 48 kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "1", DADFSEL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 59)	−0.004 to +0.199 dB	PB	0	-	22.28	kHz
	−6.0 dB		-	24.00	-	kHz
Stopband (Note 59)		SB	26.21	-	-	kHz
Passband Ripple		PR	−0.004	-	+0.199	dB
Stopband Attenuation (Note 60)		SA	70.4	-	-	dB
Group Delay (Note 61)		GD	-	27.6	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 20.0 kHz		FR	−0.12	-	+0.10	dB

Note 59. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4642 × fs (@−0.004/+0.199 dB), SB = 0.546 × fs. Each frequency response refers to that of 1 kHz.

Note 60. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 61. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-11-2. Sharp Roll-Off Filter (SRC Mode, fs = 96 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 96 kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "1", DADFSEL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 62)	−0.001 to +0.202 dB	PB	0	-	44.58	kHz
	−6.0 dB		-	48.01	-	kHz
Stopband (Note 62)		SB	52.45	-	-	kHz
Passband Ripple		PR	−0.001	-	+0.202	dB
Stopband Attenuation (Note 63)		SA	70.2	-	-	dB
Group Delay (Note 64)		GD	-	27.6	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 40.0 kHz		FR	−1.72	-	+0.11	dB

Note 62. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4644 × fs (@−0.001/+0.202 dB), SB = 0.5464 × fs. Each frequency response refers to that of 1 kHz.

Note 63. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 64. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

8-11-3. Sharp Roll-Off Filter (SRC Mode, fs = 192 kHz)

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 192 kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "1", DADFSEL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 65)	0.000 to +0.210 dB	PB	0	-	89.22	kHz
	–6.0 dB		-	96.02	-	kHz
Stopband (Note 65)		SB	104.92	-	-	kHz
Passband Ripple		PR	0.000	-	+0.210	dB
Stopband Attenuation (Note 66)		SA	70.1	-	-	dB
Group Delay (Note 67)		GD	-	27.6	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):						
Frequency Response: 0 to 80.0 kHz		FR	–8.27	-	+0.35	dB

Note 65. The passband and stopband frequencies scale with fs (system sampling rate). PB = 0.4647 × fs (@0.000/+0.210 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 66. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 67. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].