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AsahiKASEI
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AK4359A

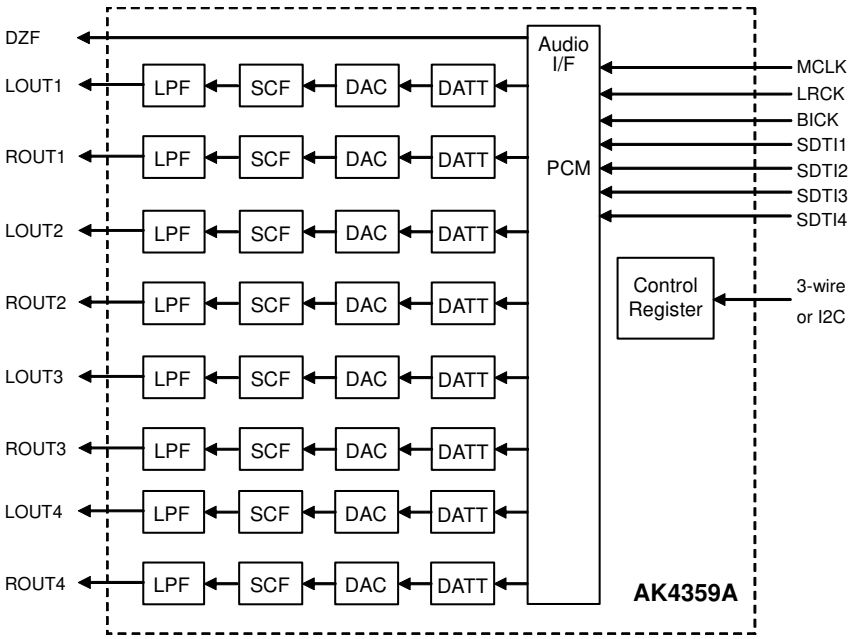
106dB 192kHz 24-Bit 8ch DAC

GENERAL DESCRIPTION

The AK4359A is an eight channels 24bit DAC corresponding to digital audio system. Using AKM's advanced multi bit architecture for its modulator the AK4359A delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4359A has single end SCF outputs, increasing performance for systems with excessive clock jitter. The AK4359A accepts 192kHz PCM data, ideal for a wide range of applications including DVD-Audio.

FEATURES

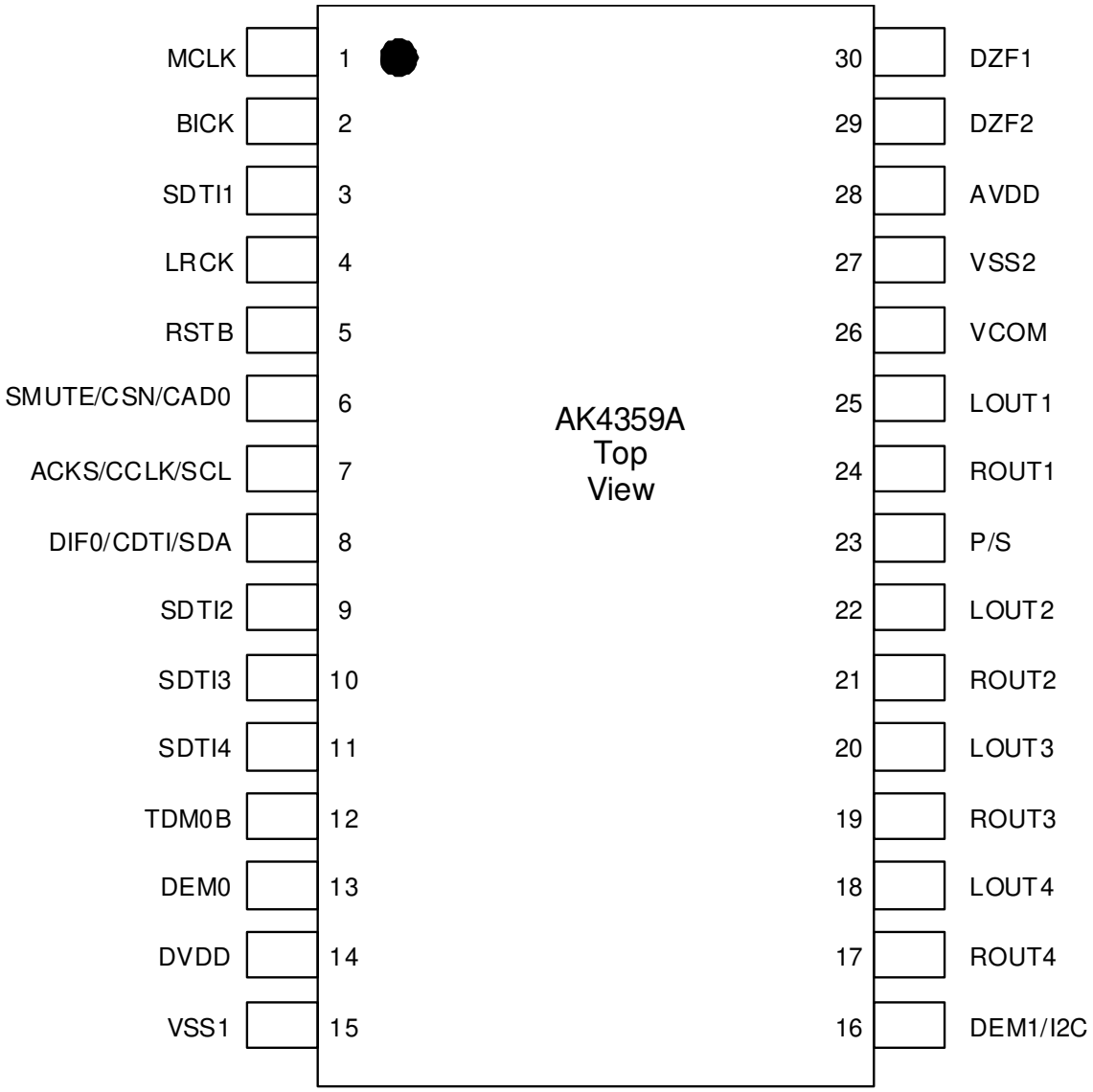
- ☐ **Sampling Rate Ranging from 8kHz to 192kHz**
- ☐ **24Bit 8 times Digital Filter with Slow roll-off option**
- ☐ **THD+N: -94dB**
- ☐ **DR, S/N: 106dB**
- ☐ **High Tolerance to Clock Jitter**
- ☐ **Single Ended Output Buffer with 2nd order Analog LPF**
- ☐ **Digital De-emphasis for 32, 44.1 & 48kHz sampling**
- ☐ **Zero Detect function**
- ☐ **Channel Independent Digital Attenuator (Linear 256 steps)**
- ☐ **3-wire Serial and I^2C Bus μP I/F for mode setting**
- ☐ **I/F format: MSB justified, LSB justified (16bit, 20bit, 24bit), I^2S, TDM**
- ☐ **Master clock: 256fs, 384fs, 512fs or 768fs or 1152fs (Normal Speed Mode)**
  128fs, 192fs, 256fs or 384fs (Double Speed Mode)
  128fs or 192fs (Quad Speed Mode)
- ☐ **Power Supply: 4.5 to 5.5V**
- ☐ **30pin VSOP Package**
- ☐ **AK4384 Semi-compatible**
- ☐ **AK4359 Compatible**



■ Ordering Guide

AK4359AEF	-20 ~ +85°C	30pin VSOP
AK4359AVF	-40 ~ +105°C	30pin VSOP
AKD4359A	Evaluation Board for AK4359A	

■ Pin Layout



■ Compatibility with AK4384/AK4359

1. Function

Functions	AK4384	AK4359	AK4359A
# of channels	2	8	8
I2C	Not available	Available	Available
DEM control	Register	Pin/Register	Pin/Register
16/20bit LSB justified format control	Register	Pin/Register	Register
TDM256 mode	Not available	Register	Pin/Register

2. Pin Configuration

AK4359/A	AK4384	Pin#	Pin#	AK4384	AK4359/A
MCLK	MCLK	1	30	DZFL	DZF1
BICK	BICK	2	29	DZFR	DZF2
SDTI1	SDTI	3	28	VDD	AVDD
LRCK	LRCK	4	27	VSS	VSS2
RSTB	PDN	5	26	VCOM	VCOM
SMUTE/CSN/CAD0	SMUTE/CSN	6	25	AOUTL	LOUT1
ACKS/CCLK/SCL	ACKS/CCLK	7	24	AOUTR	ROUT1
DIF0/CDTI/SDA	DIF0/CDTI	8	23	P/S	P/S
SDTI2		9	22		LOUT2
SDTI3		10	21		ROUT2
SDTI4		11	20		LOUT3
DIF1(AK4359)/ TDM0B(AK4359A)		12	19		ROUT3
DEM0		13	18		LOUT4
DVDD		14	17		ROUT4
VSS1		15	16		I2C/DEM1

3. Register map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	TDM1	TDM0	DIF2	DIF1	DIF0	PW1	RSTN
01H	Control 2	0	0	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	PW4	PW3	PW2	0	0	DZFB	0	0
03H	LOUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	ROUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	LOUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
06H	ROUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	LOUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
08H	ROUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
09H	LOUT4 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0AH	ROUT4 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0BH	Invert Output Signal	INVL1	INVR1	INVL2	INVR2	INVL3	INVR3	INVL4	INVR4
0CH	DZF1 Control	L1	R1	L2	R2	L3	R3	L4	R4
0DH	DZF2 Control	L1	R1	L2	R2	L3	R3	L4	R4
0EH	DEM Control	0	0	0	0	DEMA	DEMB	DEMC	DEMD

: Compatible with AK4384's register.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock
3	SDTI1	I	DAC1 Audio Serial Data Input
4	LRCK	I	L/R Clock
5	RSTB	I	Reset Mode When at "L", the AK4359A is in the reset mode. The AK4359A must be reset once upon power-up.
6	SMUTE	I	Soft Mute in parallel control mode "H": Enable, "L": Disable
	CSN	I	Chip Select in serial 3-wire mode
	CAD0	I	Chip Address in serial I2C mode
7	ACKS	I	Auto Setting Mode in parallel control mode "L": Manual Setting Mode, "H": Auto Setting Mode
	CCLK	I	Control Data Clock in serial 3-wire mode
	SCL		Control Data Clock in serial I2C mode
8	DIF0	I	Audio Data Interface Format in parallel control mode
	CDTI	I	Control Data Input in serial 3-wire mode
	SDA	I/O	Control Data in serial I2C mode
9	SDTI2	I	DAC2 Audio Serial Data Input
10	SDTI3	I	DAC3 Audio Serial Data Input
11	SDTI4	I	DAC4 Audio Serial Data Input
12	TDM0B	I	TDM I/F Format Mode in parallel control mode "L": TDM256 mode, "H": Normal mode
13	DEM0	I	De-emphasis Filter Enable
14	DVDD		Digital Power Supply, +4.5~+5.5V
15	VSS1		Ground
16	I2C	I	Control Mode Select in serial control mode "L": 3-wire Serial, "H": I^2C Bus
	DEM1	I	De-emphasis Filter Enable in parallel control mode
17	ROUT4	O	DAC4 Rch Analog Output
18	LOUT4	O	DAC4 Rch Analog Output
19	ROUT3	O	DAC3 Rch Analog Output
20	LOUT3	O	DAC3 Rch Analog Output
21	ROUT2	O	DAC2 Rch Analog Output
22	LOUT2	O	DAC2 Rch Analog Output
23	P/S	I	Parallel/Serial Select (Internal pull-up pin) "L": Serial control mode, "H": Parallel control mode
24	ROUT1	O	DAC1 Rch Analog Output
25	LOUT1	O	DAC1 Lch Analog Output
26	VCOM	O	Common Voltage, AVDD/2 Normally connected to AVSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
27	VSS2	-	Ground
28	AVDD	-	Analog Power Supply, +4.5~+5.5V
29	DZF2	O	Data Zero Input Detect
30	DZF1	O	Data Zero Input Detect

Note: All input pins except pull-up pin should not be left floating.

■ Handling of Unused Pin

The following tables illustrate recommended states for open pins:

Classification	Pin Name	Setting
Analog	LOUT4-1, ROUT4-1	Leave open.
Digital	DZF2-1	Leave open.
	SDTI4-1 SMUTE (Parallel control mode)	Connect to VSS1.
	DEM0, TDM0B (Serial control mode)	Connect to DVDD or VSS1.

ABSOLUTE MAXIMUM RATINGS

(AVSS=DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	|AVSS-DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Operating Temperature	AK4359AEF	Ta	-20	85	°C
	AK4359AVF	Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS=DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 3)	Analog	AVDD	4.5	5.0	5.5	V
	Digital	DVDD	4.5	5.0	5.5	V

Note 3. The power up sequence between AVDD and DVDD is not critical.

*AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=5V; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Input Data; Measurement frequency=20Hz ~ 20kHz; R_L ≥5kΩ; unless otherwise specified)

Parameter			min	typ	max	Units
Resolution					24	Bits
Dynamic Characteristics (Note 4)						
THD+N	Fs=44.1kHz	0dBFS		-94	-84	dB
	BW=20kHz	-60dBFS		-42	-	dB
	fs=96kHz	0dBFS		-92	-	dB
	BW=40kHz	-60dBFS		-39	-	dB
	fs=192kHz	0dBFS		-92	-	dB
	BW=40kHz	-60dBFS		-39	-	dB
Dynamic Range (-60dBFS with A-weighted) (Note 5)			98	106		dB
S/N (A-weighted) (Note 6)			98	106		dB
Interchannel Isolation (1kHz)			90	100		dB
Interchannel Gain Mismatch				0.2	0.5	dB
DC Accuracy						
Gain Drift				100	-	ppm/°C
Output Voltage (Note 7)			3.15	3.4	3.65	Vpp
Load Resistance (Note 8)			5			kΩ
Power Supplies						
Power Supply Current (AVDD+DVDD)						
Normal Operation (RSTB pin = "H", fs≤96kHz)				55	85	mA
Normal Operation (RSTB pin = "H", fs=192kHz)				63	90	mA
Reset Mode (RSTB pin = "L") (Note 9)				60	150	μA

Note 4. Measured by Audio Precision System Two. Refer to the evaluation board manual.
Note 5. 100dB at 16bit data.
Note 6. S/N does not depend on input word length.
Note 7. Full scale voltage (0dB). Output voltage scales with the voltage of the AVDD pin. AOUT (typ. @0dB) = 3.4Vpp×AVDD/5.0
Note 8. For AC-load.
Note 9. The P/S pin is tied to DVDD and the other all digital input pins including clock pins (MCLK, BICK, LRCK) are tied to DVSS.

SHARP ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; AVDD=DVDD = 4.5 ~ 5.5V; fs = 44.1kHz; DEM = OFF; SLOW = "0")

Parameter			Symbol	min	typ	max	Units
Digital filter							
Passband	±0.05dB (Note 10)		PB	0		20.0	kHz
	-6.0dB			-	22.05	-	kHz
Stopband	(Note 10)		SB	24.1			kHz
Passband Ripple			PR			± 0.02	dB
Stopband Attenuation			SA	54			dB
Group Delay	(Note 11)		GD	-	19.3	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	Fs=44.1kHz	FR	-	+ 0.06/-0.10	-	dB
	40.0kHz	Fs=96kHz	FR	-	+ 0.06/-0.13	-	dB
	80.0kHz	Fs=192kHz	FR	-	+ 0.06/-0.51	-	dB

Note 10. The passband and stopband frequencies scale with fs(system sampling rate). For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note 11. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; AVDD=DVDD = 4.5~5.5V; fs = 44.1kHz; DEM = OFF; SLOW = "1")

Parameter			Symbol	min	typ	max	Units
Digital Filter							
Passband	±0.04dB (Note 12)		PB	0		8.1	kHz
	-3.0dB			-	18.2	-	kHz
Stopband	(Note 12)		SB	39.2			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	72			dB
Group Delay	(Note 11)		GD	-	19.3	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	fs=44.kHz	FR	-	+0.1/-4.3	-	dB
	40.0kHz	fs=96kHz	FR	-	+0.1/-3.3	-	dB
	80.0kHz	fs=192kHz	FR	-	+0.1/-3.7	-	dB

Note 12. The passband and stopband frequencies scale with fs. For example, PB = 0.185×fs (@±0.04dB), SB = 0.888×fs.

DC CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 4.5 ~ 5.5V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	2.2	-	-	V
Low-Level Input Voltage		VIL	-	-	0.8	V
High-Level Output Voltage	(Iout = -80μA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage	(Iout = 80μA)	VOL	-		0.4	V
Input Leakage Current	(Note 13)	Iin	-	-	± 10	μA

Note 13. The P/S pin has an internal pull-up resistor. (typ. 100kΩ)

SWITCHING CHARACTERISTICS

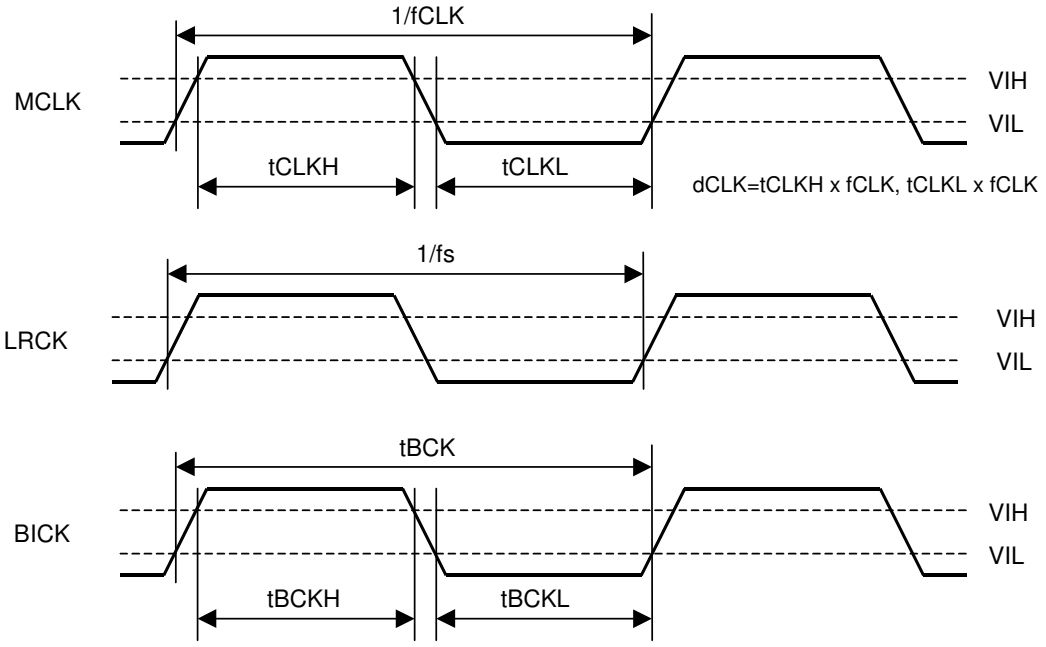
(Ta = 25°C; AVDD=DVDD = 4.5 ~ 5.5V; C_L = 20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Frequency	fCLK	2.048	11.2896	36.864	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency					
Normal Mode (TDM0= "0", TDM1= "0")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	60		96	kHz
Quad Speed Mode	fsq	120		192	kHz
Duty Cycle	Duty	45		55	%
TDM256 mode (TDM0= "1", TDM1= "0")					
Normal Speed Mode	fsn	8		48	kHz
High time	tLRH	3/256fs			ns
Low time	tLRL	3/256fs			ns
TDM128 mode (TDM0= "1", TDM1= "1")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	60		96	kHz
High time	tLRH	3/128fs			ns
Low time	tLRL	3/128fs			ns
Audio Interface Timing					
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	30			ns
Pulse Width High	tBCKH	30			ns
BICK "↑" to LRCK Edge (Note 14)	tBLR	20			ns
LRCK Edge to BICK "↑" (Note 14)	tLRB	20			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
Control Interface Timing (3-wire Serial control mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN High Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 15)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF

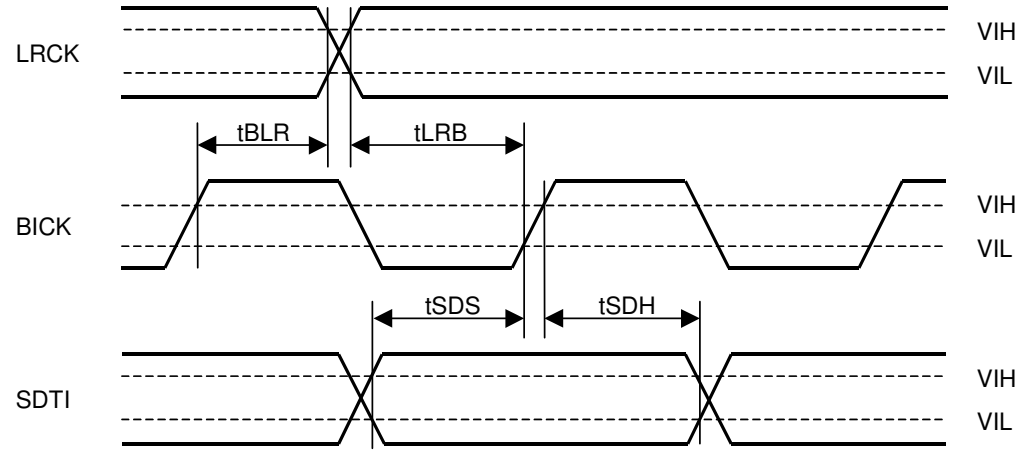
Parameter	Symbol	min	typ	max	Units
Reset Timing					
RSTB Pulse Width (Note 16)	tRST	150			ns

Note 14. BICK rising edge must not occur at the same time as LRCK edge.
Note 15. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 16. The AK4359A can be reset by bringing the RSTB pin = "L".
Note 17. I^2C is a registered trademark of Philips Semiconductors.

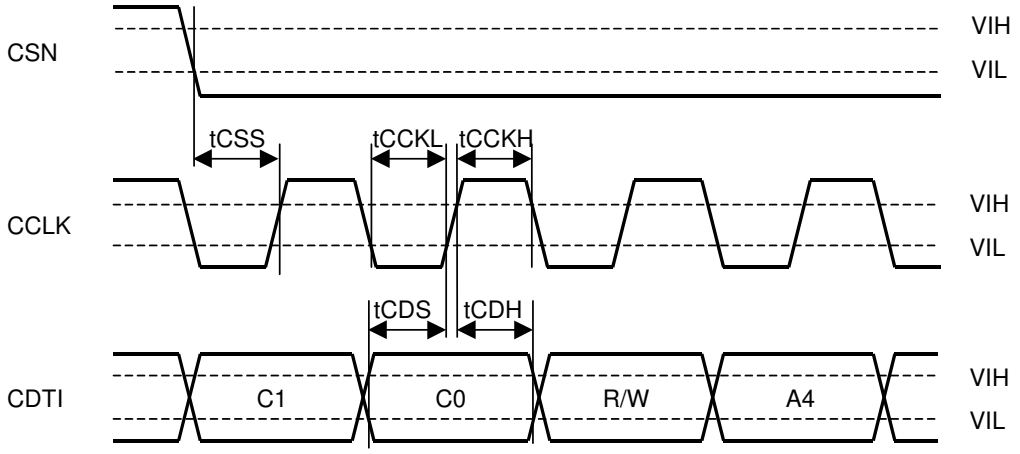
■ Timing Diagram



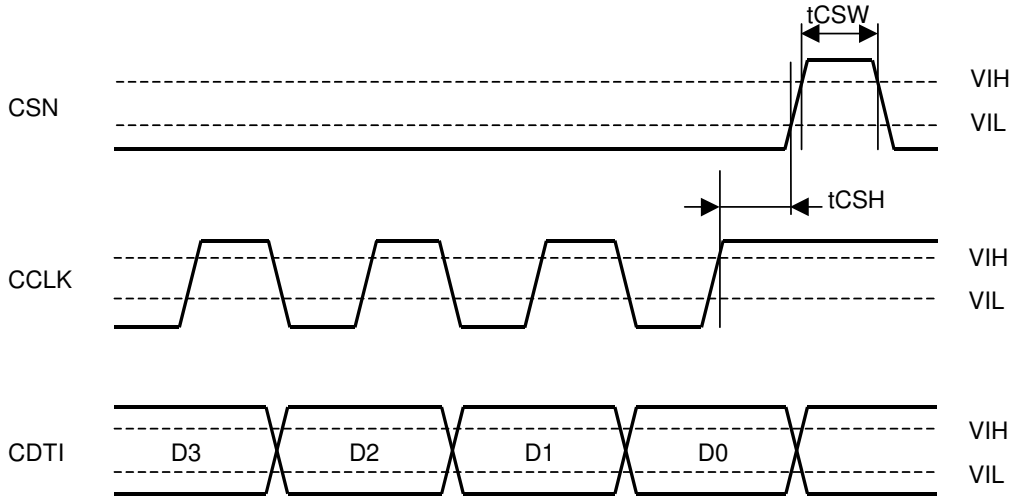
Clock Timing



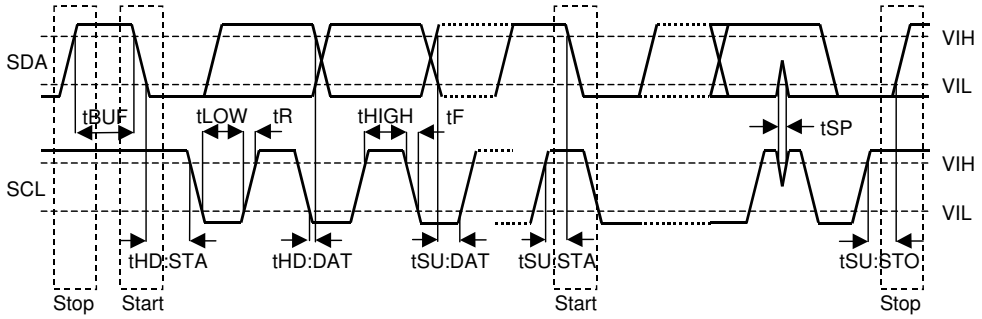
Audio Serial Interface Timing



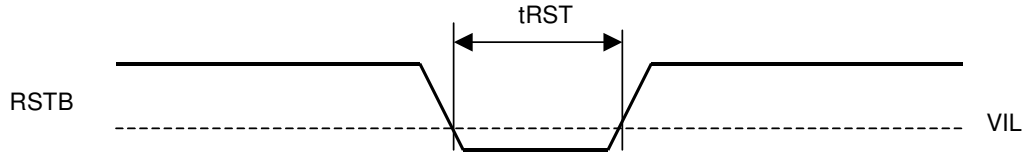
WRITE Command Input Timing



WRITE Data Input Timing



I^2C Bus mode Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4359A, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit = "0": Register 00H), the sampling speed is set by DFS1-0 bits (Table 1). The frequency of MCLK for each sampling speed is set automatically. (Table 2~Table 4) In auto setting mode (ACKS bit = "1": Default), as MCLK frequency is detected automatically (Table 5), and the internal master clock becomes the appropriate frequency (Table 6), it is not necessary to set DFS1-0 bits.

In parallel control mode, the sampling speed can be set by only the ACKS pin. When ACKS pin = "L", the AK4359A operates by Normal Speed Mode. When ACKS pin = "H", auto setting mode is enabled. The parallel control mode does not support 128fs and 192fs of double speed mode.

The AK4359A is automatically placed in reset state when the external clocks (MCLK, BICK, LRCK) are stopped during a normal operation (RSTB pin ="H"). When the external clocks are input again, the AK4359A exit reset state and starts the operation.

DFS1	DFS0	Sampling Rate (fs)		
0	0	Normal Speed Mode	8kHz~48kHz	(default)
0	1	Double Speed Mode	60kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	

Table 1. Sampling Speed (Manual Setting Mode)

LRCK	MCLK					BICK
fs	256fs	384fs	512fs	768fs	1152fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	36.8640MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	N/A	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	N/A	3.0720MHz

Table 2. System Clock Example (Normal Speed Mode @Manual Setting Mode) (N/A: Not available)

LRCK	MCLK				BICK
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	106896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 3. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK		BICK
fs	128fs	192fs	64fs
176.4kHz	22.5792MHz	33.8688MHz	106896MHz
192.0kHz	24.5760MHz	36.8640MHz	12.2880MHz

Table 4. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK		Sampling Speed
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 5. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)							Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	-	-	-	-	16.3840	24.5760	36.8640	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	-	
48.0kHz	-	-	-	-	24.5760	36.8640	-	
88.2kHz	-	-	22.5792	33.8688	-	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	-	

Table 6. System Clock Example (Auto Setting Mode)

■ Audio Serial Interface Format

In parallel control mode, the DIF0 and TDM0 pins as shown in Table 7 can select four serial data modes. The register value of DIF1-0 and TDM1-0 bits are ignored. In serial control mode, the DIF2-0 and TDM1-0 bits shown in Table 8 can select 11 serial data modes. Initial value of DIF2-0 bits is "010". The setting of the DIF1 pin is ignored. In all modes the serial data is MSB-first, 2's complement format and is latched on the rising edge of BICK. Mode 2 can be used for 16/20 MSB justified formats by zeroing the unused LSBs.

In parallel control mode, when the TDM0 pin = "L", the audio interface format is TDM256 mode (Table 7). The audio data of all DACs (eight channels) is input to the SDTI1 pin. The input data to SDTI2-4 pins is ignored. BICK should be fixed to 256fs. "H" time and "L" time of LRCK should be at least 1/256fs. The audio data is MSB-first, 2's complement format. The input data to the SDTI1 pin is latched on the rising edge of BICK.

In serial control mode, when the TDM0 bit = "1" and the TDM1 bit = "0", the audio interface format is TDM256 mode (Table 8), and the audio data of all DACs (eight channels) is input to the SDTI1 pin. The input data to the SDTI2-4 pins is ignored. BICK should be fixed to 256fs. "H" time and "L" time of LRCK should be at least 1/256fs. The audio data is MSB-first, 2's complement format. The input data to the SDTI1 pin is latched on the rising edge of BICK. In TDM128 mode (TDM0 bit = "1" and TDM1 bit = "1", Table 8), the audio data of DACs (four channels; L1, R1, L2, R2) is input to the SDTI1 pin. The other four data (L3, R3, L4, R4) are input to the SDTI2 pin. The input data to SDTI3-4 pins is ignored. BICK should be fixed to 128fs. The audio data is MSB-first, 2's complement format. The input data to SDTI1-2 pins is latched on the rising edge of BICK.

Mode		TDM0B	DIF0	SDTI Format	LRCK	BICK	Figure
Normal	2	H	L	24-bit MSB Justified	H/L	≥48fs	Figure 3
	3	H	H	24-bit I^2S Compatible	L/H	≥48fs	Figure 4
TDM256	5	L	L	24-bit MSB Justified	↑	256fs	Figure 5
	6	L	H	24-bit I^2S Compatible	↓	256fs	Figure 6

Table 7. Audio Data Formats (Parallel control mode)

Mode		TDM1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK	Figure
Normal	0	0	0	0	0	0	16-bit LSB Justified	H/L	≥32fs	Figure 1
	1	0	0	0	0	1	20-bit LSB Justified	H/L	≥40fs	Figure 2
	2	0	0	0	1	0	24-bit MSB Justified	H/L	≥48fs	Figure 3
	3	0	0	0	1	1	24-bit I^2S Compatible	L/H	≥48fs	Figure 4
	4	0	0	1	0	0	24-bit LSB Justified	H/L	≥48fs	Figure 2
TDM256		0	1	0	0	0	N/A			
		0	1	0	0	1	N/A			
	5	0	1	0	1	0	24-bit MSB Justified	↑	256fs	Figure 5
	6	0	1	0	1	1	24-bit I^2S Compatible	↓	256fs	Figure 6
	7	0	1	1	0	0	24-bit LSB Justified	↑	256fs	Figure 7
TDM128		1	1	0	0	0	N/A			
		1	1	0	0	1	N/A			
	8	1	1	0	1	0	24-bit MSB Justified	↑	128fs	Figure 8
	9	1	1	0	1	1	24-bit I^2S Compatible	↓	128fs	Figure 9
	10	1	1	1	0	0	24-bit LSB Justified	↑	128fs	Figure 10

Table 8. Audio Data Formats (Serial control mode) (N/A: Not available)

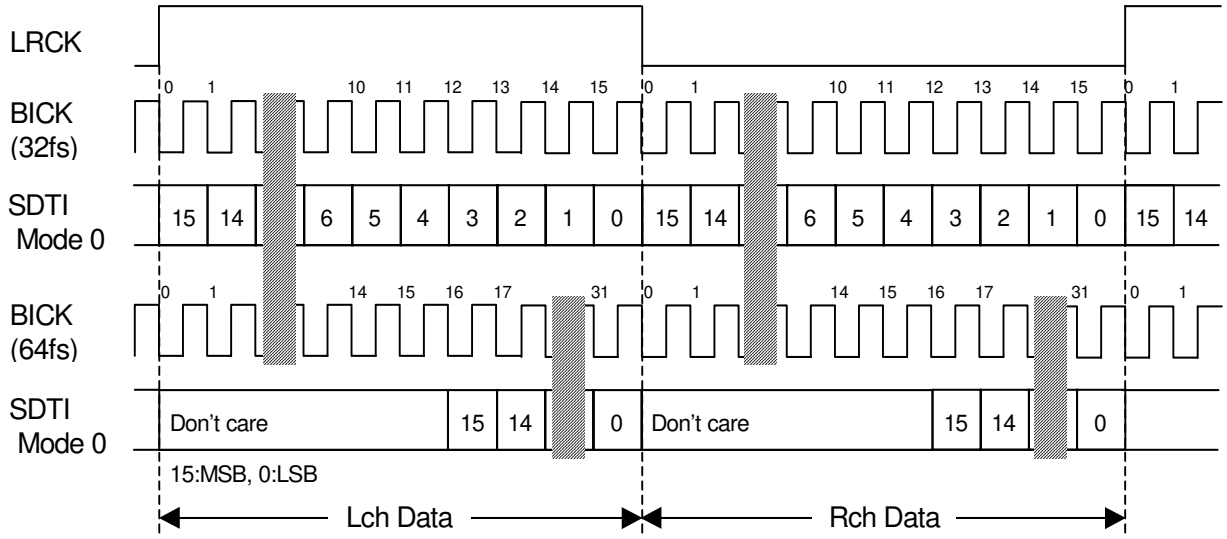


Figure 1. Mode 0 Timing

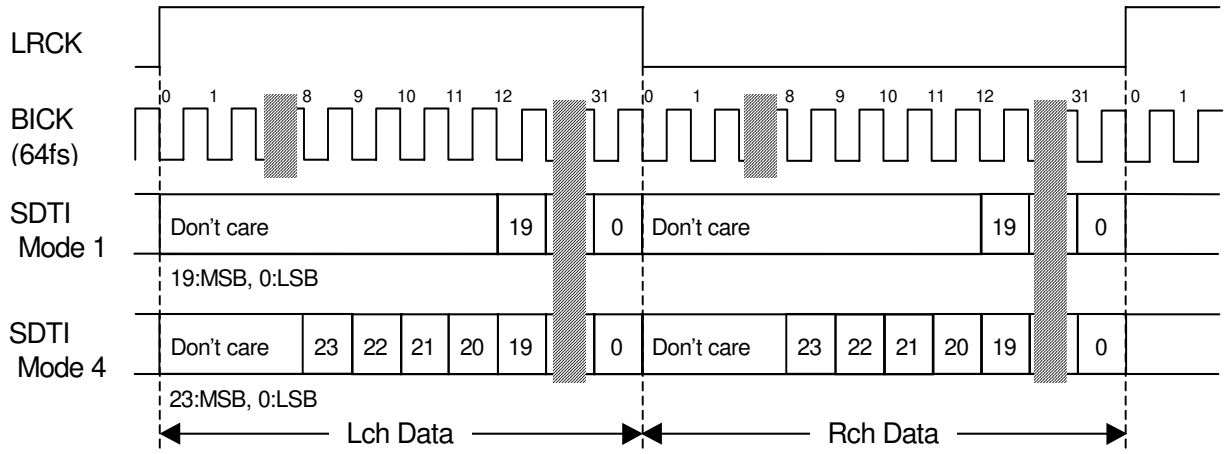


Figure 2. Mode 1/4 Timing

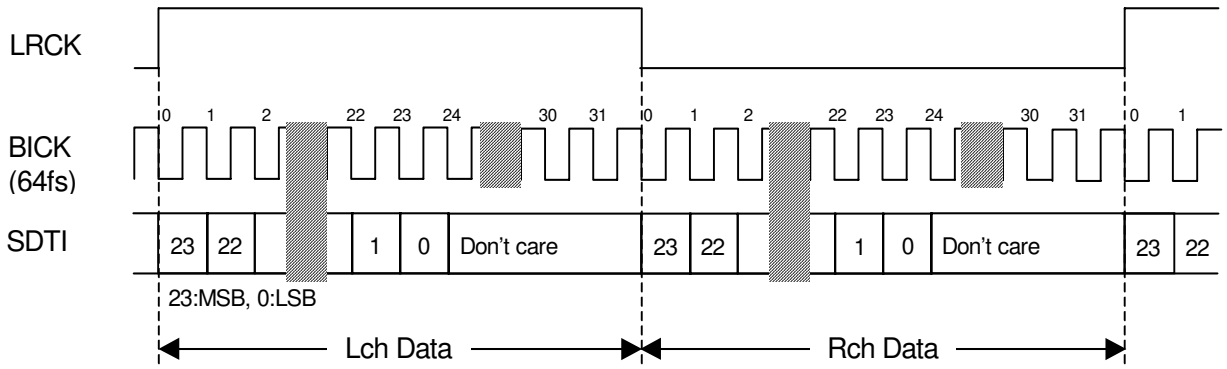


Figure 3. Mode 2 Timing

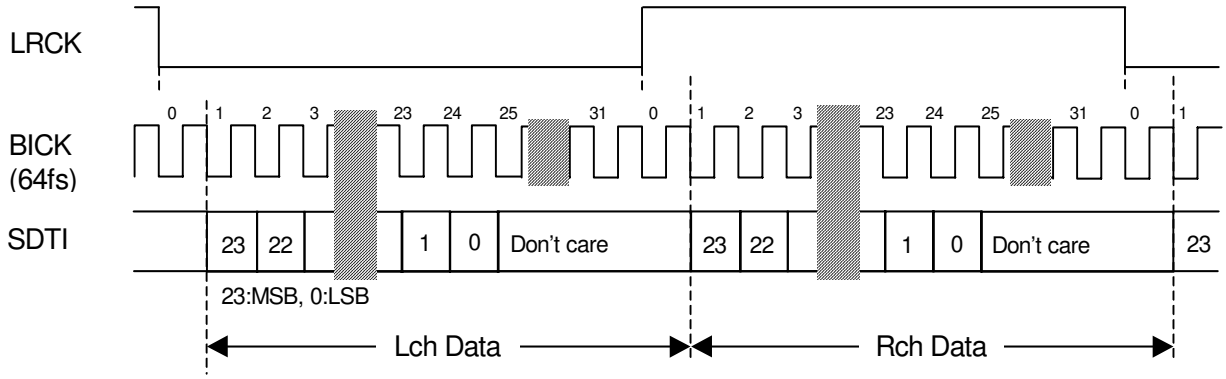


Figure 4. Mode 3 Timing

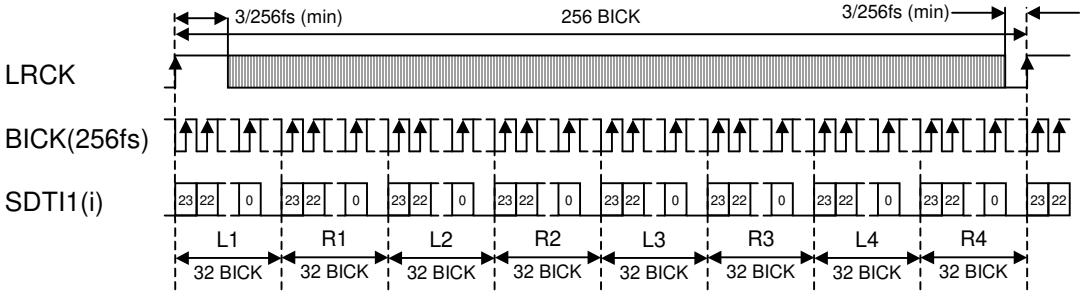


Figure 5. Mode 5 Timing

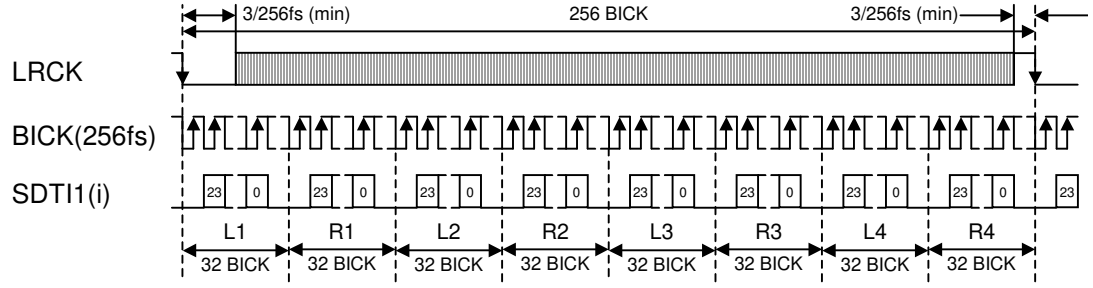


Figure 6. Mode 6 Timing

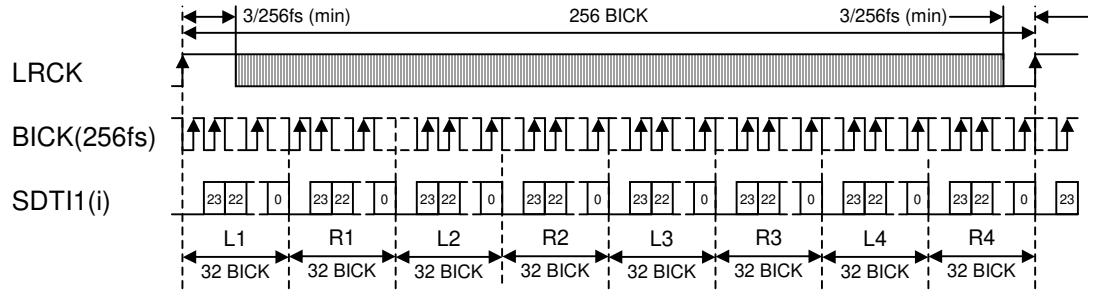


Figure 7. Mode 7 Timing

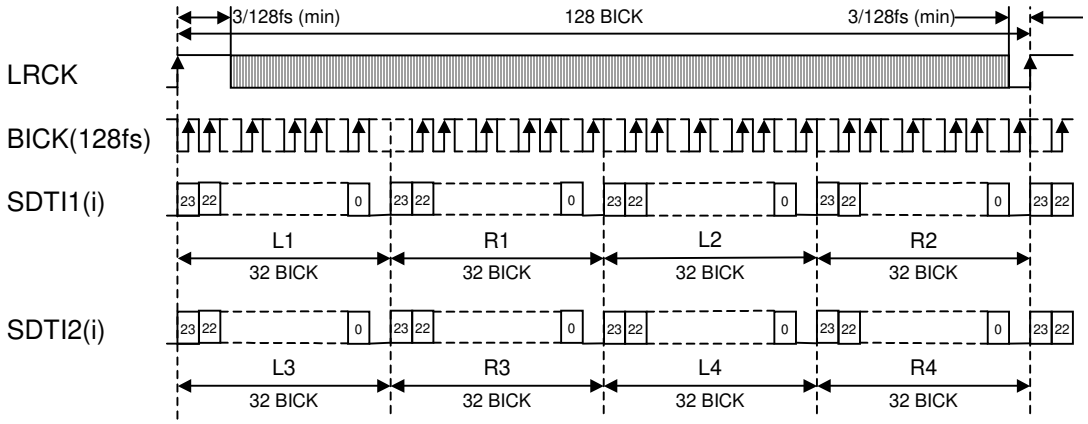


Figure 8. Mode 8 Timing

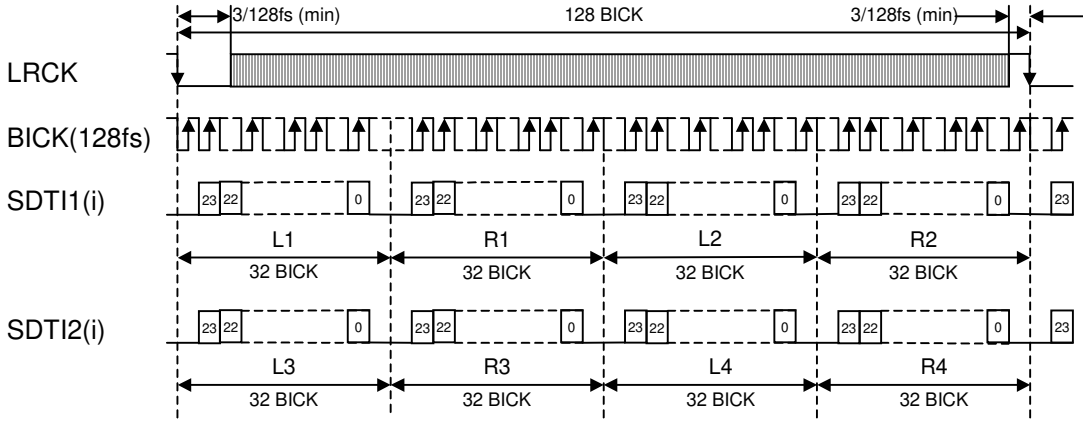


Figure 9. Mode 9 Timing

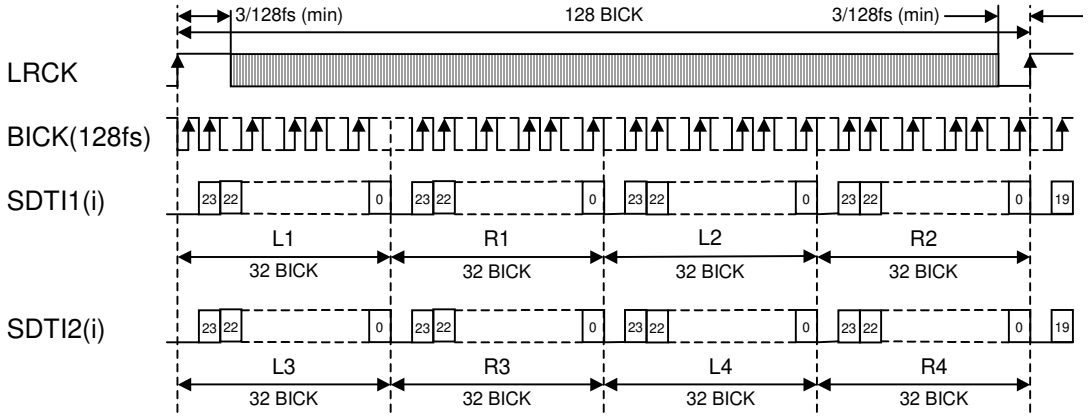


Figure 10. Mode 10 Timing

■ De-emphasis Filter

A digital de-emphasis filter is available for 32kHz, 44.1kHz or 48kHz sampling rates (tc = 50/15μs). For double speed and quad speed modes, the digital de-emphasis filter is always off. In serial control mode, the DEM1-0 bits are enabled for each DAC by the DEMA-D bits setting. In parallel control mode, DEM1-0 pins are valid.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 9. De-emphasis Filter Control (Normal Speed Mode)

■ Output Volume Control

The AK4359A includes channel independent digital output volume control (ATT) with 256 levels at linear step including MUTE. The volume control is in front of the DAC, and it can attenuate the input data from 0dB to –48dB and mute. When changing levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. The transition time of 1 level and all 256 levels is shown in Table 10. The attenuation level is calculated by ATT = 20 $\log_{10}$ (ATT_DATA / 255) [dB] and MUTE at ATT_DATA = "0".

Sampling Speed	Transition Time	
	1 Level	255 to 0
Normal Speed Mode	4LRCK	1020LRCK
Double Speed Mode	8LRCK	2040LRCK
Quad Speed Mode	16LRCK	4080LRCK

Table 10. ATT Transition time

■ Zero Detection

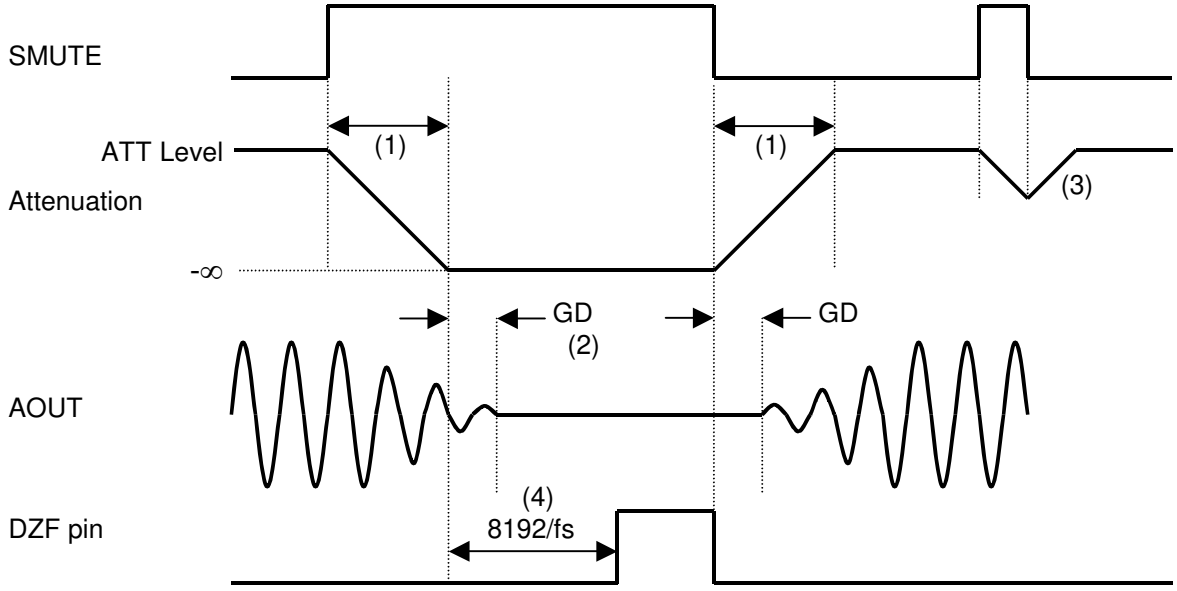
When the input data at all channels are continuously zeros for 8192 LRCK cycle, the zero detection is executed (Table 11). The DZF pin is immediately set to "L" if input data of each channel is not zero after going DZF "H". If RSTN bit is "0", the DZF pin is set to "H". The DZF pin goes "L" after 4~5LRCK after RSTN bit returns to "1". Zero detect function can be disabled by setting the DZFE bit. In this case, all DZF pins are always "L". When one of PW1-4 bit is set to "0", the input data of DAC, that the PW bit is set to "0", should be zero in order to enable zero detection of the other channels. When all PW1-4 bits are set to "0", the DZF pin fixes "L". DZFB bit can invert the polarity of the DZF pin. In parallel control mode, the zero detect function is disabled and the DZF pin is fixed to "L".

DZF Pin	Operations
DZF1	ANDed output of zero detection flag of each channel set to "1" in 0CH register
DZF2	ANDed output of zero detection flag of each channel set to "1" in 0DH register

Table 11. DZF pins Operation

■ Soft Mute Operation

The Soft mute operation is performed in the digital domain. When the SMUTE bit is set to "1", the output signal is attenuated by -∞ during ATT_DATA×ATT transition time (Table 10) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA×ATT transition time (Table 10). For this example, in Normal Speed Mode, the time is 1020LRCK cycles (1020/fs) at ATT_DATA=255.

(2) The analog output corresponding to the digital input has a group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data for each channel is continuously zero for 8192 LRCK cycles, the DZF pin for each channel changes to "H". The DZF pin immediately goes "L" if input data are not zero after going DZF "H". In parallel control mode, the DZF pin is fixed to "L" regardless of the state of the SMUTE pin.

Figure 11. Soft Mute and Zero Detection (DZFB bit = "0")

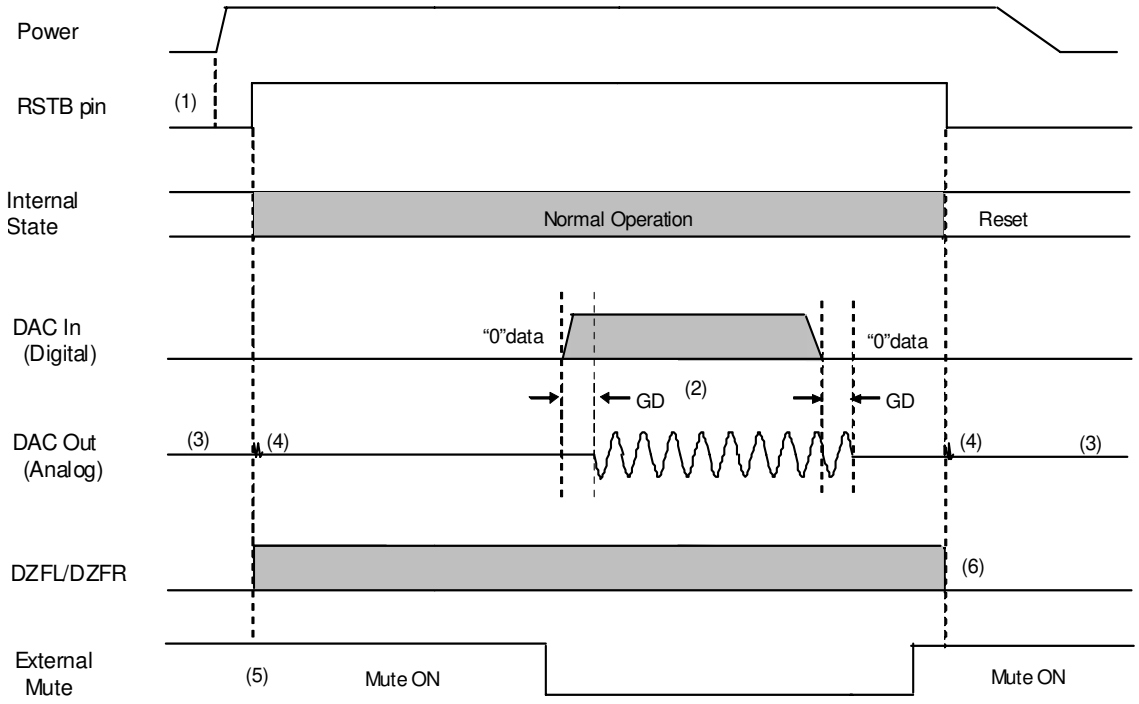
■ System Reset

The AK4359A should be reset once by bringing the RSTB pin = "L" upon power-up. The AK4359A is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4359A is in the power-down mode until MCLK and LRCK are input.

■ Power ON/OFF timing

All DACs are placed in the power-down mode by bringing the RSTB pin "L" and the registers are initialized. the analog outputs go to VCOM. As some click noise occurs at the edge of RSTB signal, the analog output should be muted externally if the click noise influences system application.

Each DAC can be powered down by setting each power-down bit (PW4-1) to "0". In this case, the registers are not initialized and the corresponding analog outputs go to VCOM. As some click noise occurs at the edge of RSTB signal, the analog output should be muted externally if click noise aversely affect system perfoemance.



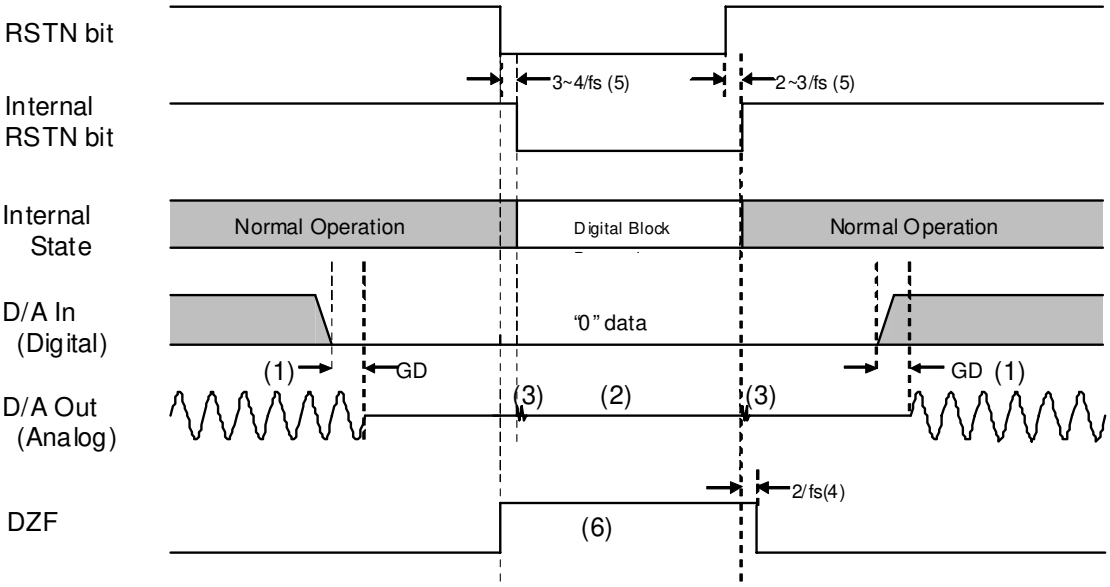
Notes:

(1) After AVDD and DVDD are powered-up, the PDN pin should be "L" for 150ns.
(2) The analog output corresponding to digital input has group delay (GD).
(3) Analog outputs are VCOM in power-down mode.
(4) Click noise occurs at the edge of RSTN signal. This noise is output even if "0" data is input.
(5) Mute the analog output externally if click noise (3) adversely affect system performance
The timing example is shown in this figure.
(6) DZFL/R pins are "L" in the reset state (RSTB pin = "L"). (DZFB bit = "0")

Figure 12. Power-down/up Sequence Example

■ Reset Function (RSTN bit)

When the RSTN bit = "0", internal circuit of DAC is powered down but the registers are not initialized. The analog outputs settle to VCOM voltage and the DZF pins go "H" at DZFB bit = "0".
Figure 13 shows the example of reset by RSTN bit. When RSTN bit = "0", pop noise is reduced at no clock state.



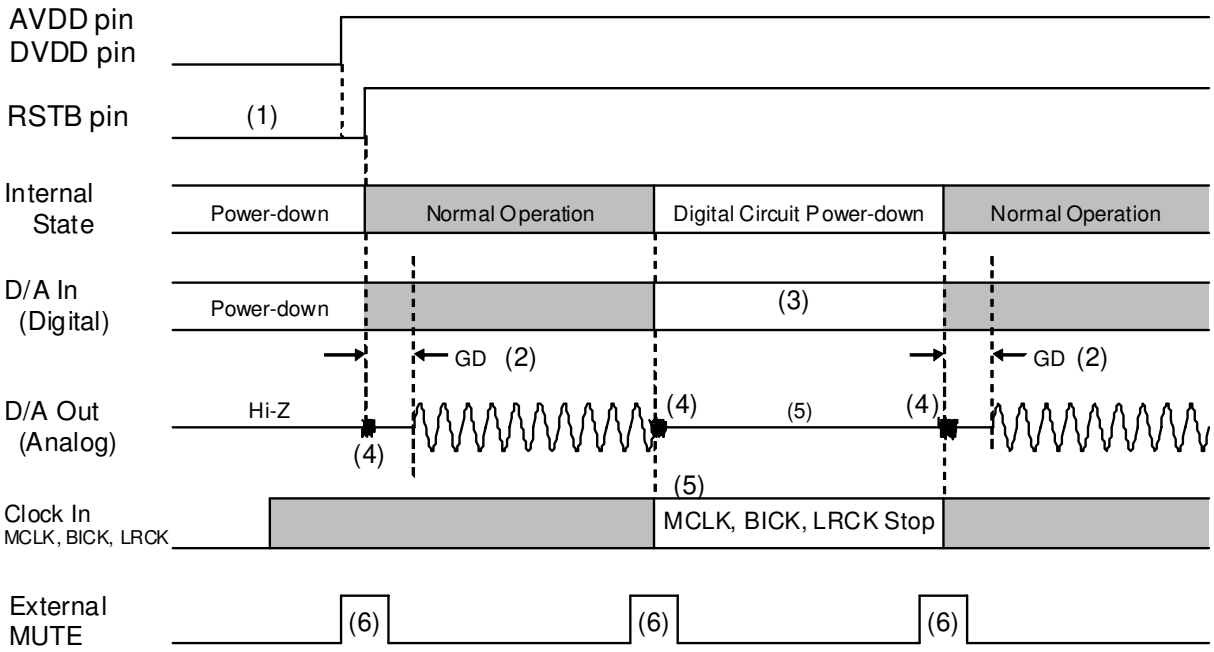
Notes:

(1) The analog output corresponding to digital input has group delay (GD).
(2) Analog outputs settle to VCOM voltage.
(3) Small pop noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The DZF pins change to "H" when the RSTN bit becomes "0", and return to "L" at 2/fs after RSTN bit becomes "1".
(5) There is a delay, 3~4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2~3/fs from RSTN bit "1" to the internal RSTN bit "1".
(6) Mute the analog output externally if click noise (3) and Hi-Z (2) adversely affect system performance

Figure 13. Reset Sequence Example (DZFB bit = "0")

■ Reset Function (MCLK, BICK and LRCK stop)

When the MCLK, LRCK or BICK stops, the digital circuit of the AK4359A is placed in power-down mode. When the MCLK, LRCK and BICK are restarted, power-down mode is released and the AK4359A returns to normal operation mode.



Notes:

(1) After AVDD and DVDD are powered-up, the PDN pin should be "L" for 150ns.
(2) The analog output corresponding to digital input has group delay (GD).
(3) The digital data can be stopped. Click noise after MCLK, BICK and LRCK are input again can be reduced by inputting "0" data during this period.
(4) Click noise occurs within 20usec or 20usec +3 ~ 4LRCK from the riding edge ("↑") of the RSTN pin or MCLK inputs. Click noise also occurs within 20usec when MCLK, LRCK or BICK is stopped.
(5) Mute the analog output externally if click noise (4) influences system applications. The timing example is shown in this figure.

Figure 14. Clock Stop Sequence

■ Register Control Interface

The functions of the AK4359A can be controlled by registers. Two types of control mode write internal registers. In the I²C-bus mode, the chip address is determined by the state of the CAD0 pin. In 3-wire mode, the chip address is fixed to "11". The RSTB pin = "L" initializes the registers to their default values. Writing "0" to the RSTN bit resets the internal timing circuit, but the registers are not initialized.

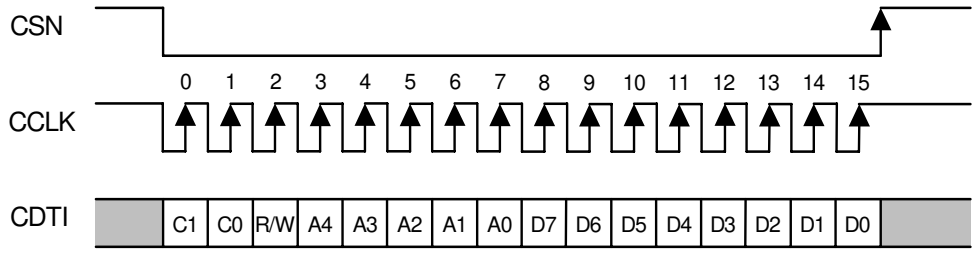
* The AK4359A does not support read command.
* When the AK4359A is in power down mode (RSTB pin = "L") or the MCLK is not provided, writing to control register is prohibited.
* When the state of the P/S pin is changed, the AK4359A should be reset by the RSTB pin = "L".
* In serial control mode, the setting of parallel pins is invalid.

Function	Parallel Control Mode	Serial Control Mode
Double sampling mode at 128/192fs	-	O
De-emphasis	O	O
SMUTE	O	O
Zero Detection	-	O
16/20/24bit LSB justified format	-	O
TDM256 mode	O	O
TDM128 mode	-	O

Table 12. Function Table (O: Supported, -: Not supported)

(1) 3-wire Serial Control Mode (I2C pin = "L")

The 3-wire μP interface pins, CSN, CCLK and CDTI, write internal registers. The data on this interface consists of Chip Address (2bits, C1/0; fixed to "11"), Read/Write (1bit; fixed to "1", Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). The AK4359A latches the data on the rising edge of CCLK, so data should clocked in on the falling edge. The writing of data becomes valid by the rising edge of CSN. The clock speed of CCLK is 5MHz (max).



C1-C0: Chip Address (Fixed to "11")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 15. Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")

The AK4359A supports the fast-mode I²C-bus system (max: 400kHz).

Figure 16 shows the data transfer sequence at the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 20). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit which is a data direction bit (R/W) (Figure 17). The most significant six bits of the slave address are fixed as "001001". The next one bit are CAD0 (device address bit). The bit identify the specific device on the bus. The hard-wired input pin (CAD0 pin) set them. If the slave address match that of the AK4359A and R/W bit is "0", the AK4359A generates the acknowledge and the write operation is executed. If R/W bit is "1", the AK4359A generates the not acknowledge since the AK4359A can be only a slave-receiver. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 21).

The second byte consists of the address for control registers of the AK4359A. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 18). Those data after the second byte contain control data. The format is MSB first, 8bits (Figure 19). The AK4359A generates an acknowledge after each byte is received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 20).

The AK4359A is capable of more than one byte write operation by one sequence. After receipt of the third byte, the AK4359A generates an acknowledge, and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the addresses exceed 1FH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 22) except for the START and the STOP condition.

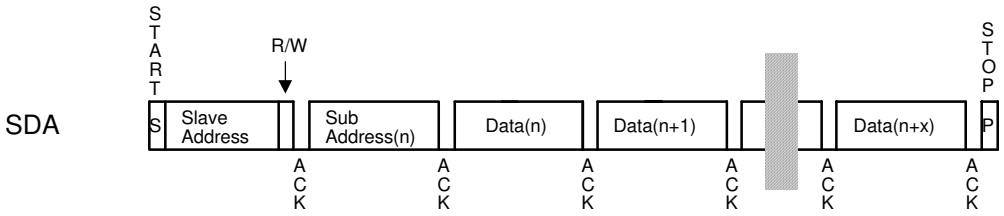


Figure 16. Data transfer sequence at the I²C-bus mode

0	0	1	0	0	1	CAD0	R/W

(This CAD0 should match with CAD0 pin)

Figure 17. The first byte

0	0	0	A4	A3	A2	A1	A0

Figure 18. The second byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 19. Byte structure after the second byte

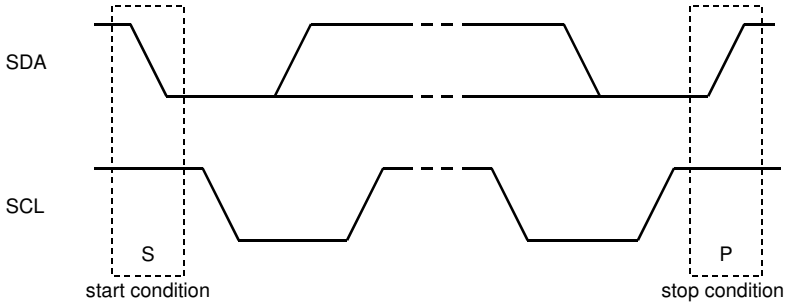


Figure 20. START and STOP conditions

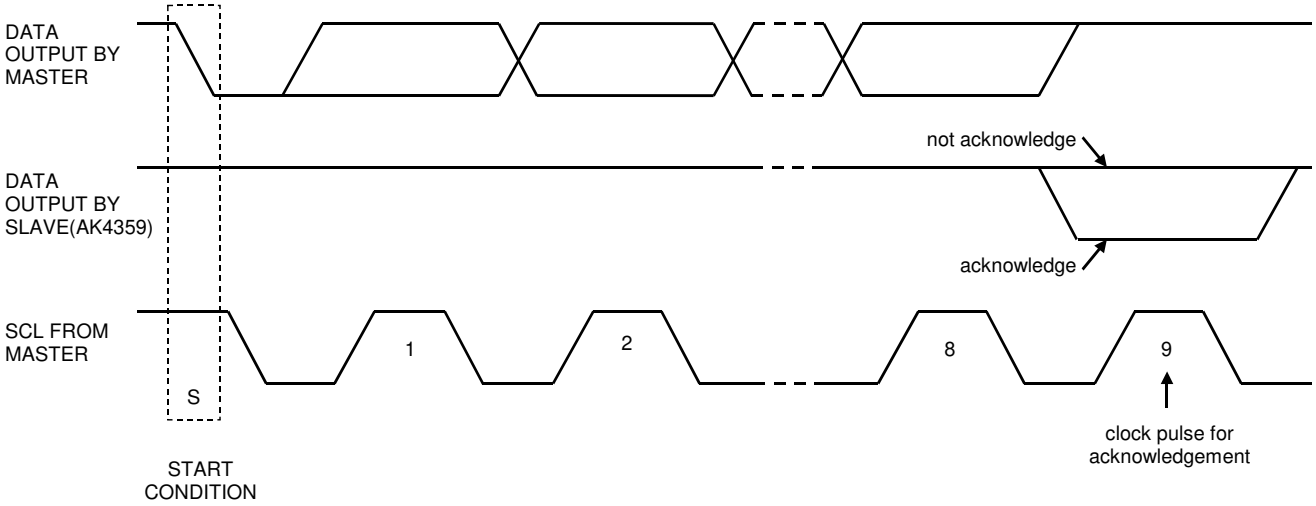


Figure 21. Acknowledge on the I^2C-bus

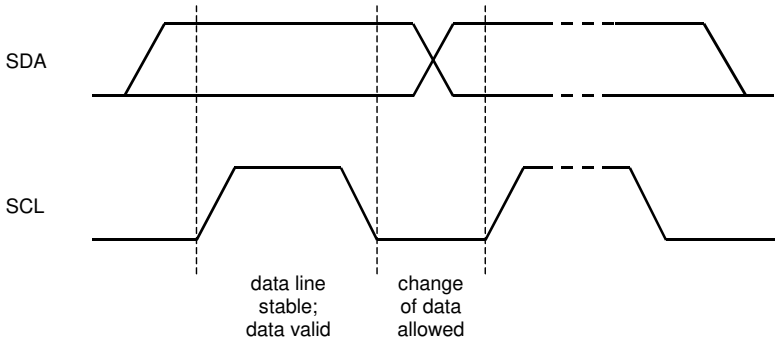


Figure 22. Bit transfer on the I^2C-bus