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AK4370

24-Bit 2ch DAC with HP-AMP & Output Mixer

GENERAL DESCRIPTION

The AK4370 is a 24-bit DAC with headphone amplifier. The AK4370 features an analog mixing circuit that allows easy interfacing in mobile phone and portable communication designs. The integrated headphone amplifier features "pop-noise free" power-on/off, a mute control, and it delivers 40mW of power into 16Ω. The AK4370 is packaged in a 24-pin QFN (4mm×4mm) package, ideal for portable applications.

FEATURE

- ☐ Multi-bit ΔΣ DAC
- ☐ Sampling Rate
  - 8kHz ~ 48kHz
- ☐ On chip perfect filtering 8 times FIR interpolator
  - Passband: 20kHz
  - Passband Ripple: ±0.02dB
  - Stopband Attenuation: 54dB
- ☐ Digital De-emphasis Filter: 32kHz, 44.1kHz and 48kHz
- ☐ System Clock
  - 256fs/384fs/512fs/768fs/1024fs
  - Input Level: AC Couple Input Available
- ☐ Audio I/F Format: MSB First, 2's Complement
  - I^2S, 24bit MSB justified, 24bit/20bit/16bit LSB justified
  - Master/Slave Mode
- ☐ Digital Mixing: LR, LL, RR, (L+R)/2
- ☐ Bass Boost Function
- ☐ Digital ATT
- ☐ Analog Mixing Circuit: 4 Inputs (Single-ended or Full-differential)
- ☐ Stereo Lineout
  - S/N: 90dB@3.3V
  - Output Volume: +6 to –24dB (or 0 to –30dB), 2dB step
- ☐ Headphone Amplifier
  - Output Power: 40mW x 2ch @16Ω, 3.3V
  - S/N: 92dB@3.3V
  - Pop Noise Free at Power-ON/OFF and Mute
  - Output Volume: 0 ~ –63dB & +12/+6/0 dB Gain
    1.5dB step (0 ~ –30dB), 3dB step (–30 ~ –63dB)
- ☐ μP Interface: 3-wire/I^2C
- ☐ Power Supply: 1.6V ~ 3.6V
- ☐ Power Supply Current: 3.8mA @1.8V (6.8mW, DAC+HP, No output)
- ☐ Ta: –30 ~ 85°C
- ☐ Small Package: 24-pin QFN (4mm x 4mm, 0.5mm pitch)
- ☐ Register Compatible with AK4368

■ Block Diagram

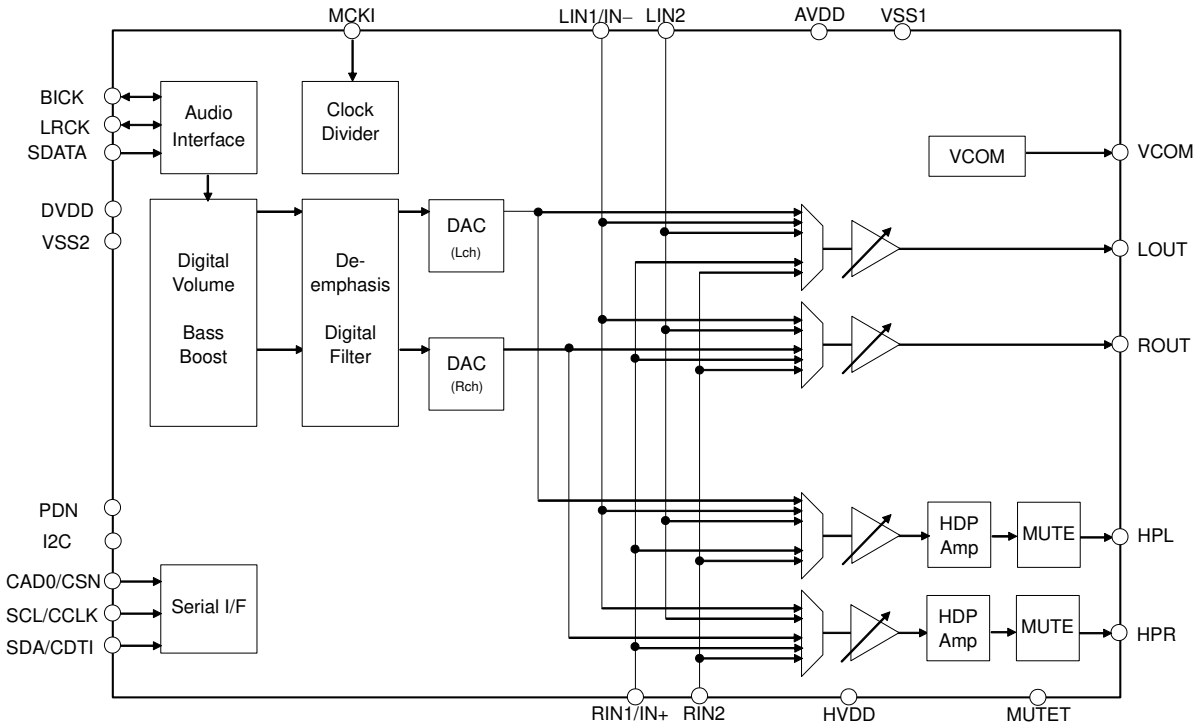
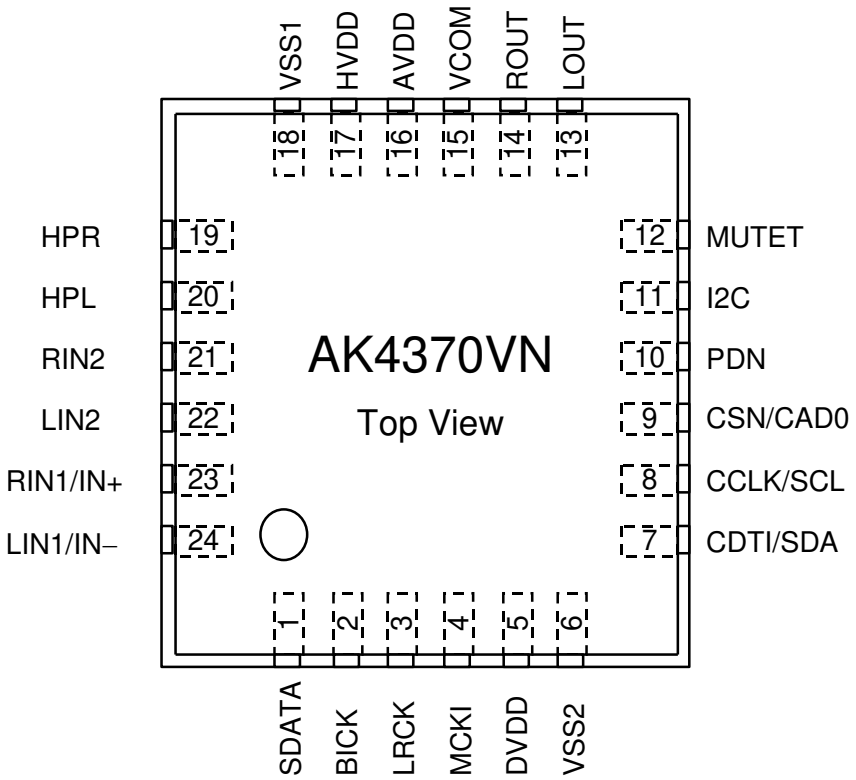


Figure 1. Block Diagram

■ Ordering Information

AK4370VN	–30 ~ +85°C	24-pin QFN (0.5mm pitch)
AKD4370	Evaluation board for AK4370	

■ Pin Layout



■ Comparison with AK4368

1 Function

Function	AK4368	AK4370
Analog Mixing	1-Stereo + 1-Mono Single-ended Input	2-Stereo Single-ended Input or Full-differential Input
MCKI at EXT Mode	256fs/512fs/1024fs, 12.288MHz(max)	256fs/384fs/512fs/768fs/1024fs, 24.576MHz(max)
HP-Amp Output Volume	No	0 to –63dB & +12/+6/0dB 1.5dB step (0 to –30dB) 3dB step (–30 to –63dB)
HP-Amp Hi-Z Setting	No	Yes
PLL	Yes	No
3D Enhancement	Yes	No
ALC	Yes	No
Package	41BGA (4mm x 4mm)	24QFN (4mm x 4mm)

2 Register (difference from AK4368)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	~~PMPLL~~	PMLO	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
01H	Clock Control 0	FS3	FS2	FS1	FS0	~~PLL3~~	~~PLL2~~	~~PLL1~~	~~PLL0~~
02H	Clock Control 1	0	0	M/S	MCKAC	BF	~~PS0~~	~~PS1~~	~~MCKO~~
03H	Mode Control 0	0	MONO1	MONO0	BCKP	LRP	DIF2	DIF1	DIF0
04H	Mode Control 1	ATS	DATTC	LMUTE	SMUTE	BST1	BST0	DEM1	DEM0
05H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
06H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
07H	Headphone Out Select 0	HPG1	HPG0	LIN2HR	LIN2HL	RIN1HR	LIN1HL	DARHR	DALHL
08H	Lineout Select 0	0	LOG	LIN2R	LIN2L	RIN1R	LIN1L	DARR	DALL
09H	Lineout ATT	0	0	0	0	ATTS3	ATTS2	ATTS1	ATTS0
0AH	Reserved	~~REF7~~	~~REF6~~	~~REF5~~	~~REF4~~	~~REF3~~	~~REF2~~	~~REF1~~	~~REF0~~
0BH	Reserved	0	0	~~ALC~~	~~ROTM1~~	~~ROTM0~~	~~LMAT1~~	~~LMAT0~~	~~RATT~~
0CH	Reserved	0	0	0	0	~~DP1~~	~~DP0~~	~~3D1~~	~~3D0~~
0DH	Headphone Out Select 1	0	0	0	0	RIN2HR	RIN2HL	LIN1HR	RIN1HL
0EH	Headphone ATT	0	HPZ	HMUTE	ATTH4	ATTH3	ATTH2	ATTH1	ATTH0
0FH	Lineout Select 1	0	0	0	0	RIN2R	RIN2L	LIN1R	RIN1L
10H	Mono Mixing	0	0	0	0	L2M	L2HM	L1M	L1HM
11H	Differential Select	0	0	0	0	0	0	LDIFH	LDIF
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	1	0	0	0	0

These bits are added in the AK4370

These bits are deleted in the AK4370

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	SDATA	I	Audio Serial Data Input Pin
2	BICK	I/O	Audio Serial Data Clock Pin
3	LRCK	I/O	Input / Output Channel Clock Pin
4	MCKI	I	External Master Clock Input Pin
5	DVDD	-	Digital Power Supply Pin, 1.6 ~ 3.6V
6	VSS2	-	Ground 2 Pin. Connected to VSS1.
7	SDA	I/O	Control Data Input/Output Pin (I2C mode : I2C pin = "H")
	CDTI	I	Control Data Input Pin (3-wire serial mode : I2C pin = "L")
8	SCL	I	Control Data Clock Pin (I2C mode : I2C pin = "H")
	CCLK	I	Control Data Clock Pin (3-wire serial mode : I2C pin = "L")
9	CAD0	I	Chip Address 0 Select Pin (I2C mode : I2C pin = "H")
	CSN	I	Chip Select Pin (3-wire serial mode : I2C pin = "L")
10	PDN	I	Power-down & Reset When "L", the AK4370 is in power-down mode and is held in reset. The AK4370 should always be reset upon power-up.
11	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire Serial
12	MUTET	O	Mute Time Constant Control pin Connected to VSS1 pin with a capacitor for mute time constant.
13	LOUT	O	Lch Stereo Line Output Pin
14	ROUT	O	Rch Stereo Line Output Pin
15	VCOM	O	Common Voltage Output Pin Normally connected to VSS1 pin with a 2.2μF electrolytic capacitor.
16	AVDD	-	Analog Power Supply Pin, 1.6 ~ 3.6V
17	HVDD	-	Power Supply Pin for Headphone Amp, 1.6 ~ 3.6V
18	VSS1	-	Ground 1 Pin
19	HPR	O	Rch Headphone Amp Output
20	HPL	O	Lch Headphone Amp Output
21	RIN2	I	Rch Analog Input 2 Pin
22	LIN2	I	Lch Analog Input 2 Pin
23	RIN1	I	Rch Analog Input 1 Pin (LDIF bit ="0" : Single-ended Input)
	IN+	I	Positive Line Input Pin (LDIF bit ="1" : Full-differential Input)
24	LIN1	I	Rch Analog Input 1 Pin (LDIF bit ="0" : Single-ended Input)
	IN−	I	Negative Line Input Pin (LDIF bit ="1" : Full-differential Input)

Note 1. All digital input pins (I2C, SDA/CDTI, SCL/CCLK, CAD0/CSN, SDATA, LRCK, BICK, MCKI, PDN) must not be left floating. MCKI pin can be left floating only when PDN pin = "L".

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LOUT, ROUT, MUTET, HPL, HPR, LIN2, RIN2, RIN1/IN+, LIN1/IN−	These pins should be open.
Digital	MCKI	This pin should be connected to VSS2.

ABSOLUATE MAXIMUM RATING

(VSS1, VSS2=0V; Note 2, Note 3)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	HP-Amp	HVDD	–0.3	4.6	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 4)		VINA	–0.3	(AVDD+0.3) or 4.6	V
Digital Input Voltage (Note 5)		VIND	–0.3	(DVDD+0.3) or 4.6	V
Ambient Temperature		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 2. All voltages with respect to ground.

Note 3. VSS1 and VSS2 must be connected to the same analog ground plane.

Note 4. LIN1/IN−, RIN1/IN+, LIN2 and RIN2 pins. Max is smaller value between (AVDD+0.3)V and 4.6V.

Note 5. SDA/CDTI, SCL/CCLK, CAD0/CSN, SDATA, LRCK, BICK, MCKI, PDN and I2C pins. Max is smaller value between (DVDD+0.3)V and 4.6V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS1, VSS2=0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 6)	Analog	AVDD	1.6	2.4	3.6	V
	Digital (Note 7)	DVDD	1.6	2.4	(AVDD+0.2) or 3.6	V
	HP-Amp	HVDD	1.6	2.4	3.6	V
	Difference	AVDD–HVDD	–0.3	0	+0.3	V

Note 2. All voltages with respect to ground.

Note 6. When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. When the AK4370 is powered-down, DVDD should be powered-down at the same time or later than AVDD. When AVDD and HVDD are supplied separately, AVDD should be powered-up at the same time or earlier than HVDD. When the AK4370 is powered-down, AVDD should be powered-down at the same time or later than HVDD.

Note 7. Max is smaller value between (AVDD+0.2)V and 3.6V.

* AKM assumes no responsibility for usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=HVDD=2.4V, VSS1=VSS2=0V; fs=44.1kHz; BOOST OFF; Slave Mode; Signal Frequency =1kHz; Measurement band width=20Hz ~ 20kHz; Headphone-Amp: Load impedance is a serial connection with R_L=16Ω and C_L=220μF. (Refer to Figure 38; unless otherwise specified)

Parameter			Min.	Typ.	Max.	Unit
DAC Resolution			-	-	24	bit
Headphone-Amp: (HPL/HPR pins) (Note 8)						
Analog Output Characteristics						
THD+N	–3dBFS Output, 2.4V, Po=10mW@16Ω		-	–50	–40	dB
	0dBFS Output, 3.3V, Po=40mW@16Ω		-	–20	-	dB
D-Range	–60dBFS Output, A-weighted, 2.4V		82	90	-	dB
	–60dBFS Output, A-weighted, 3.3V		-	92	-	dB
S/N	A-weighted, 2.4V		82	90	-	dB
	A-weighted, 3.3V		-	92	-	dB
Interchannel Isolation			60	80	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.3	0.8	dB
Gain Drift			-	200	-	ppm/°C
Load Resistance (Note 9)			16	-	-	Ω
Load Capacitance			-	-	300	pF
Output Voltage	–3dBFS Output (Note 10)		1.04	1.16	1.28	Vpp
	0dBFS Output, 3.3V, Po=40mW@16Ω		-	0.8	-	Vrms
Output Volume: (HPL/HPR pins)						
Step Size (HPG1-0 bits = "00")	0 ~ –30dB		0.1	1.5	2.9	dB
	–30 ~ –63dB		0.1	3	5.9	dB
Gain Control Range (HPG1-0 bits = "00")	Max (ATT4-0 bits = "00H")		-	0	-	dB
	Min (ATT4-0 bits = "1FH")		-	–63	-	dB
Stereo Line Output: (LOUT/ROUT pins, R_L=10kΩ) (Note 11)						
Analog Output Characteristics:						
THD+N (0dBFS Output)			-	–60	–50	dB
S/N	A-weighted, 2.4V		80	87	-	dB
	A-weighted, 3.3V		-	90	-	dB
DC Accuracy						
Gain Drift			-	200	-	ppm/°C
Load Resistance (Note 9)			10	-	-	kΩ
Load Capacitance			-	-	25	pF
Output Voltage (0dBFS Output) (Note 12)			1.32	1.47	1.61	Vpp
Output Volume: (LOUT/ROUT pins)						
Step Size			1	2	3	dB
Gain Control Range (LOG1-0 bit = "0")	Max (ATTS3-0 bits = "FH")		-	0	-	dB
	Min (ATTS3-0 bits = "0H")		-	–30	-	dB

Note 8. DALHL=DARHR bits = "1"
LIN1HL=RIN1HL=LIN2HL=RIN2HL=LIN1HR=RIN1HR=LIN2HR=RIN2HR bits = "0".
Note 9. AC load.
Note 10. Output voltage is proportional to AVDD voltage. Vout = 0.48 x AVDD(typ)@–3dBFS.
Note 11. DALL=DARR bits = "1"
LIN1L=RIN1L=LIN2L=RIN2L=LIN1R=RIN1R=LIN2R=RIN2R bits = "0"
Note 12. Output voltage is proportional to AVDD voltage. Vout = 0.61 x AVDD(typ)@0dBFS.

Parameter	Min.	Typ.	Max.	Unit
LINEIN: (LIN1/RIN1/LIN2/RIN2 pins)				
Analog Input Characteristics				
Input Resistance (Refer to Figure 21, Figure 22)				
LIN1 pin				
LIN1HL=LIN1HR=LIN1L=LIN1R bits = "1"	14	25	-	kΩ
LIN1HL bit = "1", LIN1HR=LIN1L=LIN1R bits = "0"	-	100	-	kΩ
LIN1HR bit = "1", LIN1HL=LIN1L=LIN1R bits = "0"	-	100	-	kΩ
LIN1L bit = "1", LIN1HL=LIN1HR=LIN1R bits = "0"	-	100	-	kΩ
LIN1R bit = "1", LIN1HL=LIN1HR=LIN1L bits = "0"	-	100	-	kΩ
RIN1 pin				
RIN1HL=RIN1HR=RIN1L=RIN1R bits = "1"	14	25	-	kΩ
RIN1HL bit = "1", RIN1HR=RIN1L=RIN1R bits = "0"	-	100	-	kΩ
RIN1HR bit = "1", RIN1HL=RIN1L=RIN1R bits = "0"	-	100	-	kΩ
RIN1L bit = "1", RIN1HL=RIN1HR=RIN1R bits = "0"	-	100	-	kΩ
RIN1R bit = "1", RIN1HL=RIN1HR=RIN1L bits = "0"	-	100	-	kΩ
LIN2 pin				
LIN2HL=LIN2HR=LIN2L=LIN2R= bits = "1"	14	25	-	kΩ
LIN2HL bit = "1", LIN2HR=LIN2L=LIN2R bits = "0"	-	100	-	kΩ
LIN2HR bit = "1", LIN2HL=LIN2L=LIN2R bits = "0"	-	100	-	kΩ
LIN2L bit = "1", LIN2HL=LIN2HR=LIN2R bits = "0"	-	100	-	kΩ
LIN2R bit = "1", LIN2HL=LIN2HR=LIN2L bits = "0"	-	100	-	kΩ
RIN2 pin				
RIN2HL=RIN2HR=RIN2L=RIN2R bits = "1"	14	25	-	kΩ
RIN2HL bit = "1", RIN2HR=RIN2L=RIN2R bits = "0"	-	100	-	kΩ
RIN2HR bit = "1", RIN2HL=RIN2L=RIN2R bits = "0"	-	100	-	kΩ
RIN2L bit = "1", RIN2HL=RIN2HR=RIN2R bits = "0"	-	100	-	kΩ
RIN2R bit = "1", RIN2HL=RIN2HR=RIN2L bits = "0"	-	100	-	kΩ
Gain				
LIN1/LIN2/RIN1/RIN2 → LOUT/ROUT	–1	0	+1	dB
LIN1/LIN2/RIN1/RIN2 → HPL/HPR	–0.05	+0.95	+1.95	dB
Power Supplies				
Power Supply Current				
Normal Operation (PDN pin = "H") (Note 13)				
AVDD+DVDD	-	3.8	5.5	mA
HVDD	-	1.2	2.5	mA
Power-Down Mode (PDN pin = "L") (Note 14)	-	1	100	μA

Note 13. PMDAC=PMHPL=PMHPR=PMLO bits = "1", MUTEN bit = "1", HP-Amp no output.
PMDAC=PMHPL=PMHPR= "1", PMLO bit= "0", AVDD+DVDD+HVDD=4.0mA (typ) @2.4V, 3.8mA (typ) @1.8V.

Note 14. All digital input pins are fixed to VSS2.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD=1.6 ~ 3.6V; fs=44.1kHz; De-emphasis = "OFF")

Parameter			Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter: (Note 15)							
Passband (Note 16)		–0.05dB	PB	0	-	20.0	kHz
		–6.0dB		-	22.05	-	kHz
Stopband (Note 16)			SB	24.1	-	-	kHz
Passband Ripple			PR	-	-	±0.02	dB
Stopband Attenuation			SA	54	-	-	dB
Group Delay (Note 17)			GD	-	22	-	1/fs
Group Delay Distortion			ΔGD	-	0	-	µs
DAC Digital Filter + Analog Filter: (Note 15, Note 18)							
Frequency Response	0 ~ 20.0kHz		FR	-	±0.5	-	dB
Analog Filter: (Note 19)							
Frequency Response	0 ~ 20.0kHz		FR	-	±1.0	-	dB
BOOST Filter: (Note 18, Note 20)							
Frequency Response	MIN	20Hz	FR	-	5.76	-	dB
		100Hz		-	2.92	-	dB
		1kHz		-	0.02	-	dB
	MID	20Hz	FR	-	10.80	-	dB
		100Hz		-	6.84	-	dB
		1kHz		-	0.13	-	dB
	MAX	20Hz	FR	-	16.06	-	dB
		100Hz		-	10.54	-	dB
		1kHz		-	0.37	-	dB

Note 15. BOOST OFF (BST1-0 bit = "00")

Note 16. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.4535fs(@–0.05dB). SB=0.546fs(@–54dB).

Note 17. This time is from setting the 24-bit data of both channels from the input register to the output of analog signal.

Note 18. DAC → HPL, HPR, LOUT, ROUT

Note 19. LIN1/LIN2/RIN1/RIN2 → HPL/HPR/LOUT/ROUT

Note 20. These frequency responses scale with fs. If high-level signal is input, the output clips at low frequency.

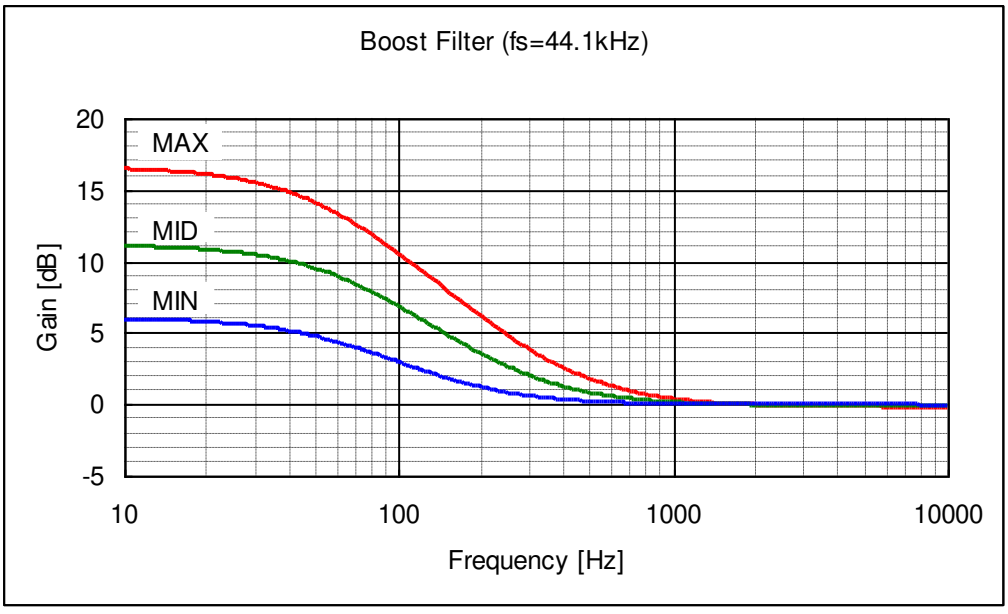


Figure 2. Boost Frequency (fs=44.1kHz)

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD=1.6 ~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage	2.2V≤DVDD≤3.6V	VIH	70%DVDD	-	-	V
	1.6V≤DVDD<2.2V	VIH	80%DVDD	-	-	V
Low-Level Input Voltage	2.2V≤DVDD≤3.6V	VIL	-	-	30%DVDD	V
	1.6V≤DVDD<2.2V	VIL	-	-	20%DVDD	V
Input Voltage at AC Coupling (Note 21)		VAC	0.4	-	-	Vpp
High-Level Output Voltage (Iout=−200μA)		VOH	DVDD−0.2	-	-	V
Low-Level Output Voltage						
(Except SDA pin: Iout=200μA)		VOL	-	-	0.2	V
(SDA pin, 2.0V≤DVDD≤3.6V: Iout=3mA)		VOL	-	-	0.4	V
(SDA pin, 1.6V≤DVDD<2.0V: Iout=3mA)		VOL	-	-	20%DVDD	V
Input Leakage Current		Iin	-	-	±10	μA

Note 21. MCKI is connected to a capacitor. (Refer to Figure 38)

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD=1.6 ~ 3.6V; C_L = 20pF; unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Input Timing					
Frequency	fCLK	2.048	-	24.576	MHz
Pulse Width Low (Note 22)	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High (Note 22)	tCLKH	0.4/fCLK	-	-	ns
AC Pulse Width (Note 23)	tACW	20.3	-	-	ns
LRCK Timing					
Frequency	fs	8	44.1	48	kHz
Duty Cycle: Slave Mode	Duty	45	-	55	%
Master Mode	Duty	-	50	-	%
Serial Interface Timing (Note 24)					
Slave Mode (M/S bit = "0"):					
BICK Period (Note 25)	tBCK	312.5 or 1/(64fs)	-	1/(32fs)	ns
BICK Pulse Width Low	tBCKL	100	-	-	ns
Pulse Width High	tBCKH	100	-	-	ns
LRCK Edge to BICK "↑" (Note 26)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 26)	tBLR	50	-	-	ns
SDATA Hold Time	tSDH	50	-	-	ns
SDATA Setup Time	tSDS	50	-	-	ns
Master Mode (M/S bit = "1"):					
BICK Frequency (BF bit = "1")	fBCK	-	64fs	-	Hz
(BF bit = "0")	fBCK	-	32fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–50	-	50	ns
SDATA Hold Time	tSDH	50	-	-	ns
SDATA Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↑" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns

Note 22. Except AC coupling.

Note 23. Pulse width to ground level when MCKI is connected to a capacitor in series and a resistor is connected to ground. (Refer to Figure 3.)

Note 24. Refer to "Serial Data Interface".

Note 25. Min is longer value between 312.5ns or 1/(64fs) except for PLL Mode, PLL4-0 bits = "EH", "FH".

Note 26. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I^2C Bus mode): (Note 27)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 28)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 29)	tPD	150	-	-	ns

Note 27. I^2C-bus is a trademark of NXP B.V.
Note 28. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 29. The AK4370 can be reset by bringing PDN pin = “L” to “H” only upon power up.

■ Timing Diagram

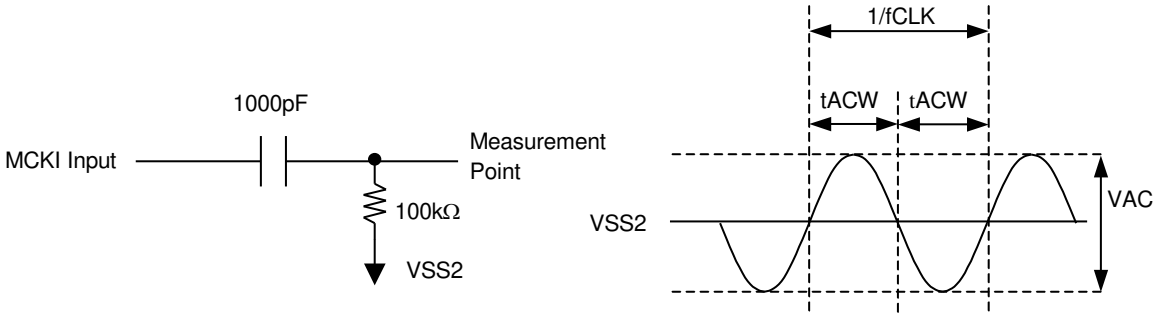


Figure 3. MCKI AC Coupling Timing

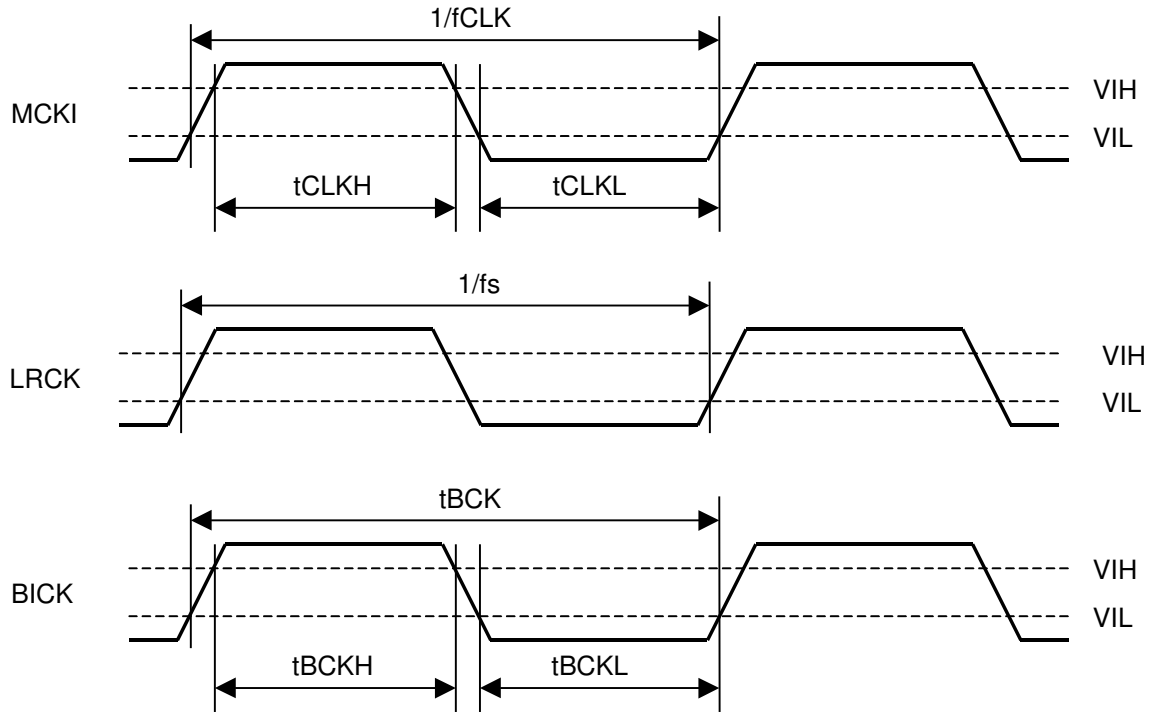


Figure 4. Clock Timing

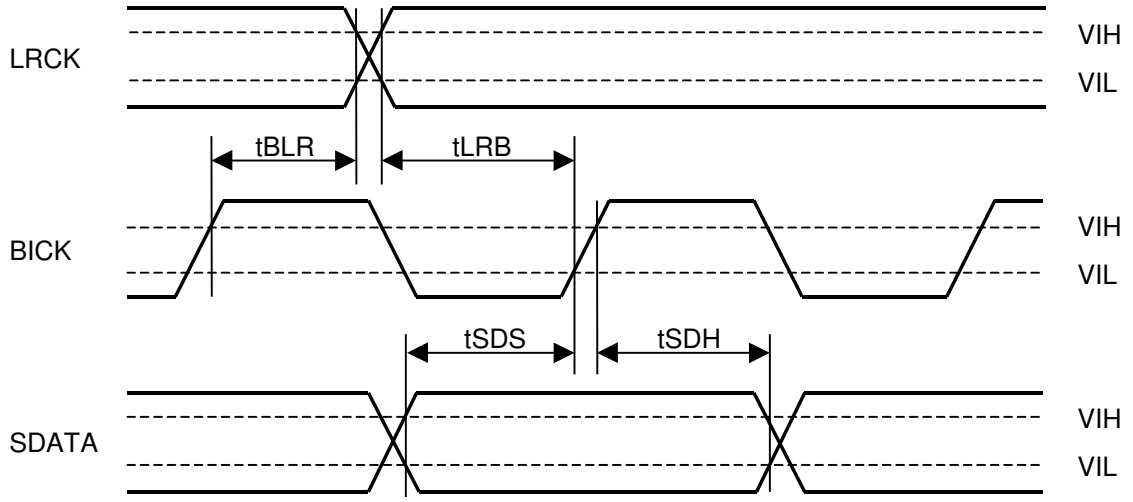


Figure 5. Serial Interface Timing (Slave Mode)

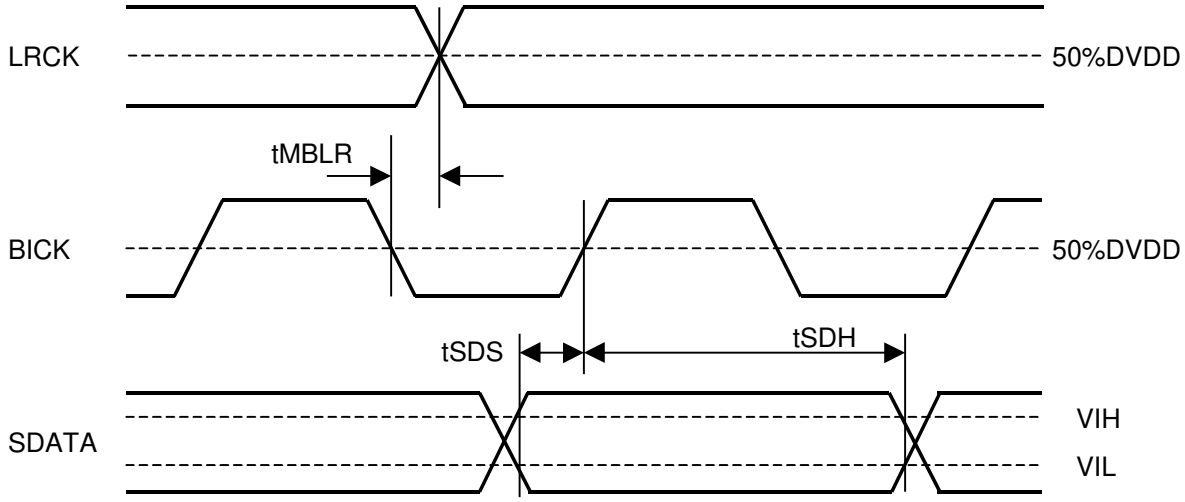


Figure 6. Serial Interface Timing (Master mode)

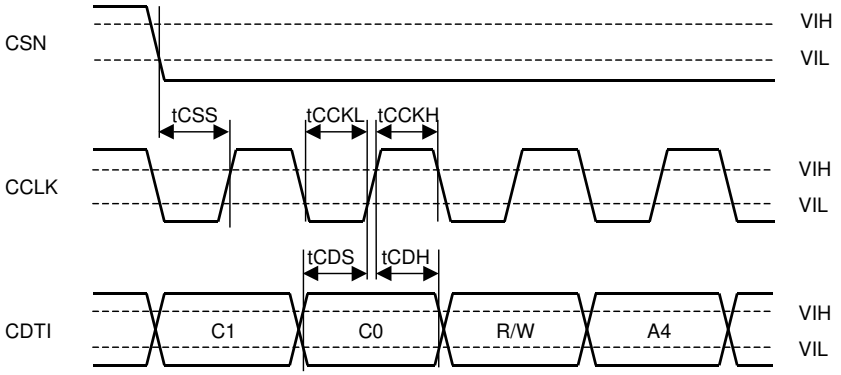


Figure 7. WRITE Command Input Timing

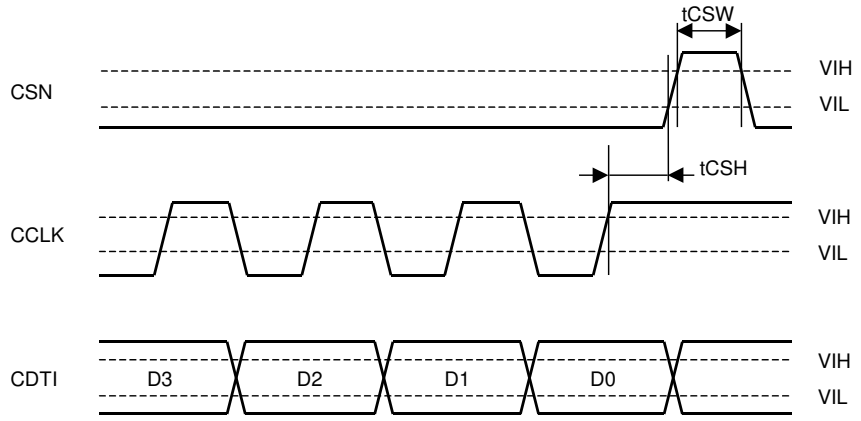


Figure 8. WRITE Data Input Timing

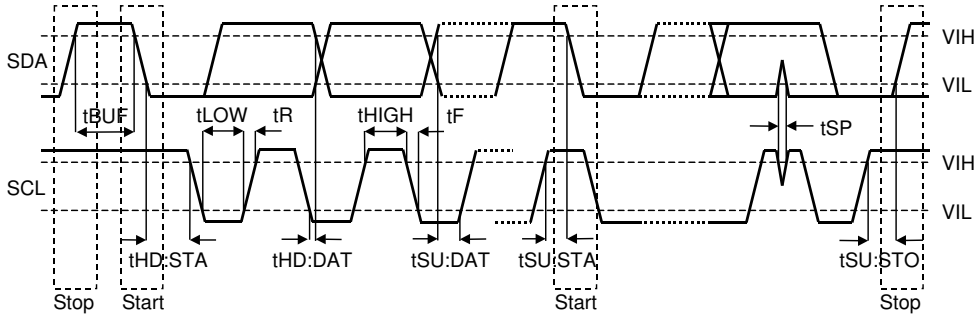


Figure 9. I^2C Bus Mode Timing

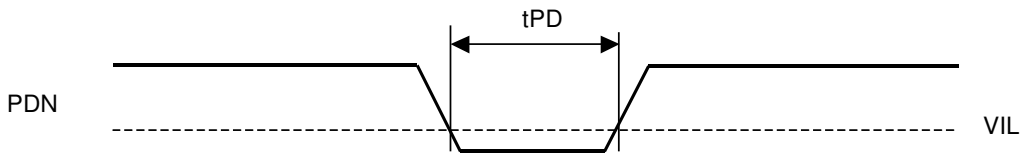


Figure 10. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The AK4370 supports both master and slave modes to interface with external devices. (See Table 1).

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4370 is power-down mode (PDN pin = "L") and exits reset state, the AK4370 is slave mode. After exiting reset state, the AK4370 goes to master mode by changing M/S bit = "1".

When the AK4370 is used by master mode, LRCK and BICK pins are a floating state until M/S bit becomes "1". LRCK and BICK pins of the AK4370 should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	MCKI pin	BICK pin	LRCK pin	Figure	
1	Master Mode	Selected by FS3-0 bits	Output (Selected by BF bit)	Output (1fs)	Figure 11	
0	Slave Mode	Selected by FS3-0 bits	Input (32fs ~ 64fs)	Input (1fs)	Figure 12	default

Table 1. Clock Mode Setting (x: Don't care)

The frequency of master clock inputted to the MCKI pin can be selected FS3-0 bits. (Refer to Table 2)
If the sampling frequency is changed during normal operation of the DAC (PMDAC bit = "1"), the change should occur after the input is muted by SMUTE bit = "1", or the input is set to "0" data.

LRCK and BICK are output from the AK4370 in master mode (Figure 11). The clock input to the MCKI pin should always be present whenever the DAC is in normal operation (PMDAC bit = "1"). If these clocks are not provided, the AK4370 may draw excessive current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the DAC should be placed in power-down mode (PMDAC bit = "0").

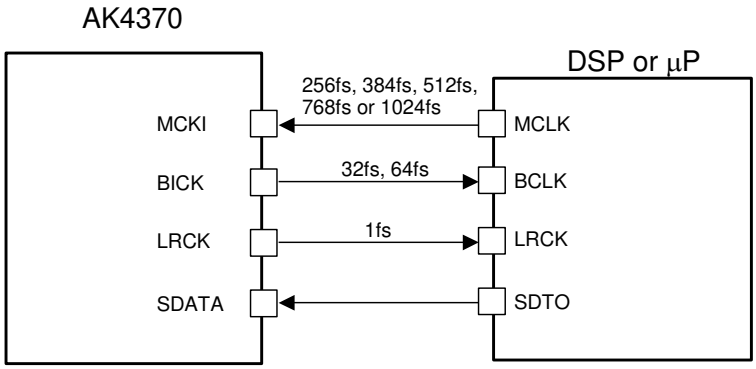


Figure 11. Master Mode

The external clocks required to operate the AK4370 in slave mode are MCKI, LRCK and BICK (Figure 12). The master clock (MCKI) should be synchronized with the sampling clock (LRCK). The phase between these clocks does not matter. All external clocks (MCKI, BICK and LRCK) should always be present whenever the DAC is in normal operation mode (PMDAC bit = "1"). If these clocks are not provided, the AK4370 may draw excessive current and will not operate properly, because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the DAC should be placed in power-down mode (PMDAC bit = "0").

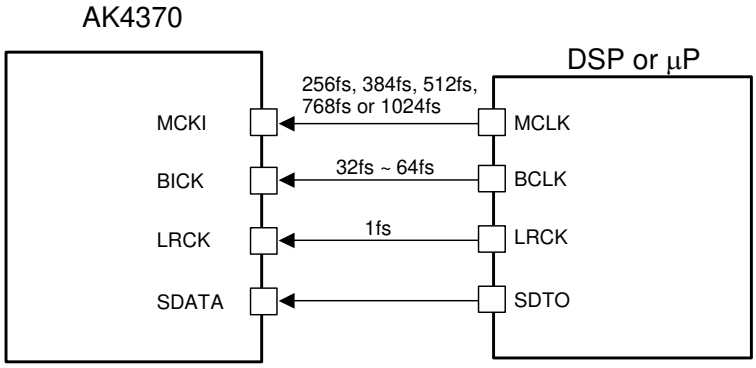


Figure 12. Slave Mode

Mode	FS3	FS2	FS1	FS0	fs	MCKI	
0	0	0	0	0	8kHz ~ 48kHz	256fs	
1	0	0	0	1	8kHz ~ 48kHz	512fs	
2	0	0	1	0	8kHz ~ 24kHz	1024fs	
4	0	1	0	0	8kHz ~ 48kHz	256fs	
5	0	1	0	1	8kHz ~ 48kHz	512fs	
6	0	1	1	0	8kHz ~ 24kHz	1024fs	
8	1	0	0	0	8kHz ~ 48kHz	256fs	Default
9	1	0	0	1	8kHz ~ 48kHz	512fs	
10	1	0	1	0	8kHz ~ 24kHz	1024fs	
12	1	1	0	0	8kHz ~ 48kHz	384fs	
13	1	1	0	1	8kHz ~ 24kHz	768fs	
Others	Others				N/A	N/A	

Table 2. Relationship between Sampling Frequency and MCKI Frequency

	Master Mode (M/S bit = "1")	
	Power Up (PMDAC bit = "1")	Power Down (PMDAC bit = "0")
MCKI pin	Refer to Table 2	Input or fixed to "L" or "H" externally
BICK pin	BF bit = "1": 64fs output BF bit = "0": 32fs output	"L"
LRCK pin	Output	"L"

Table 3. Clock Operation in Master mode

	Slave Mode (M/S bit = "0")	
	Power Up (PMDAC bit = "1")	Power Down (PMDAC bit = "0")
MCKI pin	Refer to Table 2	Input or fixed to "L" or "H" externally
BICK pin	Input	Fixed to "L" or "H" externally
LRCK pin	Input	Fixed to "L" or "H" externally

Table 4. Clock Operation in Slave mode

For low sampling rates, DR and S/N degrade because of the out-of-band noise. DR and S/N are improved by using higher frequency for MCKI. Table 5 shows DR and S/N when the DAC output is to the HP-amp.

MCKI	DR, S/N (BW=20kHz, A-weight)	
	fs=8kHz	fs=16kHz
256fs/384fs/512fs	56dB	75dB
768fs/1024fs	75dB	90dB

Table 5. Relationship between MCKI frequency and DR (and S/N) of HP-amp (2.4V)

■ Serial Data Interface

The AK4370 interfaces with external systems via the SDATA, BICK and LRCK pins. Five data formats are available, selected by setting the DIF2, DIF1 and DIF0 bits (Table 6). Mode 0 is compatible with existing 16-bit DACs and digital filters. Mode 1 is a 20-bit version of Mode 0. Mode 4 is a 24-bit version of Mode 0. Mode 2 is similar to AKM ADCs and many DSP serial ports. Mode 3 is compatible with the I^2S serial data protocol. In Modes 2 and 3 with BICK≥48fs, the following formats are also valid: 16-bit data followed by eight zeros (17th to 24th bits) and 20-bit data followed by four zeros (21st to 24th bits). In all modes, the serial data is MSB first and 2's complement format.

When master mode and BICK=32fs(BF bit = "0"), the AK4370 cannot be set to Mode 1, Mode 2 and Mode4.

Mode	DIF2	DIF1	DIF0	Format	BICK	Figure	
0	0	0	0	0: 16bit, LSB justified	32fs ≤ BICK ≤ 64fs	Figure 13	
1	0	0	1	1: 20bit, LSB justified	40fs ≤ BICK ≤ 64fs	Figure 14	
2	0	1	0	2: 24bit, MSB justified	48fs ≤ BICK ≤ 64fs	Figure 15	Default
3	0	1	1	3: I^2S Compatible	BICK=32fs or 48fs ≤ BICK ≤ 64fs	Figure 16	
4	1	0	0	4: 24bit, LSB justified	48fs ≤ BICK ≤ 64fs	Figure 14	

Table 6. Audio Data Format

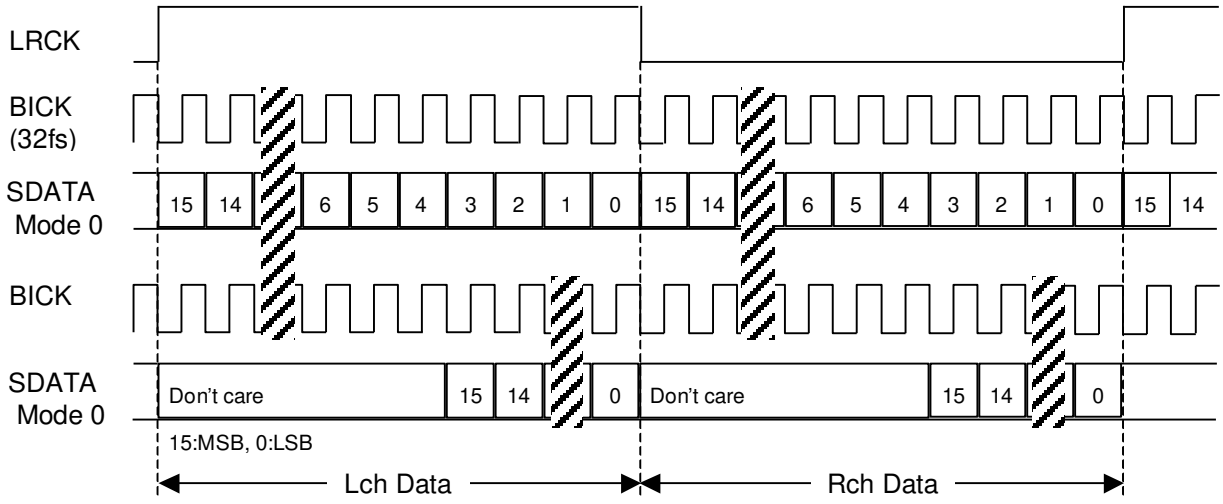


Figure 13. Mode 0 Timing (LRP = BCKP bits = "0")

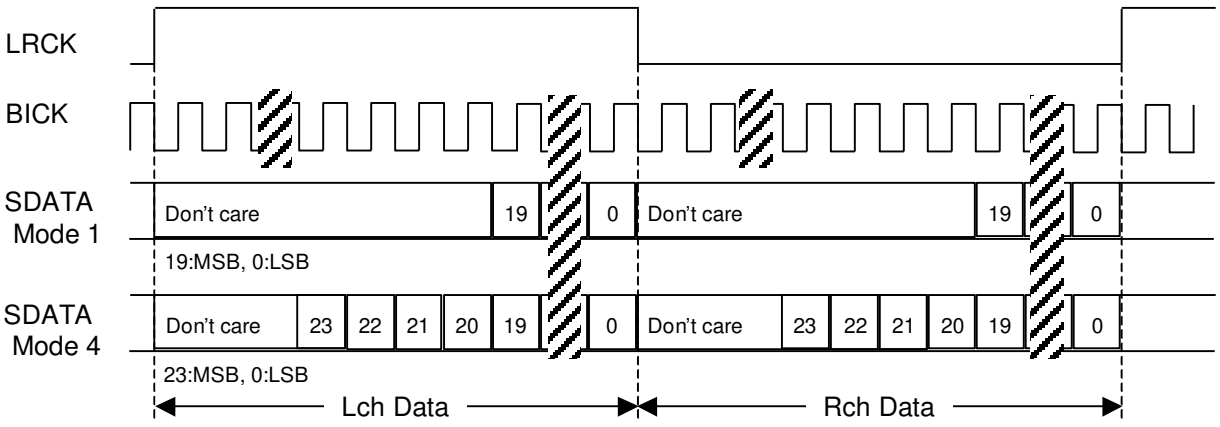


Figure 14. Mode 1, 4 Timing (LRP = BCKP bits = "0")

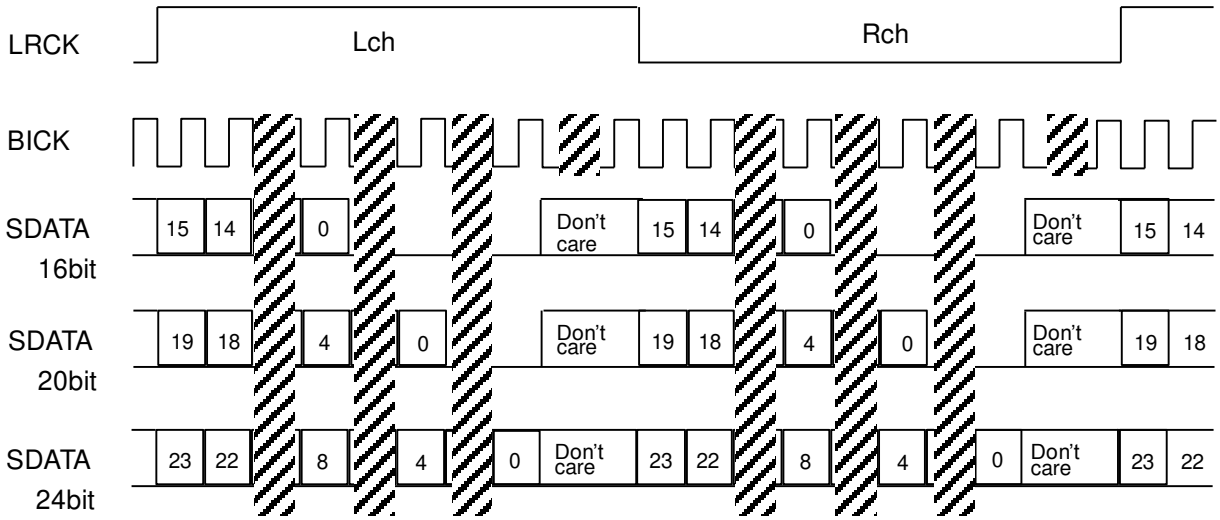


Figure 15. Mode 2 Timing (LRP = BCKP bits = "0")

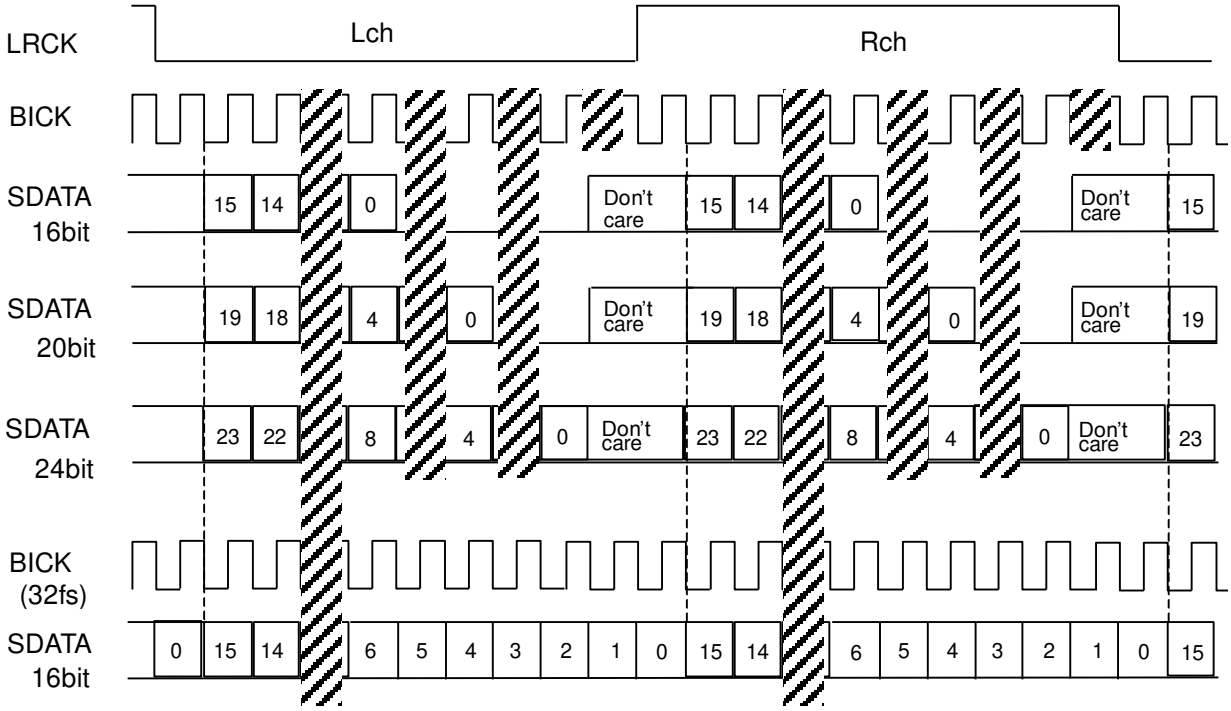


Figure 16. Mode 3 Timing (LRP = BCKP bits = "0")

■ Digital Attenuator

The AK4370 has a channel-independent digital attenuator (256 levels, 0.5dB step). This digital attenuator is placed before the D/A converter. ATTL/R7-0 bits set the attenuation level (0dB to −127dB or MUTE) for each channel (Table 7). At DATTC bit = "1", ATTL7-0 bits control both channel's attenuation levels. At DATTC bit = "0", ATTL7-0 bits control the left channel level and ATTR7-0 bits control the right channel level.

ATTL7-0 ATTR7-0	Attenuation	
FFH	0dB	
FEH	−0.5dB	
FDH	−1.0dB	
FCH	−1.5dB	
:	:	
:	:	
02H	−126.5dB	
01H	−127.0dB	
00H	MUTE (−∞)	Default

Table 7. Digital Volume ATT values

The ATS bit sets the transition time between set values of ATT7-0 bits as either 1061/fs or 7424/fs (Table 8). When the ATS bit = "0", a soft transition between the set values occurs(1062 levels). It takes 1061/fs (24ms@fs=44.1kHz) from FFH(0dB) to 00H(MUTE). The ATTs are 00H when the PMDAC bit is "0". When the PMDAC returns to "1", the ATTs fade to their current value. The digital attenuator is independent of the soft mute function.

ATS	ATT speed		
	0dB to MUTE	1 step	
0	1061/fs	4/fs	Default
1	7424/fs	29/fs	

Table 8. Transition time between set values of ATT7-0 bits

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit goes to "1", the output signal is attenuated by −∞ during the ATT_DATA×ATT transition time (Table 8) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to −∞ after starting the operation, the attenuation is discontinued and is returned to the ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

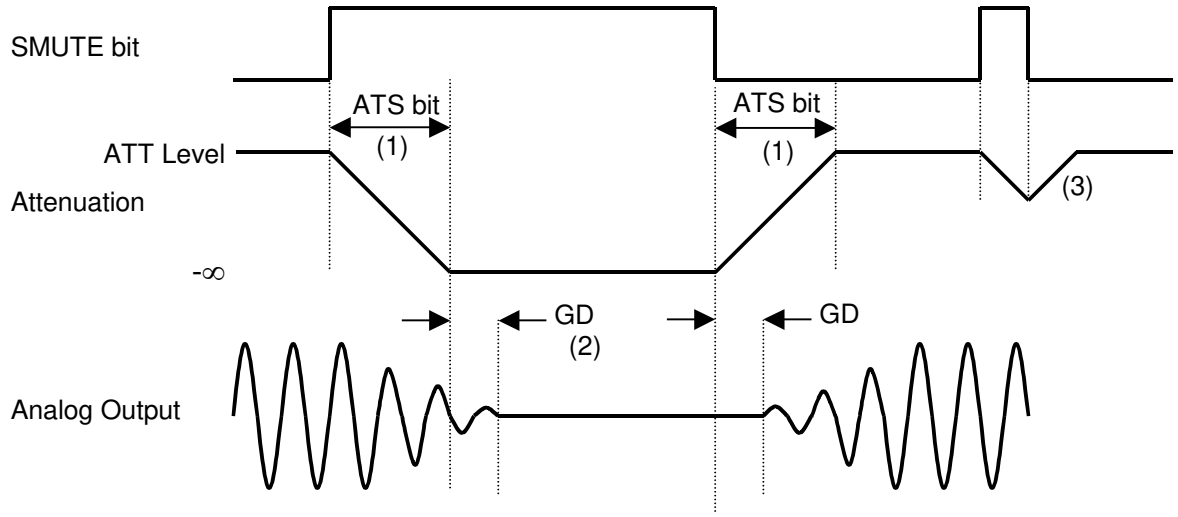


Figure 17. Soft Mute Function

Notes:

(1) ATT_DATA×ATT transition time (Table 8). For example, this time is 3712LRCK cycles (3712/fs) at ATS bit = "1" and ATT_DATA = "128" (-63.5dB).
(2) The analog output corresponding to the digital input has a group delay, GD.
(3) If the soft mute is cancelled before attenuating to −∞ after starting the operation, the attenuation is discontinued and it is returned to the ATT level by the same cycle.

■ De-emphasis Filter

The AK4370 includes a digital de-emphasis filter (tc = 50/15μs), using an IIR filter corresponding to three sampling frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter is enabled by setting DEM1-0 bits (Table 9).

DEM1 bit	DEM0 bit	De-emphasis	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 9. De-emphasis Filter Frequency Select

■ Bass Boost Function

By controlling the BST1-0 bits, a low frequency boost signal can be output from DAC. The setting value is common for both channels (Table 10).

BST1 bit	BST0 bit	BOOST	
0	0	OFF	Default
0	1	MIN	
1	0	MID	
1	1	MAX	

Table 10. Low Frequency Boost Select

■ Digital Mixing Function

MONO1-0 bits select the digital data mixing for the DAC (Table 11).

MONO1 bit	MONO0 bit	Lch	Rch	
0	0	L	R	Default
0	1	L	L	
1	0	R	R	
1	1	(L+R)/2	(L+R)/2	

Table 11. Mixer Setting

■ System Reset

PDN pin should be held to “L” upon power-up. The 4370 should be reset by bringing PDN pin “L” for 150ns or more. All of the internal register values are initialized by the system reset. After exiting reset, VCOM, DAC, HPL, HPR, LOUT and ROUT switch to the power-down state. The contents of the control register are maintained until the reset is completed.

The DAC exits reset and power down states by MCKI after the PMDAC bit is changed to “1”. The DAC is in power-down mode until MCKI is input.

■ Headphone Output (HPL, HPR pins)

The power supply voltage for the headphone-amp is supplied from the HVDD pin and is centered on the MUTET voltage. The headphone-amp output load resistance is 16Ω (min). When the MUTEN bit is "1" at PMHPL=PMHPR= "1", the common voltage rises to 0.475 x AVDD. When the MUTEN bit is "0", the common voltage of the headphone-amp falls and the outputs (HPL and HPR pins) go to VSS1.

t_r: Rise Time up to VCOM/2	70k x C (typ)
t_f: Fall Time down to VCOM/2	60k x C (typ)

Table 12. Headphone-Amp Rise/Fall Time

[Example] : Capacitor between the MUTET pin and ground = 1μF:
Rise time up to VCOM/2: t_r = 70k x 1μ = 70ms (typ).
Fall time down to VCOM/2: t_f = 60k x 1μ = 60ms (typ).

When the PMHPL and PMHPR bits are "0", the headphone-amp is powered-down, and the outputs (HPL and HPR pins) go to VSS1.

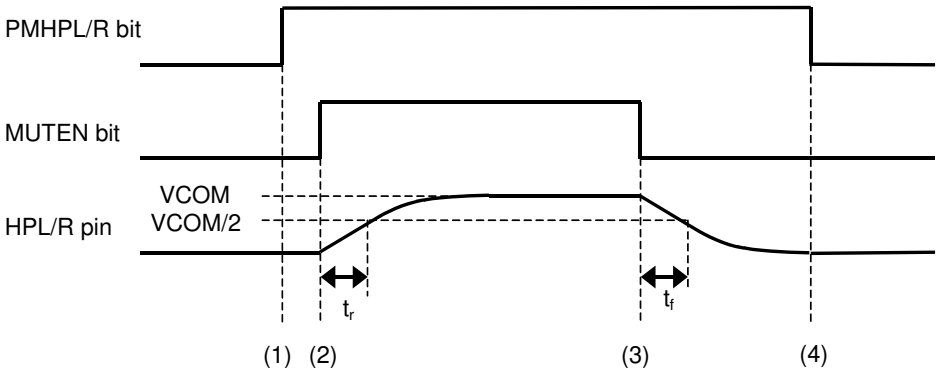


Figure 18. Power-up/Power-down Timing for the Headphone-Amp

(1) Headphone-amp power-up (PMHPL and PMHPR bits = "1"). The outputs are still at VSS1.
(2) Headphone-amp common voltage rises up (MUTEN bit = "1"). Common voltage of the headphone-amp is rising. This rise time depends on the capacitor value connected with the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ) when the capacitor value on MUTET pin is "C".
(3) Headphone-amp common voltage falls down (MUTEN bit = "0"). Common voltage of the headphone-amp is falling to VSS1. This fall time depends on the capacitor value connected with the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ) when the capacitor value on MUTET pin is "C".
(4) Headphone-amp power-down (PMHPL, PMHPR bits = "0"). The outputs are at VSS1. If the power supply is switched off or the headphone-amp is powered-down before the common voltage goes to VSS1, some pop noise may occur.

< External Circuit of Headphone-Amp >

The cut-off frequency of the headphone-amp output depends on the external resistor and capacitor used. Table 13 shows the cut off frequency and the output power for various resistor/capacitor combinations. The headphone impedance R_L is 16Ω. Output powers are shown at AVDD = 2.4, 3.0 and 3.3V. The output voltage of the headphone-amp is 0.48 x AVDD (Vpp) @−3dBFS.

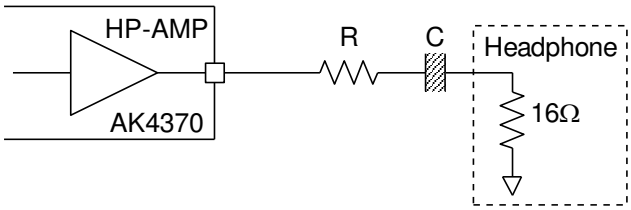


Figure 19. External Circuit Example of Headphone

R [Ω]	C [μF]	fc [Hz] BOOST=OFF	fc [Hz] BOOST=MIN	Output Power [mW]		
				2.4V	3.0V	3.3V
0	220	45	17	21	33	40
	100	100	43			
6.8	100	70	28	10	16	20
	47	149	78			
16	100	50	19	5	8	10
	47	106	47			

Table 13. Relationship of external circuit, output power and frequency response

< Wired OR with External Headphone-Amp >

When PMVCM=PMHPL=PMHPR bits = "0" and HPZ bit = "1", Headphone-amp is powered-down and HPL/R pins are pulled-down to VSS1 by 200kΩ (typ). In this setting, it is available to connect headphone-amp of AK4370 and external single supply headphone-amp by "wired OR".

PMVCM	PMHPL/R	HPMTN	HPZ	Mode	HPL/R pins	
x	0	x	0	Power-down & Mute	VSS1	Default
0	0	x	1	Power-down	Pull-down by 200kΩ	
1	1	0	x	Mute	VSS1	
1	1	1	x	Normal Operation	Normal Operation	

Table 14. HP-Amp Mode Setting (x: Don't care)

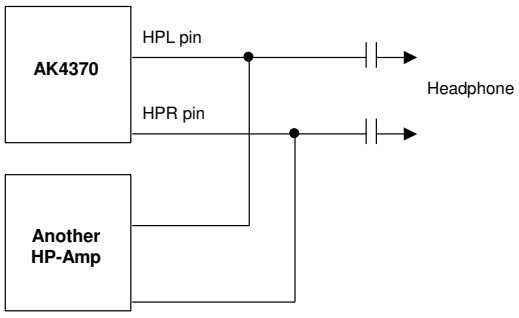


Figure 20. Wired OR with External HP-Amp