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Asahi KASEI
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AK4371

DAC with built-in PLL & HP-AMP

GENERAL DESCRIPTION

The AK4371 is 24-bit DAC with an integrated PLL and headphone amplifier. The PLL input frequency is synchronized to typical mobile phone clock frequencies. The AK4371 features an analog mixing circuit that allows easy interfacing in mobile phone and portable communication designs. The integrated headphone amplifier features “pop-noise free” power-on/off, a mute control, and it delivers 40mW of power into 16Ω. The AK4371 is packaged in a 32-pin QFN (4mm×4mm) package, deal for portable applications.

FEATURE

- **Multi-bit ΔΣ DAC**
- **Sampling Rate**
  - **8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz and 48kHz**
- **On chip perfect filtering 8 times FIR interpolator**
  - **Passband: 20kHz**
  - **Passband Ripple: ±0.02dB**
  - **Stopband Attenuation: 54dB**
- **Digital De-emphasis Filter: 32kHz, 44.1kHz and 48kHz**
- **System Clock**
  - **PLL Mode (MCKI): 27MHz, 26MHz, 19.8MHz, 19.68MHz, 19.2MHz, 15.36MHz, 14.4MHz, 13MHz, 12MHz and 11.2896MHz**
  - **PLL Mode (BICK or LRCK): 64fs, 32fs or fs**
  - **EXT Mode: 256fs/384fs/512fs/768fs/1024fs**
  - **Input Level: AC Couple Input Available**
- **Audio I/F Format: MSB First, 2’s Complement**
  - **I^2S, 24bit MSB justified, 24bit/20bit/16bit LSB justified**
  - **Master/Slave Mode**
- **Digital Mixing: LR, LL, RR, (L+R)/2**
- **Bass Boost Function**
- **Digital ATT**
- **Analog Mixing Circuit: 6 Inputs (Single-ended or Full-differential)**
- **Stereo Lineout**
  - **S/N: 90dB@3.3V**
  - **Output Volume: +6 to –24dB (or 0 to –30dB), 2dB step**
- **Mono Hands-free Output**
  - **Output Power: 0.8mW @ 600Ω 3.3V**
  - **Output Volume: +6 to –24dB (or 0 to –30dB), 2dB step**
- **Headphone Amplifier**
  - **Output Power: 40mW x 2ch @16Ω, 3.3V**
  - **S/N: 92dB@3.3V**
  - **Pop Noise Free at Power-ON/OFF and Mute**
  - **Output Volume: 0 ~ –63dB & +12/+6/0 dB Gain**
    1.5dB step (0 ~ –30dB), 3dB step (–30 ~ –63dB)
- **μP Interface: 3-wire/I^2C**
- **Power Supply: 1.6V ~ 3.6V**
- **Power Supply Current: 3.8mA @1.8V (6.8mW, DAC+HP, No output)**
- **Ta: –30 ~ 85°C**
- **Small Package: 32pin QFN (4mm x 4mm, 0.4mm pitch)**
- **Register Compatible with AK4368**

■ Block Diagram

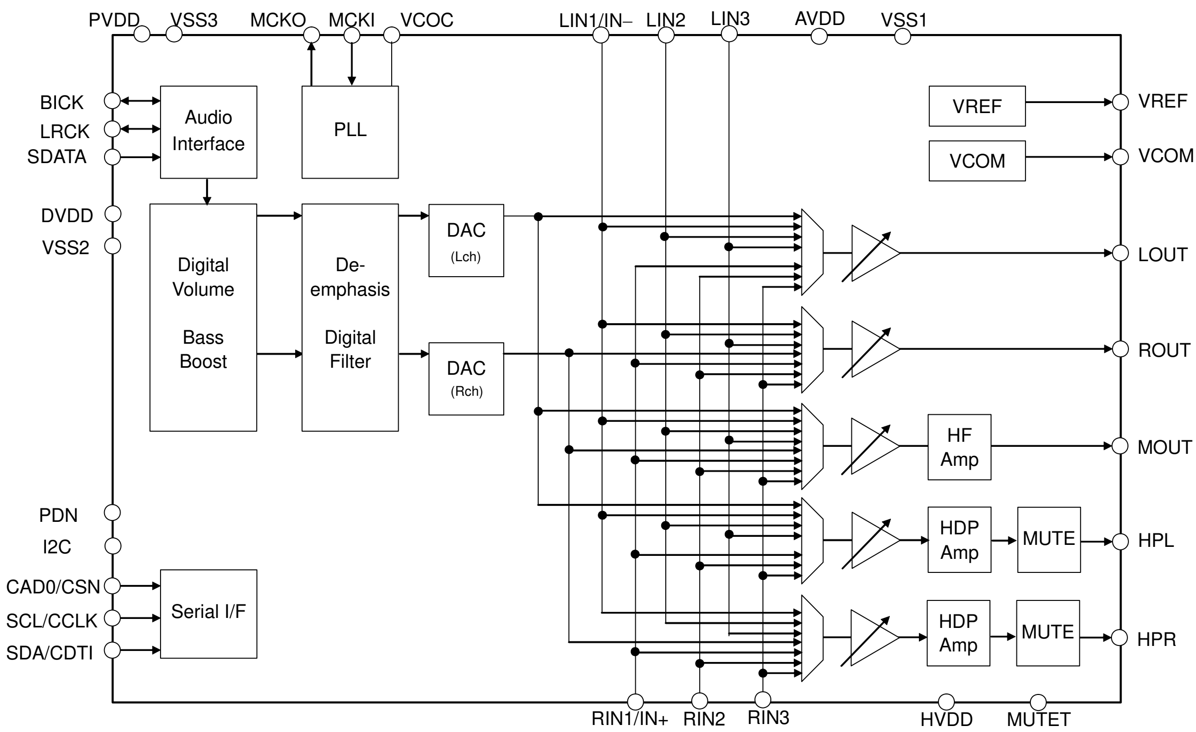
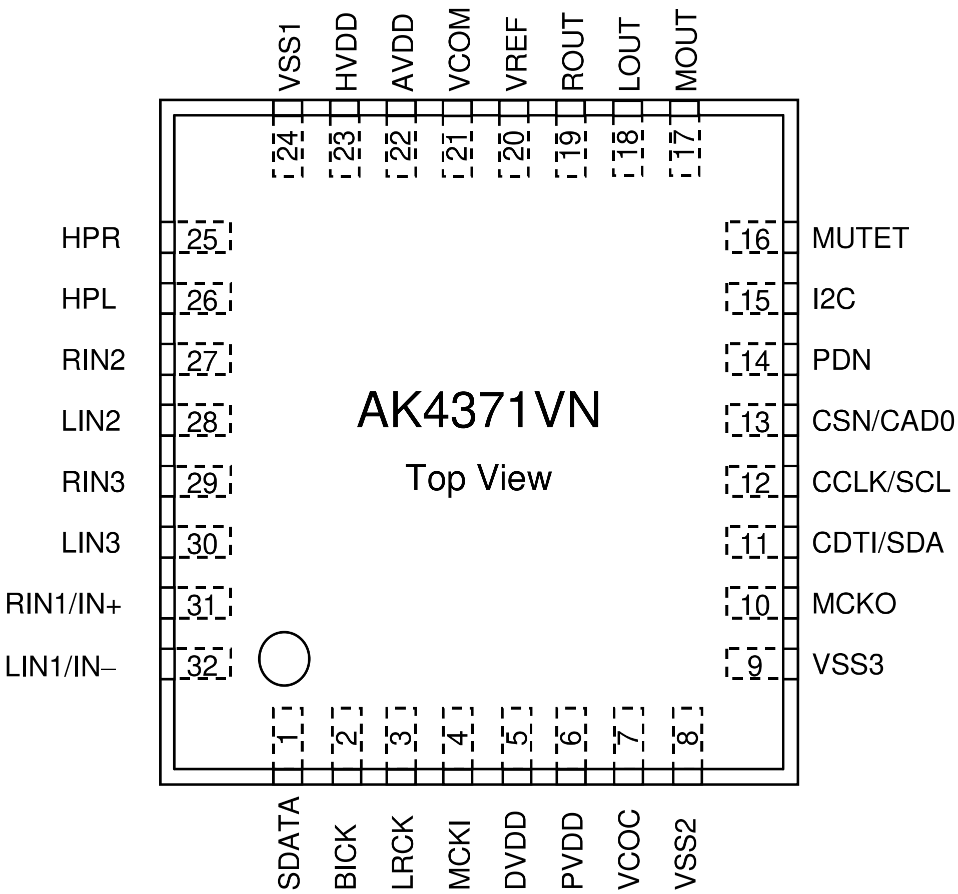


Figure 1. Block Diagram

■ Ordering Information

AK4371VN	−30 ~ +85°C	32pin QFN (0.4mm pitch)
AKD4371	Evaluation board for AK4371	

■ Pin Layout



■ Comparison with AK4368

1 Function

Function	AK4368	AK4371
Analog Mixing	1-Stereo + 1-Mono Single-ended Input	3-Stereo Single-ended or Full-differential Input
PLL Reference Clock	MCKI	MCKI/BICK/LRCK
MCKI at EXT Mode	256fs/512fs/1024fs, 12.288MHz(max)	256fs/384fs/512fs/768fs/1024fs, 24.576MHz(max)
Internal VREF	No	Yes
Handsfree Amp	No	Yes
HP-Amp Output Volume	No	0 to –63dB & +12/+6/0dB 1.5dB step (0 to –30dB) 3dB step (–30 to –63dB)
HP-Amp Hi-Z Setting	No	Yes
3D Enhancement	Yes	No
ALC	Yes	No
Package	41BGA (4mm x 4mm, 0.5mm pitch)	32QFN (4mm x 4mm, 0.4mm pitch)

2 Register (difference from AK4368)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 0	PMVREF	PMPLL	PMLO	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
01H	PLL Control	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
02H	Clock Control	PLL4	0	M/S	MCKAC	BF	PS0	PS1	MCKO
03H	Mode Control 0	0	MONO1	MONO0	BCKP	LRP	DIF2	DIF1	DIF0
04H	Mode Control 1	ATS	DATTC	LMUTE	SMUTE	BST1	BST0	DEM1	DEM0
05H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
06H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
07H	Headphone Out Select 0	HPG1	HPG0	LIN2HR	LIN2HL	RIN1HR	LIN1HL	DARHR	DALHL
08H	Lineout Select 0	0	LOG	LIN2R	LIN2L	RIN1R	LIN1L	DARR	DALL
09H	Lineout ATT	0	0	0	0	ATTS3	ATTS2	ATTS1	ATTS0
0AH	Reserved	~~REF7~~	~~REF6~~	~~REF5~~	~~REF4~~	~~REF3~~	~~REF2~~	~~REF1~~	~~REF0~~
0BH	Reserved	0	0	~~ALC~~	~~ROTM1~~	~~ROTM0~~	~~LMAT1~~	~~LMAT0~~	~~RATT~~
0CH	Reserved	0	0	0	0	~~DP1~~	~~DP0~~	~~3D1~~	~~3D0~~
0DH	Headphone Out Select 1	RIN3HR	RIN3HL	LIN3HR	LIN3HL	RIN2HR	RIN2HL	LIN1HR	RIN1HL
0EH	Headphone ATT	0	HPZ	HMUTE	ATTH4	ATTH3	ATTH2	ATTH1	ATTH0
0FH	Lineout Select	RIN3R	RIN3L	LIN3R	LIN3L	RIN2R	RIN2L	LIN1R	RIN1L
10H	Mono Mixing	0	0	L3M	L3HM	L2M	L2HM	L1M	L1HM
11H	Differential Select	0	0	0	0	0	LDIFM	LDIFH	LDIF
12H	MOUT Select	RIN3M	LIN3M	RIN2M	LIN2M	RIN1M	LIN1M	DARM	DALM
13H	MOUT ATT	0	PMMO	MOG	MMUTE	ATTM3	ATTM2	ATTM1	ATTM0

(orange) These bits are added in the AK4371.
(cyan) These bits are deleted in the AK4371.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	SDATA	I	Audio Serial Data Input Pin
2	BICK	I/O	Audio Serial Data Clock Pin
3	LRCK	I/O	Input / Output Channel Clock Pin
4	MCKI	I	External Master Clock Input Pin
5	DVDD	-	Digital Power Supply Pin, 1.6 ~ 3.6V
6	PVDD	-	Power Supply for PLL, 1.6 ~ 3.6V. Normally connected to AVDD.
7	VCOC	O	Output for Loop Filter of PLL Circuit This pin must be connected to VSS3 with one resistor and one capacitor in series.
8	VSS2	-	Ground Pin
9	VSS3	-	Ground Pin
10	MCKO	O	Master Clock Output Pin
11	SDA	I/O	Control Data Input/Output Pin (I2C mode : I2C pin = "H")
	CDTI	I	Control Data Input Pin (3-wire serial mode : I2C pin = "L")
12	SCL	I	Control Data Clock Pin (I2C mode : I2C pin = "H")
	CCLK	I	Control Data Clock Pin (3-wire serial mode : I2C pin = "L")
13	CAD0	I	Chip Address 0 Select Pin (I2C mode : I2C pin = "H")
	CSN	I	Chip Select Pin (3-wire serial mode : I2C pin = "L")
14	PDN	I	Power-down & Reset When "L", the AK4371 is in power-down mode and is held in reset. The AK4371 must always be reset upon power-up.
15	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire Serial
16	MUTET	O	Mute Time Constant Control pin Connected to VSS1 pin with a capacitor for mute time constant.
17	MOUT	O	Mono Signal Output Pin
18	LOUT	O	Lch Stereo Line Output Pin
19	ROUT	O	Rch Stereo Line Output Pin
20	VREF	O	Reference Voltage Output Pin Normally connected to VSS1 pin with a 0.22μF electrolytic capacitor.
21	VCOM	O	Common Voltage Output Pin Normally connected to VSS1 pin with a 2.2μF electrolytic capacitor.
22	AVDD	-	Analog Power Supply Pin, 1.6 ~ 3.6V
23	HVDD	-	Power Supply Pin for Headphone Amp, 1.6 ~ 3.6V
24	VSS1	-	Ground Pin
25	HPR	O	Rch Headphone Amp Output
26	HPL	O	Lch Headphone Amp Output
27	RIN2	I	Rch Analog Input 2 Pin
28	LIN2	I	Lch Analog Input 2 Pin
29	RIN3	I	Rch Analog Input 3 Pin
30	LIN3	I	Lch Analog Input 3 Pin
31	RIN1	I	Rch Analog Input 1 Pin (LDIF bit ="0" : Single-ended Input)
	IN+	I	Positive Line Input Pin (LDIF bit ="1" : Full-differential Input)
32	LIN1	I	Rch Analog Input 1 Pin (LDIF bit ="0" : Single-ended Input)
	IN−	I	Negative Line Input Pin (LDIF bit ="1" : Full-differential Input)

Note 1. All digital input pins (I2C, SDA/CDTI, SCL/CCLK, CAD0/CSN, SDATA, LRCK, BICK, MCKI, PDN) must not be left floating. The MCKI pin can be left floating only when the PDN pin = "L".

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LOUT, ROUT, MOUT, MUTET, HPR, HPL, RIN3, LIN3, RIN2, LIN2, RIN1/IN+, LIN1/IN−	These pins must be open.
Digital	MCKI	This pin must be connected to VSS2.
	MCKO	This pin must be open.

ABSOLUTE MAXIMUM RATING

(VSS1=VSS2=VSS3=0V; Note 2, Note 3)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	−0.3	4.6	V
	Digital	DVDD	−0.3	4.6	V
	PLL	PVDD	−0.3	4.6	V
	HP-Amp	HVDD	−0.3	4.6	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 4)		VINA	−0.3	(AVDD+0.3) or 4.6	V
Digital Input Voltage (Note 5)		VIND	−0.3	(DVDD+0.3) or 4.6	V
Ambient Temperature		Ta	−30	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 2. All voltages with respect to ground.

Note 3. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.

Note 4. LIN1/IN−, RIN1/IN+, LIN2, RIN2, LIN3 and RIN3 pins. Max is smaller value between (AVDD+0.3)V and 4.6V.

Note 5. SDA/CDTI, SCL/CCLK, CAD0/CSN, SDATA, LRCK, BICK, MCKI, PDN and I2C pins. Max is smaller value between (DVDD+0.3)V and 4.6V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS1=VSS2=VSS3=0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 6)	Analog	AVDD	1.6	2.4	3.6	V
	Digital (Note 7)	DVDD	1.6	2.4	(AVDD+0.2) or 3.6	V
	PLL	PVDD	1.6	2.4	3.6	V
	HP-Amp	HVDD	1.6	2.4	3.6	V
	Difference1	AVDD−PVDD	−0.3	0	+0.3	V
	Difference2	AVDD−HVDD	−0.3	0	+0.3	V

Note 2. All voltages with respect to ground.

Note 6. When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. When the AK4371 is powered-down, DVDD should be powered-down at the same time or later than AVDD. When AVDD and HVDD are supplied separately, AVDD should be powered-up at the same time or earlier than HVDD. When the AK4371 is powered-down, AVDD should be powered-down at the same time or later than HVDD.

Note 7. Max is smaller value between (AVDD+0.2)V and 3.6V.

* AKEMD assumes no responsibility for usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=PVDD=DVDD=HVDD=2.4V, VSS1=VSS2=VSS3=0V; fs=44.1kHz; EXT mode; BOOST OFF; Slave Mode; Signal Frequency =1kHz; Measurement band width=20Hz ~ 20kHz; Headphone-Amp: Load impedance is a serial connection with R_L=16Ω and C_L=220μF (Figure 57) unless otherwise specified)

Parameter			min	typ	max	Units
DAC Resolution			-	-	24	bit
Headphone-Amp: (HPL/HPR pins) (Note 8)						
	Analog Output Characteristics					
	THD+N	–3dBFS Output, 2.4V, Po=10mW@16Ω	-	–50	–40	dB
		0dBFS Output, 3.3V, Po=40mW@16Ω	-	–20	-	dB
	D-Range	–60dBFS Output, A-weighted, 2.4V	82	90	-	dB
		–60dBFS Output, A-weighted, 3.3V	-	92	-	dB
	S/N	A-weighted, 2.4V	82	90	-	dB
		A-weighted, 3.3V	-	92	-	dB
	Interchannel Isolation		60	80	-	dB
	DC Accuracy					
	Interchannel Gain Mismatch		-	0.3	0.8	dB
	Gain Drift		-	200	-	ppm/°C
	Load Resistance (Note 9)		16	-	-	Ω
	Load Capacitance		-	-	300	pF
	Output Voltage	–3dBFS Output (Note 10)	1.04	1.16	1.28	Vpp
		0dBFS Output, 3.3V, Po=40mW@16Ω	-	0.8	-	Vrms
Output Volume: (HPL/HPR pins)						
	Step Size (HPG1-0 bits = “00”)	0 ~ –30dB	0.1	1.5	2.9	dB
		–30 ~ –63dB	0.1	3	5.9	dB
	Gain Control Range (HPG1-0 bits = “00”)	Max (ATT4-0 bits = “00H”)	-	0	-	dB
		Min (ATT4-0 bits = “1FH”)	-	–63	-	dB
Stereo Line Output: (LOUT/ROUT pins, R_L=10kΩ) (Note 11)						
	Analog Output Characteristics:					
	THD+N (0dBFS Output)		-	–60	–50	dB
	S/N	A-weighted, 2.4V	80	87	-	dB
		A-weighted, 3.3V	-	90	-	dB
	DC Accuracy					
	Gain Drift		-	200	-	ppm/°C
	Load Resistance (Note 9)		10	-	-	kΩ
	Load Capacitance		-	-	25	pF
	Output Voltage (0dBFS Output) (Note 12)		1.32	1.47	1.61	Vpp
Output Volume: (LOUT/ROUT pins)						
	Step Size		1	2	3	dB
	Gain Control Range (LOG1-0 bit = “0”)	Max (ATTS3-0 bits = “FH”)	-	0	-	dB
		Min (ATTS3-0 bits = “0H”)	-	–30	-	dB

Note 8. DALHL=DARHR bits = “1”, LIN1HL=RIN1HL=LIN2HL=RIN2HL=LIN3HL=RIN3HL =LIN1HR=RIN1HR=LIN2HR=RIN2HR=LIN3HR=RIN3HR bits = “0”.

Note 9. AC load.

Note 10. Output voltage is proportional to AVDD voltage.
When PMVREF bit = “0”, Vout = 0.48 x AVDD(typ)@–3dBFS.
When PMVREF bit = “1”, Vout = 0.52 x AVDD(typ)@0dBFS.

Note 11. DALL=DARR bits = “1”, LIN1L=RIN1L=LIN2L=RIN2L=LIN3L=RIN3L =LIN1R=RIN1R=LIN2R=RIN2R=LIN3R=RIN3R bits = “0”

Note 12. Output voltage is proportional to AVDD voltage.
When PMVREF bit = “0”, Vout = 0.61 x AVDD(typ)@0dBFS.
When PMVREF bit = “1”, Vout = 0.46 x AVDD(typ)@0dBFS

Parameter			min	typ	max	Units
Mono Handsfree Output: (MOUT pin, R_L=600Ω) (Note 13)						
	Analog Output Characteristics:					
	THD+N (0dBFS Output)		-	–60	–50	dB
	S/N	A-weighted, 2.4V	80	87	-	dB
		A-weighted, 3.3V	-	90	-	dB
	DC Accuracy					
	Gain Drift		-	200	-	ppm/°C
	Load Resistance (Note 9)		600	-	-	Ω
	Load Capacitance		-	-	25	pF
	Output Voltage (0dBFS Output) (Note 14)		1.32	1.47	1.61	Vpp
Output Volume: (MOUT pin)						
	Step Size		1	2	3	dB
	Gain Control Range (MOG1-0 bit = "0")	Max (ATTM3-0 bits = "FH")	-	0	-	dB
		Min (ATTM3-0 bits = "0H")	-	–30	-	dB

Note 13. DALM=DARM bits = "1", LIN1M=RIN1M=LIN2M=RIN2M=LIN3M=RIN3M bits = "0"
Note 9. AC load.
Note 14. Output voltage is proportional to AVDD voltage.
When PMVREF bit = "0", Vout = 0.61 x AVDD(typ)@0dBFS.
When PMVREF bit = "1", Vout = 0.46 x AVDD(typ)@0dBFS

Parameter	min	typ	max	Units
LINEIN: (LIN1/RIN1/LIN2/RIN2/LIN3/RIN3 pins)				
Analog Input Characteristics				
Input Resistance (Figure 25, Figure 26, Figure 27, Figure 28)				
LIN1 pin				
LIN1HL=LIN1HR=LIN1L=LIN1R=LIN1M bits = “1”	14	20	-	kΩ
LIN1HL bit = “1”, LIN1HR=LIN1L=LIN1R=LIN1M bits = “0”	-	100	-	kΩ
LIN1HR bit = “1”, LIN1HL=LIN1L=LIN1R=LIN1M bits = “0”	-	100	-	kΩ
LIN1L bit = “1”, LIN1HL=LIN1HR=LIN1R=LIN1M bits = “0”	-	100	-	kΩ
LIN1R bit = “1”, LIN1HL=LIN1HR=LIN1L=LIN1M bits = “0”	-	100	-	kΩ
LIN1M bit = “1”, LIN1HL=LIN1HR=LIN1L=LIN1R bits = “0”	-	100	-	kΩ
RIN1 pin				
RIN1HL=RIN1HR=RIN1L=RIN1R=RIN1M bits = “1”	14	20	-	kΩ
RIN1HL bit = “1”, RIN1HR=RIN1L=RIN1R=RIN1M bits = “0”	-	100	-	kΩ
RIN1HR bit = “1”, RIN1HL=RIN1L=RIN1R=RIN1M bits = “0”	-	100	-	kΩ
RIN1L bit = “1”, RIN1HL=RIN1HR=RIN1R=RIN1M bits = “0”	-	100	-	kΩ
RIN1R bit = “1”, RIN1HL=RIN1HR=RIN1L=RIN1M bits = “0”	-	100	-	kΩ
RIN1M bit = “1”, RIN1HL=RIN1HR=RIN1L=RIN1R bits = “0”	-	100	-	kΩ
LIN2 pin				
LIN2HL=LIN2HR=LIN2L=LIN2R=LIN2M bits = “1”	14	20	-	kΩ
LIN2HL bit = “1”, LIN2HR=LIN2L=LIN2R=LIN2M bits = “0”	-	100	-	kΩ
LIN2HR bit = “1”, LIN2HL=LIN2L=LIN2R=LIN2M bits = “0”	-	100	-	kΩ
LIN2L bit = “1”, LIN2HL=LIN2HR=LIN2R=LIN2M bits = “0”	-	100	-	kΩ
LIN2R bit = “1”, LIN2HL=LIN2HR=LIN2L=LIN2M bits = “0”	-	100	-	kΩ
LIN2M bit = “1”, LIN2HL=LIN2HR=LIN2L=LIN2R bits = “0”	-	100	-	kΩ
RIN2 pin				
RIN2HL=RIN2HR=RIN2L=RIN2R=RIN2M bits = “1”	14	20	-	kΩ
RIN2HL bit = “1”, RIN2HR=RIN2L=RIN2R=RIN2M bits = “0”	-	100	-	kΩ
RIN2HR bit = “1”, RIN2HL=RIN2L=RIN2R=RIN2M bits = “0”	-	100	-	kΩ
RIN2L bit = “1”, RIN2HL=RIN2HR=RIN2R=RIN2M bits = “0”	-	100	-	kΩ
RIN2R bit = “1”, RIN2HL=RIN2HR=RIN2L=RIN2M bits = “0”	-	100	-	kΩ
RIN2M bit = “1”, RIN2HL=RIN2HR=RIN2L=RIN2R bits = “0”	-	100	-	kΩ
LIN3 pin				
LIN3HL=LIN3HR=LIN3L=LIN3R=LIN3M bits = “1”	14	20	-	kΩ
LIN3HL bit = “1”, LIN3HR=LIN3L=LIN3R=LIN3M bits = “0”	-	100	-	kΩ
LIN3HR bit = “1”, LIN3HL=LIN3L=LIN3R=LIN3M bits = “0”	-	100	-	kΩ
LIN3L bit = “1”, LIN3HL=LIN3HR=LIN3R=LIN3M bits = “0”	-	100	-	kΩ
LIN3R bit = “1”, LIN3HL=LIN3HR=LIN3L=LIN3M bits = “0”	-	100	-	kΩ
LIN3M bit = “1”, LIN3HL=LIN3HR=LIN3L=LIN3R bits = “0”	-	100	-	kΩ
RIN3 pin				
RIN3HL=RIN3HR=RIN3L=RIN3R=RIN3M bits = “1”	14	20	-	kΩ
RIN3HL bit = “1”, RIN3HR=RIN3L=RIN3R=RIN3M bits = “0”	-	100	-	kΩ
RIN3HR bit = “1”, RIN3HL=RIN3L=RIN3R=RIN3M bits = “0”	-	100	-	kΩ
RIN3L bit = “1”, RIN3HL=RIN3HR=RIN3R=RIN3M bits = “0”	-	100	-	kΩ
RIN3R bit = “1”, RIN3HL=RIN3HR=RIN3L=RIN3M bits = “0”	-	100	-	kΩ
RIN3M bit = “1”, RIN3HL=RIN3HR=RIN3L=RIN3R bits = “0”	-	100	-	kΩ
Gain				
LIN1/LIN2/LIN3/RIN1/RIN2/RIN3 → LOUT/ROUT	–1	0	+1	dB
LIN1/LIN2/LIN3/RIN1/RIN2/RIN3 → HPL/HPR	–0.05	+0.95	+1.95	dB
LIN1/LIN2/LIN3/RIN1/RIN2/RIN3 → MOUT	–1	0	+1	dB

Parameter	min	typ	max	Units
Power Supplies				
Power Supply Current				
Normal Operation (PDN pin = "H") (Note 15)				
AVDD+PVDD+DVDD	-	3.8	5.5	mA
HVDD	-	1.2	2.5	mA
Power-Down Mode (PDN pin = "L") (Note 16)	-	1	100	μA

Note 15. PMDAC=PMHPL=PMHPR=PMLO bits = "1", MUTEN bit = "1", PMMO=MCKO bits = "0", HP-Amp no output.
PMDAC=PMHPL=PMHPR= "1", PMLO=PMMO bits = "0", AVDD+PVDD+DVDD+HVDD=4.0mA (typ) @2.4V, 3.8mA (typ) @1.8V.

Note 16. All digital input pins are fixed to VSS2.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=PVDD=HVDD=1.6 ~ 3.6V; fs=44.1kHz; De-emphasis = "OFF")

Parameter			Symbol	min	typ	max	Units
DAC Digital Filter: (Note 17)							
Passband (Note 18)		–0.05dB	PB	0	-	20.0	kHz
		–6.0dB		-	22.05	-	kHz
Stopband (Note 18)			SB	24.1	-	-	kHz
Passband Ripple			PR	-	-	±0.02	dB
Stopband Attenuation			SA	54	-	-	dB
Group Delay (Note 19)			GD	-	22	-	1/fs
Group Delay Distortion			ΔGD	-	0	-	μs
DAC Digital Filter + Analog Filter: (Note 17, Note 20)							
Frequency Response		0 ~ 20.0kHz	FR	-	±0.5	-	dB
Analog Filter: (Note 21)							
Frequency Response		0 ~ 20.0kHz	FR	-	±1.0	-	dB
BOOST Filter: (Note 20, Note 22)							
Frequency Response	MIN	20Hz	FR	-	5.76	-	dB
		100Hz		-	2.92	-	dB
		1kHz		-	0.02	-	dB
	MID	20Hz	FR	-	10.80	-	dB
		100Hz		-	6.84	-	dB
		1kHz		-	0.13	-	dB
	MAX	20Hz	FR	-	16.06	-	dB
		100Hz		-	10.54	-	dB
		1kHz		-	0.37	-	dB

Note 17. BOOST OFF (BST1-0 bit = "00")
Note 18. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.4535fs(@–0.05dB). SB=0.546fs(@–54dB).
Note 19. This time is from setting the 24-bit data of both channels from the input register to the output of analog signal.
Note 20. DAC → HPL, HPR, LOUT, ROUT, MOUT
Note 21. LIN1/LIN2/LIN3/RIN1/RIN2/RIN3 → HPL/HPR/LOUT/ROUT/MOUT
Note 22. These frequency responses scale with fs. If high-level signal is input, the output clips at low frequency.

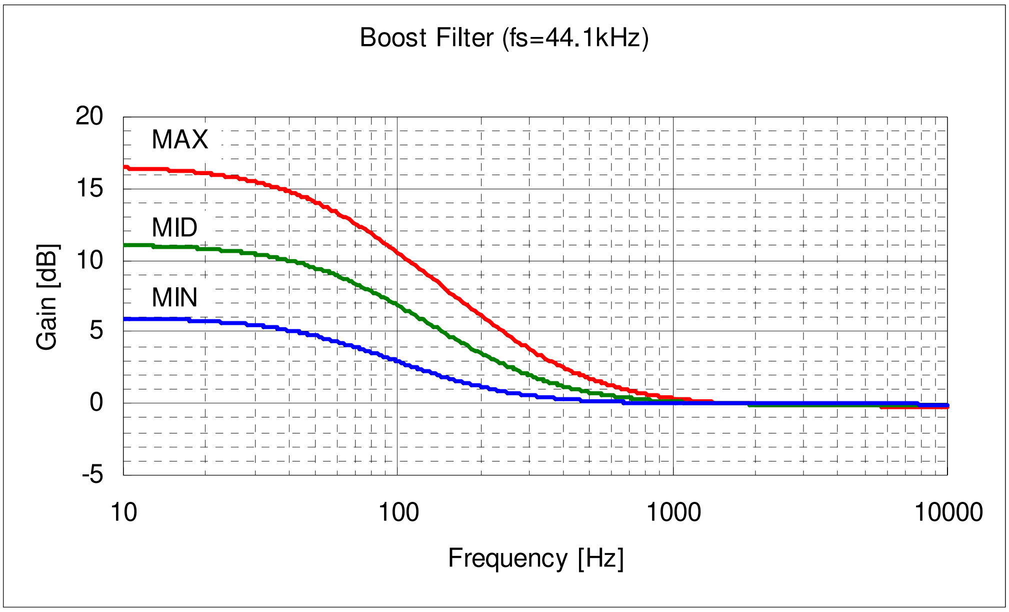


Figure 2. Boost Frequency (fs=44.1kHz)

DC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=PVDD=HVDD=1.6 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	2.2V≤DVDD≤3.6V	VIH	70%DVDD	-	-	V
	1.6V≤DVDD<2.2V	VIH	80%DVDD	-	-	V
Low-Level Input Voltage	2.2V≤DVDD≤3.6V	VIL	-	-	30%DVDD	V
	1.6V≤DVDD<2.2V	VIL	-	-	20%DVDD	V
Input Voltage at AC Coupling (Note 23)		VAC	0.4	-	-	Vpp
High-Level Output Voltage	(Iout=−200μA)	VOH	DVDD−0.2	-	-	V
Low-Level Output Voltage						
	(Except SDA pin: Iout=200μA)	VOL	-	-	0.2	V
	(SDA pin, 2.0V≤DVDD≤3.6V: Iout=3mA)	VOL	-	-	0.4	V
	(SDA pin, 1.6V≤DVDD<2.0V: Iout=3mA)	VOL	-	-	20%DVDD	V
Input Leakage Current		Iin	-	-	±10	μA

Note 23. The MCKI pin is connected to a capacitor. (Figure 57)

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=PVDD=HVDD=1.6 ~ 3.6V; C_L = 20pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
Master Clock Input Timing					
Frequency (PLL mode)	fCLK	11.2896	-	27	MHz
(EXT mode)	fCLK	2.048	-	24.576	MHz
Pulse Width Low (Note 24)	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High (Note 24)	tCLKH	0.4/fCLK	-	-	ns
AC Pulse Width (Note 25)	tACW	18.5	-	-	ns
LRCK Timing					
Frequency	fs	8	44.1	48	kHz
Duty Cycle: Slave Mode	Duty	45	-	55	%
Master Mode	Duty	-	50	-	%
MCKO Output Timing (PLL mode)					
Frequency	fCLKO	0.256	-	12.288	MHz
Duty Cycle (Except fs=32kHz, PS1-0= “00”)	dMCK	40	-	60	%
(fs=32kHz, PS1-0= “00”)	dMCK	-	33	-	%
Serial Interface Timing (Note 26)					
Slave Mode (M/S bit = “0”):					
BICK Period (Note 27)					
(Except PLL Mode, PLL4-0 = “EH”, “FH”)	tBCK	312.5 or 1/(64fs)	-	1/(32fs)	ns
(PLL Mode, PLL4-0 bits = “EH”)	tBCK	-	1/(32fs)	-	ns
(PLL Mode, PLL4-0 bits = “EH”)	tBCK	-	1/(64fs)	-	ns
BICK Pulse Width Low					
(Except PLL Mode, PLL4-0 = “EH”, “FH”)	tBCKL	100	-	-	ns
(PLL Mode, PLL4-0 bits = “EH”, “FH”)	tBCKL	0.4 x tBCK	-	-	ns
BICK Pulse Width High					
(Except PLL Mode, PLL4-0 = “EH”, “FH”)	tBCKL	100	-	-	ns
(PLL Mode, PLL4-0 bits = “EH”, “FH”)	tBCKH	0.4 x tBCK	-	-	ns
LRCK Edge to BICK “↑” (Note 28)	tLRB	50	-	-	ns
BICK “↑” to LRCK Edge (Note 28)	tBLR	50	-	-	ns
SDATA Hold Time	tSDH	50	-	-	ns
SDATA Setup Time	tSDS	50	-	-	ns
Master Mode (M/S bit = “1”):					
BICK Frequency (BF bit = “1”)	fBCK	-	64fs	-	Hz
(BF bit = “0”)	fBCK	-	32fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK “↓” to LRCK	tMBLR	−50	-	50	ns
SDATA Hold Time	tSDH	50	-	-	ns
SDATA Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN “H” Time	tCSW	150	-	-	ns
CSN “↑” to CCLK “↑”	tCSS	50	-	-	ns
CCLK “↑” to CSN “↑”	tCSH	50	-	-	ns

Note 24. Except AC coupling.

Note 25. Pulse width to ground level when the MCKI pin is connected to a capacitor in series and a resistor is connected to ground. Refer to Figure 3.

Note 26. Refer to “Serial Data Interface”.

Note 27. Min is longer value between 312.5ns or 1/(64fs) except for PLL Mode, PLL4-0 bits = “EH”, “FH”.

Note 28. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus mode): (Note 29)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 30)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 31)	tPD	150	-	-	ns

Note 29. I^2C is a registered trademark of Philips Semiconductors.
Note 30. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 31. The AK4371 can be reset by bringing PDN pin = “L” to “H” only upon power up.

■ Timing Diagram

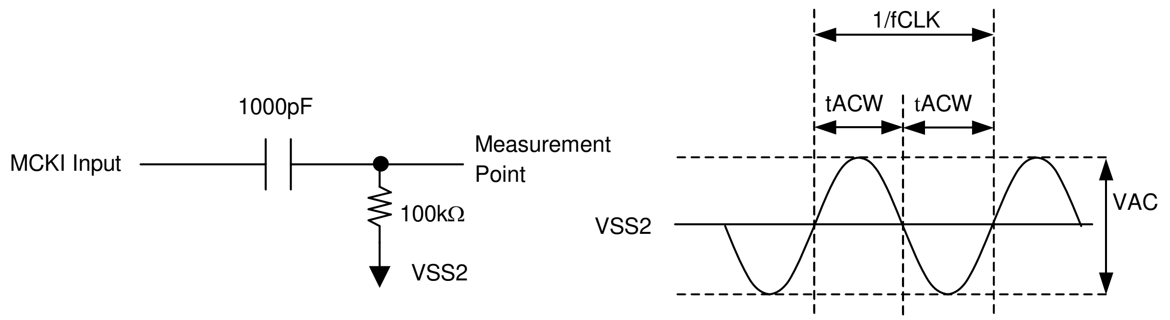


Figure 3. MCKI AC Coupling Timing

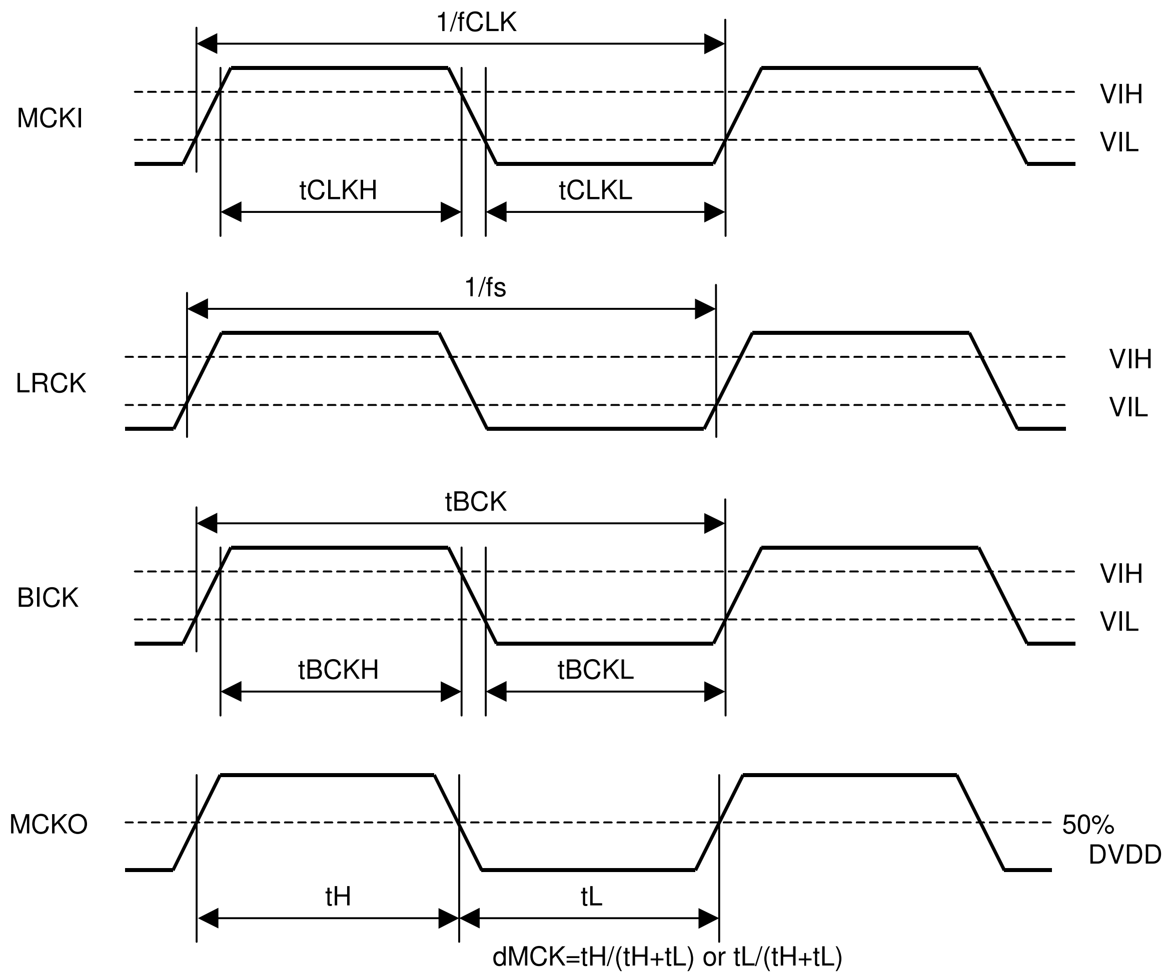


Figure 4. Clock Timing

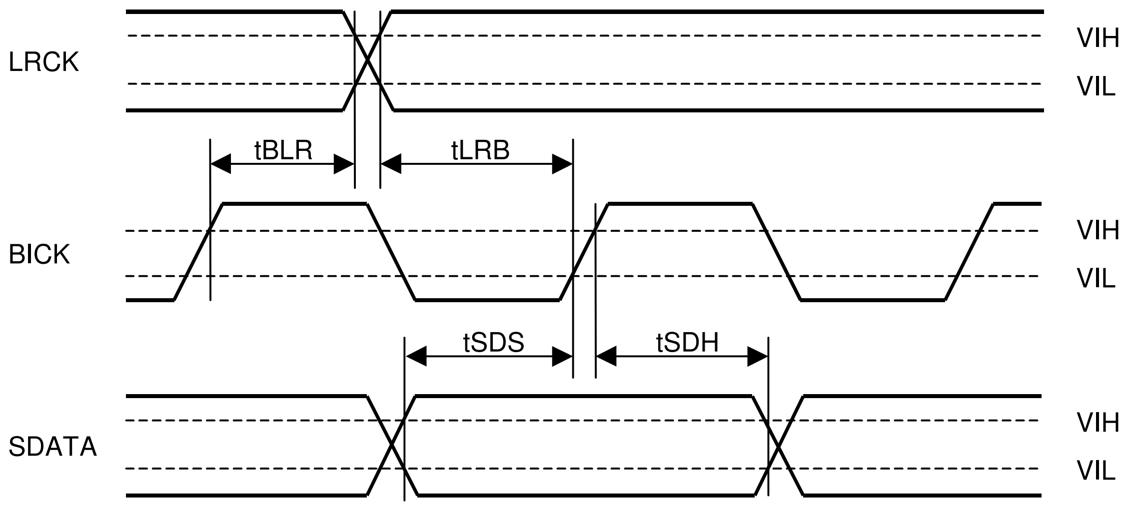


Figure 5. Serial Interface Timing (Slave Mode)

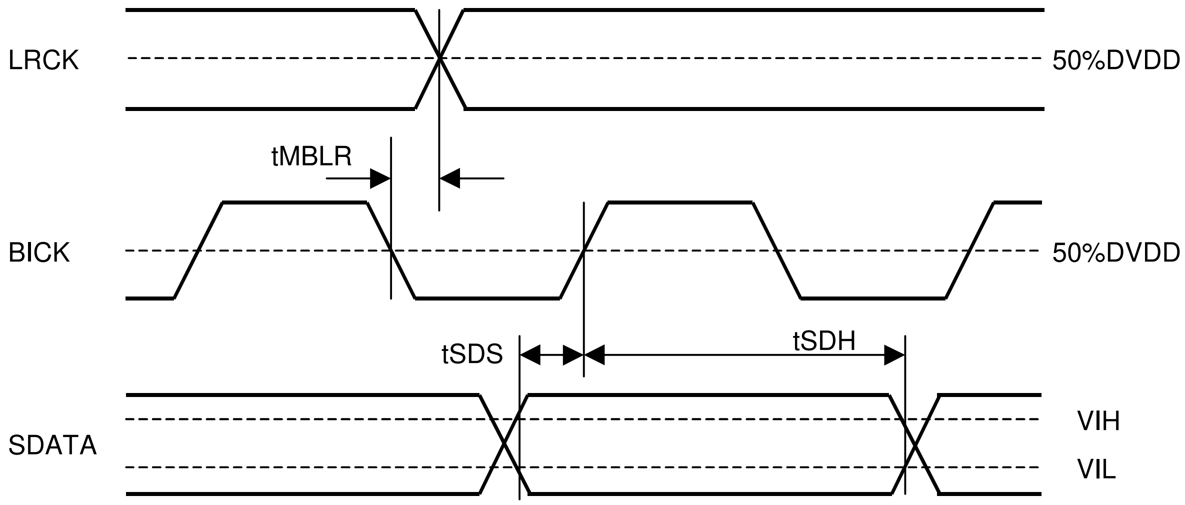


Figure 6. Serial Interface Timing (Master mode)

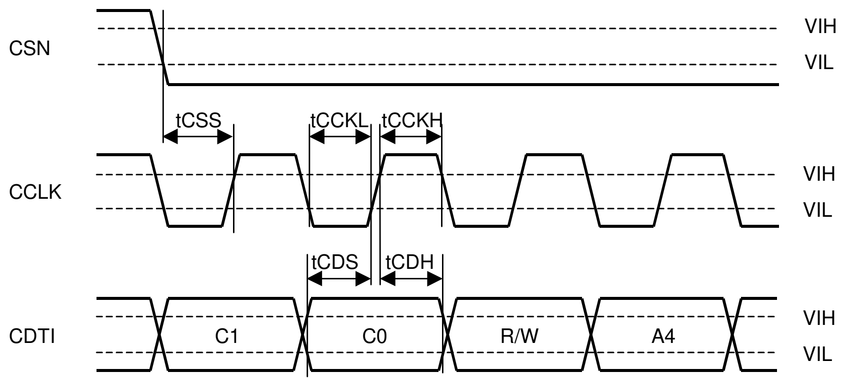


Figure 7. WRITE Command Input Timing

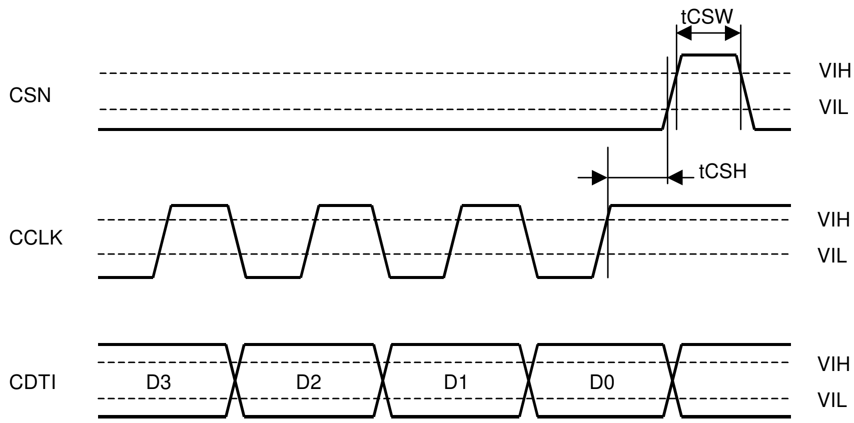


Figure 8. WRITE Data Input Timing

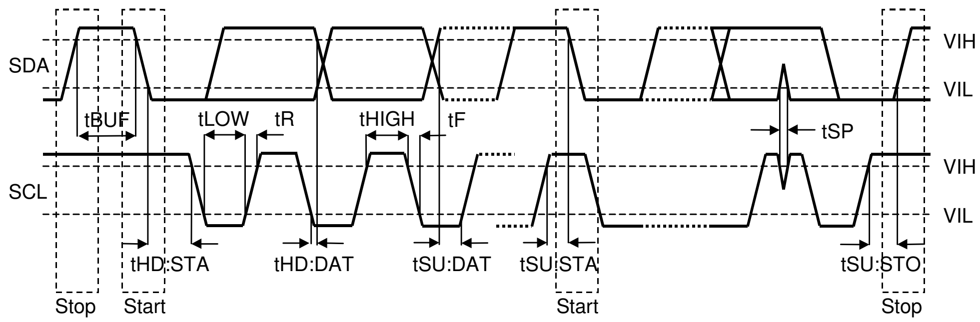


Figure 9. I^2C Bus Mode Timing

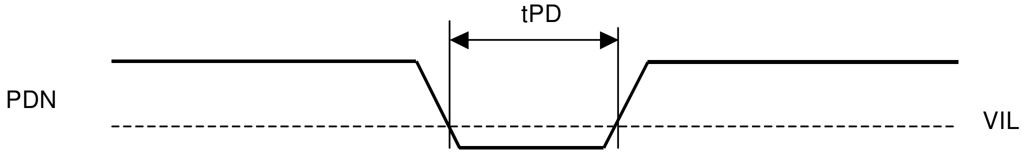


Figure 10. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

There are the following six clock modes to interface with external devices (Table 1 and Table 2).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode	1	1	See Table 4	Figure 11
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	See Table 4	Figure 12
PLL Slave Mode 2 (PLL Reference Clock: BICK pin)	1	0	See Table 4	Figure 13
PLL Slave Mode 3 (PLL Reference Clock: LRCK pin)	1	0	See Table 4	Figure 14
EXT Master Mode	0	1	x	Figure 15
EXT Slave Mode	0	0	x	Figure 16

Table 1. Clock Mode Setting (x: Don’t care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	“L”	Selected by PLL4-0 bits	Output (Selected by BF bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	0	“L”	Selected by PLL4-0 bits	Input (32fs ~ 64fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode 2 (PLL Reference Clock: BICK pin)	0	“L”	GND	Input (Selected by PLL4-0 bits)	Input (1fs)
PLL Slave Mode 3 (PLL Reference Clock: LRCK pin)	0	“L”	GND	Input (32fs ~ 64fs)	Input (1fs)
EXT Master Mode	0	“L”	Selected by FS3-0 bits	Output (Selected by BF bit)	Output (1fs)
EXT Slave Mode	0	“L”	Selected by FS3-0 bits	Input (32fs ~ 64fs)	Input (1fs)

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = “1” selects master mode and “0” selects slave mode. When the AK4371 is power-down mode (PDN pin = “L”) and exits reset state, the AK4371 is slave mode. After exiting reset state, the AK4371 goes to master mode by changing M/S bit = “1”.

When the AK4371 is used by master mode, LRCK and BICK pins are a floating state until M/S bit becomes “1”. LRCK and BICK pins of the AK4371 should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Slave Mode

■ PLL Mode (PMPLL bit = “1”)

When PMPLL bit is “1”, a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL4-0 and FS3-0 bits (Table 4, Table 5, Table 6). The PLL lock time is shown in Table 4, whenever the AK4371 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = “0” → “1”) or sampling frequency changes.

1) Setting of PLL Mode

Mode	PLL4	PLL3	PLL 2	PLL1	PLL0	Reference Clock		fs (Note 32)	R,C at VCOC		PLL Lock Time (typ)	
									R[Ω]	C[F]		
0	0	0	0	0	0	MCKI	11.2896MHz	Type 1	10k	22n	20ms	(default)
1	0	0	0	0	1	MCKI	14.4MHz	Type 1	10k	22n	20ms	
2	0	0	0	1	0	MCKI	12MHz	Type 1	10k	47n	20ms	
3	0	0	0	1	1	MCKI	19.2MHz	Type 1	10k	22n	20ms	
4	0	0	1	0	0	MCKI	15.36MHz	Type 1	10k	22n	20ms	
5	0	0	1	0	1	MCKI	13MHz	Type 1	15k	330n	100ms	
6	0	0	1	1	0	MCKI	19.68MHz	Type 1	10k	47n	20ms	
7	0	0	1	1	1	MCKI	19.8MHz	Type 1	10k	47n	20ms	
8	0	1	0	0	0	MCKI	26MHz	Type 1	15k	330n	100ms	
9	0	1	0	0	1	MCKI	27MHz	Type 1	10k	47n	20ms	
10	0	1	0	1	0	MCKI	13MHz	Type 2	10k	22n	20ms	
11	0	1	0	1	1	MCKI	26MHz	Type 2	10k	22n	20ms	
12	0	1	1	0	0	MCKI	19.8MHz	Type 3	10k	22n	20ms	
13	0	1	1	0	1	MCKI	27MHz	Type 4	10k	22n	20ms	
14	0	1	1	1	0	BICK	32fs	Table 6	6.8k	47n	20ms	
15	0	1	1	1	1	BICK	64fs	Table 6	6.8k	47n	20ms	
16	1	0	0	0	0	LRCK	fs	Table 6	6.8k	330n	80ms	
Others	Others					N/A						

Note 32. Refer to Table5 about Type1-4
Note 33. Clock jitter is lower in Mode10 ~13 than Mode5, 7, 8 and 9, respectively.
Note 34. Modes 14~16 are available at Slave Mode only.

Table 4. Setting of PLL Mode (*fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode

When PLL reference clock input is the MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3	FS2	FS1	FS0	fs				
					Type 1	Type 2	Type 3	Type 4	
0	0	0	0	0	48kHz	48.0007kHz	47.9992kHz	47.9997kHz	
1	0	0	0	1	24kHz	24.0004kHz	23.9996kHz	23.9999kHz	
2	0	0	1	0	12kHz	12.0002kHz	11.9998kHz	11.9999kHz	
4	0	1	0	0	32kHz	32.0005kHz	31.9994kHz	31.9998kHz	
5	0	1	0	1	16kHz	16.0002kHz	15.9997kHz	15.9999kHz	
6	0	1	1	0	8kHz	8.0001kHz	7.9999kHz	7.9999kHz	
8	1	0	0	0	44.1kHz	44.0995kHz	44.0995kHz	44.0995kHz	(default)
9	1	0	0	1	22.05kHz	22.0498kHz	22.0498kHz	22.0498kHz	
10	1	0	1	0	11.025kHz	11.0249kHz	11.0249kHz	11.0249kHz	
3, 7, 11-15	Others				N/A	N/A	N/A	N/A	

Table 5. Setting of Sampling Frequency (PLL reference clock input is the MCKI pin)

When PLL reference clock input is the LRCK or BICK pin, the sampling frequency is selected by FS3-0 bits. (Table 6)

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	1	0	0	0	32kHz < fs ≤ 48kHz	(default)
1	1	0	0	1	24kHz < fs ≤ 32kHz	
2	1	0	1	0	16kHz < fs ≤ 24kHz	
3	1	0	1	1	12kHz < fs ≤ 16kHz	
4	1	1	0	0	8kHz ≤ fs ≤ 12kHz	
Others	Others				N/A	

Table 6. Setting of Sampling Frequency (PLL reference clock input is LRCK or BICK pin)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

In master mode (M/S bits = “1”), LRCK and BICK pins output “L” before the PLL is locked by setting PMPLL = PMDAC bits = “0” → “1”. At that time, the MCKO pin outputs an abnormal frequency clock at MCKO bit = “1”. When MCKO bit = “0”, the MCKO pin outputs “L”. After the PLL is locked, LRCK and BICK start to output the clocks (Table 7).

	Master Mode (M/S bit = “1”)		
	Power Up (PMDAC bit= PMPLL bit= “1”)	Power Down (PMDAC bit= PMPLL bit= “0”)	PLL Unlock
MCKI pin	Refer to Table 4.	Input or fixed to “L” or “H” externally	Refer to Table 4.
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”	MCKO bit = “0”: “L” MCKO bit = “1”: Unsettling
BICK pin	BF bit = “1”: 64fs output BF bit = “0”: 32fs output	“L”	“L”
LRCK pin	Output	“L”	“L”

Table 7. Clock Operation in Master mode (PLL mode)

2) PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

In slave mode (M/S bits = “0”), an invalid clock is output from the MCKO pin when MCKO bit = “1”, before the PLL is locked by setting PMPLL = PMDAC bits = “0” → “1”. When MCKO bit = “0”, the MCKO pin outputs “L”. After the PLL is locked, the MCKO pin starts to output the clocks (Table 9).

	Slave Mode (M/S bit = “0”)		
	Power Up (PMDAC bit= PMPLL bit= “1”)	Power Down (PMDAC bit= PMPLL bit= “0”)	PLL Unlock
MCKI pin	Refer to Table 4.	Input or fixed to “L” or “H” externally	Refer to Table 4.
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”	MCKO bit = “0”: “L” MCKO bit = “1”: Unsettling
BICK pin	Input	Fixed to “L” or “H” externally	Input or Fixed to “L” or “H” externally
LRCK pin	Input	Fixed to “L” or “H” externally	Input or Fixed to “L” or “H” externally

Table 8. Clock Operation in Slave mode (PLL mode)

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 13MHz, 14.4MHz, 15.36MHz, 19.2MHz, 19.68MHz,19.8MHz, 26MHz or 27MHz) is input to the MCKI pin, the MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BF bit (Table 10).

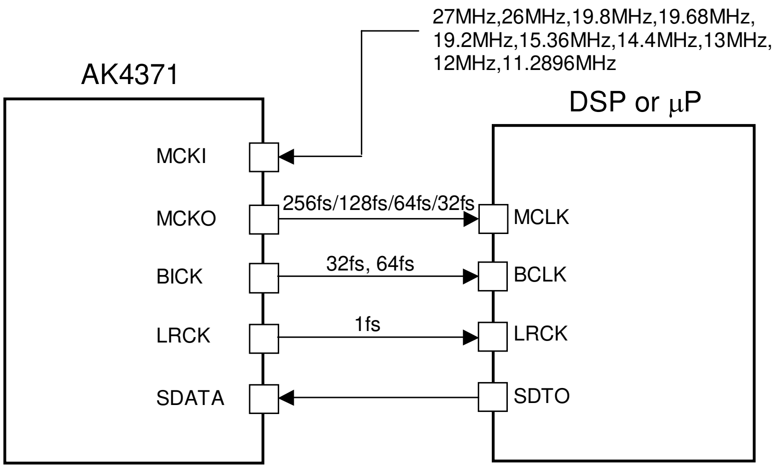


Figure 11. PLL Master Mode

PS1	PS0	MCKO	
0	0	256fs	(default)
0	1	128fs	
1	0	64fs	
1	1	32fs	

Table 9. MCKO Frequency (PLL mode, MCKO bit = "1")

BF bit	BICK Frequency	
0	32fs	(default)
1	64fs	

Table 10. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to MCKI, BICK or LRCK pin. The required clock to the AK4371 is generated by an internal PLL circuit. Input frequency is selected by PLL4-0 bits (Table 4).

a) PLL reference clock: MCKI pin

BICK and LRCK inputs should be synchronized with MCKO output. The phase between MCKO and LRCK dose not matter. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).

The external clocks (MCKI, BICK and LRCK) should always be present whenever the DAC is in operation (PMDAC bit = "1"). If these clocks are not provided, the AK4371 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the DAC should be in the power-down mode (PMDAC bits = "0").

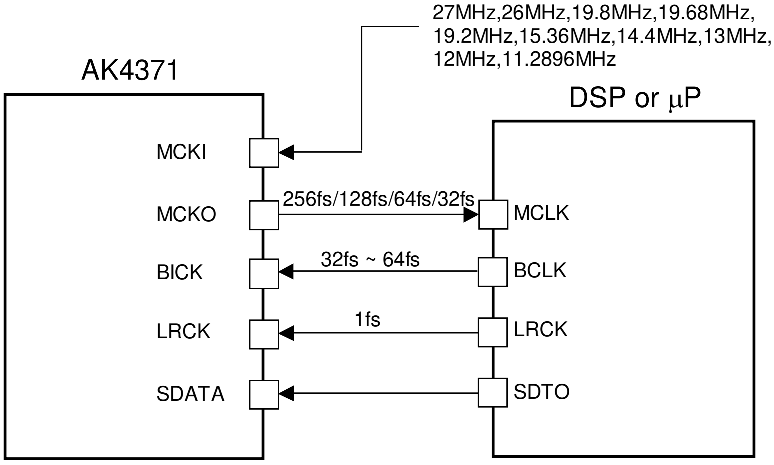


Figure 12. PLL Slave Mode (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK pin

Sampling frequency corresponds to 8kHz to 48kHz by changing FS3-0 bits (Table 6).

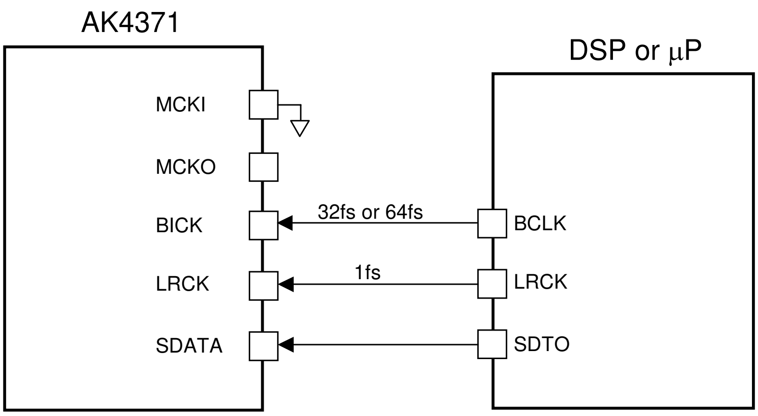


Figure 13. PLL Slave Mode (PLL Reference Clock: BICK pin)

c) PLL reference clock: LRCK pin

Sampling frequency corresponds to 8kHz to 48kHz by changing FS3-0 bits (Table 6).

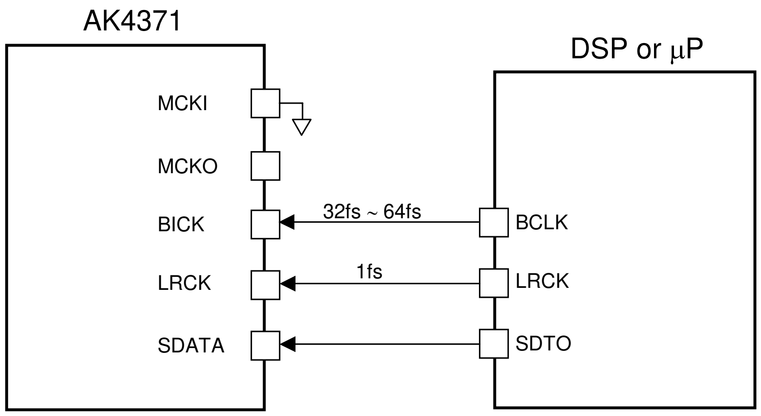


Figure 14. PLL Slave Mode (PLL Reference Clock: LRCK pin)

■ EXT Mode (PMPLL bit = “0”: Default)

The AK4371 can be placed in external clock mode (EXT mode) by setting the PMPLL bit to “0”. In EXT mode, the master clock can directly input to the DAC via the MCKI pin without going through the PLL. In this case, the sampling frequency and MCKI frequency can be selected by FS3-0 bits (Table 11). In EXT mode, PLL4-0 bits are ignored. MCKO output is enabled by controlling the MCKO bit. MCKO output frequency can be controlled by PS1-0 bits. If the sampling frequency is changed during normal operation of the DAC (PMDAC bit = “1”), the change should occur after the input is muted by SMUTE bit = “1”, or the input is set to “0” data.

LRCK and BICK are output from the AK4371 in master mode (Figure 15). The clock input to the MCKI pin should always be present whenever the DAC is in normal operation (PMDAC bit = “1”). If these clocks are not provided, the AK4371 may draw excessive current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the DAC should be placed in power-down mode (PMDAC bit = “0”).

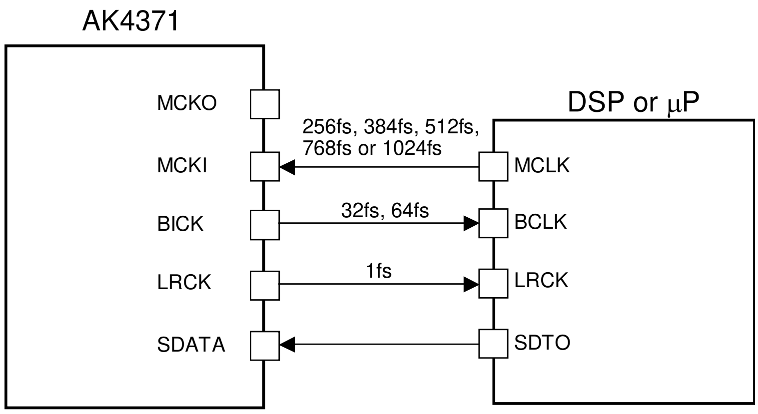


Figure 15. EXT Master Mode

The external clocks required to operate the AK4371 in slave mode are MCKI, LRCK and BICK (Figure 16). The master clock (MCKI) should be synchronized with the sampling clock (LRCK). The phase between these clocks does not matter. All external clocks (MCKI, BICK and LRCK) should always be present whenever the DAC is in normal operation mode (PMDAC bit = “1”). If these clocks are not provided, the AK4371 may draw excessive current and will not operate properly, because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the DAC should be placed in power-down mode (PMDAC bit = “0”).

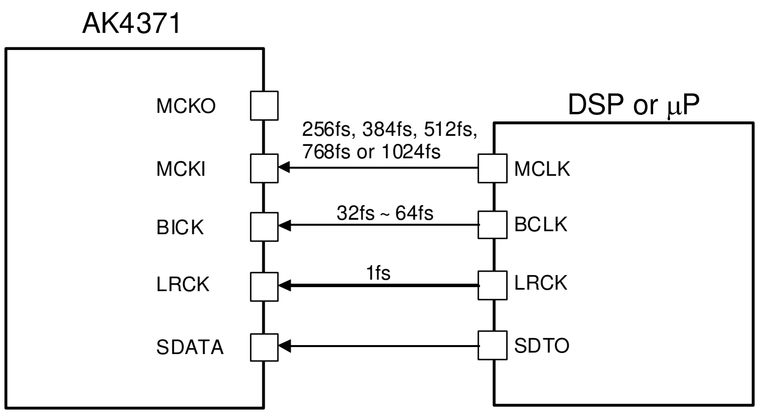


Figure 16. EXT Slave Mode

Mode	FS3	FS2	FS1	FS0	fs	MCKI	
0	0	0	0	0	8kHz ~ 48kHz	256fs	
1	0	0	0	1	8kHz ~ 48kHz	512fs	
2	0	0	1	0	8kHz ~ 24kHz	1024fs	
4	0	1	0	0	8kHz ~ 48kHz	256fs	
5	0	1	0	1	8kHz ~ 48kHz	512fs	
6	0	1	1	0	8kHz ~ 24kHz	1024fs	
8	1	0	0	0	8kHz ~ 48kHz	256fs	(default)
9	1	0	0	1	8kHz ~ 48kHz	512fs	
10	1	0	1	0	8kHz ~ 24kHz	1024fs	
12	1	1	0	0	8kHz ~ 48kHz	384fs	
13	1	1	0	1	8kHz ~ 24kHz	768fs	
Others	Others				N/A	N/A	

Table 11. Relationship between Sampling Frequency and MCKI Frequency (EXT mode)

PS1	PS0	MCKO	
0	0	256fs	(default)
0	1	128fs	
1	0	64fs	
1	1	32fs	

Table 12. MCKO frequency (EXT mode, MCKO bit = “1”)

	Master Mode (M/S bit = “1”)	
	Power Up (PMDAC bit = “1”)	Power Down (PMDAC bit = “0”)
MCKI pin	Refer to Table 11	Input or fixed to “L” or “H” externally
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”
BICK pin	BF bit = “1”: 64fs output BF bit = “0”: 32fs output	“L”
LRCK pin	Output	“L”

Table 13. Clock Operation in Master mode (EXT mode)

	Slave Mode (M/S bit = “0”)	
	Power Up (PMDAC bit = “1”)	Power Down (PMDAC bit = “0”)
MCKI pin	Refer to Table 11	Input or fixed to “L” or “H” externally
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”
BICK pin	Input	Fixed to “L” or “H” externally
LRCK pin	Input	Fixed to “L” or “H” externally

Table 14. Clock Operation in Slave mode (EXT mode)

For low sampling rates, DR and S/N degrade because of the out-of-band noise. DR and S/N are improved by using higher frequency for MCKI. Table 15 shows DR and S/N when the DAC output is to the HP-amp.

MCKI	DR, S/N (BW=20kHz, A-weight)	
	fs=8kHz	fs=16kHz
256fs/384fs/512fs	56dB	75dB
768fs/1024fs	75dB	90dB

Table 15. Relationship between MCKI frequency and DR (and S/N) of HP-amp (2.4V)