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AK4373

Low Power Stereo DAC with HP/SPK-Amp

GENERAL DESCRIPTION

The AK4373 is a low power stereo 24bit DAC with an integrated stereo headphone amplifier and a monaural speaker driver. It can be used for a variety of portable audio and media player applications, including game consoles, dedicated headphone drivers, personal navigation devices, and portable media players. The output drivers can be configured for three unique use cases: mono speaker driver or single-ended ac-coupled headphones which can be used as stereo line-out, DC-coupled BTL headphones and Pseudo Cap-less. The AK4373 operates off of a low-voltage power supply, ranging from 2.2V to 3.6V. The output amplifiers operate at up to 4.0V of the headphone power supply. The device is packaged in a space-saving 32-pin QFN package.

FEATURES

- **Sampling Rate: 8 kHz ~ 48 kHz**
- **8-times Over sampling Digital Filter**
- **SCF with high tolerance to clock jitter**
- **Stereo Headphone Amplifier**
  - **65mW output (Single-ended mode) into 16Ω 3.3V**
  - **SNR: 96dB**
  - **130mW output (Differential mode) into 32Ω 3.3V**
  - **SNR: 96dB**
  - **60mW output (Pseudo cap-less mode) into 16Ω 3.3V**
  - **SNR: 86dB**
  - **Pop-noise free at power-up and reset**
- **Stereo Lineout**
  - **SNR: 96dB**
- **Mono Speaker Driver**
  - **Available for both Dynamic and Piezo Speaker**
  - **0.8W @ 8Ω HVDD = 4.0V**
  - **1.0W @ 4Ω HVDD = 4.0V**
  - **SNR: 97dB**
- **Digital Processing**
  - **HPF, LPF, 3D Enhance, Frequency Compensation, 5-BiQuads,**
  - **Digital ALC/Limiter: +36dB to -54dB, 0.375dB/step**
- **Digital Volume Control: +12dB to -115dB, 0.5dB/step, Mute**
- **Analog Mixing: Mono input**
- **PLL: Input Frequency: 27MHz, 25MHz, 24MHz, 13.5MHz, 12.288MHz, 12MHz, and 11.2896MHz (MCKI pin)**
  - **1fs (LRCK pin)**
  - **32fs or 64fs (BICK pin)**
  - **Input Level: CMOS or AC coupling Input**
- **Master Clock (MCKI pin): 256/512/1024fs**
- **Master Clock Output (MCKO pin): 32fs, 64fs, 128fs, 256fs**
- **µP Interface: 3-Wire serial, I^2C bus (version1.0, 400 KHz Fast-mode)**
- **Audio Interface Format: MSB First, 2's complement**
  - **16/20/24bit MSB justified, 16/20/24bit LSB justified,**
  - **16/20/24bit I^2S, 16/20/24bit DSP Mode**
- **CMOS Input Level**

☐ **Power Supply:**
Analog (AVDD): 2.2 to 3.6V
Digital (DVDD): 1.6 to 3.6V
Driver (HVDD): 2.2 to 4.0V
☐ **Power Consumption:**
11.9mW headphone playback
☐ **Ta = -30 ~ +85°C**
☐ **Package: 32-pin QFN (5mm x 5mm, 0.5mm pitch)**
☐ **Pin/Register compatible with AK4343**

■ Block Diagram

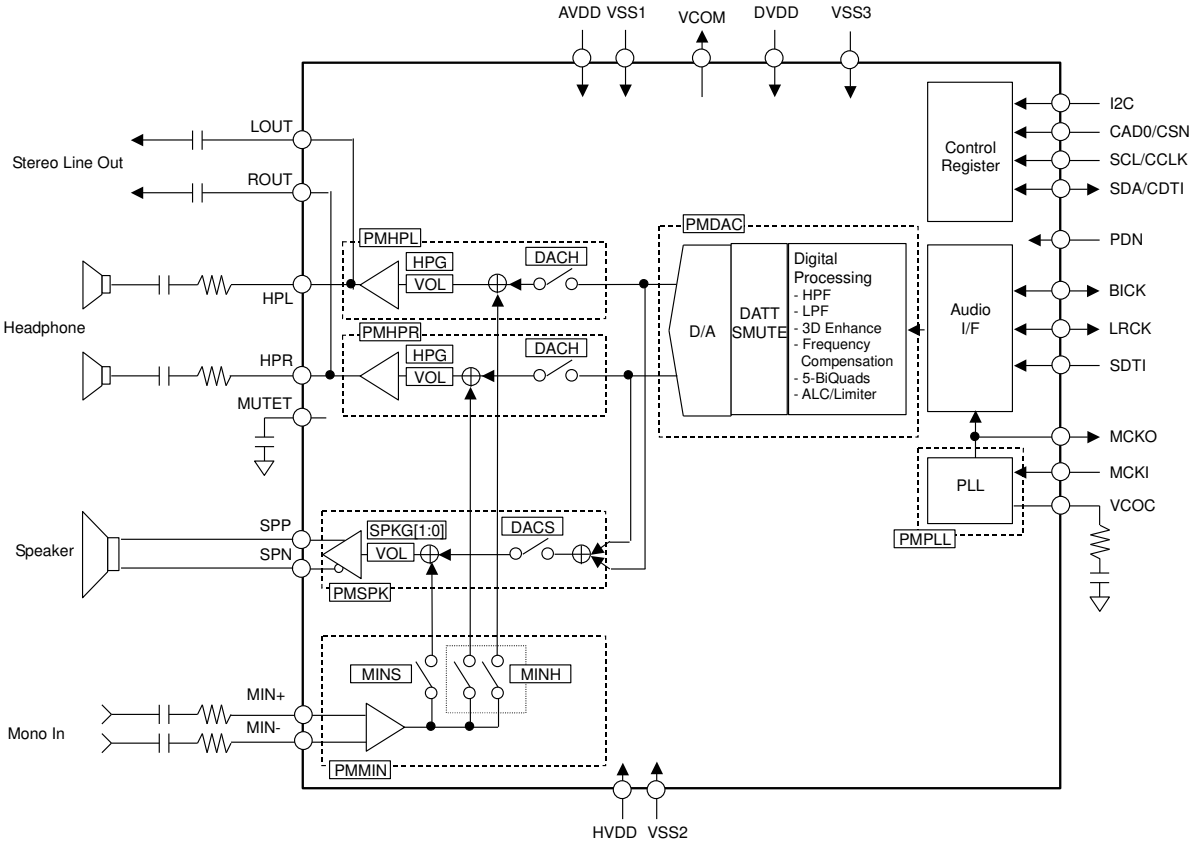


Figure 1. Block Diagram (Single-ended mode, HPBTL bit =PSEUDO bit = "0")

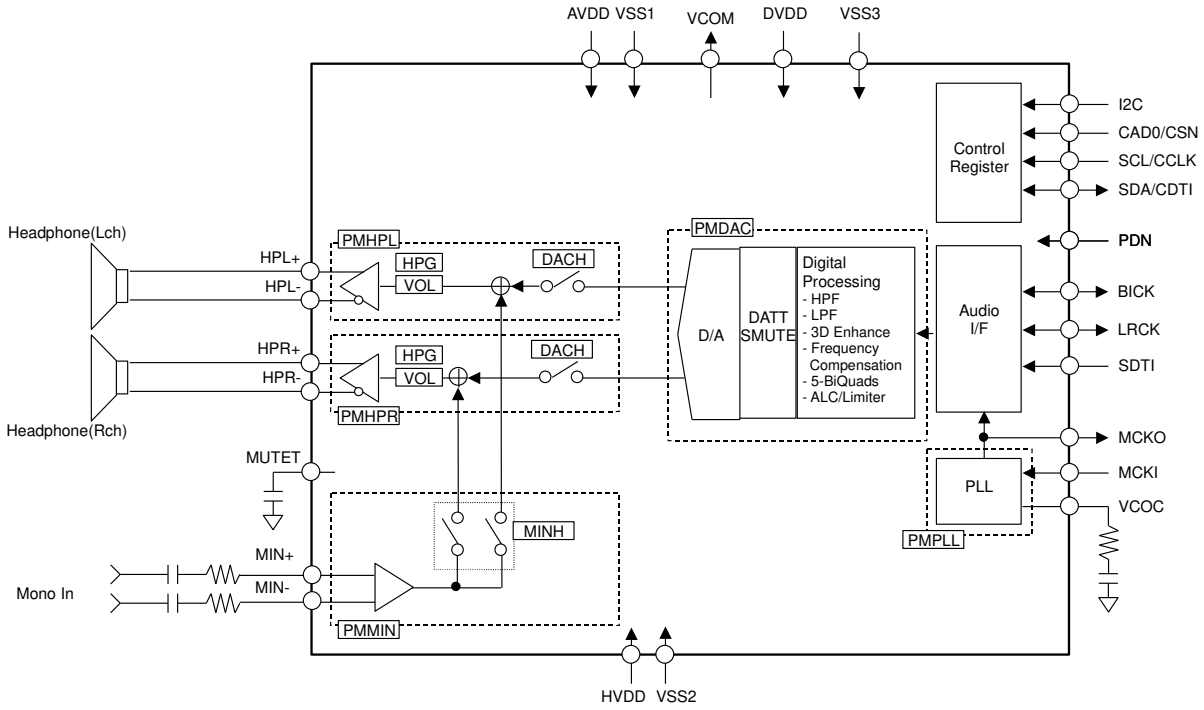


Figure 2. Block Diagram (Differential mode, HPBTL bit = "1", PSEUDO bit = "0")

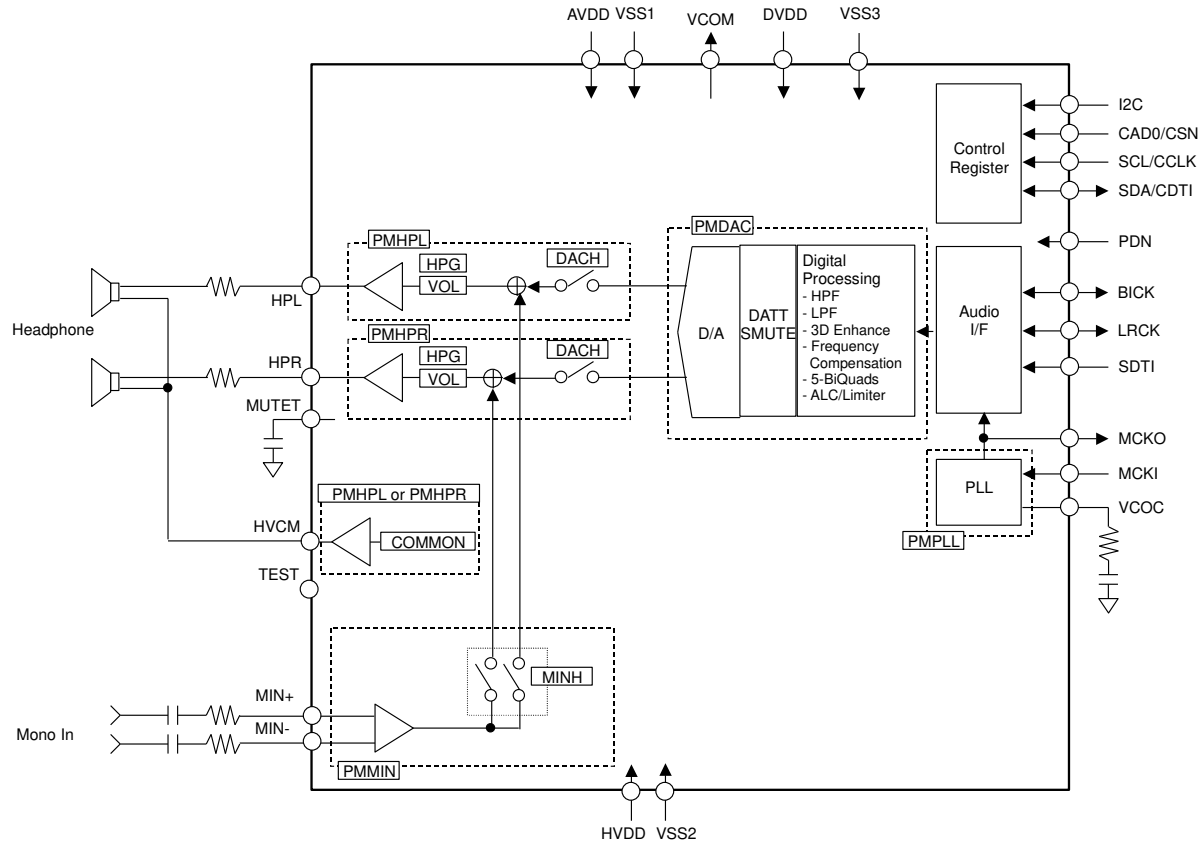
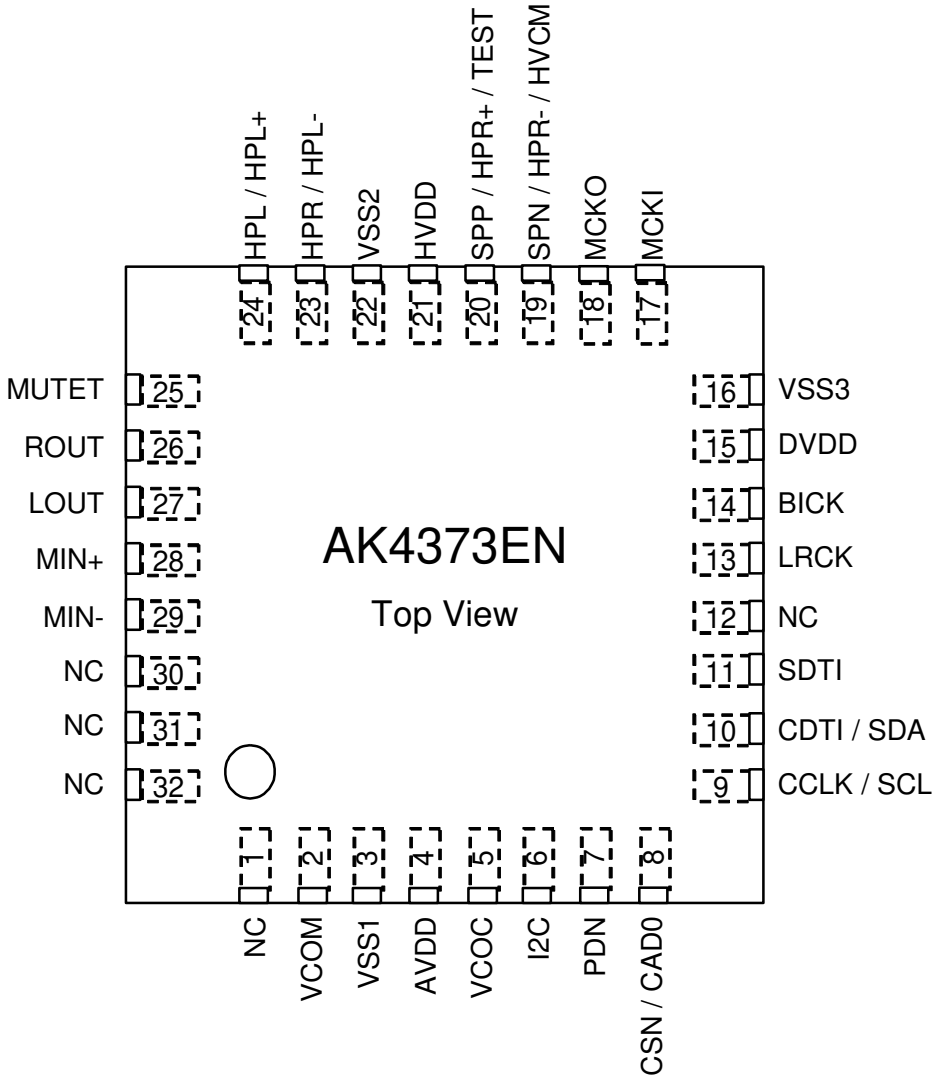


Figure 3. Block Diagram (Pseudo cap-less mode, HPBTL bit = "0", PSEUDO bit = "1")

■ Ordering Guide

AK4373EN	–30 ~ +85°C	32pin QFN (0.5mm pitch)
AKD4373	Evaluation board for AK4373	

■ Pin Layout



■ Comparison table between AK4343 and AK4373

1. Function

Function	AK4343	AK4373
DAC Resolution	16bit	24bit
HP-Amp S/N	90dB	96dB(single), 96dB(BTL)
HP-Amp Output Type	Single-ended	Single-ended, Differential or Pseudo cap-less
Five Programmable Biquads	No	Yes
Line Output Pins	Independent from HP/SPK	Shared with HPL/HPR
MCKI Input Level	CMOS	CMOS or 0.4Vpp AC coupling
Analog Mixing	3-Stereo	1-Mono (Single/Differential)
Receiver Amp	Yes	No
SPK AMP	1.2W@8Ω, 5V	1.0W@4Ω, 4.0V

2. Pin

Pin#	AK4343	AK4373
1	TEST1	NC
3	AVSS	VSS1
5	VCOC / RIN3	VCOC
12	TEST2	NC
16	DVSS	VSS3
19	SPN	SPN / HPR− / HVCM
20	SPP	SPP / HPR+ / TEST
22	HVSS	VSS2
23	HPR	HPR / HPL−
24	HPL	HPL / HPL+
28	MIN / LIN3	MIN+
29	RIN2 / IN2−	MIN-
30	LIN2 / IN2+	NC
31	LIN1 / IN1−	NC
32	RIN1 / IN1+	NC

3. Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMVCM	PMMIN	PMSPK	~~PMLO~~	PMDAC	0	0
01H	Power Management 2	0	HPMTN	PMHPL	PMHPR	M/S	MCKAC	MCKO	PMPLL
02H	Signal Select 1	SPPSN	MINS	DACS	~~DACL~~	HPBTL	~~PMMP~~	PSEUDO	~~MGAIN0~~
03H	Signal Select 2	~~LOVL~~	~~LOPS~~	~~MGAIN1~~	SPKG1	SPKG0	~~MINL~~	0	0
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	DIF2	DIF1	DIF0
05H	Mode Control 2	PS1	PS0	FS3	MSBS	BCKP	FS2	FS1	FS0
06H	Timer Select	DVTM	WTM2	ZTM1	ZTM0	WTM1	WTM0	RFST1	RFST0
07H	ALC Mode Control 1	0	0	ALC	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
08H	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
09H	Lch Input Volume Control	AVL7	AVL6	AVL5	AVL4	AVL3	AVL2	AVL1	AVL0
0AH	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
0BH	ALC Mode Control 3	RGAIN1	LMTH1	0	0	0	FRN	VBAT	0
0CH	Rch Input Volume Control	AVR7	AVR6	AVR5	AVR4	AVR3	AVR2	AVR1	AVR0
0DH	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
0EH	Mode Control 3	0	0	SMUTE	DVOLC	~~BST1~~	~~BST0~~	DEM1	DEM0
0FH	Mode Control 4	0	0	0	0	AVOLC	HPM	MINH	DACH
10H	Power Management 3	~~INR1~~	~~INL1~~	HPG	~~MDIF2~~	~~MDIF1~~	~~INR0~~	~~INL0~~	0
11H	Digital Filter Select 1	GN1	GN0	LPF	HPF	EQ	FIL3	0	0
12H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
13H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
14H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
15H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
16H	EQ Co-efficient 0	EQA7	EQA6	EQA5	EQA4	EQA3	EQA2	EQA1	EQA0
17H	EQ Co-efficient 1	EQA15	EQA14	EQA13	EQA12	EQA11	EQA10	EQA9	EQA8
18H	EQ Co-efficient 2	EQB7	EQB6	EQB5	EQB4	EQB3	EQB2	EQB1	EQB0
19H	EQ Co-efficient 3	0	0	EQB13	EQB12	EQB11	EQB10	EQB9	EQB8
1AH	EQ Co-efficient 4	EQC7	EQC6	EQC5	EQC4	EQC3	EQC2	EQC1	EQC0
1BH	EQ Co-efficient 5	EQC15	EQC14	EQC13	EQC12	EQC11	EQC10	EQC9	EQC8
1CH	HPF Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1DH	HPF Co-efficient 1	~~F1AS~~	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1EH	HPF Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1FH	HPF Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
20H	Reserved	0	0	~~PMAINR3~~	~~PMAINL3~~	~~PMAINR2~~	~~PMAINL2~~	~~PMMICR~~	~~PMMICL~~
21H	Reserved	0	0	~~MICR3~~	~~MICL3~~	0	0	~~AIN3~~	~~RCV~~
22H	Reserved	0	0	0	0	~~RINR3~~	~~LINL3~~	~~RINR2~~	~~LINL2~~
23H	Reserved	0	0	0	0	~~RINH3~~	~~LINH3~~	~~RINH2~~	~~LINH2~~
24H	Reserved	0	0	0	0	~~RINS3~~	~~LINS3~~	~~RINS2~~	~~LINS2~~
25H	Reserved	0	0	0	0	0	0	0	0
26H	Reserved	0	0	0	0	0	0	0	0
27H	Reserved	0	0	0	0	0	0	0	0
28H	Reserved	0	0	0	0	0	0	0	0
29H	Reserved	0	0	0	0	0	0	0	0
2AH	Reserved	0	0	0	0	0	0	0	0
2BH	Reserved	0	0	0	0	0	0	0	0
2CH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8

These bits were added to the AK4373.
These bits were removed from the AK4343.
These bits name were changed.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Reserved	0	0	0	0	0	0	0	0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

These bits were added to the AK4373.
These bits were removed from the AK4343.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	NC	-	No Connect Pin No internal bonding. This pin should be open or connected to the ground.
2	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD Bias voltage of DAC outputs.
3	VSS1	-	Analog Ground Pin
4	AVDD	-	Analog Power Supply Pin 2.2 ~ 3.6V
5	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin must be connected to VSS1 with one resistor and capacitor in series.
6	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire Serial
7	PDN	I	Power-Down Mode Pin "H": Power-up, "L": Power-down, reset and initialization of the control register. The AK4373 must be reset once upon power-up.
8	CSN	I	Chip Select Pin (I2C pin = "L": 3-wire Serial Mode)
	CAD0	I	Chip Address 1 Select Pin (I2C pin = "H": I^2C Bus Mode)
9	CCLK	I	Control Data Clock Pin (I2C pin = "L": 3-wire Serial Mode)
	SCL	I	Control Data Clock Pin (I2C pin = "H": I^2C Bus Mode)
10	CDTI	I	Control Data Input Pin (I2C pin = "L": 3-wire Serial Mode)
	SDA	I/O	Control Data Input Pin (I2C pin = "H": I^2C Bus Mode)
11	SDTI	I	Audio Serial Data Input Pin
12	NC	-	No Connect Pin No internal bonding. This pin should be open or connected to the ground.
13	LRCK	I/O	Input / Output Channel Clock Pin
14	BICK	I/O	Audio Serial Data Clock Pin
15	DVDD	-	Digital Power Supply Pin. 1.6 ~ 3.6V
16	VSS3	-	Digital Ground Pin
17	MCKI	I	External Master Clock Input Pin
18	MCKO	O	Master Clock Output Pin

No.	Pin Name	I/O	Function
19	SPN	O	Speaker Amp Negative Output Pin Single-ended mode (HPBTL bit = PSEUDO bit = “0”)
	HPR−	O	Rch Headphone-Amp Negative Output Pin Differential mode (HPBTL bit = “1”, PSEUDO bit = “0”)
	HVCM	O	Common Output Voltage for Headphone-Amp Pin Pseudo cap-less mode (HPBTL bit = “0”, PSEUDO bit = “1”)
20	SPP	O	Speaker Amp Positive Output Pin Single-ended mode (HPBTL bit = PSEUDO bit = “0”)
	HPR+	O	Rch Headphone-Amp Positive Output Pin Differential mode (HPBTL bit = “1”, PSEUDO bit = “0”)
	TEST	O	This pin must be open. Pseudo cap-less mode (HPBTL bit = “0”, PSEUDO bit = “1”)
21	HVDD	-	Headphone & Speaker Amp Power Supply Pin. 2.2 ~ 4.0V
22	VSS2	-	Headphone & Speaker Amp Ground Pin
23	HPR	O	Rch Headphone-Amp Output Pin Single-ended mode (HPBTL bit = PSEUDO bit = “0”) Pseudo cap-less mode (HPBTL bit = “0”, PSEUDO bit = “1”)
	HPL−	O	Lch Headphone-Amp Negative Output Pin Differential mode (HPBTL bit = “1”, PSEUDO bit = “0”)
24	HPL	O	Lch Headphone-Amp Output Pin Single-ended mode (HPBTL bit = PSEUDO bit = “0”) Pseudo cap-less mode (HPBTL bit = “0”, PSEUDO bit = “1”)
	HPL+	O	Lch Headphone-Amp Positive Output Pin Differential mode (HPBTL bit = “1”, PSEUDO bit = “0”)
25	MUTET	O	Mute Time Constant Control Pin Connected to the VSS2 pin with a capacitor for mute time constant.
26	ROUT	O	Rch Line Output Pin This pin is internal connected to the HPR pin.
27	LOUT	O	Lch Line Output Pin This pin is internal connected to the HPL pin.
28	MIN+	I	Mono Signal Positive Input (Differential Input) or Mono Signal Input (Single-ended Input)
29	MIN-	I	Mono Signal Negative Input (Differential Input) If the MIN+ pin is used as single-ended, this pin should be connected to the VSS1 with a capacitor.
30	NC	-	No Connect Pin No internal bonding. This pin should be open or connected to the ground.
31	NC	-	No Connect Pin No internal bonding. This pin should be open or connected to the ground.
32	NC	-	No Connect Pin No internal bonding. This pin should be open or connected to the ground.

Note 1. All input pins must not be left floating.

Note 2. DVDD or VSS3 voltage must be input to I2C pin.

Note 3. All analog input pins (MIN+/- pins) must be supplied signal via AC-coupling capacitor.

Note 4. Analog output pins (HPL, HPR, LOUT, and ROUT pins) must deliver signal via AC-coupling capacitor except speaker output (SPP, SPN pins) and headphone output in Differential mode (HPL+/- and HPR+/- pins) and headphone output in Pseudo cap-less mode (HPL and HPR pins).

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	VCOC, SPN/HPR–/HVCM, SPP/HPR+/TEST, HPR/HPL-, HPL/HPL+, MIN+, MIN-, MUTET	These pins must be open.
Digital	MCKO	This pin must be open.
	MCKI	This pin must be connected to VSS3.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=0V; Note 5)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	Headphone-Amp / Speaker-Amp	HVDD	–0.3	4.6	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 7)		VINA	–0.3	(AVDD+0.3) or 4.6	V
Digital Input Voltage (Note 8)		VIND	–0.3	(DVDD+0.3) or 4.6	V
Ambient Temperature (powered applied)		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation	(Note 9)	Pd	-	511	mW

Note 5. All voltages are with respect to ground.
Note 6. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.
Note 7. I2C, MIN+, MIN- pin
Note 8. PDN, CSN/CAD0, CCLK/SCL, CDTI/SDA, SDTI, LRCK, BICK, MCKI pins
Pull-up resistors at SDA and SCL pins must be connected to (DVDD+0.3)V or less voltage.
Note 9. In case that the exposed pad is connected to the ground and PCB drawing density is 100%.This power is the AK4373 internal dissipation that does not include power of externally connected speaker and headphone.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=0V; Note 5)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 10)	Analog	AVDD	2.2	3.3	3.6	V
	Digital	DVDD	1.6	3.3	3.6	V
	HP / SPK-Amp	HVDD	2.2	3.3	4.0	V
	Difference1	DVDD – AVDD	-	-	+0.3	V
	Difference2	DVDD – HVDD	-	-	+0.3	V
	Difference3	AVDD – HVDD	-	-	+0.6	V

Note 5. All voltages are with respect to ground.
Note 10. The power-up sequence between AVDD, DVDD and HVDD is not critical. When only AVDD or HVDD is powered OFF, the power supply current of DVDD at power-down mode may be increased. DVDD must not be powered OFF while AVDD or HVDD is powered ON.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=HVDD=3.3V; VSS1=VSS2=VSS3=0V; fs=44.1kHz, BICK=64fs;
Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Unit
DAC Characteristics:					
Resolution		-	-	24	Bits
Stereo Line Output Characteristics: DAC → LOUT/ROUT pins, Single-ended mode (Figure 4), HPBTL bit = "0", PSEUDO bit = "0", HPG bit = "0", HVDD=3.3V, C=1μF, R_L=10kΩ, ALC=OFF, AVOL=0dB, DVOL=0dB; unless otherwise specified.					
Output Voltage (0dBFS) (Note 11)		1.78	1.98	2.18	Vpp
S/(N+D) (0dBFS)		-	77	-	dB
S/N (A-weighted)		86	96	-	dB
Interchannel Isolation		60	80	-	dB
Load Resistance	RL	10	-	-	kΩ
Load Capacitance	C1	-	-	30	pF

Note 11. Output voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ).

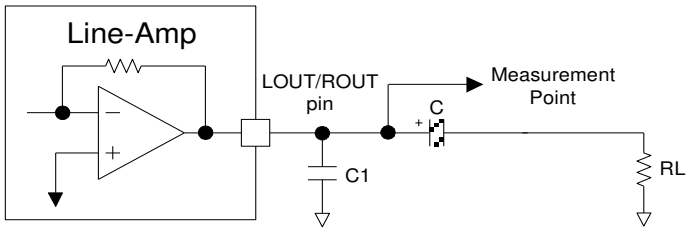


Figure 4. Line-Amp output circuit

Parameter		min	typ	max	Unit
Headphone-Amp Characteristics: DAC → HPL/HPR pins, Single-ended mode (Figure 5), HPBTL bit = "0", PSEUDO bit = "0", HPG bit = "0", HVDD=3.3V, C=47μF, R_L=22.8Ω, ALC=OFF, AVOL=0dB, DVOL=0dB; unless otherwise specified.					
Output Voltage (Note 12)	0dBFS	1.58	1.98	2.38	Vpp
	0dBFS (Note 13)	-	3.00	-	Vpp
	0dBFS (Note 14)	-	1.02	-	Vrms
S/(N+D)	–3dBFS	50	60	-	dB
	–3dBFS (Note 13)	-	65	-	dB
	0dBFS (Note 14)	-	20	-	dB
S/N (A-weighted)		86	96	-	dB
	(Note 13)	-	96	-	dB
Interchannel Isolation		60	75	-	dB
Interchannel Gain Mismatch		-	0	0.8	dB
Load Resistance	R_L=R1+R2	16	-	-	Ω
Load Capacitance	C1	-	-	30	pF
	C2	-	-	300	pF

Note 12. Output voltage is proportional to AVDD voltage.
Vout = 0.6 x AVDD(typ)@HPG bit = "0", 0.91 x AVDD(typ)@HPG bit = "1".
Note 13. HPG bit = "1", HVDD=3.8V, C=47μF, R_L=100Ω.
Note 14. HPG bit = "1", HVDD=3.3V, C=47μF, R_L=16Ω.

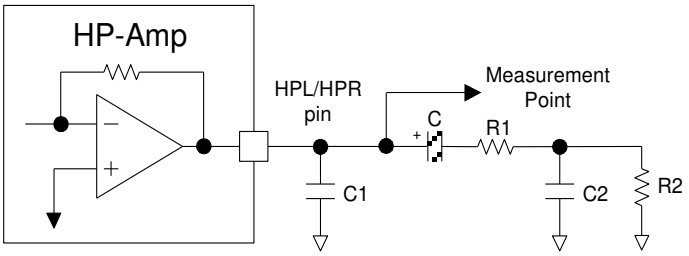


Figure 5. HP-Amp Output Circuit in single-ended mode

Parameter		min	typ	max	Unit
Headphone-Amp Characteristics: DAC → HPL+/-, HPR+/- pins, Differential mode(Figure 6), HPBTL bit = "1", PSEUDO bit = "0" , HPG bit = "0", HVDD=3.3V, R_L=32Ω, ALC=OFF, AVOL=0dB, DVOL=0dB; unless otherwise specified.					
Output Voltage (Note 15)	0dBFS	-	3.96	-	Vpp
	0dBFS (Note 16)	-	2.05	-	Vrms
S/(N+D)	–3dBFS	-	60	-	dB
	0dBFS (Note 16)	-	20	-	dB
S/N (A-weighted)		-	96	-	dB
Interchannel Isolation		-	75	-	dB
Interchannel Gain Mismatch		-	0.2	-	dB
Load Resistance	R_L =2 x R1 + R2	16	-	-	Ω
Load Capacitance	C1	-	-	30	pF
	C2	-	-	300	pF

Note 15. Output voltage is proportional to AVDD voltage.
Vout = 1.2 x AVDD(typ)@HPG bit = "0", 1.82 x AVDD(typ)@HPG bit = "1".
Note 16. HPG bit = "1", HVDD=3.3V, R_L=32Ω.

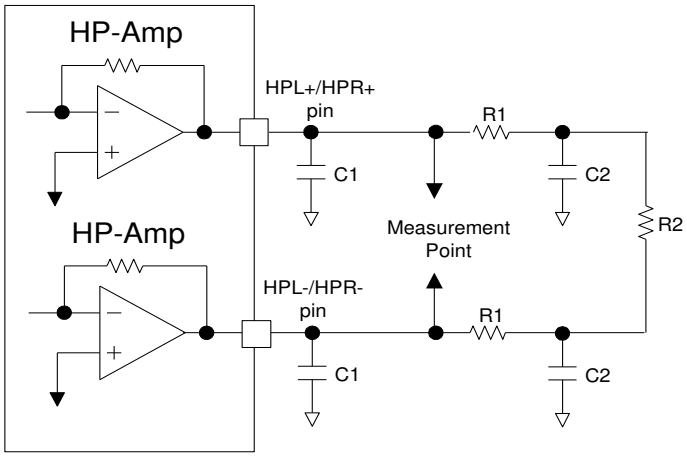
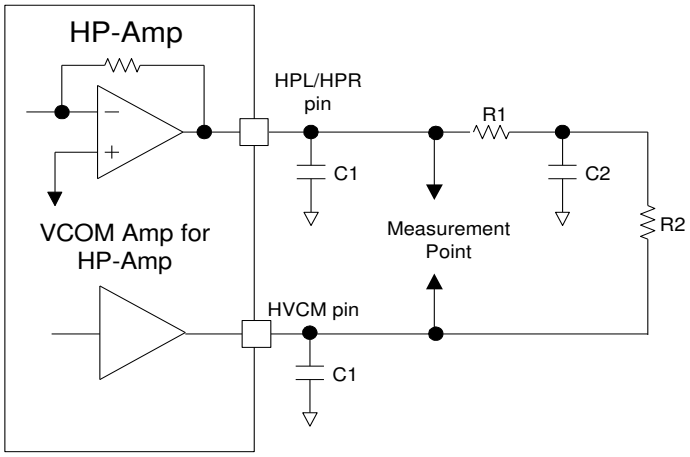


Figure 6. HP-Amp Output Circuit in differential mode

Parameter		min	typ	max	Unit
Headphone-Amp Characteristics: DAC → HPL/HPR pins, Pseudo cap-less mode(Figure 7), HPBTL bit = "0", PSEUDO bit = "1" , HPG bit = "0", HVDD=3.3V, R_L=22.8Ω, ALC=OFF, AVOL=0dB, DVOL=0dB; unless otherwise specified.					
Output Voltage (Note 17)	0dBFS	-	1.98	-	Vpp
	0dBFS (Note 18)	-	0.98	-	Vrms
S/(N+D)	–3dBFS	-	38	-	dB
	0dBFS (Note 18)	-	20	-	dB
S/N (A-weighted)		-	86	-	dB
Interchannel Isolation		-	38	-	dB
Interchannel Gain Mismatch		-	0	-	dB
Load Resistance	R_L = R1 + R2	16	-	-	Ω
Load Capacitance	C1	-	-	30	pF
	C2	-	-	300	pF

Note 17. Output voltage is proportional to AVDD voltage.
Vout = 0.6 x AVDD(typ)@HPG bit = "0", 0.91 x AVDD(typ)@HPG bit = "1".
Note 18. HPG bit = "1", HVDD=3.3V, R_L=16Ω.



Note: Impedance between headphone and the HVCM pin must be as low as possible. If the impedance is larger, crosstalk and distortion might be degraded.

Figure 7. HP-Amp Output Circuit in pseudo cap-less mode

Parameter			min	typ	max	Unit
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, AVOL=0dB, DVOL=0dB, R_L=8Ω, BTL, HVDD=3.3V; unless otherwise specified.						
Output Voltage (Note 19)						
	SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	3.11	-	Vpp
	SPKG1-0 bits = "01", –0.5dBFS (Po=240mW)		3.13	3.92	4.71	Vpp
	SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			2.04		Vrms
S/(N+D)						
	SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	50	-	dB
	SPKG1-0 bits = "01", –0.5dBFS (Po=240mW)		20	50	-	dB
	SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			20		dB
S/N (A-weighted)			87	97	-	dB
Load Resistance			8	-	-	Ω
Load Capacitance			-	-	30	pF
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, AVOL=0dB, DVOL=0dB, C_L=3μF, R_{series}=20Ω x 2, BTL, HVDD=3.8V; unless otherwise specified. (Figure 53)						
Output Voltage (Note 19)	SPKG1-0 bits = "10", -0.5dBFS		–	6.37	–	Vpp
S/(N+D) (Note 20)	SPKG1-0 bits = "10", -0.5dBFS		–	58	-	dB
S/N (A-weighted)				97	-	dB
Load Resistance (Note 21)			50	-	-	Ω
Load Capacitance (Note 21)			-	-	3	μF
Mono Input: MIN+ pin (External Input Resistance=20kΩ) Single-ended Input MIN- pin is connected to VSS1 via input capacitor.						
Maximum Input Voltage (Note 22)			-	1.98	-	Vpp
Gain (Note 23)						
	MIN+ → HPL/HPR	HPBTL bit = "0" HPG bit = "0"	-	0	-	dB
	MIN+ → HPL/HPR	HPBTL bit = "0" HPG bit = "1"	-	+3.6	-	dB
	MIN+ → HPL+/-, HPR+/-	HPBTL bit = "1" HPG bit = "0"	-	+6	-	dB
	MIN+ → HPL+/-, HPR+/-	HPBTL bit = "1" HPG bit = "1"	-	+9.6	-	dB
	MIN → SPP/SPN					
		ALC bit = "0", SPKG1-0 bits = "00"	-0.07	+4.43	+8.93	dB
		ALC bit = "0", SPKG1-0 bits = "01"	-	+6.43	-	dB
		ALC bit = "0", SPKG1-0 bits = "10"	-	+10.65	-	dB
		ALC bit = "0", SPKG1-0 bits = "11"	-	+12.65	-	dB
		ALC bit = "1", SPKG1-0 bits = "00"	-	+6.43	-	dB
		ALC bit = "1", SPKG1-0 bits = "01"	-	+8.43	-	dB
		ALC bit = "1", SPKG1-0 bits = "10"	-	+12.65	-	dB
		ALC bit = "1", SPKG1-0 bits = "11"	-	+14.65	-	dB

Mono Input: MIN+/MIN- pins (External Input Resistance=20kΩ) Differential Input						
Maximum Input Voltage (Note 24)			-	1.98	-	Vpp
Gain (Note 23)						
	MIN+/- → HPL/HPR	HPBTL bit = "0" HPG bit = "0"	-	0	-	dB
	MIN+/- → HPL/HPR	HPBTL bit = "0" HPG bit = "1"	-	+3.6	-	dB
	MIN+/- → HPL+/-, HPR+/-	HPBTL bit = "1" HPG bit = "0"	-	+6	-	dB
	MIN+/- → HPL+/-, HPR+/-	HPBTL bit = "1" HPG bit = "1"	-	+9.6	-	dB
	MIN+/MIN- → SPP/SPN					
		ALC bit = "0", SPKG1-0 bits = "00"	-0.07	+4.43	+8.93	dB
		ALC bit = "0", SPKG1-0 bits = "01"	-	+6.43	-	dB
		ALC bit = "0", SPKG1-0 bits = "10"	-	+10.65	-	dB
		ALC bit = "0", SPKG1-0 bits = "11"	-	+12.65	-	dB
		ALC bit = "1", SPKG1-0 bits = "00"	-	+6.43	-	dB
		ALC bit = "1", SPKG1-0 bits = "01"	-	+8.43	-	dB
		ALC bit = "1", SPKG1-0 bits = "10"	-	+12.65	-	dB
		ALC bit = "1", SPKG1-0 bits = "11"	-	+14.65	-	dB

Note 19. Output voltage is proportional to AVDD voltage.
Vout = 1.00 x AVDD(typ)@SPKG1-0 bits = "00", 1.25 x AVDD(typ)@SPKG1-0 bits = "01", 2.04 x AVDD(typ)@SPKG1-0 bits = "10", 2.57 x AVDD(typ)@SPKG1-0 bits = "11" at Differential output.

Note 20. In case of measuring at SPP and SPN pins.

Note 21. Load impedance is total impedance of series resistance (R_{series}) and piezo speaker impedance at 1kHz in Figure 56. Load capacitance is capacitance of piezo speaker. When piezo speaker is used, 20Ω or more series resistors should be connected at both SPP and SPN pins, respectively.

Note 22. Maximum voltage is in proportion to both AVDD and external input resistance (Rin).
Vin = 0.6 x AVDD x 20kΩ (typ)/Rin.

Note 23. The gain is in inverse proportional to external resistance.

Note 24. The Maximum voltage is in proportion to both AVDD and external input resistance (Rin).
Vin = (MIN+) – (MIN-) = 0.6 x AVDD x 20kΩ (typ)/Rin.
The signals with same amplitude and inverted phase should be input to MIN+ and MIN- pins, respectively.

Parameter			min	typ	max	Unit
Power Supplies:						
Power-Up (PDN pin = "H")						
	All Circuit Power-up:					
		AVDD+DVDD (Note 25)	-	7.8	-	mA
		AVDD+DVDD (Note 26)	-	8.1	12	mA
		HVDD: HP-Amp Normal Operation No Output (Note 27)	-	2.2	4	mA
		HVDD: SPK-Amp Normal Operation No Output (Note 28)	-	4.1	12	mA
Power-Down (PDN pin = "L") (Note 29)						
	AVDD+DVDD+HVDD		-	1	20	μA

Note 25. PLL Master Mode (MCKI=12.288MHz) and PMDAC = PMHPL = PMHPR = PMVCM = PMPLL = MCKO = M/S bits = "1", PMMIN bit = "0".
AVDD=3.9mA(typ), DVDD=3.9mA(typ).
EXT Slave Mode (PMPLL = M/S = MCKO bits = "0"): AVDD=3.1mA(typ), DVDD=2.7mA(typ).

Note 26. PLL Master Mode (MCKI=12.288MHz) and PMDAC = PMHPL = PMHPR = PMVCM = PMPLL = MCKO = M/S bits = "1", PMMIN bit = "1".
AVDD=4.2mA(typ), DVDD=3.9mA(typ).
EXT Slave Mode (PMPLL = M/S = MCKO bits = "0"): AVDD=3.5mA(typ), DVDD=2.7mA(typ).

Note 27. PMDAC = PMHPL = PMHPR = PMVCM = PMPLL = PMMIN bits = "1" and PMSPK bit = "0".

Note 28. PMDAC = PMSPK = PMVCM = PMPLL = PMMIN bits = "1" and PMHPL = PMHPR bits = "0".

Note 29. All digital input pins are fixed to DVDD or VSS3.

■ Power Consumption for each operation mode

Common Conditions: Ta=25°C; VSS1=VSS2=VSS3=0V; fs=44.1kHz, External Slave Mode, BICK=64fs; 1kHz, 0dBFS input; (PMMIN bit = "0")Headphone & Speaker = No output

Mode	Power Management Bit						Typical Current						
	00H				01H		AVDD		DVDD		HVDD		Total Power
	PMVCM	PMMIN	PMSPK	PMDAC	PMHPL	PMHPR	[V]	[mA]	[V]	[mA]	[V]	[mA]	[mW]
All Power-down	0	0	0	0	0	0	3.3	0	3.3	0	3.3	0	0
DAC → HP/Line Out	1	0	0	1	1	1	2.2	2.7	1.8	1.0	2.2	1.9	11.9
											4.0	2.6	18.1
							3.3	3.1	3.3	2.7	3.3	2.2	26.4
DAC → SPK	1	0	1	1	0	0	2.2	2.7	1.8	1.0	2.2	4.2	17.0
											4.0	5.2	28.5
							3.3	3.2	3.3	2.7	3.3	4.1	33.0

Table 1. Power Consumption for each operation mode (typ)

FILTER CHARACTERISTICS

(Ta=-30 ~ 85°C; AVDD=2.2 ~ 3.6V, DVDD=1.6 ~ 3.6V; HVDD=2.2 ~ 4.0V; fs=44.1kHz; DEM=OFF; HPF=LPF=FIL3=EQ=5-BiQuads=ALC=OFF)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF):						
Passband (Note 30)	-0.05dB −6.0dB	PB	0 -	- 22.05	20.0 -	kHz kHz
Stopband		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.02	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 31)		GD	-	25	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 30. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.454*fs (@−0.05dB). Each response refers to that of 1kHz.

Note 31. The calculated delay time caused by digital filtering. This time is from setting the 16-bit data of both channels from the input register to the output of analog signal. HPF=LPF=FIL3=EQ=5-BiQuads=ALC=OFF.

DC CHARACTERISTICS

(Ta=-30 ~ 85°C; AVDD=2.2 ~ 3.6V, DVDD=1.6 ~ 3.6V; HVDD=2.2 ~ 4.0V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	2.2V≤DVDD≤3.6V	VIH	70%DVDD	-	-	V
	1.6V≤DVDD<2.2V	VIH	80%DVDD	-	-	V
Low-Level Input Voltage	2.2V≤DVDD≤3.6V	VIL	-	-	30%DVDD	V
	1.6V≤DVDD<2.2V	VIL	-	-	20%DVDD	V
Input Voltage at AC Coupling (Note 32)		VAC	0.4	-	-	Vpp
High-Level Output Voltage	(Iout = −200μA)	VOH	DVDD−0.2	-	-	V
Low-Level Output Voltage						
	(Except SDA pin: Iout = 200μA)	VOL	-	-	0.2	V
	(SDA pin, 2.0V≤DVDD≤3.6V: Iout = 3mA)	VOL	-	-	0.4	V
	(SDA pin, 1.6V≤DVDD<2.0V: Iout = 3mA)	VOL	-	-	20%DVDD	V
Input Leakage Current		Iin	-	-	±10	μA

Note 32. MCKI is connected to a capacitor. (Figure 8)

SWITCHING CHARACTERISTICS

(Ta=-30 ~ 85°C; AVDD=2.2 ~ 3.6V, DVDD=1.6 ~ 3.6V; HVDD=2.2 ~ 4.0V;C_L=20pF; unless otherwise specified)

Parameter		Symbol	min	typ	max	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
AC Pulse Width		tACW	18.5	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter		Symbol	min	typ	max	Unit
PLL Slave Mode (PLL Reference Clock = LRCK pin)						
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period	PLL3-0 bits = “0010”	tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = “0011”	tBCK	-	1/(64fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	12.288	MHz
	512fs	fCLK	3.7632	-	13.312	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing						
Frequency	256fs	fs	7.35	-	48	kHz
	512fs	fs	7.35	-	26	kHz
	1024fs	fs	7.35	-	13	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	312.5	-	-	ns
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	12.288	MHz
	512fs	fCLK	3.7632	-	13.312	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = “0”	tBCK	-	1/(32fs)	-	ns
	BCKO bit = “1”	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (DSP Mode)					
Master Mode					
LRCK "↑" to BICK "↑" (Note 33)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
LRCK "↑" to BICK "↓" (Note 34)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK "↑" to BICK "↑" (Note 33)	tLRB	0.4 x tBCK	-	-	ns
LRCK "↑" to BICK "↓" (Note 34)	tLRB	0.4 x tBCK	-	-	ns
BICK "↑" to LRCK "↑" (Note 33)	tBLR	0.4 x tBCK	-	-	ns
BICK "↓" to LRCK "↑" (Note 34)	tBLR	0.4 x tBCK	-	-	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Audio Interface Timing (Right/Left justified & I^2S)					
Master Mode					
BICK "↓" to LRCK Edge (Note 35)	tMBLR	–40	-	40	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 35)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	50	-	-	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Note 33. MSBS, BCKP bits = "00" or "11".
Note 34. MSBS, BCKP bits = "01" or "10".
Note 35. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (3-wire Serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 37)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 37)	tCSH	50	-	-	ns
Control Interface Timing (I^2C Bus mode): (Note 36)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 38)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 39)	tPD	150	-	-	ns

Note 36. I^2C-bus is a trademark of NXP B.V.
Note 37. CCLK rising edge must not occur at the same time as CSN edge.
Note 38. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 39. The AK4373 can be reset by the PDN pin = "L".

■ Timing Diagram

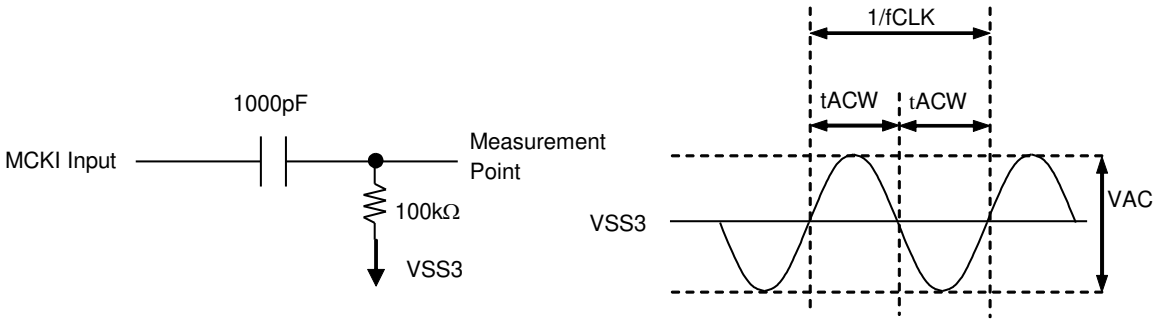


Figure 8. MCKI AC Coupling Timing

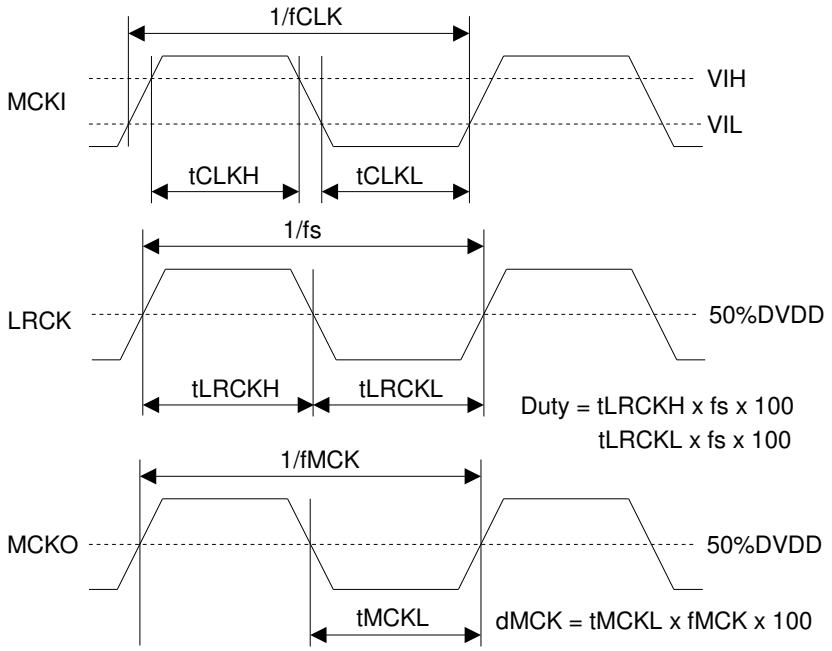


Figure 9. Clock Timing (PLL/EXT Master mode)

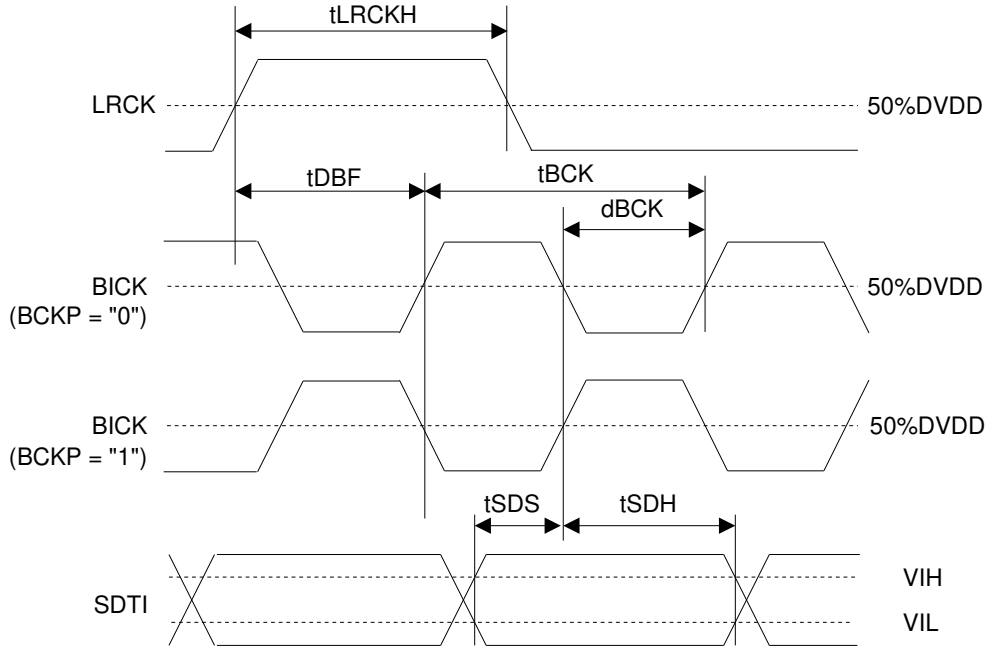


Figure 10. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = “0”)

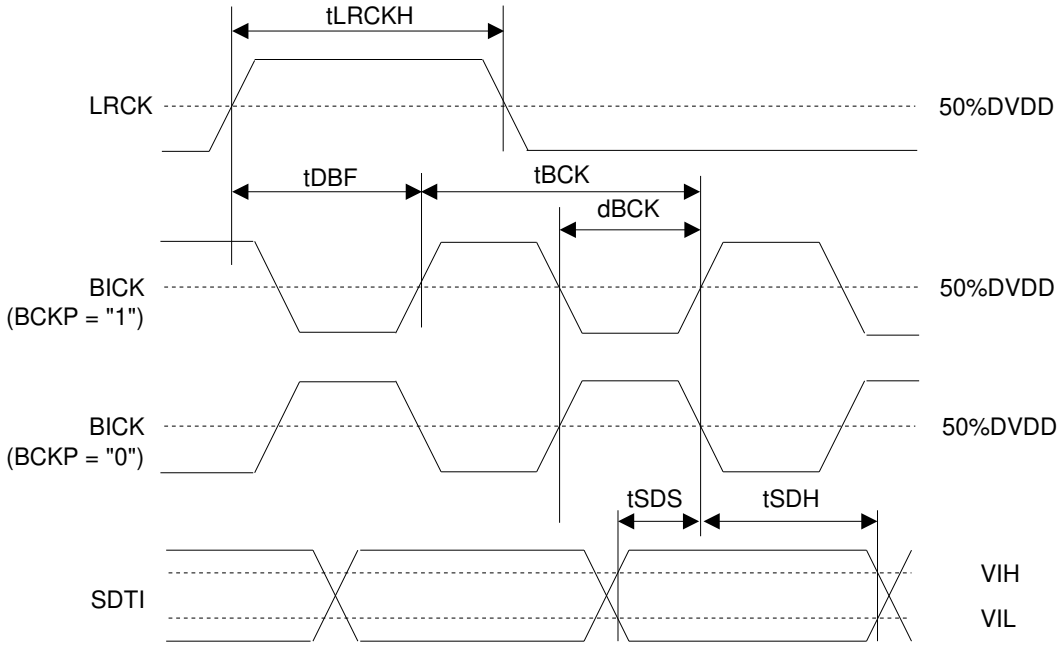


Figure 11. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = "1")

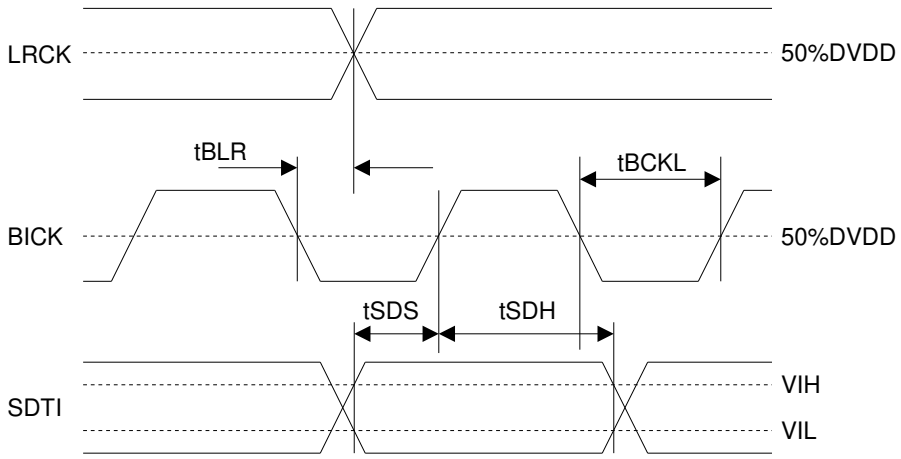


Figure 12. Audio Interface Timing (PLL/EXT Master mode, Except DSP mode)

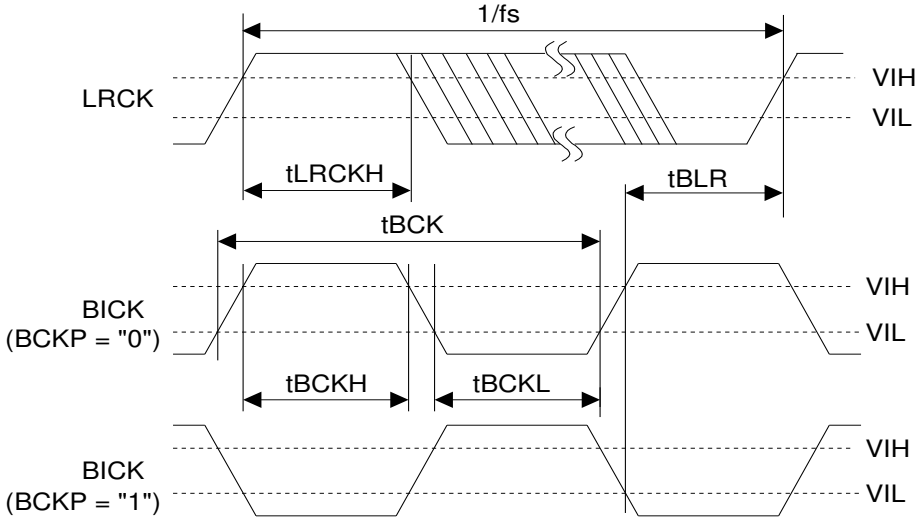


Figure 13. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = "0")

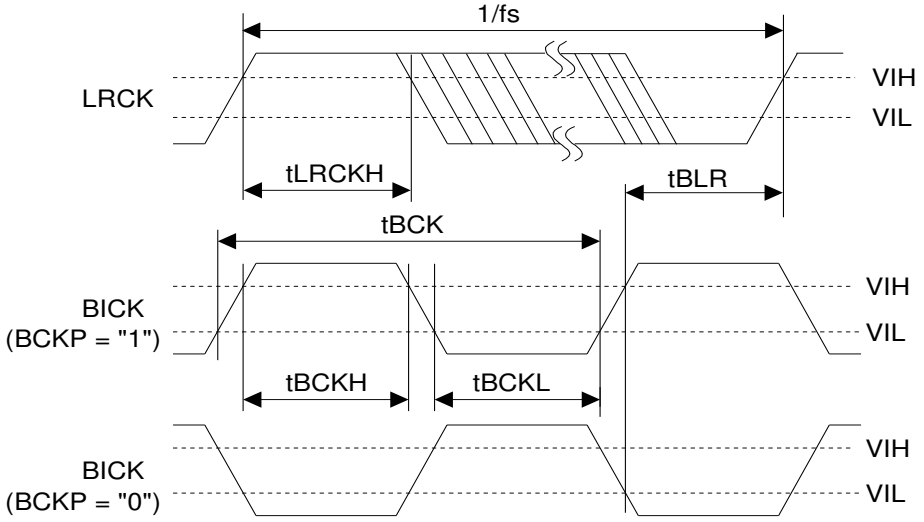


Figure 14. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = "1")

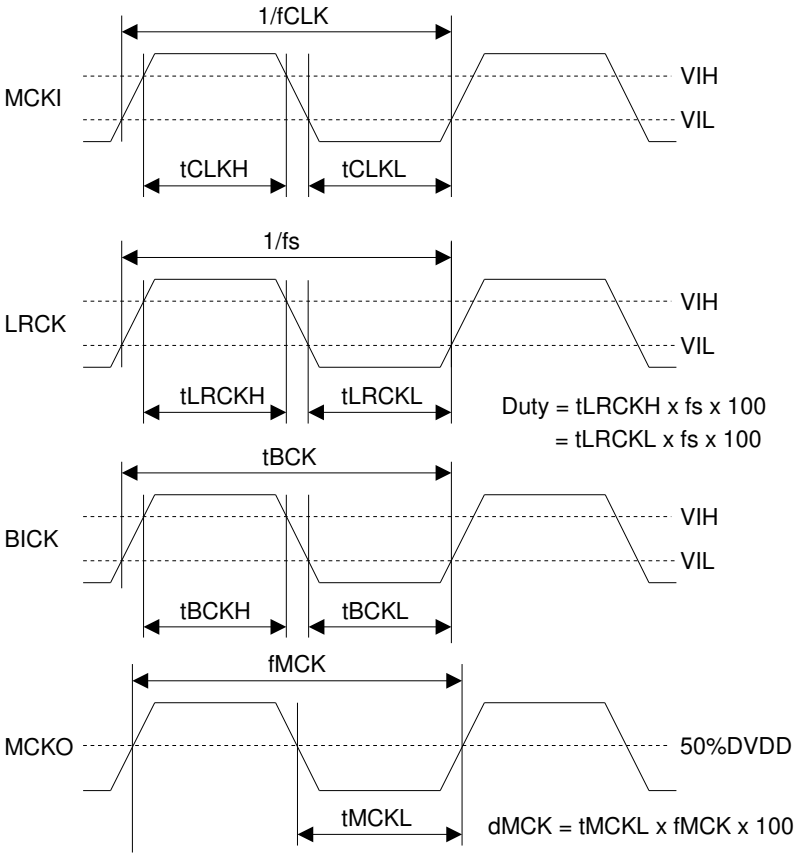


Figure 15. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin, Except DSP mode)

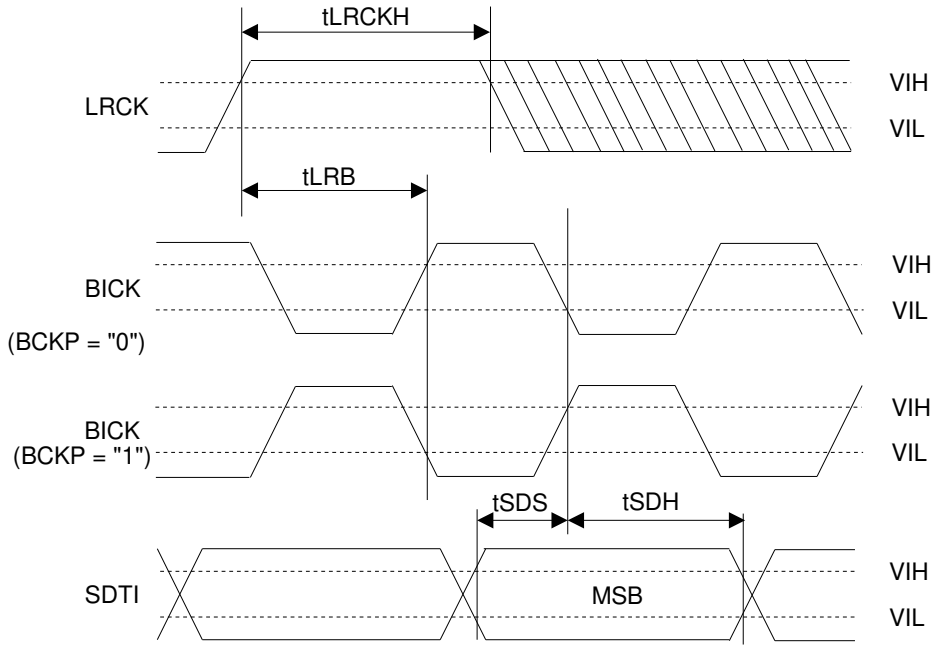


Figure 16. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = “0”)