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AK4376A

Low-Power Advanced 32-bit DAC with HP

1. General Description

The AK4376A is stereo advanced 32-bit high sound quality audio DAC with a built-in ground-referenced headphone amplifier. An internal circuit newly developed 32-bit digital filters for better sound quality, achieving low distortion characteristics and wide dynamic range. The sampling frequency supports up to 384 kHz. The AK4376A is available in a 36-pin CSP package, utilizing less board space than competitive offerings.

2. Features

1. Stereo High Sound Quality Low Power Advanced 32-bit DAC
- **4 types of Digital Filter for Sound Color Selection**
- **2 types of Operation Mode (High Performance Mode / Low Power Mode)**

2. Ground-referenced Class-G Stereo Headphone-Amp
- **Output Power: 25 mW @ 32Ω, THD+N < –60 dB**
  45 mW @ 16Ω, THD+N < –60 dB
- **THD+N: –107 dB**
- **S/N: 125 dB**
- **Output Noise Level: –125 dBV (Analog Volume ≤ –14 dB)**
- **Analog Volume: +6 to –20 dB & Mute, 2 dB Step**
- **Ground Loop Noise Cancellation**

3. HeadPhone-Amp Output comply with IEC61000-4-2 Level4 ESD Protection

4. Digital Audio interface
- **Master/Slave mode**
- **Sampling Frequency:**
  Slave Mode: 8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 128 k,176.4 k, 192 kHz, 256 k, 352.8 k, 384 kHz
  Master Mode: 8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 176.4 k, 192 kHz
- **Interface Format: 32/24/16-bit I^2S/MSB justified**

5. Power Management

6. PLL

7. X'tal Oscillator

8. µP I/F: I^2C (400 kHz)

9. Ta = –40 to 85°C

10. Power Supply:
- **AVDD (DAC, PLL): 1.7 to 1.9 V**
- **CVDD (HP-Amp, Charge Pump): 1.7 to 1.9 V**
- **LVDD (LDO2 for Digital Core): 1.7 to 1.9 V (built-in LDO)**
- **TVDD (Audio I/F): 1.65 to 3.6 V**

11. Package: 36-pin CSP (2.74 x 2.56 mm, 0.4 mm pitch)

3. Table of Contents

4. Block Diagram and Functions

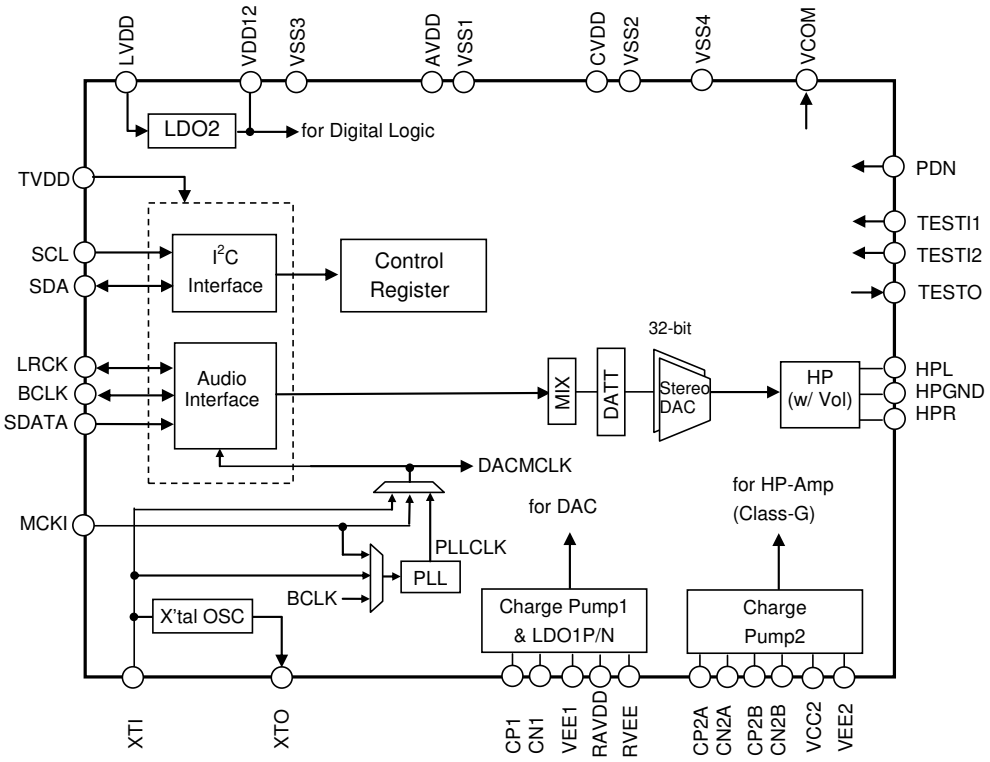
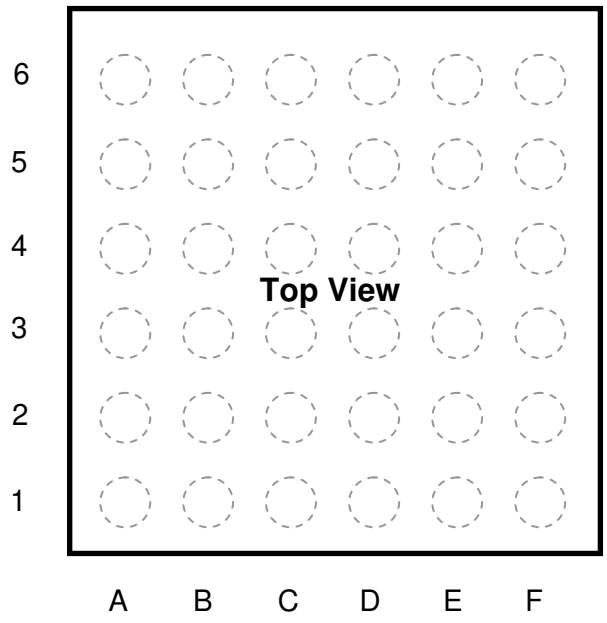


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations

36-pin CSP (2.74 x 2.56 mm, 0.4 mm pitch)



6	VDD12	SDATA	LVDD	VEE1	CN1	CVDD
5	VSS3	LRCK	PDN	CP1	CP2B	CN2B
4	BCLK	TVDD	TESTI1	VSS2	CP2A	CN2A
3	MCKI	SDA	TESTI2	TESTO	VCC2	VEE2
2	XTO	SCL	VSS4	VSS1	HPGND	HPR
1	XTI	RAVDD	RVEE	AVDD	VCOM	HPL
	A	**B**	**C**	**D**	**E**	**F**

Top View

■ Pin Functions

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Power Supply					
D1	AVDD	-	Analog Power Supply Pin		AVDD
D2	VSS1	-	Analog Ground Pin		
F6	CVDD	-	HP-Amp/Charge Pump Power Supply Pin		CVDD
D4	VSS2	-	HP-Amp/Charge Ground Pin		
C6	LVDD	-	Digital Core & LDO2 Power Supply Pin		LVDD
A5	VSS3	-	Digital Ground Pin		
C2	VSS4	-	Substrate Pin		
B4	TVDD	-	Digital I/F Power Supply Pin		TVDD
E1	VCOM	O	Common Voltage Output Pin This pin must be connected to the VSS1 pin with a 10 μF ±50% Ceramic capacitor in series.	AVDD/ VSS1	
A6	VDD12	-	LDO2 (1.2 V) Output Power Supply Pin (Note 1) This pin must be connected to the VSS3 pin with a capacitor in series.	LVDD/ VSS1	LVDD

Note 1. Capacitor value for the VDD12 pin should be selected from 2.2 μF±50% to 4.7 μF±50%.
Note 2. Do not connect a load to VCOM pin and VDD12 pin.

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Charge Pump & LDO					
E3	VCC2	O	Charge Pump Circuit Positive Voltage Output Pin (CVDD or 1/2*CVDD) This pin must be connected to the VSS2 pin with a 2.2 μF ±50% capacitor in series.	CVDD/ VSS2	CVDD
E4	CP2A	O	Positive Charge-Pump Capacitor Terminal 2A Pin This pin must be connected to the CN2A pin with a 2.2 μF ±50% capacitor in series.	CVDD/ VSS2	CVDD
F4	CN2A	I	Negative Charge Pump Capacitor Terminal 2A Pin This pin must be connected to the CP2A pin with a 2.2 μF ±50% capacitor in series.	CVDD	CVDD
E5	CP2B	O	Positive Charge Pump Capacitor Terminal 2B Pin This pin must be connected to the CN2B pin with a 2.2 μF ±50% capacitor in series.	CVDD/ VSS2	CVDD
F5	CN2B	I	Negative Charge Pump Capacitor Terminal 2B Pin This pin must be connected to the CP2B pin with a 2.2 μF ±50% capacitor in series.	CVDD	CVDD
F3	VEE2	O	Charge Pump Circuit Negative Voltage (−CVDD or −1/2*CVDD) Output 2 Pin This pin must be connected to the VSS2 pin with a 2.2 μF ±50% capacitor in series.	CVDD/ VSS2	
D5	CP1	O	Positive Charge Pump Capacitor Terminal 1 Pin This pin must be connected to the CN1 pin with a 1 μF ±50% capacitor in series.	CVDD/ VSS2	CVDD
E6	CN1	I	Negative Charge Pump Capacitor Terminal 1 Pin This pin must be connected to the CP1 pin with a 1 μF ±50% capacitor in series.	CVDD	CVDD
D6	VEE1	O	Charge Pump Circuit Negative Voltage (−CVDD) Output 1 Pin This pin must be connected to the VSS2 pin with a 1 μF ±50% capacitor in series.	CVDD/ VSS2	
B1	RAVDD	O	LDO1P (1.5V) Output Pin (Note 3) This pin must be connected to the VSS1 pin with a capacitor in series.	AVDD/ VSS1	
C1	RVEE	O	LDO1N (−1.5V) Output Pin (Note 3) This pin must be connected to the VSS1 pin with a capacitor in series.	AVDD/ VSS1	

Note 3. Capacitor values for the RAVDD pin and RVEE pin should be selected from 1 μF±50% to 4.7 μF±50%.

Note 4. Do not connect a load to VEE1 pin, VCC2 pin, VEE2 pin, RAVDD pin and RVEE pin.

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
Control Interface					
B2	SCL	I	I^2C Serial Data Clock Pin	TVDD/ VSS3	TVDD
B3	SDA	I/O	I^2C Serial Data Input/Output Pin	TVDD/ VSS3	TVDD
Audio Interface					
A3	MCKI	I	External Master Clock Input Pin	TVDD/ VSS3	TVDD
A1	XTI	I	X'tal Oscillator Input Pin	AVDD/ VSS1	AVDD
A2	XTO	O	X'tal Oscillator Output Pin	AVDD/ VSS1	AVDD
A4	BCLK	I/O	Audio Serial Data Clock Pin	TVDD/ VSS3	TVDD
B5	LRCK	I/O	Frame Sync Clock Pin	TVDD/ VSS3	TVDD
B6	SDATA	I	Audio Serial Data Input Pin	TVDD/ VSS3	TVDD
Analog Output					
F1	HPL	O	Lch Headphone-Amp Output Pin	CVDD/ VEE2	CVDD/ VEE2
F2	HPR	O	Rch Headphone-Amp Output Pin	CVDD/ VEE2	CVDD/ VEE2
E2	HPGND	I	Headphone-Amp Ground Loop Noise Cancellation Pin	-	-
Others					
C5	PDN	I	Power down Pin "L": Power-down, "H": Power-up	TVDD/ VSS3	TVDD
C4	TESTI1	I	Test Input Pin It must be tied "L".	TVDD/ VSS3	TVDD
D3	TESTO	O	Test Output Pin	AVDD/ VSS1	AVDD
C3	TESTI2	I	Test Input Pin It must be tied "L".	TVDD/ VSS3	TVDD

Note 5. All input pins except analog input pin must not be allowed to float. I/O pin should be connected appropriately.

■ Handing of Unused Pins

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	HPL, HPR, XTO	Open
	XTI	Open (PMOSC bit is fixed to "0")
Digital	TESTO	Open
	MCKI, TESTI1, TESTI2	Connect to VSS3

6. Absolute Maximum Ratings

(VSS1 = VSS2 = VSS3 = VSS4 = 0 V; Note 7, Note 8)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies: (Note 6)	Analog	AVDD	−0.3	4.3	V
	HP-Amp/Charge Pump	CVDD	−0.3	4.3	V
	LDO2 for Digital Core	LVDD	−0.3	4.3	V
	Digital I/F	TVDD	−0.3	4.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 9)		VINA	−0.3	AVDD+0.3 or 4.3	V
Digital Input Voltage (Note 10)		VIND	−0.3	TVDD+0.3 or 4.3	V
Ambient Temperature (powered applied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 6. Charge pump 1 & 2 are not in operation. In the case that charge pump 1 & 2 are in operation, the maximum values of AVDD and CVDD become 2.15 V.

Note 7. All voltages with respect to ground.

Note 8. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog plane.

Note 9. XTI pin

The maximum value of input voltage is lower value between (AVDD+0.3)V and 4.3V.

Note 10. MCKI, BCLK, LRCK, SDATA, SCL, SDA, PDN, TESTI1, TESTI2 pins

The maximum value of input voltage is lower value between (TVDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal Operation is not guranteed at these extremes.

7. Recommended Operating Conditions

(VSS1 = VSS2 = VSS3 = VSS4 = 0 V; Note 11)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power supplies (Note 12)	Analog	AVDD	1.7	1.8	1.9	V
	HP-Amp / Charge Pump	CVDD	1.7	1.8	1.9	V
	LDO2 for Digital Core	LVDD	1.7	1.8	1.9	V
	Digital I/F	TVDD	1.65	1.8	3.6	V

Note 11. All voltages with respect to ground.

Note 12. Each power up/down sequence is shown below.

<Power-up>

1. PDN pin = “L”
2. TVDD, AVDD, LVDD, CVDD
   (AVDD must be powered up before or at the same time of CVDD. The power-up sequence of TVDD and LVDD is not critical.)
3. The PDN pin is allowed to be “H” after all power supplies are applied and settled.

<Power-down>

1. PDN pin = “L”
2. TVDD, AVDD, LVDD, CVDD
   (CVDD must be powered down before or at the same time of AVDD. The power-down sequence of TVDD and LVDD is not critical.)

8. Electrical Characteristics

■ Analog Characteristics

(Ta = 25°C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V; Signal Frequency = 1 kHz; 24-bit Data; fs = 44.1 kHz, BCLK = 64 fs; Measurement Bandwidth = 20 Hz to 20 kHz; unless otherwise specified)

<High Performance Mode>

Parameter		Min.	Typ.	Max.	Unit
Stereo DAC Characteristics:					
Resolution		-	-	32	Bit
Headphone-Amp Characteristics: DAC (Stereo) → HPL/HPR pins, OVL/R = 0 dB, HPG = 0 dB, R_L = 32Ω					
Output Power					
0 dBFS, R_L = 32Ω, HPG = 0 dB, THD+N < −60 dB		-	25	-	mW
0 dBFS, R_L = 32Ω, HPG = −4 dB		-	10	-	mW
0 dBFS, R_L = 16Ω, HPG = 0 dB, THD+N < −60 dB		-	45	-	mW
−1.5 dBFS, R_L = 16Ω, HPG = +2 dB, THD+N < −20 dB		-	60	-	mW
Output Level (0 dBFS, R_L = 32Ω, HPG = −4 dB)		0.52	0.57	0.61	Vrms
THD+N					
0 dBFS, R_L = 32Ω, OVL/R = −4 dB, HPG = 0 dB (Po = 10 mW)	fs = 44.1 kHz BW = 20 kHz	-	−107	-	dB
	fs = 96 kHz BW = 40 kHz	-	−103	-	dB
	fs = 192 kHz BW = 40 kHz	-	−103	-	dB
	fin = 10kHz fs = 44.1kHz BW = 20kHz	-	−104	-	dB
0 dBFS, R_L = 32Ω, OVL/R = −10 dB, HPG = 0 dB (Po = 2.5 mW)	fs = 44.1 kHz BW = 20 kHz	-	−100	−90	dB
0 dBFS, R_L = 16Ω, OVL/R = −4 dB, HPG = 0 dB (Po = 20 mW)	fs = 44.1 kHz BW = 20 kHz	-	−106	-	dB
−4 dBFS, R_L = 600Ω, HPG = +6 dB, (Po = 2.0 mW @ 1.1Vrms)	fs = 44.1 kHz BW = 20 kHz	-	−99	-	dB

Parameter		Min.	Typ.	Max.	Unit
Dynamic Range −60 dBFS, A-weighted, HPG = 0 dB		108	116	-	dB
S/N (A-weighted, Noise Gate Enable) Po = 25 mW, HPG = 0 dB (Data = 0 dBFS / "0" Data)		-	125	-	dB
S/N (A-weighted, Noise Gate Disable) Po = 25 mW, HPG = 0 dB (Data = 0 dBFS / "0" Data)		108	116	-	dB
Output Noise Level (Noise Gate Enable, A-weighted)		-	−126	-	dBV
Output Noise Level (Noise Gate Disable, A-weighted, HPG ≤ −14 dB)		-	−125	-	dBV
Interchannel Isolation 0 dBFS, HPG = −4 dB (Po = 10 mW) External Impedance = 0.01Ω (Note 13) External Impedance = 0.1Ω (Note 13)		 80 -	 100 80	 - -	 dB dB
Interchannel Gain Mismatch		-	0	0.8	dB
Load Resistance		14.4	32	-	Ω
Load Capacitance		-	-	1000	pF
Load Inductance		-	-	0.375	μH
PSRR (HPG = −4 dB) (Note 14) 217 Hz 1 kHz		 - -	 85 85	 - -	 dB dB
DC-offset (Note 15) HPG = 0 dB HPG = All Gain		 −0.25 −0.4	 0 0	 +0.25 +0.4	 mV mV
Headphone Output Volume Characteristics:					
Gain Setting		−20	-	+6	dB
Step Width	Gain: +6 to −20 dB	1	2	3	dB

Note 13. Impedance between the HPGND pin and the system ground.
Note 14. PSRR is referred to all power supplies with 100 mVpp sine wave.
Note 15. When there is no gain change and temperature drift after HP-Amp is powered up.

Parameter	Value	Unit
ESD Immunity IEC61000-4-2 Level4, Contact (Note 16)	±8	kV

Note 16. It is measured at the HPL and HPR pins on an evaluation board (AKD4376A-SC Rev.1).

<Low Power Mode>

Parameter			Min.	Typ.	Max.	Unit
Headphone-Amp Characteristics: DAC(Stereo) → HPL/HPR pins, OVL/R = 0 dB, HPG = 0 dB, R_L = 32Ω						
Output Power						
0 dBFS, R_L = 32Ω, HPG = 0 dB, THD+N < −60 dB			-	25	-	mW
0 dBFS, R_L = 32Ω, HPG = −4 dB			-	10	-	mW
0 dBFS, R_L = 16Ω, HPG = 0 dB, THD+N < −60 dB			-	45	-	mW
−1.5 dBFS, R_L = 16Ω, HPG = +2 dB, THD+N < −20 dB			-	60	-	mW
Output Level (0 dBFS, R_L = 32Ω, HPG = −4 dB)			0.52	0.57	0.61	Vrms
THD+N						
0 dBFS, R_L = 32Ω, HPG = −4 dB (Po = 10 mW)		fs = 44.1 kHz BW = 20 kHz	-	−92	-	dB
0dBFS, R_L = 16Ω, HPG = −4dB (Po = 20 mW)		fs = 44.1 kHz BW = 20 kHz	-	−92	-	dB
−4dBFS,R_L = 600Ω,HPG = + 6dB (Po = 2.0 mW @ 1.1 Vrms)		fs = 44.1 kHz BW = 20 kHz	-	−98	-	dB
Dynamic Range (−60 dBFS, A-weighted, HPG = 0 dB, Data = 0 dBFS)			-	113	-	dB
S/N (A-weighted) Po = 25 mW, HPG = 0 dB (Data = 0 dBFS / "0" Data)			-	113	-	dB
Interchannel Isolation 0 dBFS, HPG = −4 dB (Po = 10 mW)						
External Impedance = 0.01Ω (Note 17)			80	100	-	dB
External Impedance = 0.1Ω (Note 17)			-	80	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Load Resistance			14.4	32	-	Ω
Load Capacitance			-	-	1000	pF
Load Inductance			-	-	0.375	μH
PSRR (HPG = −4 dB) (Note 18)						
217 Hz			-	85	-	dB
1 kHz			-	85	-	dB
DC-offset (Note 19)						
HPG = 0 dB			−0.35	0	+0.35	mV
HPG = All Gain			−0.5	0	+0.5	mV
Headphone Output Volume Characteristics:						
Gain Setting			−20	-	+6	dB
Step Width	Gain: +6 to −20 dB		1	2	3	dB

Note 17. Impedance between the HPGND pin and the system ground.
Note 18. PSRR is referred to all power supplies with 100 mVpp sine wave.
Note 19. When there is no gain change and temperature drift after HP-Amp is powered up.

■ PLL Characteristics

(Ta = –40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; unless otherwise specified)

Parameter	Min.	Typ.	Max.	Unit
PLL Characteristics				
Reference Clock (Figure 11)	0.256	-	3.072	MHz
Output Frequency (PLLCLK) (Figure 11)				
44.1 kHz * 256fs * 9	-	101.606	-	MHz
48.0 kHz * 256fs * 9	-	110.592	-	MHz
44.1 kHz * 256fs * 10	-	112.896	-	MHz
48.0 kHz * 256fs * 10	-	122.880	-	MHz
Lock Time	-	-	2	ms

■ Charge Pump & LDO Circuit Power-up Time

(Ta = -40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; unless otherwise specified)

Parameter	Capacitor	Min.	Typ.	Max.	Unit
Block power up time					
CP1 (Note 20)	1 μF @ VEE1	-	-	6.5	ms
CP2 (Class-G) (Note 20, Note 21)	2.2 μF @ VEE2	-	-	4.5	ms
LDO1P (Note 22)	1 μF @ RAVDD	-	-	1	ms
LDO1N (Note 22)	1 μF @ RVEE	-	-	1	ms
LDO2 (Note 20)	2.2 μF @ VDD12	-	-	1	ms

Note 20. Power up time is a fixed value that is not affected by a capacitor.

Note 21. Power up time is a value to -1/2CVDD, since CP2 starts with 1/2 VDD Mode as part of Class-G operation.

Note 22. Power-up time is proportional to a capacitor value.
For instance, if a 2.2 μF capacitor is connected to the RVEE pin, LDO1N power-up time is 2.2ms (max.).

■ Power Supply Current

(Ta = 25°C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = VSS4 = HPGND = 0 V, BCLK = 64fs; Slave Mode, No Data input, R_L = 32Ω; unless otherwise specified)

Parameter	Min.	Typ.	Max.	Unit
Power Supply Current:				
Power Up (PDN pin = "H", All Circuits Power-up) (Note 23)				
AVDD+ CVDD + LVDD + TVDD	-	23	-	mA
Power Up (PDN pin = "H", DAC+HP-amp Power-Up, PLL & X'tal OSC Power Down) (Note 24)				
AVDD+ CVDD + LVDD + TVDD	-	20	30	mA
Power Down (PDN pin = "L")				
AVDD + CVDD + LVDD + TVDD	-	0	10	μA

Note 23. DAC, HP-Amp, PLL and X'tal OSC are all powered up.

Note 24. All digital input pins are fixed to TVDD or VSS3.

■ Power Consumptions for Each Operation Mode

(Ta = 25°C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = VSS4 = 0 V; MCKI = 256fs, BCLK = 64fs; Slave Mode, No data input, R_L = 32Ω, X'tal OSC Power-down)

<High Performance Mode>

	AVDD [mA]	CVDD [mA]	LVDD [mA]	TVDD [mA]	Total Power [mW]
DAC → HP (fs = 44.1 kHz)	8.38	11.34	0.47	0.02	36.32
DAC → HP (fs = 96 kHz)	8.38	11.34	0.57	0.02	36.55
DAC → HP (fs = 192 kHz)	8.38	11.34	0.62	0.02	36.64

<Low Power Mode>

	AVDD [mA]	CVDD [mA]	LVDD [mA]	TVDD [mA]	Total Power [mW]
DAC → HP (fs = 44.1 kHz)	3.23	4.03	0.36	0.02	13.75

■ DAC Sharp Roll-Off Filter (fs = 44.1 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 44.1 kHz; DASD bit = "0", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter(LPF):						
Passband (Note 25)	−0.006 to +0.124 dB −6.0 dB	PB	0 -	- 22.05	20.42 -	kHz kHz
Stopband (Note 25)		SB	24.1	-	-	kHz
Passband Ripple		PR	−0.006	-	+0.124	dB
Stopband Attenuation (Note 26)		SA	69.9	-	-	dB
Group Delay (Note 27)		GD	-	26	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode :						
Frequency Response: 0 to 20.0 kHz		FR	−0.12	-	+0.03	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode :						
Frequency Response: 0 to 20.0 kHz		FR	−0.68	-	+0.03	dB

Note 25. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4630 x fs (@−0.006 /+0.124 dB), SB = 0.5465 x fs. Each frequency response refers to that of 1 kHz.

Note 26. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 27. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Sharp Roll-Off Filter (fs = 96 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 96 kHz; DASD bit = "0", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter(LPF):						
Passband (Note 28)	−0.003 to +0.127 dB −6.0 dB	PB	0 -	- 48.01	44.4 -	kHz kHz
Stopband (Note 28)		SB	52.5	-	-	kHz
Passband Ripple		PR	−0.003	-	+0.127	dB
Stopband Attenuation (Note 29)		SA	69.9	-	-	dB
Group Delay (Note 30)		GD	-	26	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode :						
Frequency Response: 0 to 40.0 kHz		FR	−0.72	-	+0.11	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode :						
Frequency Response: 0 to 40.0 kHz		FR	−2.18	-	+0.10	dB

Note 28. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4625 x fs (@−0.003/+0.127 dB), SB = 0.547 x fs. Each frequency response refers to that of 1 kHz.

Note 29. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 30. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Sharp Roll-Off Filter (fs = 192 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 192 kHz; DASD bit = "0", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter(LPF):						
Passband (Note 31)	−0.002 to +0.13 dB	PB	0	-	88.94	kHz
	−6.0 dB		-	96.01	-	kHz
Stopband (Note 31)		SB	105	-	-	kHz
Passband Ripple		PR	−0.002	-	+0.13	dB
Stopband Attenuation (Note 32)		SA	69.9	-	-	dB
Group Delay (Note 33)		GD	-	26	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode :						
Frequency Response: 0 to 80.0 kHz		FR	−2.90	-	+0.35	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode :						
Frequency Response: 0 to 80.0 kHz		FR	−6.42	-	+0.35	dB

Note 31. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4538 x fs (@−0.002/+0.13 dB), SB = 0.5469 x fs. Each frequency response refers to that of 1 kHz.

Note 32. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 33. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Slow Roll-Off Filter (fs = 44.1 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 44.1 kHz; DASD bit = "0", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter(LPF):						
Passband (Note 34)	−0.07 to +0.006 dB	PB	0	-	7.7	kHz
	−3.0 dB		-	18.34	-	kHz
Stopband (Note 34)		SB	39.1	-	-	kHz
Passband Ripple		PR	−0.07	-	+0.006	dB
Stopband Attenuation (Note 35)		SA	72.8	-	-	dB
Group Delay (Note 36)		GD	-	26	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode :						
Frequency Response: 0 to 20.0 kHz		FR	−4.44	-	+0.03	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode :						
Frequency Response: 0 to 20.0 kHz		FR	−5.00	-	+0.03	dB

Note 34. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.1746 × fs (@−0.07/+0.006 dB), SB = 0.887 x fs. Each frequency response refers to that of 1 kHz.

Note 35. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 36. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Slow Roll-Off Filter (fs = 96 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 96 kHz; DASD bit = "0", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 37)	−0.07 to +0.007 dB	PB	0	-	16.76	kHz
	−3.0 dB		-	39.9	-	kHz
Stopband (Note 37)		SB	85.2	-	-	kHz
Passband Ripple		PR	−0.07	-	+0.007	dB
Stopband Attenuation (Note 38)		SA	72.8	-	-	dB
Group Delay (Note 39)		GD	-	26	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode:						
Frequency Response: 0 to 40.0 kHz		FR	−4.00	-	+0.10	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode:						
Frequency Response: 0 to 40.0 kHz		FR	−5.46	-	+0.10	dB

Note 37. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.1746 × fs (@−0.07/+0.007 dB), SB = 0.887 x fs. Each frequency response refers to that of 1 kHz.

Note 38. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 39. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ **DAC Slow Roll-Off Filter (fs = 192 kHz)**

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 192 kHz; DASD bit = "0", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 40)	−0.07 to +0.007 dB	PB	0	-	33.56	kHz
	−3.0 dB		-	79.9	-	kHz
Stopband (Note 40)		SB	170.3	-	-	kHz
Passband Ripple		PR	−0.07	-	+0.007	dB
Stopband Attenuation (Note 41)		SA	72.8	-	-	dB
Group Delay (Note 42)		GD	-	26	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode :						
Frequency Response: 0 to 80.0 kHz		FR	−6.00	-	+0.35	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode :						
Frequency Response: 0 to 80.0 kHz		FR	−9.47	-	+0.35	dB

Note 40. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.1748 × fs (@−0.07/+0.007 dB), SB = 0.887 x fs. Each frequency response refers to that of 1 kHz.

Note 41. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 42. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Short Delay Sharp Roll-Off Filter (fs = 44.1 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 44.1 kHz; DASD bit = "1", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 43)	−0.008 to +0.126 dB −6.0 dB	PB	0 -	- 22.18	20.4 -	kHz kHz
Stopband (Note 43)		SB	24.1	-	-	kHz
Passband Ripple		PR	−0.008	-	+0.126	dB
Stopband Attenuation (Note 44)		SA	56.4	-	-	dB
Group Delay (Note 45)		GD	-	5.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode :						
Frequency Response: 0 to 20.0 kHz		FR	−0.12	-	+0.03	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode :						
Frequency Response: 0 to 20.0 kHz		FR	−0.68	-	+0.03	dB

Note 43. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4626 × fs (@−0.008/+0.126 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 44. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 45. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Short Delay Sharp Roll-Off Filter (fs = 96 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 96 kHz; DASD bit = "1", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 46)	−0.003 to +0.132dB −6.0 dB	PB	0 -	- 48.28	44.4 -	kHz kHz
Stopband (Note 46)		SB	52.5	-	-	kHz
Passband Ripple		PR	−0.003	-	+0.132	dB
Stopband Attenuation (Note 47)		SA	56.4	-	-	dB
Group Delay (Note 48)		GD	-	5.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode:						
Frequency Response: 0 to 40.0 kHz		FR	−0.90	-	+0.11	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode:						
Frequency Response: 0 to 40.0 kHz		FR	−2.36	-	+0.10	dB

Note 46. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4625 × fs (@−0.003/+0.132 dB), SB = 0.5465 × fs. Each frequency response refers to that of 1 kHz.

Note 47. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 48. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Short Delay Sharp Roll-Off Filter (fs = 192 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 192 kHz; DASD bit = "1", DASL bit = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 49)	−0.001 to +0.135 dB −6.0 dB	PB	0 -	- 96.57	88.8 -	kHz kHz
Stopband (Note 49)		SB	105	-	-	kHz
Passband Ripple		PR	−0.001	-	+0.135	dB
Stopband Attenuation (Note 50)		SA	56.4	-	-	dB
Group Delay (Note 51)		GD	-	5.5	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode :						
Frequency Response: 0 to 80.0 kHz		FR	−3.00	-	+0.36	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode :						
Frequency Response: 0 to 80.0 kHz		FR	−6.52	-	+0.35	dB

Note 49. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.4625 × fs (@−0.001/+0.135 dB), SB = 0.5469 × fs. Each frequency response refers to that of 1 kHz.

Note 50. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 51. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Short Delay Slow Roll-Off Filter (fs = 44.1 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 44.1 kHz; DASD bit = "1", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 52)	−0.07 to +0.025 dB	PB	0	-	8.83	kHz
	−3.0 dB		-	18.72	-	kHz
Stopband (Note 52)		SB	39.5	-	-	kHz
Passband Ripple		PR	−0.07	-	+0.025	dB
Stopband Attenuation (Note 53)		SA	75.1	-	-	dB
Group Delay (Note 54)		GD	-	4.7	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode :						
Frequency Response: 0 to 20.0 kHz		FR	−4.16	-	+0.05	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode :						
Frequency Response: 0 to 20.0 kHz		FR	−4.66	-	+0.03	dB

Note 52. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.2002 × fs (@−0.07/+0.025 dB), SB = 0.8957 × fs. Each frequency response refers to that of 1 kHz.

Note 53. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 54. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Short Delay Slow Roll-Off Filter (fs = 96 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 96 kHz; DASD bit = "1", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 55)	−0.07 to +0.027 dB	PB	0	-	19.29	kHz
	−3.0 dB		-	40.78	-	kHz
Stopband (Note 55)		SB	86	-	-	kHz
Passband Ripple		PR	−0.07	-	+0.027	dB
Stopband Attenuation (Note 56)		SA	75.1	-	-	dB
Group Delay (Note 57)		GD	-	4.7	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode :						
Frequency Response: 0 to 40.0 kHz		FR	−3.80	-	+0.10	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode :						
Frequency Response: 0 to 40.0 kHz		FR	−5.26	-	+0.10	dB

Note 55. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.2009 × fs (@−0.07/+0.027 dB), SB = 0.8958 × fs. Each frequency response refers to that of 1 kHz.

Note 56. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 57. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DAC Short Delay Slow Roll-Off Filter (fs = 192 kHz)

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; fs = 192 kHz; DASD bit = "1", DASL bit = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 58)	−0.07 to +0.027 dB	PB	0	-	38.63	kHz
	−3.0 dB		-	81.57	-	kHz
Stopband (Note 58)		SB	172	-	-	kHz
Passband Ripple		PR	−0.07	-	+0.027	dB
Stopband Attenuation (Note 59)		SA	75.1	-	-	dB
Group Delay (Note 60)		GD	-	4.7	-	1/fs
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ High performance mode:						
Frequency Response: 0 to 80.0 kHz		FR	−5.90	-	+0.35	dB
DAC Digital Filter (LPF) + DACANA (Headphone-Amp) @ Low power mode:						
Frequency Response: 0 to 80.0 kHz		FR	−9.38	-	+0.35	dB

Note 58. The passband and stopband frequencies scale with fs (system sampling rate).
PB = 0.2012× fs (@−0.07/+0.027 dB), SB = 0.8958 × fs. Each frequency response refers to that of 1 kHz.

Note 59. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 60. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for Lch of SDATA to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

■ DC Characteristics

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
I/O Pins (Note 61)					
High-Level Input Voltage					
Except for XTI pin	VIH	70 %TVDD	-	-	V
XTI pin	VIH	70 %AVDD	-	-	V
Low-Level Input Voltage					
Except for XTI pin	VIL	-	-	30 %TVDD	V
XTI pin	VIL	-	-	30 %AVDD	V
High-Level Output Voltage (Iout = −200 μA)	VOH	TVDD −0.2	-	-	V
Low-Level Output Voltage					
Except for SDA, XTO pin, Iout = 200 μA	VOL	-	-	0.2	V
SDA pin					
2 V < TVDD ≤ 3.6 V (Iout = 3 mA)	VOL	-	-	0.4	V
1.65 V ≤ TVDD ≤ 2 V (Iout = 2 mA)	VOL	-	-	20 %TVDD	V
Input Leakage Current	Iin	−5	-	+5	μA

Note 61. MCKI, BCLK, LRCK, SDATA, SCL, SDA, PDN, TESTI1, TESTO, TESTI2 pins

■ Switching Characteristics

(Ta = −40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; C_L = 80 pF; unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCKI					
Input Frequency	fMCK	0.256	-	28.8	MHz
Pulse Width Low	tMCKL	0.4 / fMCK	-	-	ns
Pulse Width High	tMCKH	0.4 / fMCK	-	-	ns
X'tal Oscillator (XTI pin)					
Input Frequency	fMCK	11.2896	-	24.576	MHz
Audio Interface Timing					
Master Mode					
LRCK Output Timing					
Frequency (Note 62)	fs	8	-	192	kHz
Pulse Width High	Duty	-	50	-	%
BCLK Output Timing					
Period (BCKO bit = "0")	tBCK	-	1/(64fs)	-	ns
(BCKO bit = "1")	tBCK	-	1/(32fs)	-	ns
Duty	Duty	-	50	-	%
BCLK "↓" to LRCK Edge	tBSYD	−20	-	20	ns
SDATA Hold Time	tBIDS	10	-	-	ns
SDATA Setup Time	tBIDH	10	-	-	ns
Slave Mode					
LRCK Input Timing					
Frequency	fs	8	-	384	kHz
Pulse Width High	tLRCKH	45	50	55	%
BCLK Input Timing					
Period (Note 63)	tBCK	0.256	-	24.576 or 512fs	MHz
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns
BCLK "↑" to LRCK Edge	tBSYD	16	-	-	ns
LRCK Edge to BCLK "↑"	tSYBD	16	-	-	ns
SDATA Hold Time	tBIDS	10	-	-	ns
SDATA Setup Time	tBIDH	10	-	-	ns

Note 62. Supported sampling rates are 8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 176.4 k and 192 kHz

Note 63. The maximum value is shorter period between "24.576 MHz" and "512fs".

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I^2C Bus mode): (Note 64)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 65)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN accept pulse width (Note 66)	tPDN	1	-	-	ms
PDN Reject Pulse Width (Note 66)	tRPD	-	-	50	ns

Note 64. I^2C-bus is a registered trademark of NXP B.V.

Note 65. Data must be held long enough to bridge the 300ns-transition time of SCL.

Note 66. The AK4376A will be reset by the PDN pin = "L" for tPDN (Min.). The PDN pin must held "L" for longer period than or equal to tPDN (Min.). The AK4376A will not be reset by the "L" pulse shorter than or equal to tRPD (Max.).