Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AsahiKASEI
ASAHI KASEI EMD

AK4399

High Performance 123dB Premium 32-Bit DAC

GENERAL DESCRIPTION

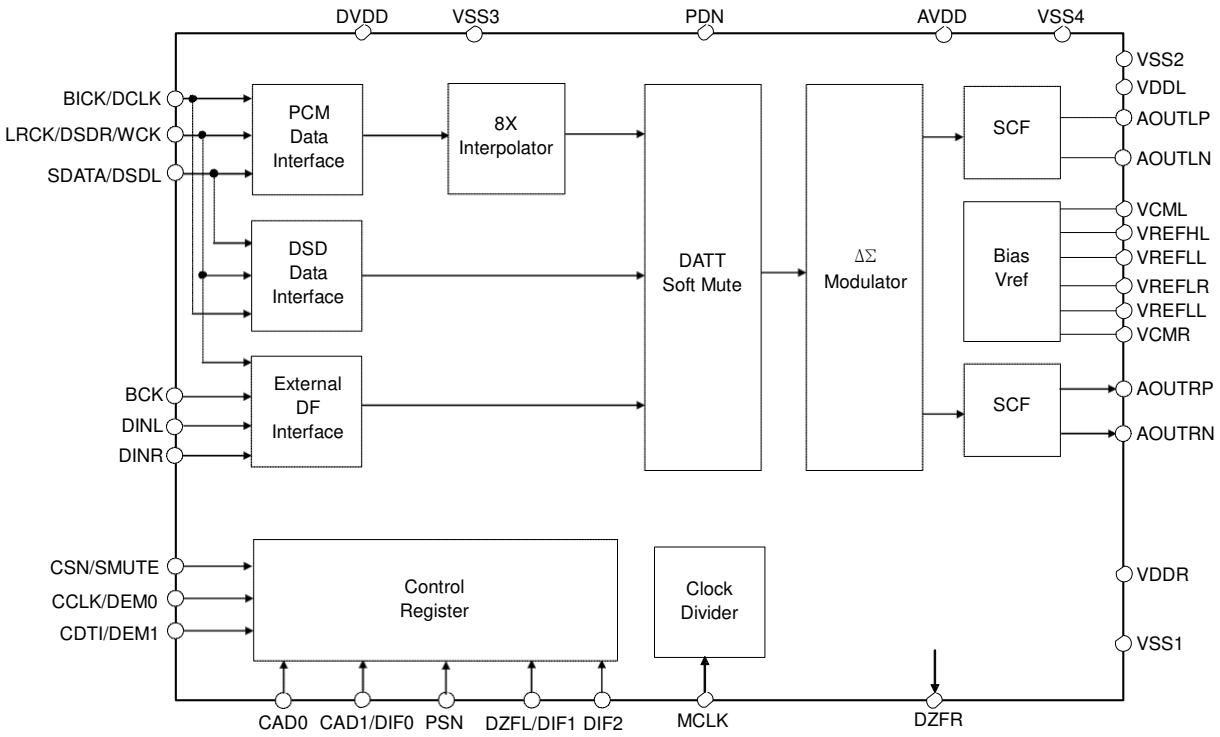
AK4399 is a 32-bit DAC, which corresponds to DVD-Audio systems. An internal circuit includes newly developed 32bit Digital Filter for better sound quality achieving low distortion characteristics and wide dynamic range. The AK4399 has full differential SCF outputs, removing the need for AC coupling capacitors and increasing performance for systems with excessive clock jitter. The AK4399 accepts 192kHz PCM data and 1-bit DSD data, ideal for a wide range of applications including DVD-Audio and SACD.

FEATURES

- **128x Over sampling**
- **Sampling Rate: 30kHz ~ 216kHz**
- **32Bit 8x Digital Filter (Short delay option GD=7/fs)**
  - **Ripple: ±0.005dB, Attenuation: 100dB**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **DSD data input**
- **Digital De-emphasis for 32, 44.1, 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (255 levels and 0.5dB step)**
- **Mono Mode**
- **External Digital Filter Mode**
- **THD+N: -105dB**
- **DR, S/N: 123dB**
- **I/F Format: 24/32bit MSB justified, 16/20/24/32bit LSB justified, I^2S, DSD**
- **Master Clock:**
  - **30kHz ~ 32kHz: 1152fs**
  - **30kHz ~ 54kHz: 512fs or 768fs**
  - **30kHz ~ 108kHz: 256fs or 384fs**
  - **108kHz ~ 216kHz: 128fs or 192fs**
- **Power Supply: 4.75 ~ 5.25V**
- **Digital Input Level: TTL**
- **Package: 44pin LQFP**

Audio 4pro™

■ Block Diagram

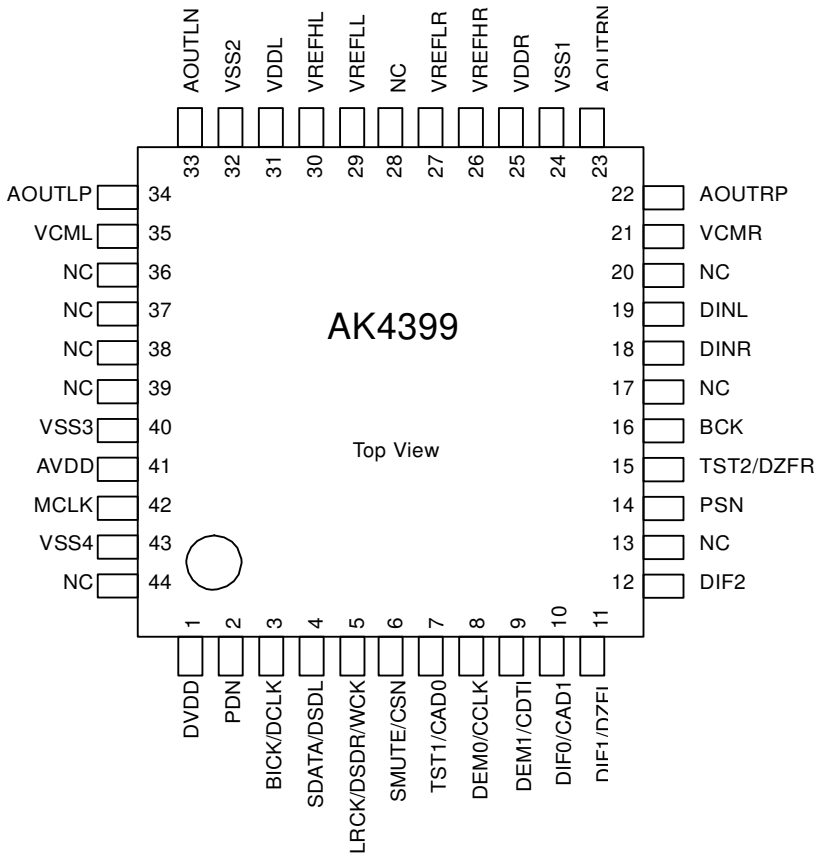


Block Diagram

■ Ordering Guide

AK4399EQ	−10 ~ +70°C	44pin LQFP (0.8mm pitch)
AKD4399	Evaluation Board for AK4399	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DVDD	-	Digital Power Supply Pin, 4.75 ~ 5.25V
2	PDN	I	Power-Down Mode Pin When at "L", the AK4399 is in power-down mode and is held in reset. The AK4399 should always be reset upon power-up.
3	BICK	I	Audio Serial Data Clock Pin in PCM Mode
	DCLK	I	DSD Clock Pin in DSD Mode
4	SDATA	I	Audio Serial Data Input Pin in PCM Mode
	DSDL	I	DSD Lch Data Input Pin in DSD Mode
5	LRCK	I	L/R Clock Pin in PCM Mode
	DSDR	I	DSD Rch Data Input Pin in DSD Mode
	WCK	I	Word Clock input pin
6	SMUTE	I	Soft Mute Pin in Parallel Control Mode When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.
	CSN	I	Chip Select Pin in Serial Control Mode
7	TST1	I	Test Pin in Parallel Control Mode (Internal pull-down pin)
	CAD0	I	Chip Address 0 Pin in Serial Control Mode (Internal pull-down pin)
8	DEM0	I	De-emphasis Enable 0 Pin in Parallel Control Mode
	CCLK	I	Control Data Clock Pin in Serial Control Mode
9	DEM1	I	De-emphasis Enable 1 Pin in Parallel Control Mode
	CDTI	I	Control Data Input Pin in Serial Control Mode
10	DIF0	I	Digital Input Format 0 Pin in PCM Mode
	CAD1	I	Chip Address 1 Pin in Serial Control Mode
11	DIF1	I	Digital Input Format 1 Pin in PCM Mode
	DZFL	O	Lch Zero Input Detect Pin in Serial Control Mode
12	DIF2	I	Digital Input Format 2 Pin in PCM Mode
13	NC	-	No internal bonding. Connect to GND.

Note: All input pins except internal pull-up/down pins must not be left floating.

14	PSN	I	Parallel or Serial Select Pin (Internal pull-up pin) "L": Serial Control Mode, "H": Parallel Control Mode
15	TST2	I	Test pin in Parallel Control Mode. Connect to GND.
	DZFR	O	Rch Zero Input Detect Pin in Serial Control Mode
16	BCK	I	Audio Serial Data Clock Pin (Internal pull-down pin)
17	NC	-	No internal bonding. Connect to GND.
18	DINR	I	Rch Audio Serial Data Input Pin (Internal pull-down pin)
19	DINL	I	Lch Audio Serial Data Input Pin (Internal pull-down pin)
20	NC	-	No internal bonding. Connect to GND.
21	VCMR	-	Right channel Common Voltage Pin, Normally connected to VSS with a 10uF electrolytic cap.
22	AOUTRP	O	Rch Positive Analog Output Pin
23	AOUTRN	O	Rch Negative Analog Output Pin
24	VSS1	-	Ground Pin
25	VDDR	-	Rch Analog Power Supply Pin, 4.75 ~ 5.25V
26	VREFHR	I	Rch High Level Voltage Reference Input Pin
27	VREFLR	I	Rch Low Level Voltage Reference Input Pin
28	NC	-	No internal bonding. Connect to GND.
29	VREFLL	I	Lch Low Level Voltage Reference Input Pin
30	VREFHL	I	Lch High Level Voltage Reference Input Pin
31	VDDL	-	Lch Analog Power Supply Pin, 4.75 ~ 5.25V
32	VSS2	-	Ground Pin
33	AOUTLN	O	Lch Negative Analog Output Pin
34	AOUTLP	O	Lch Positive Analog Output Pin
35	VCML	-	Left channel Common Voltage Pin, Normally connected to VSS with a 10uF electrolytic cap.
36	NC	-	No internal bonding. Connect to GND.
37	NC	-	No internal bonding. Connect to GND.
38	NC	-	No internal bonding. Connect to GND.
39	NC	-	No internal bonding. Connect to GND.
40	VSS3	-	Ground Pin
41	AVDD	-	Analog Power Supply Pin, 4.75 ~ 5.25V
42	MCLK	I	Master Clock Input Pin
43	VSS4	-	Ground Pin
44	NC	-	No internal bonding. Connect to GND.

Note: All input pins except internal pull-up/down pins must not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

(1) Parallel Mode (PCM Mode only)

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	SMUTE	This pin must be connected to VSS4.
	TST1	This pin must be open.
	TST2	This pin must be connected to VSS4.

(2) Serial Mode

1. PCM Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	DIF2	These pins must be connected to VSS4.
	DZFL, DZFR	These pins must be open.

2. DSD Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
	DZFL, DZFR	These pins must be open.

ABSOLUTE MAXIMUM RATINGS

(VSS1-4 =0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	−0.3	6.0	V
	Analog	VDDL/R	−0.3	6.0	V
	Digital	DVDD	−0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	−0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	−10	70	°C
Storage Temperature		Tstg	−65	150	°C

Note 1. All voltages with respect to ground.
Note 2. VSS1-4 must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1-4 =0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 3)	Analog	AVDD	4.75	5.0	5.25	V
	Analog	VDDL/R	4.75	5.0	5.25	V
	Digital	DVDD	4.75	5.0	5.25	V
Voltage Reference (Note 4)	"H" voltage reference	VREFHL/R	AVDD−0.5	-	AVDD	V
	"L" voltage reference	VREFLL/R	VSS	-	-	V
	VREFH − VREFL	ΔVREF	3.0	-	AVDD	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD, VDDL/R and DVDD is not critical.
Note 4. The analog output voltage scales with the voltage of (VREFH − VREFL).
AOUT (typ.@0dB) = (AOUT+) − (AOUT−) = ±2.8Vpp × (VREFHL/R − VREFLL/R)/5.

* AKEMD assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=VDDL/R=DVDD=5.0V; VSS1-4 =0V; VREFHL/R=AVDD, VREFLL/R= VSS;
Input data = 24bit; $R_L \geq 1k\Omega$; BICK=64fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz;
Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: Figure 20; unless otherwise specified.)

Parameter			min	typ	max	Units
Resolution			-	-	24	Bits
Dynamic Characteristics (Note 5)						
THD+N	fs=44.1kHz	0dBFS	-	-105	98	dB
	BW=20kHz	−60dBFS	-	-60	-	dB
	fs=96kHz	0dBFS	-	102	-	dB
	BW=40kHz	−60dBFS	-	-57	-	dB
	fs=192kHz	0dBFS		102	-	dB
	BW=40kHz	−60dBFS		-57	-	dB
	BW=80kHz	−60dBFS		-54	-	dB
Dynamic Range (−60dBFS with A-weighted) (Note 6)			117	123		dB
S/N (A-weighted) (Note 7)			117	123		dB
Interchannel Isolation (1kHz)			110	120		dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.15	0.3	dB
Gain Drift (Note 8)			-	20	-	ppm/°C
Output Voltage (Note 9)			±2.65	±2.8	±2.95	Vpp
Load Capacitance			-	-	25	pF
Load Resistance (Note 10)			1	-	-	kΩ
Power Supplies						
Power Supply Current						
	Normal operation (PDN pin = "H")					
	AVDD + VDDL/R		-	60	90	mA
	DVDD (fs ≤ 96kHz)		-	43	-	mA
	DVDD (fs = 192kHz)		-	46	70	mA
	Power down (PDN pin = "L") (Note 11)					
	AVDD+VDDL/R+DVDD		-	10	100	μA

Note 5. Measured by Audio Precision, System Two. Averaging mode. Refer to the evaluation board manual.
Note 6. Figure 20 External LPF Circuit Example 2. 101dB for 16-bit data and 118dB for 20-bit data.
Note 7. Figure 20 External LPF Circuit Example 2. S/N does not depend on input data size.
Note 8. The voltage on (VREFH − VREFL) is held +5V externally.
Note 9. Full-scale voltage(0dB). Output voltage scales with the voltage of (VREFHL/R − VREFLL/R).
AOUT (typ.@0dB) = (AOUT+) − (AOUT−) = ±2.8Vpp × (VREFHL/R − VREFLL/R)/5.
Note 10. Regarding Load Resistance, AC load is 1kΩ (min) with a DC cut capacitor (Figure 20). DC load is 1.5k ohm (min) without a DC cut capacitor (Figure 19). The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore the capacitive load must be minimized.
Note 11. In the power down mode. The P/S pin = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held VSS4.

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Normal Speed Mode; DEM=OFF; SD bit="0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 12)		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	36	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-	±0.2	-	dB

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Double Speed Mode; DEM=OFF; SD bit="0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		43.5	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 12)		SB	52.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	95			dB
Group Delay (Note 13)		GD	-	36	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-	±0.3	-	dB

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Quad Speed Mode; DEM=OFF; SD bit="0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 12)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	90			dB
Group Delay (Note 13)		GD	-	36	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-	+0/−1	-	dB

Note 12. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.
Note 13. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

SHORT DELAY FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Normal Speed Mode; DEM=OFF; SD bit="1")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 12)		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-	±0.2	-	dB

SHORT DELAY FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Double Speed Mode; DEM=OFF; SD bit="1")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		43.5	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 12)		SB	52.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	95			dB
Group Delay (Note 13)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-	±0.3	-	dB

SHORT DELAY FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Quad Speed Mode; DEM=OFF; SD bit="1")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 12)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	90			dB
Group Delay (Note 13)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-	+0/−1	-	dB

DC CHARACTERISTICS

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	2.4	-	-	V
Low-Level Input Voltage		VIL	-	-	0.8	V
High-Level Output Voltage	(Iout=−100μA)	VOH	DVDD−0.5	-	-	V
Low-Level Output Voltage	(Iout=100μA)	VOL	-	-	0.5	V
Input Leakage Current	(Note 14)	Iin	-	-	±10	μA

Note 14. The TST1/CAD0 and P/S pins have internal pull-up devices, nominally 100kΩ. Therefore The TST1/CAD0 and P/S pins are not included.

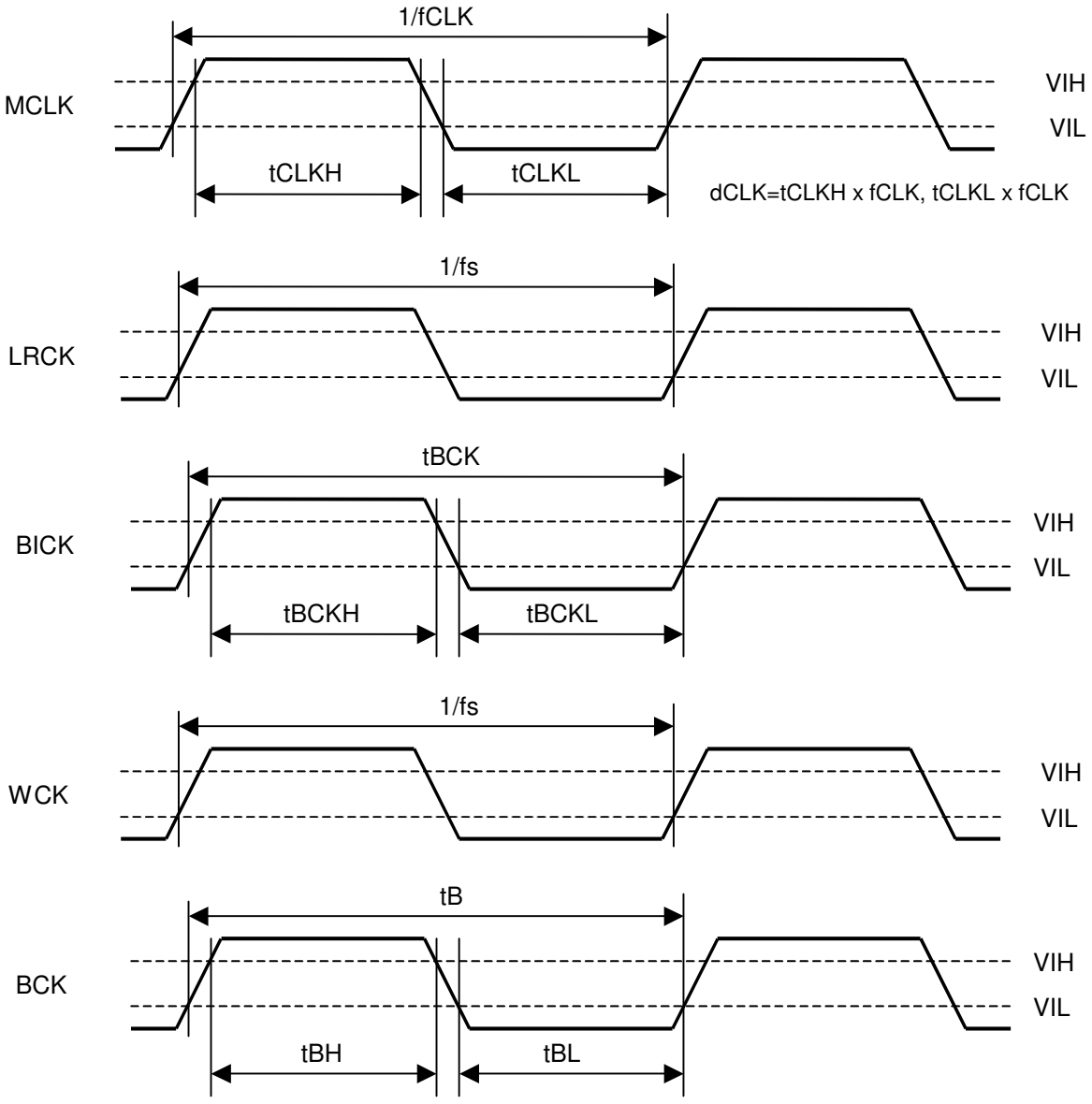
SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V)

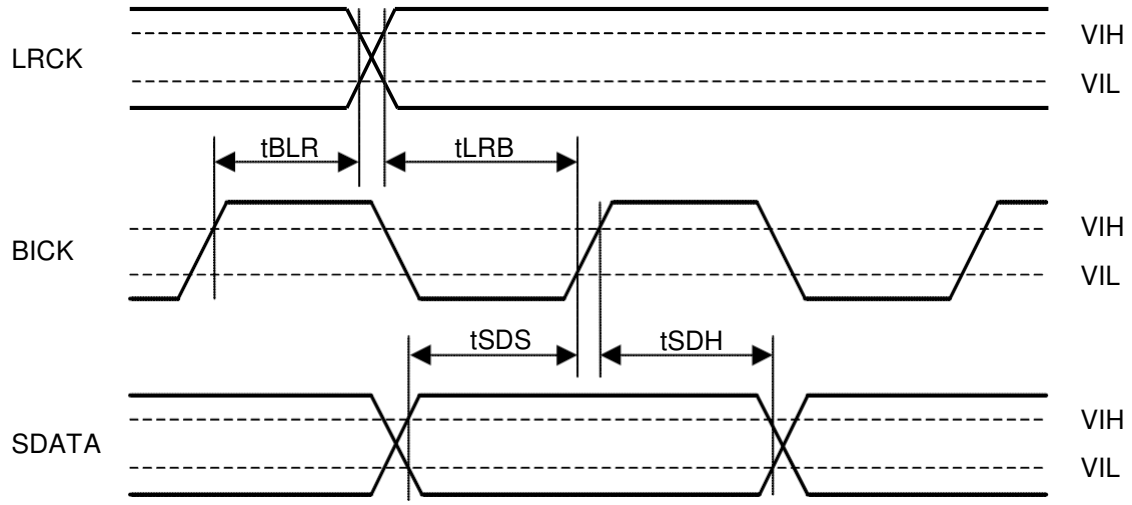
Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency		fCLK	7.7		41.472	MHz
Duty Cycle		dCLK	40		60	%
LRCK Frequency	(Note 15)					
1152fs, 512fs or 768fs		fsn	30		54	kHz
256fs or 384fs		fsd	54		108	kHz
128fs or 192fs		fsq	108		216	kHz
Duty Cycle		Duty	45		55	%
PCM Audio Interface Timing						
BICK Period						
1152fs, 512fs or 768fs		tBCK	1/128fsn			ns
256fs or 384fs		tBCK	1/64fsd			ns
128fs or 192fs		tBCK	1/64fsq			ns
BICK Pulse Width Low		tBCKL	30			ns
BICK Pulse Width High		tBCKH	30			ns
BICK "↑" to LRCK Edge	(Note 16)	tBLR	20			ns
LRCK Edge to BICK "↑"	(Note 16)	tLRB	20			ns
SDATA Hold Time		tSDH	20			ns
SDATA Setup Time		tSDS	20			ns
External Digital Filter Mode						
BICK Period		tB tBL	27			ns
BCK Pulse Width Low		tBH	10			ns
BCK Pulse Width High		tBW	10			ns
BCK "↑" to WCK Edge		tWB	5			ns
WCK Edge to BCK "↑"		tWCK	5			ns
WCK Pulse Width Low		tWCH	54			ns
WCK Pulse Width High		tDH	54			ns
DATA Hold Time		tDS	5			ns
DATA Setup Time			5			ns
DSD Audio Interface Timing						
DCLK Period		tDCK	1/64fs			ns
DCLK Pulse Width Low		tDCKL	160			ns
DCLK Pulse Width High		tDCKH	160			ns
DCLK Edge to DSDL/R	(Note 17)	tDDD	−20		20	ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	50			ns
CDTI Hold Time		tCDH	50			ns
CSN High Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Reset Timing						
PDN Pulse Width	(Note 18)	tPD	150			ns

Note 15. When the 1152fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK4399 should be reset by the PDN pin or RSTN bit.
Note 16. BICK rising edge must not occur at the same time as LRCK edge.
Note 17. DSD data transmitting device must meet this time.
Note 18. The AK4399 can be reset by bringing the PDN pin "L" to "H" upon power-up.

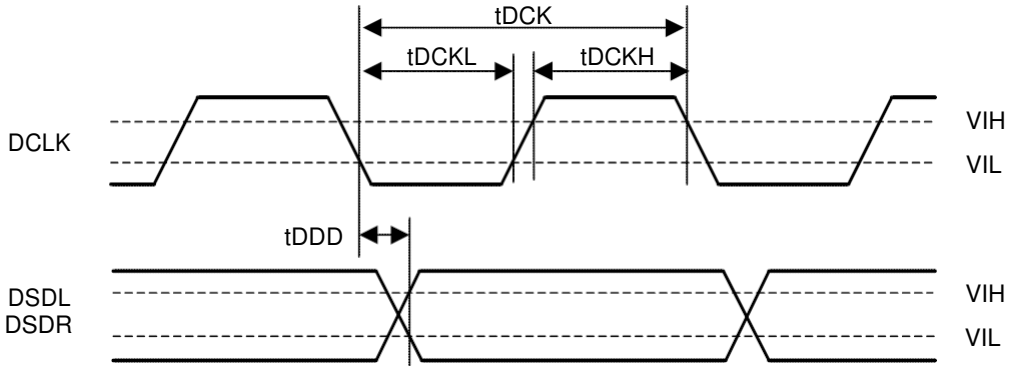
■ Timing Diagram



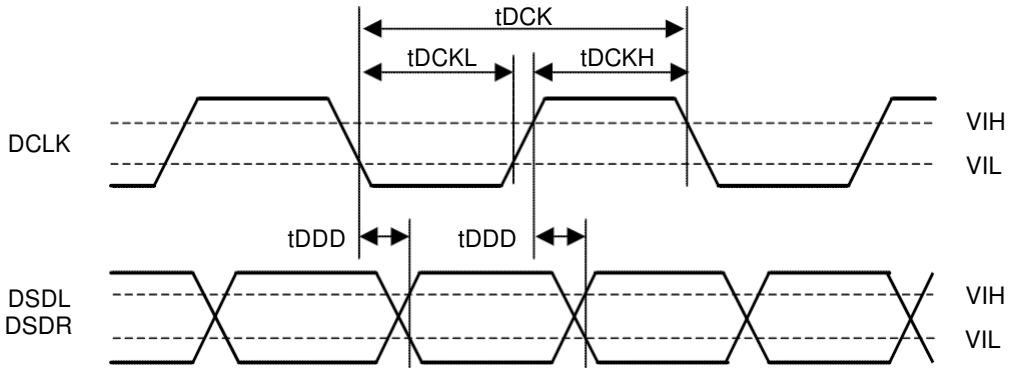
Clock Timing



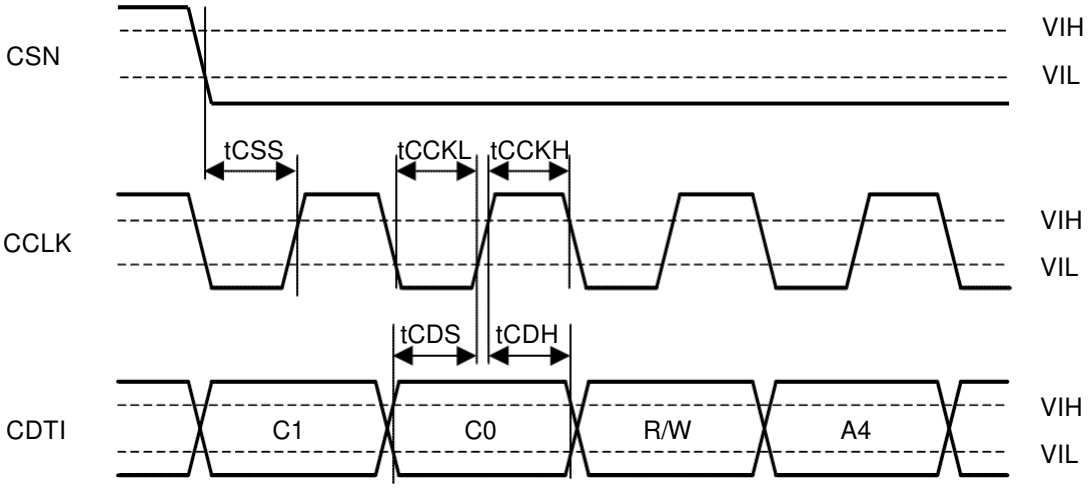
Audio Interface Timing (PCM Mode)



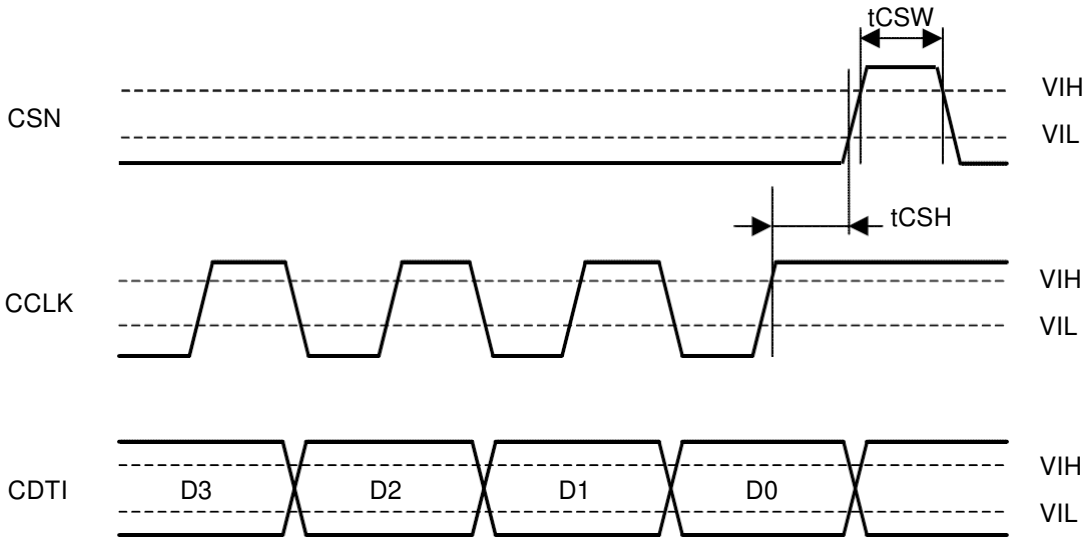
Audio Serial Interface Timing (DSD Normal Mode, DCKB bit = "0")



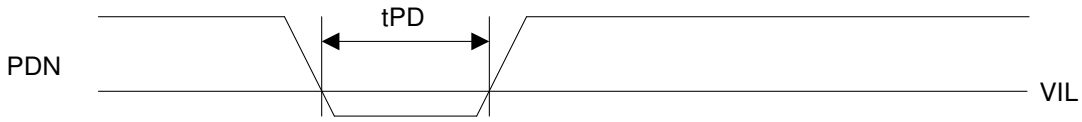
Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB bit = "0")



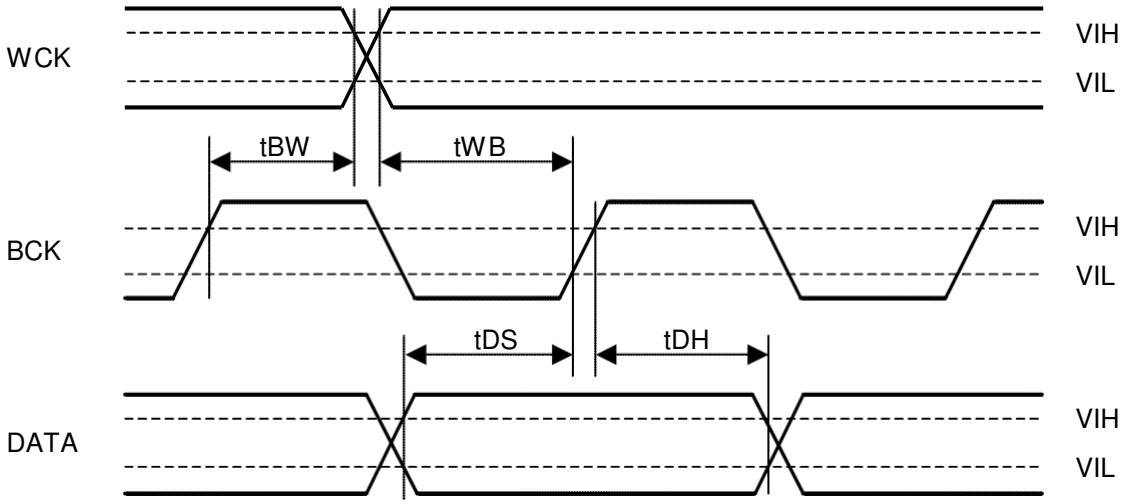
WRITE Command Input Timing



WRITE Data Input Timing



Power Down & Reset Timing



External Digital Filter I/F mode

OPERATION OVERVIEW

■ D/A Conversion Mode

In serial mode, the AK4399 can perform D/A conversion for either PCM data or DSD data. The D/P bit controls PCM/DSD mode. When DSD mode, DSD data can be input from DCLK, DSDL and DSDR pins. When PCM mode, PCM data can be input from BICK, LRCK and SDATA pins. When PCM/DSD mode is changed by D/P bit, the AK4399 should be reset by RSTN bit. It takes about 2/fs to 3/fs to change the mode. In parallel mode, the AK4399 performs for only PCM data.

DP bit	Interface
0	PCM
1	DSD

Table 1. PCM/DSD Mode Control

When DP bit= "0", an internal digital filter or external digital filter can be selected. When using an external digital filter (EX DF I/F mode), data is input to each MCLK, BCK, WCK, DINL and DINR pin. EXD bit controls the modes. When switching internal and external digital filters, the AK4399 must be reset by RSTN bit. A Digital filter switching takes 2~3k/fs.

Ex DF bit	Interface
0	PCM
1	EX DF I/F

Table 2. Digital Filter Control (DP bit = "0")

■ System Clock

[1] PCM Mode

The external clocks, which are required to operate the AK4399, are MCLK, BICK and LRCK. MCLK should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. Sampling speed and MCLK frequency are detected automatically and then the initial master clock is set to the appropriate frequency (Table 3). When external clocks are changed, the AK4399 should be reset by the PDN pin or RSTN bit.

The AK4399 is automatically placed in reset state when MCLK and LRCK are stopped during a normal operation (PDN pin ="H"), and the analog output becomes Hi-Z. When MCLK and LRCK are input again, the AK4399 exit reset state and starts the operation. After exiting system reset (PDN pin ="L"→"H") at power-up and other situations, the AK4399 is in power-down mode until MCLK and LRCK are supplied.

The MCLK frequency corresponding to each sampling speed should be provided (Table 4).

MCLK		Mode	Sampling Rate
1152fs		Normal	30kHz~32kHz
512fs	768fs	Normal	30kHz~54kHz
256fs	384fs	Double	30kHz~108kHz
128fs	192fs	Quad	108kHz~216kHz

Table 3. Sampling Speed

LRCK	MCLK (MHz)						
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A
88.2kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A
96.0kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	N/A
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A

Table 4. System Clock Example (Parallel Control Mode) (N/A: Not available)

MCLK= 256fs/384fs supports sampling rate of 30kHz~108kHz (Table 5). But, when the sampling rate is 30kHz~54kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

MCLK	DR,S/N
256fs/384fs	120dB
512fs/768fs	123dB

Table 5. Relationship between MCLK frequency and DR, S/N (fs= 44.1kHz)

[2] DSD Mode

The external clocks, which are required to operate the AK4399, are MCLK and DCLK. MCLK should be synchronized with DCLK but the phase is not critical. The frequency of MCLK is set by DCKS bit.

The AK4399 is automatically placed in reset state when MCLK is stopped during a normal operation (PDN pin ="H"), and the analog output becomes Hi-Z. After exiting system reset (PDN pin ="L"→"H") at power-up and other situations, the AK4399 is in power-down mode until MCLK is supplied.

DCKS bit	MCLK Frequency	DCLK Frequency	
0	512fs	64fs	(default)
1	768fs	64fs	

Table 6. System Clock (DSD Mode)

■ Audio Interface Format

[1] PCM Mode

Data is shifted in via the SDATA pin using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF2-0 pins (Parallel control mode) or DIF2-0 bits (Serial control mode) as shown in Table 7. In all formats the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20-bit and 16-bit MSB justified formats by zeroing the unused LSBs. Settings should be made by DIF2-0 pins in parallel mode and DIF2-0 bits in serial mode.

Mode	DIF2	DIF1	DIF0	Input Format	BICK	Figure	
0	0	0	0	16bit LSB justified	≥ 32fs	Figure 1	
1	0	0	1	20bit LSB justified	≥ 48fs	Figure 2	
2	0	1	0	24bit MSB justified	≥ 48fs	Figure 3	(default)
3	0	1	1	24bit I^2S Compatible	≥ 48fs	Figure 4	
4	1	0	0	24bit LSB justified	≥ 48fs	Figure 2	
5	1	0	1	32bit LSB justified	≥ 64fs	Figure 5	
6	1	1	0	32bit MSB justified	≥64fs	Figure 6	
7	1	1	1	32bit I^2S Compatible	≥ 64fs	Figure 7	

Table 7. Audio Interface Format

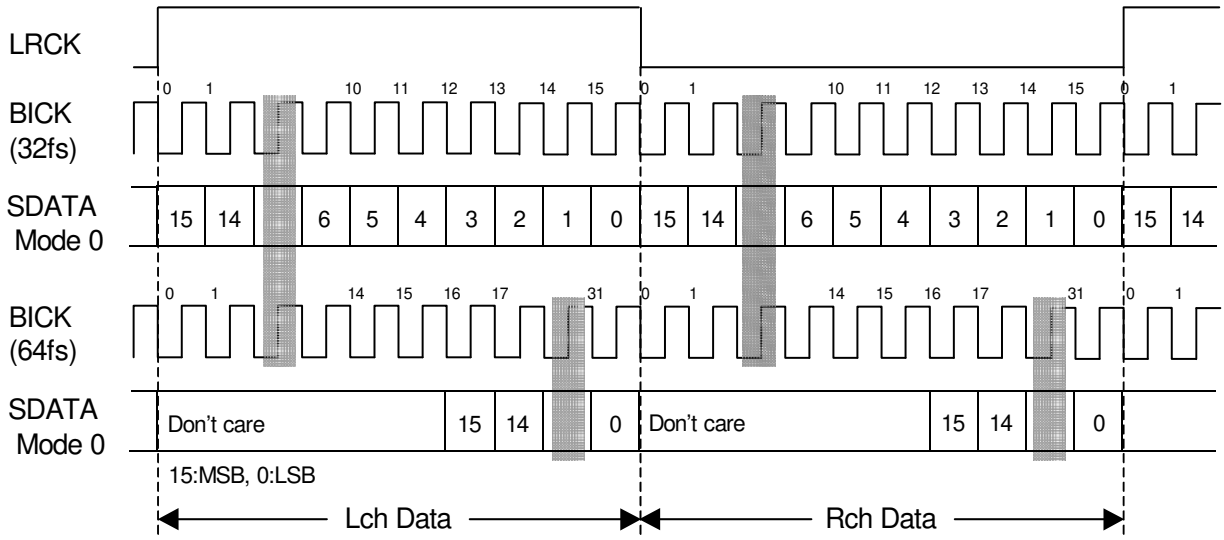


Figure 1. Mode 0 Timing

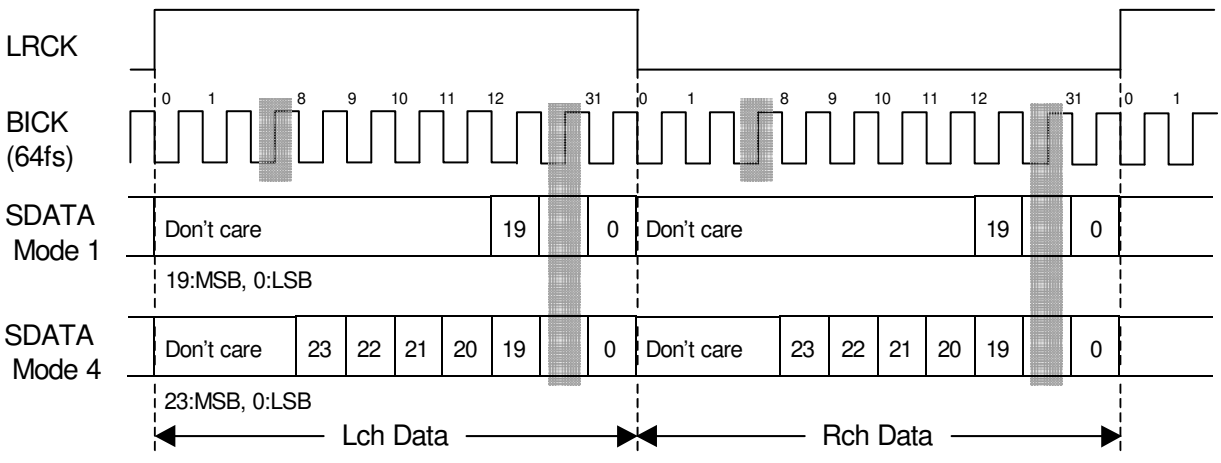


Figure 2. Mode 1/4 Timing

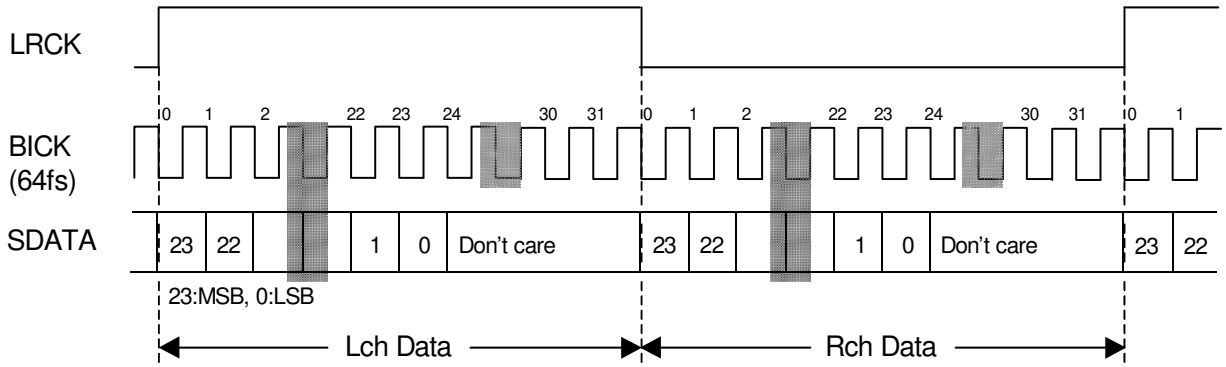


Figure 3. Mode 2 Timing

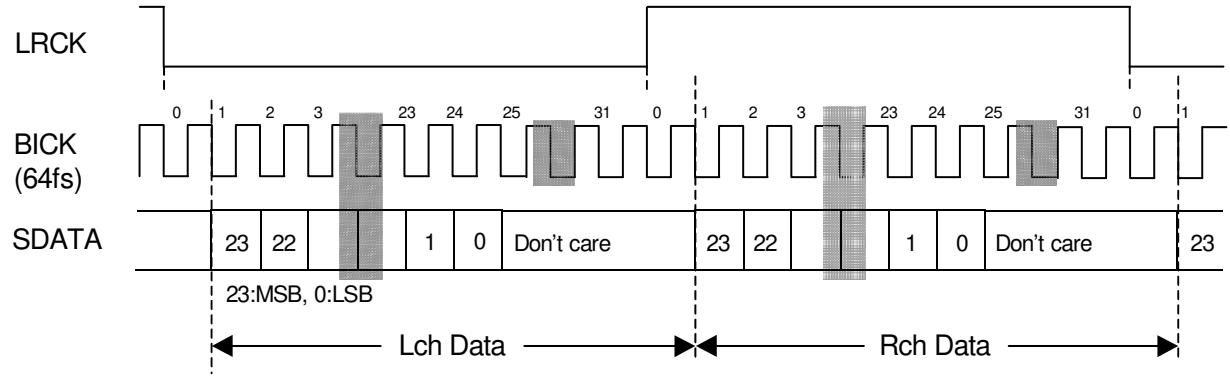


Figure 4. Mode 3 Timing

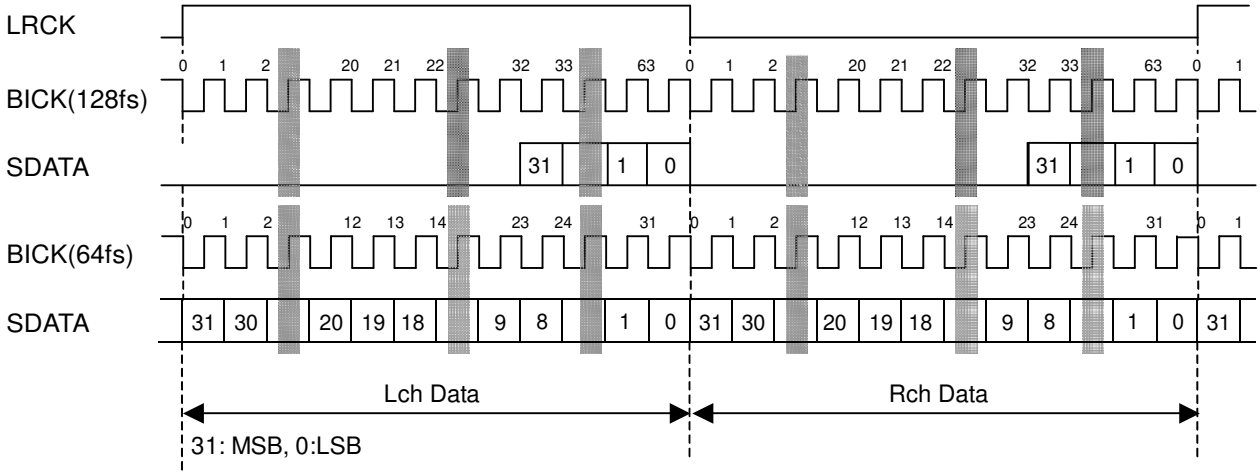


Figure 5. Mode 5 Timing

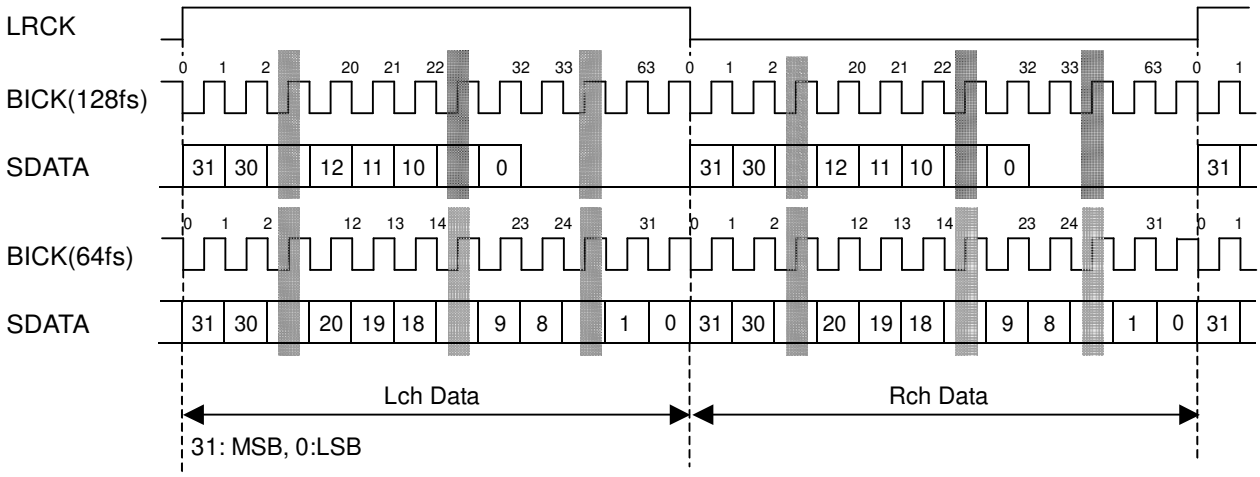


Figure 6. Mode 6 Timing

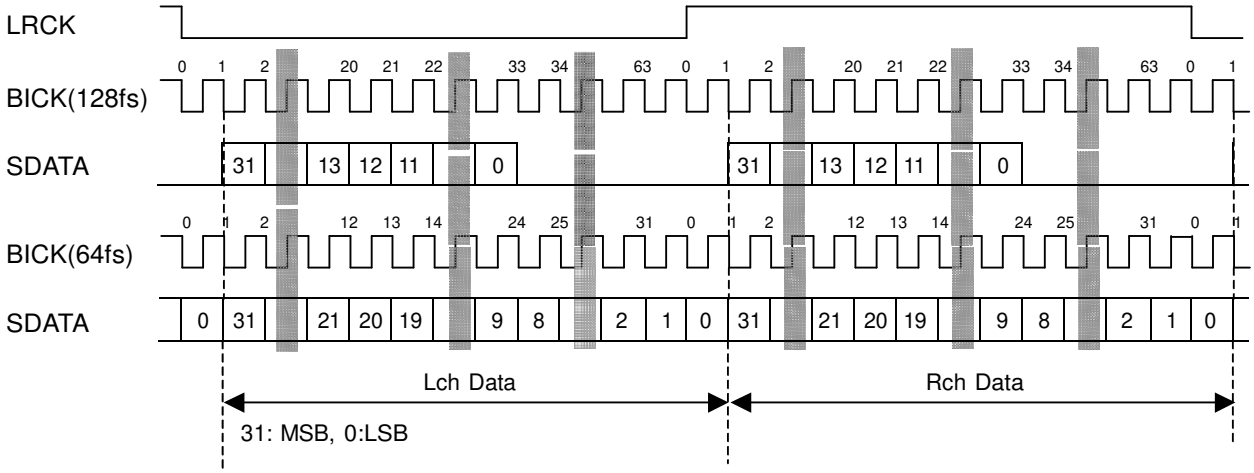


Figure 7. Mode 7 Timing

[2] DSD Mode

In case of DSD mode, DIF2-0 pins and DIF2-0 bits are ignored. The frequency of DCLK is fixed to 64fs. DCKB bit can invert the polarity of DCLK.

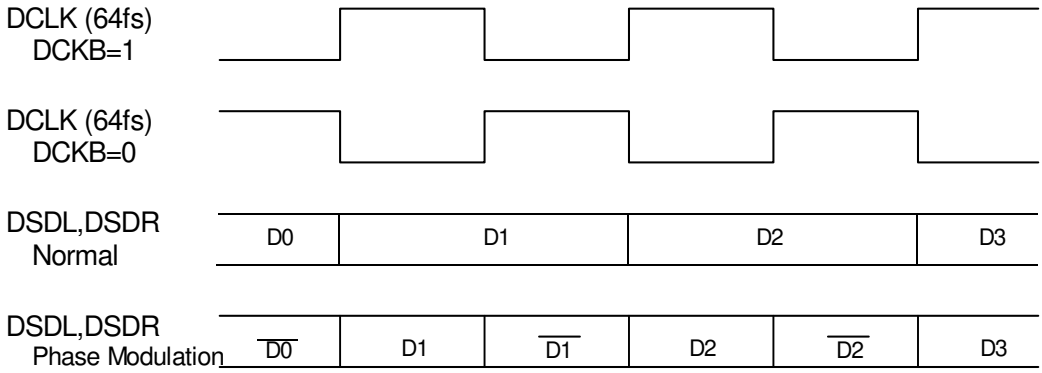


Figure 8. DSD Mode Timing

[3] External Digital Filter Mode (EX DF I/F Mode)

DW indicates the number of BCK in one WCK cycle. The audio data is input by MCLK, BCK and WCK from the DINL and DINR pins. Three formats are available (Table 9) by DIF2-0 bits setting. The data is latched on the rising edge of BCK. The BCK and MCLK clocks must be the same frequency and must not burst. BCK and MCLK frequencies for each sampling speed are shown in Table 8.

The AK4399 is automatically placed in reset state when MCLK and WCK are stopped during a normal operation (PDN pin ="H"), and the analog output becomes Hi-Z. When MCLK and WCK are input again, the AK4399 exit reset state and starts the operation. After exiting system reset (PDN pin ="L"→"H") at power-up and other situations, the AK4399 is in power-down mode until MCLK and WCK are supplied.

Sampling Speed[kHz]	MCLK&BCK [MHz]						WCK	ECS
	128fs	192fs	256fs	384fs	512fs	768fs		
44.1(30~54)	N/A	N/A	N/A	N/A	22.5792	33.8688	16fs	0
					32	48	DW	
44.1(30~54)	N/A	N/A	11.2896	16.9344	N/A	33.8688	8fs	1
			32	48		96	DW	
96(54~108)	N/A	N/A	24.576	36.864	N/A	N/A	8fs	0
			32	48			DW	
96(54~108)	12.288	18.432	N/A	36.864	N/A	N/A	4fs	1
	32	48		96			DW	
192(108~216)	24.576	36.864	N/A	N/A	N/A	N/A	4fs	0
	32	48					DW	
192(108~216)	N/A	36.864	N/A	N/A	N/A	N/A	2fs	1
		96					DW	

Table 8 System Clock Example (EX DF I/F mode) (N/A: Not available)

Mode	DIF2	DIF1	DIF0	Input Format
0	0	0	0	16bit LSB justified
1	0	0	1	N/A
2	0	1	0	N/A
3	0	1	1	N/A
4	1	0	0	24bit LSB justified
5	1	0	1	32bit LSB justified
6	1	1	0	N/A
7	1	1	1	N/A

Table 9 Audio Interface Format (EX DF I/F mode) (N/A: Not available)

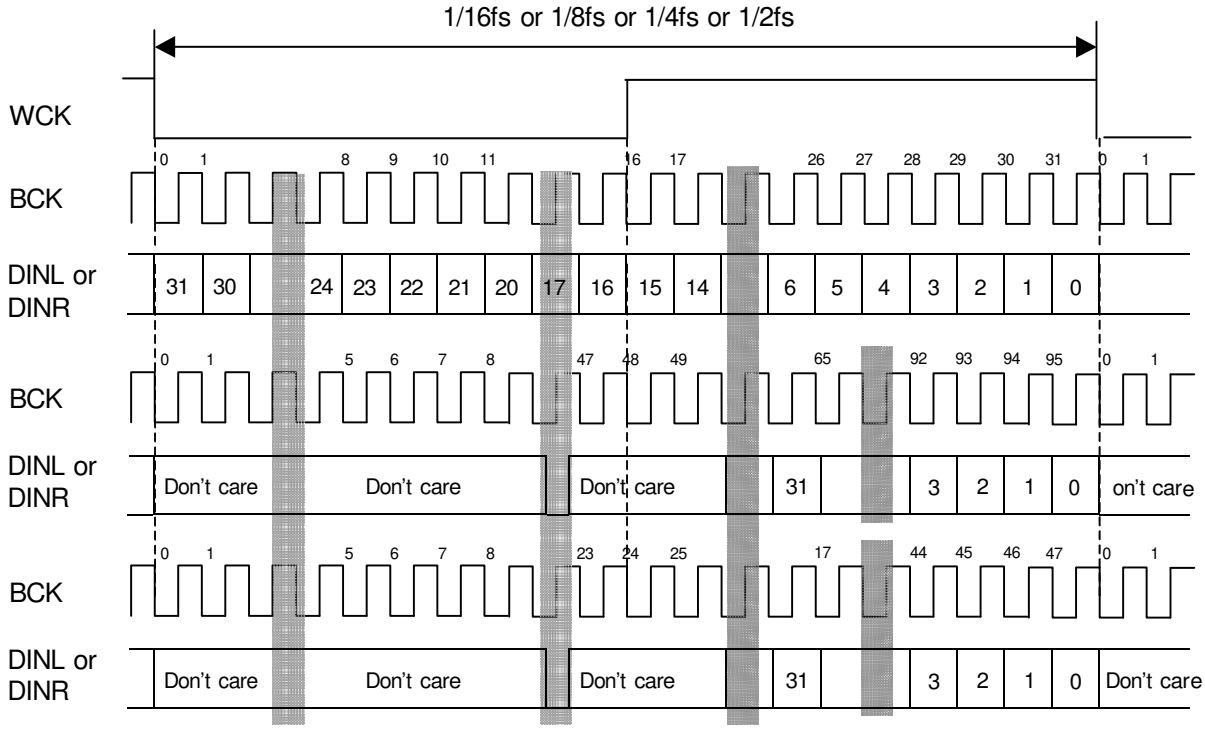


Figure 9 EX DF I/F Mode Timing

■ D/A Conversion Mode Switching Timing

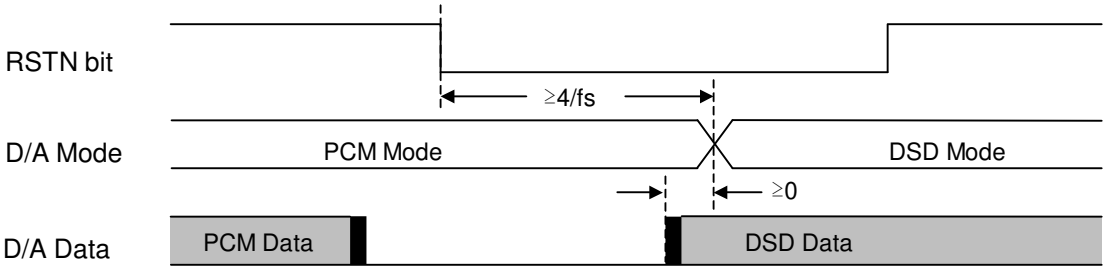


Figure 10. D/A Mode Switching Timing (PCM to DSD)

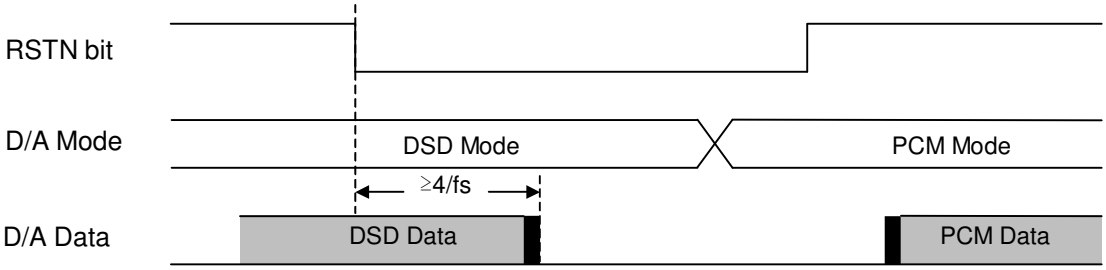


Figure 11. D/A Mode Switching Timing (DSD to PCM)

Note. The signal range is identified as 25% ~ 75% duty ratios in DSD mode. DSD signal must not go beyond this duty range at the SACD format book (Scarlet Book).

■ De-emphasis Filter

A digital de-emphasis filter is available for 32kHz, 44.1kHz or 48kHz sampling rates (tc = 50/15µs) and is enabled or disabled with DEM1-0 pins or DEM1-0 bits. In case of 256fs/384fs and 128fs/192fs, the digital de-emphasis filter is always off. When DSD mode, DEM1-0 bits are ignored. The setting value is held even if PCM mode and DSD mode are switched.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 10. De-emphasis Control

■ Output Volume

The AK4399 includes channel independent digital output volumes (ATT) with 255 levels at linear step including MUTE. These volume control is in front of the DAC and it can attenuate the input data from 0dB to –127dB and mute. When changing output levels, transitions are executed in soft change; thus no switching noise occurs during these transitions.

■ Zero Detection (PCM mode, DSD mode)

The AK4399 has channel-independent zeros detect function. When the input data at each channel is continuously zeros for 8192 LRCK cycles, the DZF pin of each channel goes to "H". The DZF pin of each channel immediately return to "L" if the input data of each channel is not zero after going to "H". If the RSTN bit is "0", the DZF pins of both channels go to "H". The DZF pins of both channels go to "L" at 4 ~ 5/fs after RSTN bit returns to "1". If DZFM bit is set to "1", the DZF pins of both channels go to "H" only when the input data for both channels are continuously zeros for 8192 LRCK cycles. The zero detect function can be disabled by setting the DZFE bit. In this case, DZF pins of both channels are always "L". The DZFB bit can invert the polarity of the DZF pin.

■ Mono Output

The AK4399 can select input/output for both output channels by setting the MONO bit and SELLR bit. This function is available for any audio format.

MONO bit	SELLR bit	Lch Out	Rch Out
0	0	Lch In	Rch In
0	1	Rch In	Lch In
1	0	Lch In	Lch In
1	1	Rch In	Rch In

Table 11 MONO Mode Output Select