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# AK4413

## High Performance 120dB 24-Bit 4ch DAC

### GENERAL DESCRIPTION

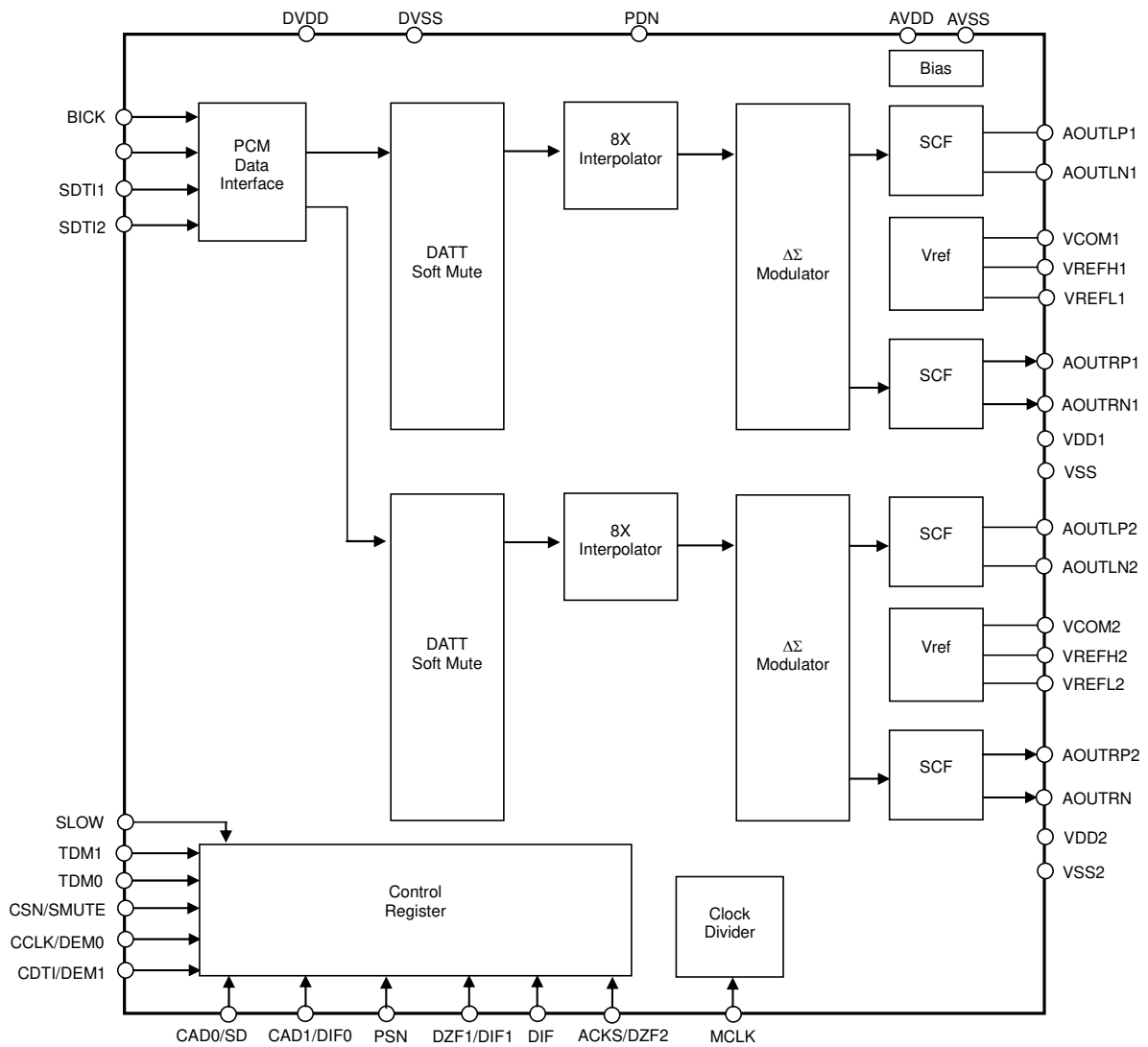
AK4413 is a 24-bit DAC, which corresponds to BD systems. An internal circuit includes newly developed 24bit Digital Filter for better sound quality achieving low distortion characteristics and wide dynamic range. The AK4413 has full differential SCF outputs, removing the need for AC coupling capacitors and increasing performance for systems with excessive clock jitter. The AK4413 accepts 216kHz PCM data, ideal for a wide range of applications including DVD-Audio.

### FEATURES

- 128x Over sampling
- Sampling Rate: 30kHz ~ 216kHz
- 24Bit 8x Digital Filter
  - Ripple:  $\pm 0.005$ dB, Attenuation: 80dB
  - High Quality Sound Short Delay Option; GD=7/fs and GD=5.5/fs
  - Sharp Roll-Off Filter
  - Slow Roll-Off Filter
- High Tolerance to Clock Jitter
- Low Distortion Differential Output
- Digital De-emphasis for 32, 44.1, 48kHz sampling
- Soft Mute
- Digital Attenuator (255 levels and 0.5dB step)
- Stereo Mode
- THD+N: -104dB
- DR, S/N: 120dB (Stereo mode: 123dB)
- I/F Format: 24-bit MSB justified, 16/20/24bit LSB justified, I<sup>2</sup>S, TDM
- Master Clock:
  - 30kHz ~ 32kHz: 1152fs
  - 30kHz ~ 54kHz: 512fs or 768fs
  - 30kHz ~ 108kHz: 256fs or 384fs
  - 108kHz ~ 216kHz: 128fs or 192fs
- Power Supply: DVDD=AVDD=2.7 ~ 3.6V, VDD1/2=4.75 ~ 5.25V
- Digital Input Level: CMOS
- Package: 44pin LQFP



■ Block Diagram



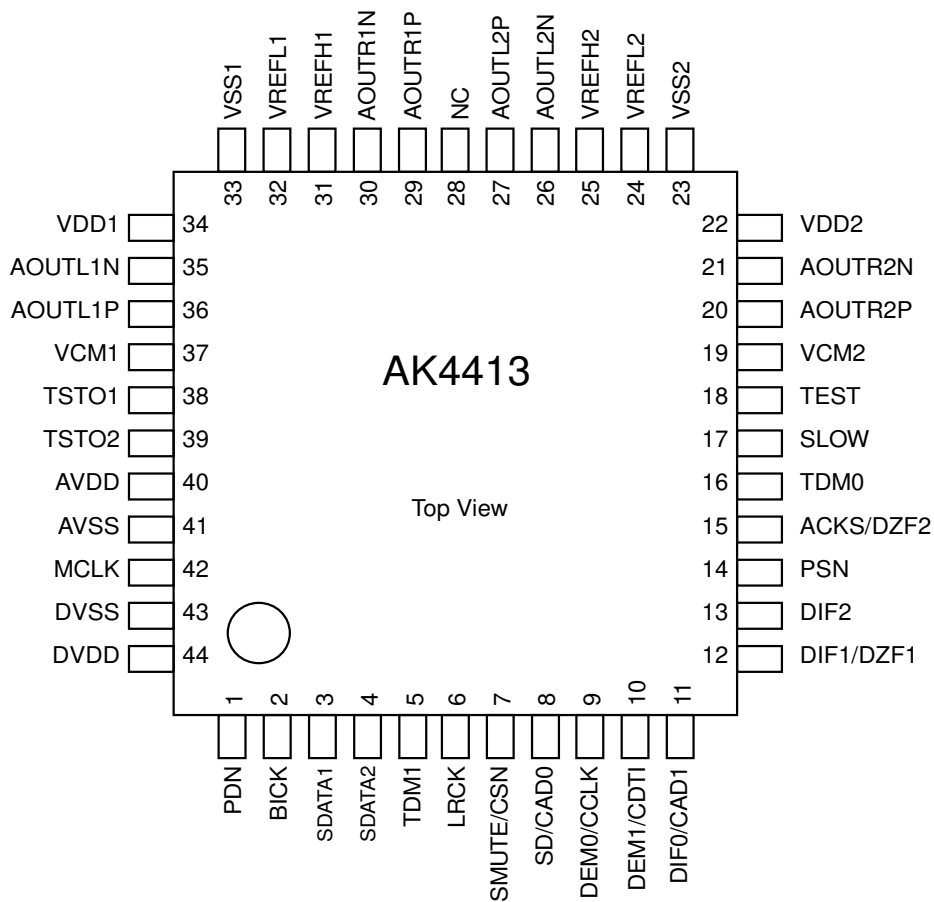
Block Diagram

■ Ordering Guide

AK4413EQ  
AKD4413

-10 ~ +70°C                      44pin LQFP (0.8mm pitch)  
Evaluation Board for AK4413

■ Pin Layout



## PIN/FUNCTION

No.	Pin Name	I/O	Function
1	PDN	I	Power-Down Mode When at "L", the AK4413 is in power-down mode and is held in reset. The AK4413 should always be reset upon power-up.
2	BICK	I	Audio Serial Data Clock in PCM Mode
3	SDATA1	I	Audio Serial Data Input in PCM Mode
4	SDATA2	I	Audio Serial Data Input in PCM Mode
5	TDM1	I	TDM I/F Format Mode in PCM Mode
6	LRCK	I	L/R Clock in PCM Mode
7	SMUTE	I	Soft Mute in Parallel Control Mode When this pin goes to "H", soft mute cycle is initiated. When returning to "L", the output mute releases.
	CSN	I	Chip Select in Serial Control Mode
8	SD		Digital Filter setting pin in Parallel Control mode
	CAD0	I	Chip Address 0 in Serial Control Mode (Internal pull-down pin)
9	DEM0	I	De-emphasis Enable 0 in Parallel Control Mode
	CCLK	I	Control Data Clock in Serial Control Mode
10	DEM1	I	De-emphasis Enable 1 in Parallel Control Mode
	CDTI	I	Control Data Input in Serial Control Mode
11	DIF0	I	Digital Input Format 0 in PCM Mode
	CAD1	I	Chip Address 1 in Serial Control Mode
12	DIF1	I	Digital Input Format 1 in PCM Mode
	DZF1	O	Zero Input Detect in Serial Control Mode
13	DIF2	I	Digital Input Format 2 in PCM Mode
14	PSN	I	Parallel/Serial Select (Internal pull-up pin) "L": Serial Control Mode, "H": Parallel Control Mode
15	ACKS	I	Auto Clock Setting Mode in Parallel Control mode "L": Manual Setting Mode, "H": Auto Setting Mode
	DZF2	O	Zero Input Detect in Serial Control Mode
16	TDM0	I	TDM I/F Format Mode in Parallel Control mode
17	SLOW	I	Digital filter setting pin
18	TEST	-	No internal bonding. Connect to DVSS.
19	VCM2	-	Common Voltage 2 Normally connected to VSS with a 10uF electrolytic cap.
20	AOUTR2P	O	Right Channel Positive Analog Output 2
21	AOUTR2N	O	Right Channel Negative Analog Output 2
22	VDD2	-	Analog Power Supply, 4.75 to 5.25V
23	VSS2	-	Ground (connected to DVSS, AVSS, VSS1 ground)
24	VREFL2	I	Low Level Voltage Reference Input 2
25	VREFH2	I	High Level Voltage Reference Input 2
26	AOUTL2N	O	Left Channel Negative Analog Output 2
27	AOUTL2P	O	Left Channel Positive Analog Output 2
28	NC	-	No internal bonding. Connect to GND.

No.	Pin Name	I/O	Function
29	AOUTR1P	O	Right Channel Positive Analog Output 1
30	AOUTR1N	O	Right Channel Negative Analog Output 1
31	VREFH1	I	High Level Voltage Reference Input 1
32	VREFL1	I	Low Level Voltage Reference Input 1
33	VSS1	-	Connected to DVSS, AVSS, VSS2 Ground
34	VDD1	-	Analog Power Supply Pin, 4.75 ~ 5.25V
35	AOUTL1N	O	Left Channel Negative Analog Output 1
36	AOUTL1P	O	Left Channel Positive Analog Output 1
37	VCM1	-	Common Voltage 1 Normally connected to VSS with a 10uF electrolytic cap.
38	TSTO1	I	Test Output pin. "Hi-Z" at Normal Operation. Connect to AVSS.
39	TSTO2	I	Test Output pin. "Hi-Z" at Normal Operation. Connect to AVSS.
40	AVDD	-	Analog Power Supply, 2.7 to 3.6V
41	AVSS	-	Analog Ground Pin
42	MCLK	I	Master Clock Input
43	DVSS	-	Digital Ground Pin
44	DVDD	-	Digital Power Supply, 3.0 ~ 3.6V

Note: All input pins except internal pull-up/down pins should not be left floating.

## ■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

### (1) Parallel Mode

Classification	Pin Name	Setting
Analog	AOUTL1P, AOUTL1N	These pins must be open.
	AOUTR1P, AOUTR1N	These pins must be open.
	AOUTL2P, AOUTL2N	These pins must be open.
	AOUTR2P, AOUTR2N	These pins must be open.
Analog	TSTO1, TSTO2	This pin must be connected to AVSS
Digital	TEST	This pin must be connected to DVSS

### (2) Serial Mode

Classification	Pin Name	Setting
Analog	AOUTL1P, AOUTL1N	These pins must be open.
	AOUTR1P, AOUTR1N	These pins must be open.
	AOUTL2P, AOUTL2N	These pins must be open.
	AOUTR2P, AOUTR2N	These pins must be open.
Analog	TSTO1, TSTO2	This pin must be connected to AVSS
Digital	DIF2, PSN, TDM0, SLOW, TEST	This pin must be connected to DVSS
	DZF1, DZF2	These pins must be open.

<b>ABSOLUTE MAXIMUM RATINGS</b>
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(VSS1-2=AVSS=DVSS=0V; [Note 1](#))

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	-0.3	4.6	V
	Analog	VDD1/2	-0.3	6.0	V
	Digital	DVDD	-0.3	4.6	V
	AVSS – DVSS	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	-10	70	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

Note 2. AVSS, VSS1/2, DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

<b>RECOMMENDED OPERATING CONDITIONS</b>
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(VSS1-2=AVSS=DVSS=0V; [Note 1](#))

Parameter		Symbol	min	typ	max	Unit
Power Supplies ( <a href="#">Note 3</a> )	Analog	AVDD	2.7	3.0	3.6	V
	Analog	VDD1/2	4.75	5.0	5.25	V
	Digital	DVDD	2.7	3.0	3.6	V
Voltage Reference ( <a href="#">Note 4</a> )	“H” voltage reference	VREFH1	VDD1-0.5	-	VDD1	V
	“H” voltage reference	VREFH2	VDD2-0.5	-	VDD2	V
	“L” voltage reference	VREFL1	-	AVSS	-	V
	“L” voltage reference	VREFL2	-	AVSS	-	V

Note 1. All voltages with respect to ground.

Note 3. The power up sequence between AVDD, VDD1/2 and DVDD is not critical.

Note 4. The analog output voltage scales with the voltage of (VREFH1/2 – VREFL1/2).

Connect a resistor of 20ohm or less and a capacitor of 100uF or more to the VREFH1/2 pin. ([Figure 19](#)) $AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = \pm 2.8V_{pp} \times (VREFH1/2 - VREFL1/2)/5.$ 

\* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.



<b>ANALOG CHARACTERISTICS</b>
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(Ta=25°C; AVDD=DVDD=3.0V, VDD1/2=5.0V; AVSS=VSS1/2=DVSS=0V; VREFH1/2=VDD1/2, VREFL1/2=AVSS; Input data = 24bit; R<sub>L</sub> ≥ 1kΩ; BICK=64fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: [Figure 22](#); unless otherwise specified.)

Parameter		min	typ	max	Unit	
Resolution		-	-	24	Bits	
<b>Dynamic Characteristics</b> (Note 5)						
THD+N	fs=44.1kHz (Note 6) BW=20kHz	0dBFS	-	-104	-95	dB
		-60dBFS		-57	-	dB
	fs=96kHz BW=40kHz	0dBFS	-	-99	-	dB
		-60dBFS	-	-54	-	dB
	fs=192kHz BW=40kHz	0dBFS		-99	-	dB
		-60dBFS		-54	-	dB
fs=192kHz BW=80kHz	0dBFS		-99	-	dB	
	-60dBFS		-51	-	dB	
Dynamic Range (-60dBFS with A-weighted)		(Note 6)	113	120	dB	
S/N (A-weighted)		(Note 7)	113	120	dB	
Interchannel Isolation (1kHz)			100	110	dB	
<b>DC Accuracy</b>						
Interchannel Gain Mismatch			-	0	0.3	dB
Gain Drift		(Note 8)	-	20	-	ppm/°C
Output Voltage		(Note 9)	±2.65	±2.8	±2.95	V <sub>pp</sub>
Load Capacitance			-	-	10	pF
Load Resistance		(Note 10)	1	-	-	kΩ
<b>Power Supplies</b>						
Power Supply Current						
	Normal operation (PDN pin = "H")					
	VDD1+VDD2		-	41	60	mA
	AVDD		-	1	1.5	mA
	DVDD (fs ≤ 44.1kHz)		-	7	11	mA
	DVDD (fs=96kHz)		-	12	18	mA
	DVDD (fs = 192kHz)		-	18	27	mA
	Power down (PDN pin = "L")		(Note 11)			
	AVDD+VDD1/2+DVDD		-	10	100	μA

Note 5. Measured by Audio Precision, System Two. Averaging mode. Refer to the evaluation board manual.

Note 6. [Figure 22](#) External LPF Circuit Example 2. 100dB for 16-bit data.

Note 7. [Figure 22](#) External LPF Circuit Example 2. S/N does not depend on input data size.

Note 8. The voltage on (VREFH1/2 – VREFL1/2) is held +5V externally.

Note 9. Full scale voltage (0dB). Output voltage scales with the voltage of (VREFH1/2 – VREFL1/2).

$$AOUT(\text{typ.}@0\text{dB}) = (AOUT+) - (AOUT-) = \pm 2.8V_{pp} \times (VREFH1/2 - VREFL1/2)/5.$$

Note 10. Regarding Load Resistance, AC load is 1kΩ (min) with a DC cut capacitor ([Figure 22](#)). DC load is 1.5kΩ (min) without a DC cut capacitor ([Figure 21](#)). The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore the capacitive load must be minimized.

Note 11. In the power down mode. The PSN pin = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.

**SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="0")

Parameter	Symbol	min	typ	max	Unit
<b>Digital Filter</b>					
Passband (Note 12)	±0.01dB -6.0dB	PB	0	22.05	20.0
			-		-
Stopband (Note 12)	SB	24.1			kHz
Passband Ripple	PR	-0.0032	-	0.0032	dB
Stopband Attenuation	SA	80			dB
Group Delay (Note 13)	GD	-	29	-	1/fs
<b>Digital Filter + SCF</b>					
Frequency Response: 0 ~ 20.0kHz		-0.2	-	0.2	dB

**SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="0")

Parameter	Symbol	min	typ	max	Unit
<b>Digital Filter</b>					
Passband (Note 12)	±0.01dB -6.0dB	PB	0	48.0	43.5
			-		-
Stopband (Note 12)	SB	52.5			kHz
Passband Ripple	PR	-0.0032	-	0.0032	dB
Stopband Attenuation	SA	80			dB
Group Delay (Note 13)	GD	-	29	-	1/fs
<b>Digital Filter + SCF</b>					
Frequency Response: 0 ~ 40.0kHz		-0.3	-	0.3	dB

**SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "0". SD bit="0")

Parameter	Symbol	min	typ	max	Unit
<b>Digital Filter</b>					
Passband (Note 12)	±0.01dB -6.0dB	PB	0	96.0	87.0
			-		-
Stopband (Note 12)	SB	105			kHz
Passband Ripple	PR	-0.0032	-	0.0032	dB
Stopband Attenuation	SA	80			dB
Group Delay (Note 13)	GD	-	29	-	1/fs
<b>Digital Filter + SCF</b>					
Frequency Response: 0 ~ 80.0kHz		-1	-	0.1	dB

Note 12. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs, SB=0.546×fs.

Note 13. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24-bit data of both channels to input register to the output of analog signal.

**SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit="1", SD bit = "0")

Parameter	Symbol	min	typ	max	Unit	
<b>Digital Filter</b>						
Passband (Note 14)	±0.04dB -3.0dB	PB	0	18.2	8.1	kHz
			-		-	kHz
Stopband (Note 14)	SB	39.2			kHz	
Passband Ripple	PR	-0.043	-	0.043	dB	
Stopband Attenuation	SA	73			dB	
Group Delay (Note 13)	GD	-	6	-	1/fs	
<b>Digital Filter + SCF</b>						
Frequency Response: 0 ~ 20.0kHz		-5	-	0.1	dB	

**SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Double Speed Mode DEM=OFF; SLOW bit="1", SD bit = "0")

Parameter	Symbol	min	typ	max	Unit	
<b>Digital Filter</b>						
Passband (Note 14)	±0.04dB -3.0dB	PB	0	39.6	17.7	kHz
			-		-	kHz
Stopband (Note 14)	SB	85.3			kHz	
Passband Ripple	PR	-0.043	-	0.043	dB	
Stopband Attenuation	SA	73			dB	
Group Delay (Note 13)	GD	-	6	-	1/fs	
<b>Digital Filter + SCF</b>						
Frequency Response: 0 ~ 40.0kHz		-4	-	0.1	dB	

**SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit="1", SD bit = "0")

Parameter	Symbol	min	typ	max	Unit	
<b>Digital Filter</b>						
Passband (Note 14)	±0.04dB -3.0dB	PB	0	79.1	35.5	kHz
			-		-	kHz
Stopband (Note 14)	SB	171			kHz	
Passband Ripple	PR	-0.043	-	0.043	dB	
Stopband Attenuation	SA	73			dB	
Group Delay (Note 13)	GD	-	6	-	1/fs	
<b>Digital Filter + SCF</b>						
Frequency Response: 0 ~ 80.0kHz		-5	-	0.1	dB	

Note 14. The passband and stopband frequencies scale with fs. For example, PB=0.185×fs, SB=0.888×fs.

**SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter	Symbol	min	typ	max	Unit	
<b>Digital Filter</b>						
Passband (Note 12)	±0.01dB -6.0dB	PB	0	22.05	20.0	kHz
			-		-	kHz
Stopband (Note 12)	SB	24.1			kHz	
Passband Ripple	PR	-0.0031	-	0.0031	dB	
Stopband Attenuation	SA	80			dB	
Group Delay (Note 13)	GD	-	7	-	1/fs	
<b>Digital Filter + SCF</b>						
Frequency Response : 0 ~ 20.0kHz		-0.2	-	0.2	dB	

**SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter	Symbol	min	typ	max	Unit	
<b>Digital Filter</b>						
Passband (Note 12)	±0.01dB -6.0dB	PB	0	48.0	43.5	kHz
			-		-	kHz
Stopband (Note 12)	SB	52.5			kHz	
Passband Ripple	PR	-0.0031	-	0.0031	dB	
Stopband Attenuation	SA	80			dB	
Group Delay (Note 13)	GD	-	7	-	1/fs	
<b>Digital Filter + SCF</b>						
Frequency Response : 0 ~ 40.0kHz		-0.3	-	0.3	dB	

**SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter	Symbol	min	typ	max	Unit	
<b>Digital Filter</b>						
Passband (Note 12)	±0.01dB -6.0dB	PB	0	96.0	87.0	kHz
			-		-	kHz
Stopband (Note 12)	SB	105			kHz	
Passband Ripple	PR	-0.0031	-	0.0031	dB	
Stopband Attenuation	SA	80			dB	
Group Delay (Note 13)	GD	-	7	-	1/fs	
<b>Digital Filter + SCF</b>						
Frequency Response : 0 ~ 80.0kHz		-1	-	0.1	dB	

**SHORT DELAY SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter	Symbol	min	typ	max	Unit
<b>Digital Filter</b>					
Passband (Note 12)	±0.01dB -6.0dB	PB	0	11.1	kHz
			-	22.3	kHz
Stopband (Note 12)	SB	38.1			kHz
Passband Ripple	PR	-0.05	-	0.05	dB
Stopband Attenuation	SA	82			dB
Group Delay (Note 13)	GD	-	5.5	-	1/fs
<b>Digital Filter + SCF</b>					
Frequency Response : 0 ~ 20.0kHz		-5	-	0.1	dB

**SHORT DELAY SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter	Symbol	min	typ	max	Unit
<b>Digital Filter</b>					
Passband (Note 12)	±0.01dB -6.0dB	PB	0	24.2	kHz
			-	44.6	kHz
Stopband (Note 12)	SB	83.0			kHz
Passband Ripple	PR	-0.05	-	0.05	dB
Stopband Attenuation	SA	82			dB
Group Delay (Note 13)	GD	-	5.5	-	1/fs
<b>Digital Filter + SCF</b>					
Frequency Response : 0 ~ 40.0kHz		-5	-	0.1	dB

**SHORT DELAY SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)**

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter	Symbol	min	typ	max	Unit
<b>Digital Filter</b>					
Passband (Note 12)	±0.01dB -6.0dB	PB	0	48.4	kHz
			-	89.2	kHz
Stopband (Note 12)	SB	165.9			kHz
Passband Ripple	PR	-0.05	-	0.05	dB
Stopband Attenuation	SA	82			dB
Group Delay (Note 13)	GD	-	5.5	-	1/fs
<b>Digital Filter + SCF</b>					
Frequency Response : 0 ~ 80.0kHz		-5	-	0.1	dB

<b>DC CHARACTERISTICS</b>
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(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=-100μA)	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage (Iout=100μA)	VOL	-	-	0.5	V
Input Leakage Current (Note 15)	Iin	-	-	±10	μA

Note 15. The PSN pin has an internal pull-up device nominally 100kΩ. Therefore the PSN pin is not included.

## SWITCHING CHARACTERISTICS

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V)

Parameter	Symbol	min	typ	max	Unit
<b>Master Clock Timing</b>					
Frequency	fCLK	2.048		41.472	MHz
Duty Cycle	dCLK	40		60	%
<b>LRCK Frequency (Note 16)</b>					
<b>Normal Mode (TDM0= "L", TDM1= "L")</b>					
1152fs, 512fs or 768fs	f <sub>sn</sub>	8		54	kHz
256fs or 384fs	f <sub>sd</sub>	54		108	kHz
128fs or 192fs	f <sub>sq</sub>	108		216	kHz
Duty Cycle	Duty	45		55	%
<b>TDM256 mode (TDM0= "H", TDM1= "L")</b>					
Normal Speed Mode High time	f <sub>sn</sub>	8		54	kHz
Low time	t <sub>LRH</sub>	1/256fs			ns
	t <sub>LRL</sub>	1/256fs			ns
<b>TDM128 mode (TDM0= "H", TDM1= "H")</b>					
Normal Speed Mode	f <sub>sn</sub>	8		54	kHz
Double Speed Mode	f <sub>sd</sub>	54		108	kHz
Quad Speed Mode	f <sub>sq</sub>	108		216	kHz
High time	t <sub>LRH</sub>	1/128fs			ns
Low time	t <sub>LRL</sub>	1/128fs			ns
<b>PCM Audio Interface Timing</b>					
<b>Normal Mode (TDM0= "L", TDM1= "L")</b>					
BICK Period					
1152fs, 512fs or 768fs	t <sub>BCK</sub>	1/128f <sub>sn</sub>			ns
256fs or 384fs	t <sub>BCK</sub>	1/64f <sub>sd</sub>			ns
128fs or 192fs	t <sub>BCK</sub>	1/64f <sub>sq</sub>			ns
BICK Pulse Width Low	t <sub>BCKL</sub>	14			ns
BICK Pulse Width High	t <sub>BCKH</sub>	14			ns
BICK "↑" to LRCK Edge (Note 17)	t <sub>BLR</sub>	14			ns
LRCK Edge to BICK "↑" (Note 17)	t <sub>LRB</sub>	14			ns
SDATA Hold Time	t <sub>SDH</sub>	5			ns
SDATA Setup Time	t <sub>SDS</sub>	5			ns
<b>TDM256 mode (TDM0= "H", TDM1= "L")</b>					
BICK Period					
Normal Speed Mode	t <sub>BCK</sub>	1/256f <sub>sn</sub>			ns
BICK Pulse Width Low	t <sub>BCKL</sub>	14			ns
BICK Pulse Width High	t <sub>BCKH</sub>	14			ns
BICK "↑" to LRCK Edge (Note 17)	t <sub>BLR</sub>	14			ns
LRCK Edge to BICK "↑" (Note 17)	t <sub>LRB</sub>	14			ns
SDATA1/2 Hold Time	t <sub>SDH</sub>	5			ns
SDATA1/2 Setup Time	t <sub>SDS</sub>	5			ns

<b>TDM128 mode (TDM0= “H”, TDM1= “H”)</b>					
BICK Period					
Normal Speed Mode	tBCK	1/128fsn			ns
Double Speed Mode	tBCK	1/128fsd			ns
Quad Speed Mode	tBCK	1/128fsq			ns
BICK Pulse Width Low	tBCKL	14			ns
BICK Pulse Width High	tBCKH	14			ns
BICK “↑” to LRCK Edge (Note 17)	tBLR	14			ns
LRCK Edge to BICK “↑” (Note 17)	tLRB	14			ns
SDATA1/2 Hold Time	tSDH	5			ns
SDATA1/2 Setup Time	tSDS	5			ns
<b>Control Interface Timing</b>					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN High Time	tCSW	150			ns
CSN “↓” to CCLK “↑”	tCSS	50			ns
CCLK “↑” to CSN “↑”	tCSH	50			ns
<b>Reset Timing</b>					
PDN Pulse Width (Note 18)	tPD	150			ns

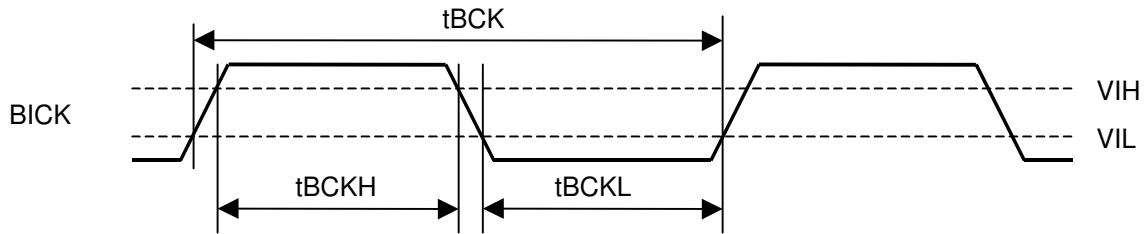
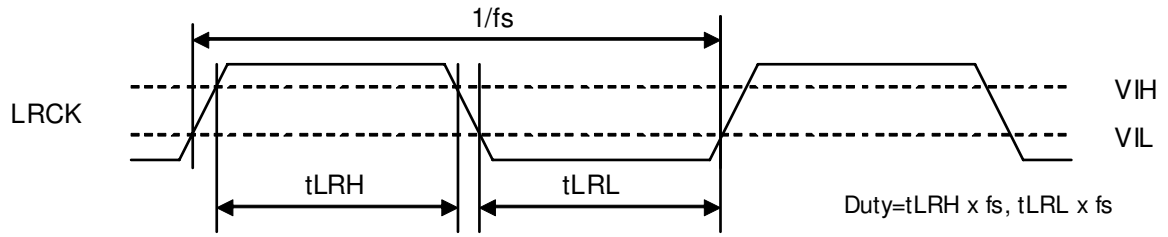
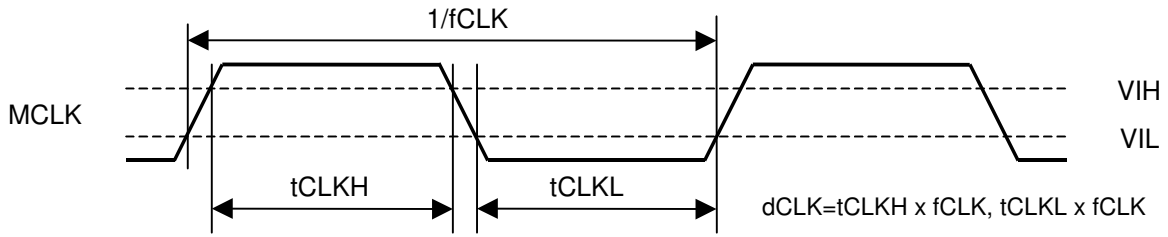
Note 16. When the 1152fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK4413 should be reset by the PDN pin or RSTN bit.

Note 17. BICK rising edge must not occur at the same time as LRCK edge.

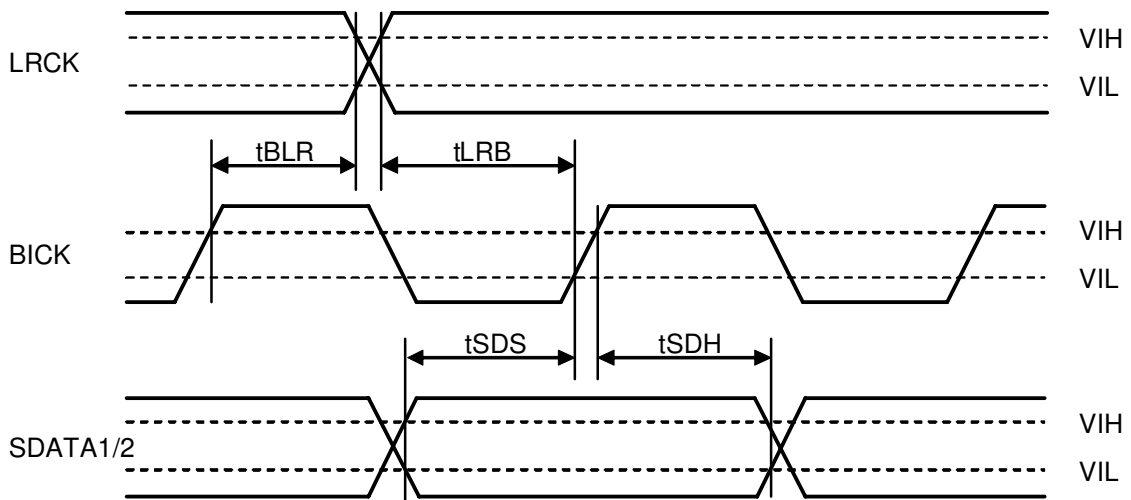
Note 18. The AK4413 can be reset by bringing the PDN pin “L” to “H” upon power-up.



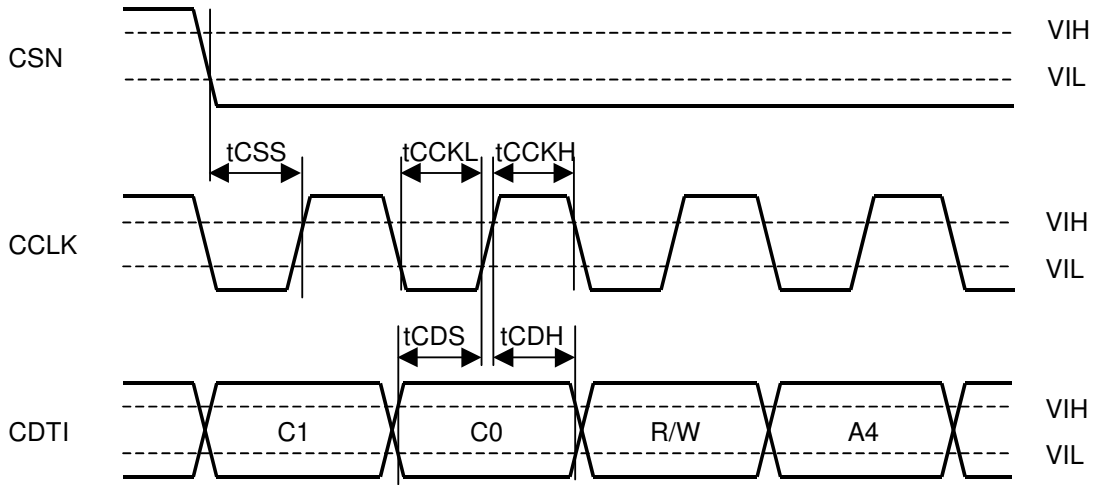
■ Timing Diagram



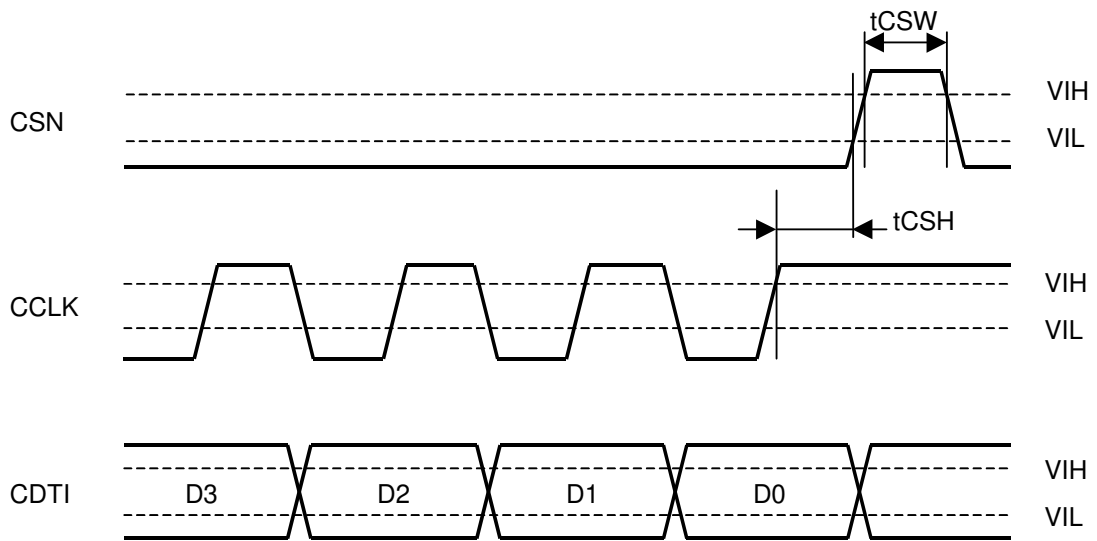
Clock Timing



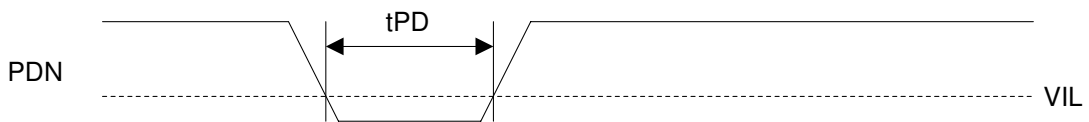
Audio Interface Timing (PCM Mode)



WRITE Command Input Timing



WRITE Data Input Timing



Power Down & Reset Timing

<b>OPERATION OVERVIEW</b>
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## ■ System Clock

### [1] PCM Mode

The external clocks, which are required to operate the AK4413, are MCLK, BICK and LRCK. MCLK should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator.

The AK4413 is automatically placed in reset state when MCLK and LRCK are stopped during a normal operation (PDN pin = "H"), and the analog output becomes AVDD/2 (typ). When MCLK and LRCK are input again, the AK4413 exit reset state and starts the operation. After exiting system reset (PDN pin = "L" → "H") at power-up and other situations, the AK4413 is in power-down mode until MCLK and LRCK are supplied.

(1) Parallel Mode (PSN pin = "H")

#### 1. Manual Setting Mode

In manual setting mode (ACKS pin = "L") only Normal Speed mode is supported with the sample rate range shown in (Table 1). The AK4413 automatically configures itself to operate with the supported MCLK frequencies which are required to be provided as input and are shown in (Table 2).

Sampling Rate (fs)	
Normal Speed Mode	8kHz ~ 54kHz

Table 1. Sampling Speed (Manual Setting Mode @Parallel Mode)

LRCK fs	MCLK (MHz)							BICK 64fs
	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	2.0480MHz
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	2.8224MHz
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	3.0720MHz

Table 2. System Clock Example (Manual Setting Mode @Parallel Mode), (N/A: Not available)

## 2. Auto Setting Mode (ACKS pin = "H")

In this mode, sampling speed and MCLK frequency are detected automatically (Table 3) The MCLK must be supplied at the correct frequency according to Table 4.

MCLK		Sampling Speed
1152fs		Normal (fs≤32kHz)
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 3. Sampling Speed (Auto Setting Mode @Parallel Mode)

LRCK fs	MCLK (MHz)							Sampling Speed
	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	N/A	N/A	(8.1920*)	(12.2880*)	16.3840	24.5760	36.8640	Normal/ (Double*)
44.1kHz	N/A	N/A	(11.2896*)	(16.9344*)	22.5792	33.8688	N/A	
48.0kHz	N/A	N/A	(12.2880*)	(18.4320*)	24.5760	36.8640	N/A	
88.2kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	N/A	
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A	

Table 4. System Clock Example (Auto Setting Mode @Parallel Mode), (N/A: Not available)

MCLK= 256fs/384fs supports sampling rate of 32kHz~96kHz (Table 5). However, when the sampling rate is 32kHz~48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

ACKS pin	MCLK	DR,S/N
L	256fs/384fs/512fs/768fs	120dB
H	256fs/384fs	117dB
H	512fs/768fs	120dB

Table 5. Relationship between MCLK frequency and DR, S/N (fs= 44.1kHz)

## 3. Digital Filter Setting

SD pin	SLOW pin	Mode
0	0	Sharp roll-off filter
0	1	Slow roll-off filter
1	0	Short delay sharp roll-off
1	1	Short delay slow roll-off

Table 6. Digital Filter Setting (Parallel Mode)

## (2) Serial Mode (PSN pin = “L”)

## 1. Manual Setting Mode (ACKS bit = “0”)

MCLK frequency is detected automatically and the sampling rate is set by DFS1-0 bits (Table 7). The MCLK frequency corresponding to each sampling speed should be provided externally (Table 8). The AK4413 is set to Manual Setting Mode at power-up (PDN pin = “L” → “H”). When DFS1-0 bits are changed, the AK4413 should be reset by RSTN bit.

DFS1 bit	DFS0 bit	Sampling Rate (fs)	
0	0	Normal Speed Mode	30kHz ~ 54kHz
0	1	Double Speed Mode	54kHz ~ 108kHz
1	0	Quad Speed Mode	120kHz ~ 216kHz

(default)

Table 7. Sampling Speed (Manual Setting Mode @Serial Mode)

LRCK fs	MCLK (MHz)							BICK 64fs
	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	2.0480MHz
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	2.8224MHz
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	3.0720MHz
88.2kHz	11.2896	16.9344	22.5792	33.8688	N/A	N/A	N/A	5.6448MHz
96.0kHz	12.2880	18.4320	24.5760	36.8640	N/A	N/A	N/A	6.1440MHz
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	11.2896MHz
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A	12.2880MHz

Table 8. System Clock Example (Manual Setting Mode @Serial Mode)

## 2. Auto Setting Mode (ACKS bit = “1”)

MCLK frequency and the sampling speed are detected automatically (Table 9) and DFS1-0 bits are ignored. The MCLK frequency corresponding to each sampling speed should be provided externally (Table 10).

MCLK		Sampling Speed
1152fs		Normal (fs≤32kHz)
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 9. Sampling Speed (Auto Setting Mode @Serial Mode)

LRCK fs	MCLK (MHz)							Sampling Speed
	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	N/A	N/A	(8.1920*)	(12.2880*)	16.3840	24.5760	36.8640	Normal/ (Double*)
44.1kHz	N/A	N/A	(11.2896*)	(16.9344*)	22.5792	33.8688	N/A	
48.0kHz	N/A	N/A	(12.2880*)	(18.4320*)	24.5760	36.8640	N/A	
88.2kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	N/A	
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A	

Table 10. System Clock Example (Auto Setting Mode @Serial Mode)

MCLK= 256fs/384fs supports sampling rate of 32kHz~96kHz (Table 11). However, when the sampling rate is 32kHz~48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

ACKS pin	MCLK	DR,S/N
L	256fs/384fs/512fs/768fs	120dB
H	256fs/384fs	117dB
H	512fs/768fs	120dB

Table 11. Relationship between MCLK frequency and DR, S/N (fs= 44.1kHz)

### 3. Digital Filter Setting

SD bit	SLOW bit	Mode
0	0	Sharp roll-off filter
0	1	Slow roll-off filter
1	0	Short delay sharp roll-off
1	1	Short delay slow roll-off

(default)

Table 12. Digital Filter Setting (Serial Mode)

## ■ Audio Interface Format

### [1] PCM Mode

#### (1) Parallel Control Mode (PSN pin = “H”)

Twenty formats are selectable by DIF2-0 and TDM1-0 pins (Table 13). In this mode, register settings are ignored. In all formats the serial data is MSB-first, 2's complement format and is latched on the rising edge of BICK. Mode 2 can be used for 20 and 16 MSB justified formats by zeroing the unused LSBs.

If TDM1-0 pins = “LH” the audio interface is TDM256 mode (Table 13) and all eight channels of DAC data are input to the SDTI1 pin. The input data to the SDTI2 pin is ignored. BICK is fixed to 256fs, “H” time and “L” time of LRCK should be 1/256fs at least. The data format is MSB first, 2's complement and the SDTI1 is latched on the rising edge of BICK. Only the first four channels of DAC data may be selected to be converted into four channels of DAC analog output.

If TDM1-0 pins = “HH” the audio interface is TDM128 mode (Table 13) and the serial data of DAC (four channels: L1, R1, L2, R2) is input to the SDTI1 pin.

Mode	TDM1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK	
Normal	-	0	0	0	0	16-bit LSB justified	H/L	≥32fs	
			1	0	1	20-bit LSB justified	H/L	≥40fs	
			2	0	1	0	24-bit MSB justified	H/L	≥48fs
			3	0	1	1	24-bit I <sup>2</sup> S compatible	L/H	≥48fs
			4	1	0	0	24-bit LSB justified	H/L	≥48fs
			5	1	0	1	32-bit LSB justified	H/L	≥64fs
			6	1	1	0	32-bit MSB justified	H/L	≥64fs
			7	1	1	1	32-bit I <sup>2</sup> S compatible	L/H	≥64fs
TDM256	0	1	0	0	0	N/A			
			0	0	1	N/A			
			8	0	1	0	24-bit MSB justified	↑	256fs
			9	0	1	1	24-bit I <sup>2</sup> S compatible	↓	256fs
			10	1	0	0	24-bit LSB justified	↑	256fs
			11	1	0	1	32-bit LSB justified	↑	256fs
			12	1	1	0	32-bit MSB justified	↑	256fs
			13	1	1	1	32-bit I <sup>2</sup> S compatible	↓	256fs
TDM128	1	1	0	0	0	N/A			
			0	0	1	N/A			
			14	0	1	0	24-bit MSB justified	↑	128fs
			15	0	1	1	24-bit I <sup>2</sup> S compatible	↓	128fs
			16	1	0	0	24-bit LSB justified	↑	128fs
			17	1	0	1	32-bit LSB justified	↑	128fs
			18	1	1	0	32-bit MSB justified	↑	128fs
			19	1	1	1	32-bit I <sup>2</sup> S compatible	↓	128fs

Table 13. Audio Interface Format (Parallel mode)

## (2) Serial Control Mode (PSN pin = “L”)

Twenty formats are selected by setting DIF2-0 and TDM1-0 bits (Table 14). The initial setting of DIF2-0 bits is “010”. In this mode, the DIF1 pin setting is ignored.

The audio I/F format is TDM256 mode (Table 14) and all the serial data of eight DAC channels are input to the SDTI1 pin (Figure 15). The input data to the SDTI2 pin is ignored. BICK is fixed to 256fs, high and low amplitude of LRCK is 1/256fs (min). The data format is MSB first, 2’s complement and the SDTI1 is latched on the rising edge of BICK. The eight channels of DAC data may be mapped to two pieces of AK4413 (Table 15).

In TDM128 mode, the serial data of DAC (four channels: L1, R1, L2, R2) is input to the SDTI pin and other serial data of DAC (four channels: L3, R3, L4, R4) are input to the SDTI2 pin (Figure 14). BICK is fixed to 128fs. The data format is MSB first and 2’s complement and the input data to SDTI1-2 pins are latched on the rising edge of BICK. The eight channels of DAC data may be mapped to two pieces of AK4413 (Table 15).

Mode	TDM1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK	
Normal	-	0	0	0	0	16-bit LSB justified	H/L	≥32fs	
			1	0	1	20-bit LSB justified	H/L	≥40fs	
			2	0	1	0	24-bit MSB justified	H/L	≥48fs
			3	0	1	1	24-bit I <sup>2</sup> S compatible	L/H	≥48fs
			4	1	0	0	24-bit LSB justified	H/L	≥48fs
			5	1	0	1	32-bit LSB justified	H/L	≥64fs
			6	1	1	0	32-bit MSB justified	H/L	≥64fs
			7	1	1	1	32-bit I <sup>2</sup> S compatible	L/H	≥64fs
TDM256	0	1	0	0	0	N/A			
			0	0	1	N/A			
			8	0	1	0	24-bit MSB justified	↑	256fs
			9	0	1	1	24-bit I <sup>2</sup> S compatible	↓	256fs
			10	1	0	0	24-bit LSB justified	↑	256fs
			11	1	0	1	32-bit LSB justified	↑	256fs
			12	1	1	0	32-bit MSB justified	↑	256fs
			13	1	1	1	32-bit I <sup>2</sup> S compatible	↓	256fs
TDM128	1	1	0	0	0	N/A			
			0	0	1	N/A			
			14	0	1	0	24-bit MSB justified	↑	128fs
			15	0	1	1	24-bit I <sup>2</sup> S compatible	↓	128fs
			16	1	0	0	24-bit LSB justified	↑	128fs
			17	1	0	1	32-bit LSB justified	↑	128fs
			18	1	1	0	32-bit MSB justified	↑	128fs
			19	1	1	1	32-bit I <sup>2</sup> S compatible	↓	128fs

Table 14. Audio Interface Format (Serial mode)





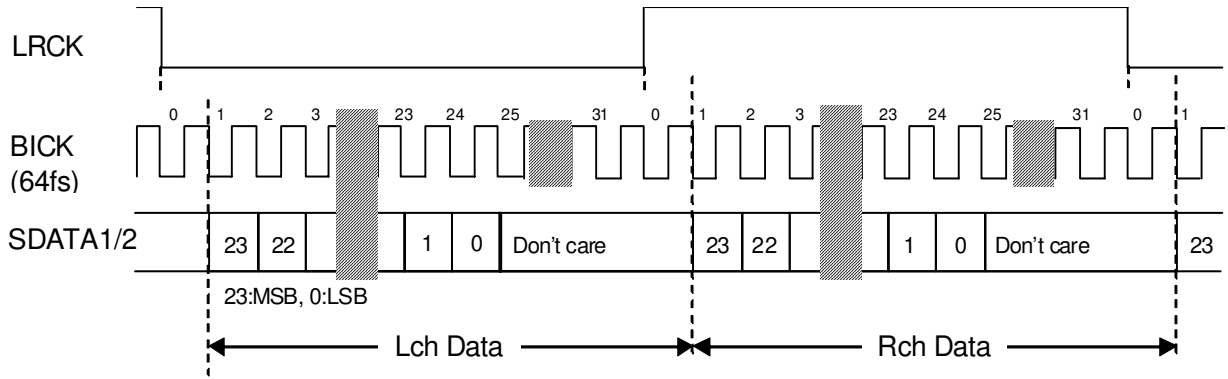


Figure 4. Mode 3 Timing

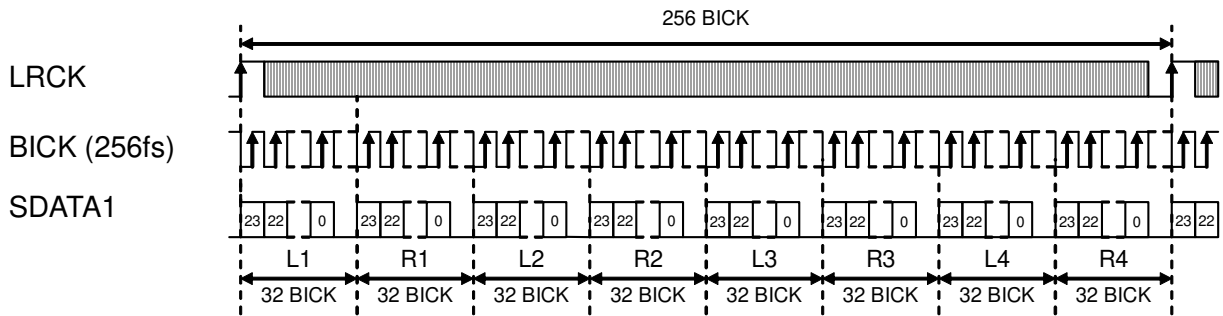


Figure 5. Mode 8 Timing

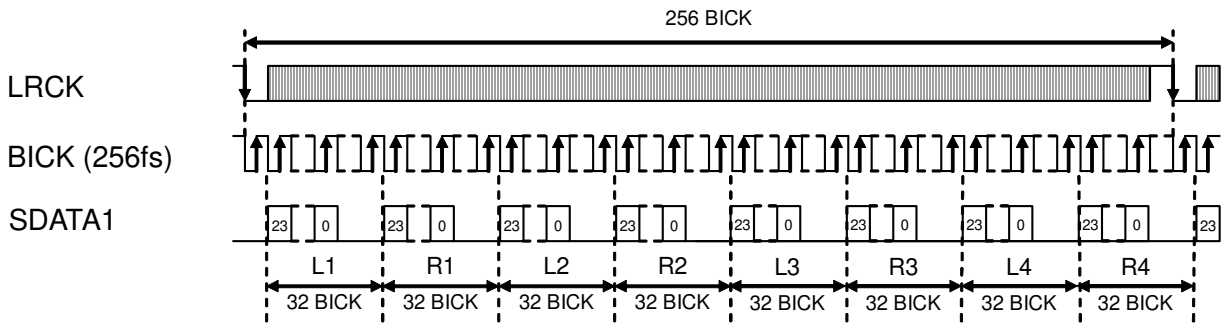


Figure 6. Mode 9 Timing