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AK4432

108dB 192kHz 32bit 2-Channel Audio DAC

1. General Description

The AK4432 is a 32-bit Stereo DAC which corresponds to digital audio systems. An internal circuit includes newly developed 32-bit Digital Filter achieving short group delay and high quality sound. The AK4432 has single end SCF outputs, increasing performance for systems with excessive clock jitter. The AK4432 is ideal for a wide range of applications that demands high sound quality including Home Theater and Car audio surround systems. It is housed in a 16-pin TSSOP package, saving more board space.

2. Features

1. 2ch 32bit DAC
- **128 times Oversampling**
- **32-bit High Quality Sound Low Group Delay Digital Filter**
- **Single Ended Output, Smoothing Filter**
- **THD+N: 91dB**
- **DR, S/N: 108dB**
- **Channel Isolation Digital Volume (12dB～-115dB, 0.5dB Step, Mute)**
- **Soft Mute**
- **De-emphasis Filter (32kHz, 44.1kHz, 48kHz)**
- **I/F Format: MSB justified, LSB justified, I^2S, TDM**
- **Zero Detection**

2. Sampling Frequency
- **Normal Speed Mode: 8kHz to 48kHz**
- **Double Speed Mode: 64kHz to 96kHz**
- **Quad Speed Mode: 128kHz to 192kHz**

3. Master Clock

256fs, 384fs, 512fs or 768fs	**(Normal Speed Mode: fs=8kHz ~ 48kHz)**
256fs or 384fs	**(Double Speed Mode: fs=48kHz ~ 96kHz)**
128fs or 192fs	**(Quad Speed Mode: fs=96kHz ~ 192kHz)**

4. μP Interface: 3-wire Serial (7MHz max)/ I^2C bus (400kHz Mode, 1MHz Mode)

5. Power Supply
- **Analog: AVDD = 3.0 ~ 3.6V**
- **Input/Output Buffer: LVDD = 3.0 ~ 3.6V**
- **Integrated LDO for Digital Power Supply**

6. Power Consumptions: 7.8mA (fs=48kHz)

7. Operational Temperature: Ta = - 40 ~ 105°C

8. Package: 16-pin TSSOP (0.65mm pitch)

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4. Block Diagram

■ Block Diagram

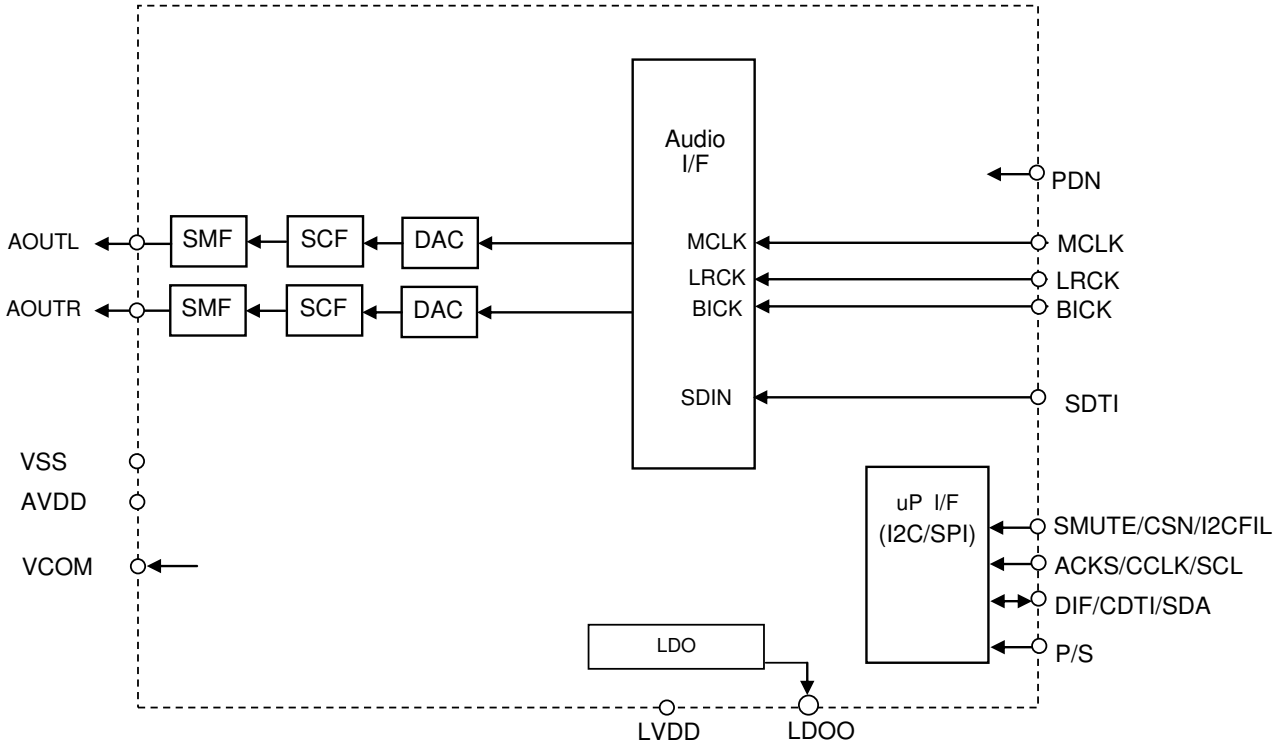

Figure 1. Block Diagram

■Compatibility with AK4438, AK4452 and AK4458

		AK4432	AK4436 / 38	AK4452 / 54 / 56 / 58
Channel		2ch	6ch / 8ch	2ch / 4ch / 6ch / 8ch
fs		8k to 192kHz	8k to 768kHz	8k to 768kHz
S/(N+D)		91dB	91dB	107dB
DR		108dB	108dB	115dB
AVDD (Analog Supply)		3.0 to 3.6V	3.0 to 3.6V	3.0 to 5.5V
TVDD or LVDD (I/O Buffer)		3.0 to 3.6V	1.7 to 3.6V	1.7 to 3.6V
Digital Filter	SA(Sharp)	69.9dB	80dB	80dB
	GD(Sharp)	26.4/fs	26.8/fs	26.8/fs
	GD (SD Slow)	5.2/fs	4.8/fs	4.8/fs
	Super Slow Roll-off	No	Yes	Yes
OSR Doubler (Over Sampling)		No (128x)	Yes (256x)	Yes (256x)
Zero Detection		No	Yes	Yes
Digital Volume		+12 to -115.0dB	+0 to -127.0dB	+0 to -127.0dB
ATT Speed (*Default)		1020/fs (*) 4080	4080/fs (*) 2040、510、255	4080/fs (*) 2040、510、255
LR Ch Output Select		No	Yes	Yes
Reset Function (MCLK detect)		No	Yes	Yes
Clock Synchronization		Yes (Note)	Yes	Yes
Package		16-pin TSSOP	32-pin QFN	AK4452/54: 32-pin QFN AK4456/58: 48-pin QFN

Note. MSB justified and 32-bit I^2S compatible formats are available for audio interface but LSB justified format is not available.

5. Pin Configurations and Functions

■ Ordering Guide

AK4432VT	-40 ~ +105°C	16-pin TSSOP (0.65mm pitch)
AKD4432	Evaluation Board for the AK4432	

■ Pin Layout

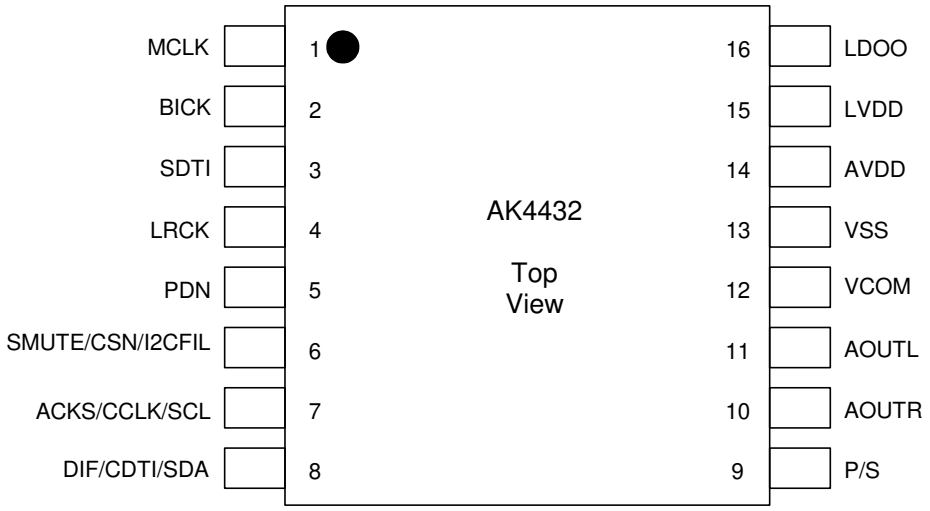

Figure 2. Pin Layout

■ Pin Functions

No.	Pin Name	I/O	PD state	Function
1	MCLK	I	-	External Master Clock Input Pin
2	BICK	I	-	Audio Serial Data Clock Pin
3	SDTI	I	-	Audio Serial Data Input
4	LRCK	I	-	Input Channel Clock Pin
5	PDN	I	-	Power-Down & Reset Pin When "L", the AK4432 is powered-down and the control registers are reset to default state.
6	SMUTE	I	-	Soft Mute Pin in Parallel control mode. When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.
	CSN	I		Chip Select Pin in 3-wire serial control mode
	I2CFIL	I		I2C Interface Mode Select Pin "L": Fast Mode (400kHz), "H": Fast Mode Plus (1MHz). Do not change this pin during PDN pin = "H".
7	ACKS	I	-	Auto Setting Mode in Parallel control mode "L": Manual Setting Mode, "H": Auto Setting Mode
	CCLK	I		Control Data Clock Pin in 3-wire serial control mode
	SCL	I		Control Data Clock Pin in I2C Bus serial control mode
8	DIF	I	-	Audio Data Format Select in Parallel control mode. "L": 32bit MSB, "H": 32bit I2S
	CDTI	I		Control Data Input Pin in 3-wire serial control mode
	SDA	I/O		Control Data Input Pin in I2C Bus serial control mode
9	P/S	I	-	Parallel/Serial Mode Select Pin "L": Serial Mode, "H": Parallel Mode Do not change this pin during PDN pin = "H".
10	AOUTR	O	Hi-z	Rch Analog Output Pin
11	AOUTL	O	Hi-z	Lch Analog Output Pin
12	VCOM	O	500ohm Pull-down	Common Voltage Output Pin, AVDDx1/2 Large external capacitor around 2.2μF is used to reduce power-supply noise.
13	VSS	-	-	Ground Pin
14	AVDD	-	-	Analog Power Supply Pin, 3.0V~3.6V
15	LVDD	-	-	LDO Power Supply / Digital I/F Power Supply Pin, 3.0V~3.6V
16	LDOO	O	580ohm Pull-down	LDO Output Pin This pin should be connected to ground with 1.0uF.

Note 1. All digital input pins must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	AOUTL, AOUTR	Open

6. Absolute Maximum Ratings

(VSS =0V; Note 2)

Parameter	Symbol	Min.	Max.	Unit
Power Supply	AVDD	-0.3	4.3	V
Power Supply	LVDD	-0.3	4.3	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage (Note 3)	VIN	-0.3	(LVDD+0.3) or 4.3	V
Ambient Temperature (power applied)	Ta	-40	105	°C
Storage Temperature	Tstg	-65	150	°C

Note 2. All voltages with respect to ground. VSS must be connected to the same analog ground plane.
Note 3. The maximum Digital input voltage is smaller value between (LVDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(VSS=0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog	AVDD	3.0	3.3	3.6	V
	LDO, Digital (I/F)	LVDD	3.0	3.3	3.6	V

Note 4. Do not turn off the power supply of the AK4432 with the power supply of the peripheral device turned on. When using the I^2C interface, pull-up resistors of SDA and SCL pins should be connected to LVDD or less voltage.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Analog Characteristics

(Ta=25°C; AVDD = LVDD=3.3V; VSS =0V; fs=48kHz, 96kHz, 192kHz; BICK=64fs; Signal Frequency=1kHz; 32bit Data; Measurement Frequency=20Hz~20kHz at fs=48kHz, 20Hz~40kHz at fs=96kHz, 20Hz~40kHz at fs=192kHz, unless otherwise specified.)

Parameter		Min.	Typ.	Max.	Unit
DAC Analog Output Characteristics					
Resolution				32	bit
Output Voltage (Note 5)		2.55	2.83	3.11	Vpp
S/(N+D) (0dBFS)	fs=48kHz	80	91		dB
	fs=96kHz		89		dB
	fs=192kHz		89		dB
Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)		108		dB
	fs=96kHz		101		
	fs=192kHz		101		
S/N	fs=48kHz (A-weighted)		108		dB
	fs=96kHz		101		
	fs=192kHz		101		
Interchannel Isolation		90	110		dB
Interchannel Gain Mismatch			0	0.7	dB
Load Resistance (Note 6)		10			kΩ
Load Capacitance				30	pF

Note 5. Full-scale output voltage. The output voltage is always proportional to AVDD (AVDD x 0.86).
Note 6. AC Load

Parameter		Min.	Typ.	Max.	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")					
AVDD	fs=48kHz, 96kHz, 192kHz		6.5	9.0	mA
LVDD	fs=48kHz		1.3	2	mA
	fs=96kHz		1.6	2.5	mA
	fs=192kHz		2.1	3.0	mA
Power-down mode (PDN pin = "L") (Note 7)			10	200	μA

Note 7. Quiescent Current. All digital input pins including clock pins are fixed to VSS.

9. Filter Characteristics (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD =3.0~ 3.6V, LVDD=3.0~ 3.6V; DEM=OFF)

■ Sharp Roll-Off Filter (DASD bit = "0", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.08dB~+0.08dB	PB	0	-	22.2	kHz
	-6.0dB	PB	-	23.99	-	kHz
Passband Ripple		PR	-0.08		+0.08	dB
Stopband (Note 8)		SB	26.2			kHz
Stopband Attenuation		SA	69.9			dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 20kHz		FR	-0.20		-0.10	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.08dB~+0.08dB	PB	0	-	44.4	kHz
	-6.0dB	PB	-	48.00	-	kHz
Passband Ripple		PR	-0.08		+0.08	dB
Stopband (Note 8)		SB	52.5			kHz
Stopband Attenuation		SA	69.8			dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 40kHz		FR	-0.50		-0.10	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.08dB~+0.08dB	PB	0	-	88.8	kHz
	-6.0dB	PB	-	96.00	-	kHz
Passband Ripple		PR	-0.08		+0.08	dB
Stopband (Note 8)		SB	104.9			kHz
Stopband Attenuation		SA	69.8			dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 80kHz		FR	-2.00		0.00	dB

■ Slow Roll-Off Filter (DASD bit = "0", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB~+0.021dB	PB	0	-	9.0	kHz
	-3.0dB	PB	-	19.75	-	kHz
Passband Ripple		PR	-0.07		+0.021	dB
Stopband (Note 8)		SB	42.6			kHz
Stopband Attenuation		SA	72.6			dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 20kHz		FR	-3.75		-2.75	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB~+0.023dB	PB	0	-	18.1	kHz
	-3.0dB	PB	-	39.6	-	kHz
Passband Ripple		PR	-0.07		+0.023	dB
Stopband (Note 8)		SB	85.1			kHz
Stopband Attenuation		SA	72.6			dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 40kHz		FR	-4.25		-2.75	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB~+0.023dB	PB	0	-	36.1	kHz
	-3.0dB	PB	-	79.3	-	kHz
Passband Ripple		PR	-0.07		+0.023	dB
Stopband (Note 8)		SB	170.3			kHz
Stopband Attenuation		SA	72.6			dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 80kHz		FR	-5.00		-3.00	dB

■ **Short Delay Sharp Roll-Off Filter (DASD bit = "1", DASL bit = "0")**

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB~+0.07dB	PB	0	-	22.0	kHz
	-6.0dB	PB	-	24.11	-	kHz
Passband Ripple		PR	-0.07		+0.07	dB
Stopband (Note 8)		SB	26.2			kHz
Stopband Attenuation		SA	56.6			dB
Group Delay (Note 9)		GD	-	5.9	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 20kHz		FR	-0.20		-0.10	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.08dB~+0.08dB	PB	0	-	44.3	kHz
	-6.0dB	PB	-	48.25	-	kHz
Passband Ripple		PR	-0.08		+0.08	dB
Stopband (Note 8)		SB	52.5			kHz
Stopband Attenuation		SA	56.4			dB
Group Delay (Note 9)		GD	-	5.9	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 40kHz		FR	-0.50		-0.10	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.08dB~+0.08dB	PB	0	-	88.6	kHz
	-6.0dB	PB	-	96.50	-	kHz
Passband Ripple		PR	-0.08		+0.08	dB
Stopband (Note 8)		SB	104.9			kHz
Stopband Attenuation		SA	56.4			dB
Group Delay (Note 9)		GD	-	5.9	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 80kHz		FR	-2.00		0.00	dB

■ **Short Delay Slow Roll-Off Filter (DASD bit = "1", DASL bit = "1")**

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB~+0.05dB	PB	0	-	10.1	kHz
	-3.0dB	PB	-	20.24	-	kHz
Passband Ripple		PR	-0.07		+0.05	dB
Stopband (Note 8)		SB	43.0			kHz
Stopband Attenuation		SA	74.9			dB
Group Delay (Note 9)		GD	-	5.2	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 20kHz		FR	-3.50		-2.50	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB~+0.05dB	PB	0	-	20.3	kHz
	-3.0dB	PB	-	40.50	-	kHz
Passband Ripple		PR	-0.07		+0.05	dB
Stopband (Note 8)		SB	86.0			kHz
Stopband Attenuation		SA	74.9			dB
Group Delay (Note 9)		GD	-	5.2	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 40kHz		FR	-4.00		-2.50	dB

fs=192kH

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB~+0.05dB	PB	0	-	40.6	kHz
	-3.0dB	PB	-	81.00	-	kHz
Passband Ripple		PR	-0.07		+0.05	dB
Stopband (Note 8)		SB	172.0			kHz
Stopband Attenuation		SA	74.9			dB
Group Delay (Note 9)		GD	-	5.2	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz ~ 80kHz		FR	-4.75		-2.75	dB

Note 8. The passband and stopband frequencies are proportional to "fs" (system sampling rate). Each frequency response refers to that of 1kHz.

Note 9. The calculated delay time caused by digital filtering. The digital filter's delay is calculated as the time from setting 16/24/32bit impulse data into the input register until an analog peak signal is output.

10. DC Characteristics

(Ta= -40 ~ +105°C; AVDD =3.0~ 3.6V, LVDD =3.0~ 3.6V, VSS=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
All digital input pins except SCL and SDA pins					
High-Level Input Voltage	VIH1	80%LVDD	-	-	V
Low-Level Input Voltage	VIL1	-	-	20%LVDD	V
SCL, SDA Pin					
High-Level Input Voltage	VIH2	70%LVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	30%LVDD	V
SDA Pin					
Low-Level Output Voltage					
Fast Mode (Iout= 3mA)	VOL1	-		0.4	V
Fast Mode Plus (Iout= 20mA)	VOL2	-		0.4	V
Input Leakage Current	Iin	-	-	±10	μA

11. Switching Characteristics

(Ta=-40 ~ 105°C; AVDD=LVDD=3.0 ~ 3.6V; C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
External Clock					
256fsn:	fCLK	2.048		12.288	MHz
Pulse Width Low	tCLKL	32			ns
Pulse Width High	tCLKH	32			ns
384fsn:	fCLK	3.072		18.432	MHz
Pulse Width Low	tCLKL	22			ns
Pulse Width High	tCLKH	22			ns
512fsn, 256fsd, 128fsq:	fCLK	4.096		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
768fsn, 384fsd, 192fsq:	fCLK	16.384		36.864	MHz
Pulse Width Low	tCLKL	11			ns
Pulse Width High	tCLKH	11			ns
LRCK Timing (Slave Mode)					
Stereo mode (TDM1-0 bits = "00")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	48		96	kHz
Quad Speed Mode	fsq	96		192	kHz
Duty Cycle	Duty	-	50	-	%
TDM128 mode (TDM1-0 bits = "01")					
LRCK frequency	fsn	8		48	kHz
	fsd	48		96	kHz
	fsq	96		192	kHz
I^2S compatible: Pulse Width Low	tLRL	1/(128fsq)		127/(128fsq)	s
MSB or LSB justified: Pulse Width High	tLRH	1/(128fsq)		127/(128fsq)	s
TDM256 mode (TDM1-0 bits = "10")					
LRCK frequency	fsn	8		48	kHz
	fsd	48		96	kHz
I^2S compatible: Pulse Width Low	tLRL	1/(256fsd)		255/(256fsd)	s
MSB or LSB justified: Pulse Width High	tLRH	1/(256fsd)		255/(256fsd)	s

Parameter		Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing						
Normal Mode (TDM1-0 bits = "00")						
BICK Period						
Normal Speed Mode		tBCK	1/256fsn			ns
Double Speed Mode		tBCK	1/256fsd			ns
Quad Speed Mode		tBCK	1/128fsq			ns
BICK Pulse Width Low		tBCKL	18			ns
BICK Pulse Width High		tBCKH	18			ns
BICK "↑" to LRCK Edge	(Note 10)	tBLR	5			ns
LRCK Edge to BICK "↑"	(Note 10)	tLRB	5			ns
SDTI Hold Time		tSDH	5			ns
SDTI Setup Time		tSDS	5			ns
TDM128 mode (TDM1-0 bits = "01")						
BICK Period						
Normal Speed Mode		tBCK	1/128fsn			ns
Double Speed Mode		tBCK	1/128fsd			ns
Quad Speed Mode		tBCK	1/128fsq			ns
BICK Pulse Width Low		tBCKL	18			ns
BICK Pulse Width High		tBCKH	18			ns
BICK "↑" to LRCK Edge	(Note 10)	tBLR	5			ns
LRCK Edge to BICK "↑"	(Note 10)	tLRB	5			ns
SDTI Hold Time		tSDH	5			ns
SDTI Setup Time		tSDS	5			ns
TDM256 mode (TDM1-0 bits = "10")						
BICK Period						
Normal Speed Mode		tBCK	1/256fsn			ns
Double Speed Mode		tBCK	1/256fsd			ns
BICK Pulse Width Low		tBCKL	18			ns
BICK Pulse Width High		tBCKH	18			ns
BICK "↑" to LRCK Edge	(Note 10)	tBLR	5			ns
LRCK Edge to BICK "↑"	(Note 10)	tLRB	5			ns
SDTI Hold Time		tSDH	5			ns
SDTI Setup Time		tSDS	5			ns

Note 10. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (3-wire Serial mode):					
CCLK frequency	fCCK			7	MHz
CCLK Pulse Width Low	tCCKL	60			ns
Pulse Width High	tCCKH	60			ns
CDTI Setup Time	tCDS	60			ns
CDTI Hold Time	tCDH	60			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↓"	tCSS	150			ns
CCLK "↑" to CSN "↑"	tCSH	240			ns
Control Interface Timing (I^2C Fast mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 11)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Control Interface Timing (I^2C Fast mode Plus):					
SCL Clock Frequency	fSCL	-		1	MHz
Bus Free Time Between Transmissions	tBUF	0.5		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.26		-	µs
Clock Low Time	tLOW	0.5		-	µs
Clock High Time	tHIGH	0.26		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.26		-	µs
SDA Hold Time from SCL Falling (Note 12)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.05		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.12	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.12	µs
Setup Time for Stop Condition	tSU:STO	0.26		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		550	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 13)	tPD	800			ns

Note 11. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 12. Data must be held for sufficient time to bridge the 120ns transition time of SCL.
Note 13. The AK4432 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 800ns for a certain reset. The AK4432 is not reset by the "L" pulse less than 50ns.
Note 14. I^2C is a trademark of NXP B.V.

■ Timing Diagram

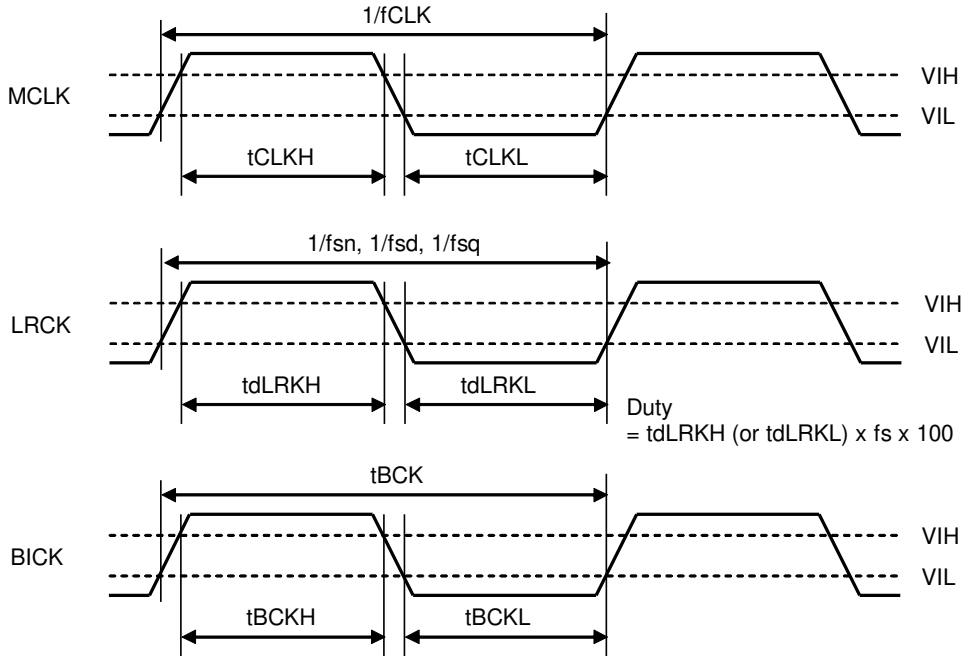

Figure 3. Clock Timing (TDM1-0 bits = “00”)

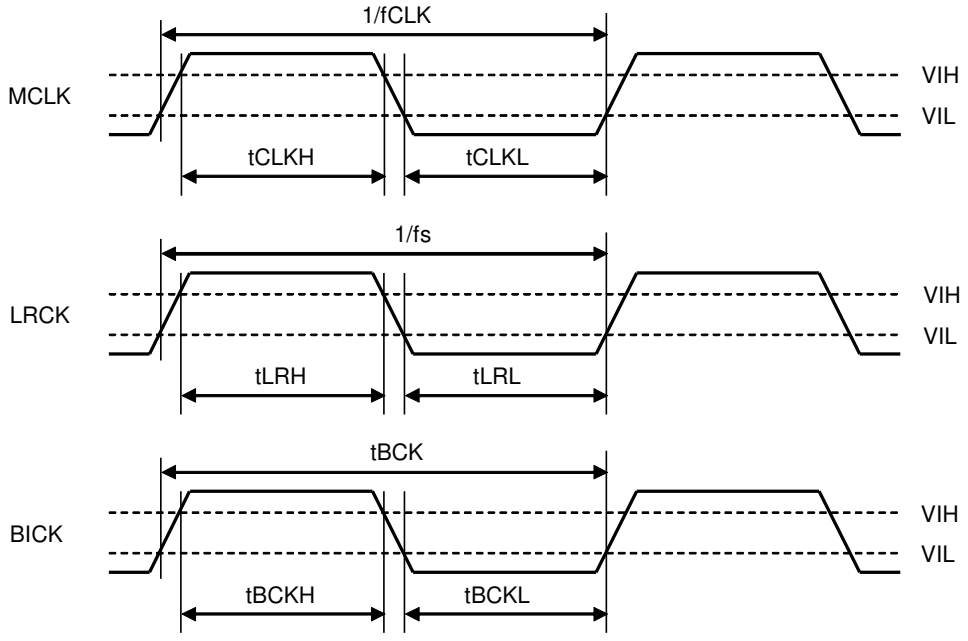

Figure 4. Clock Timing (Except TDM1-0 bits = “00”)

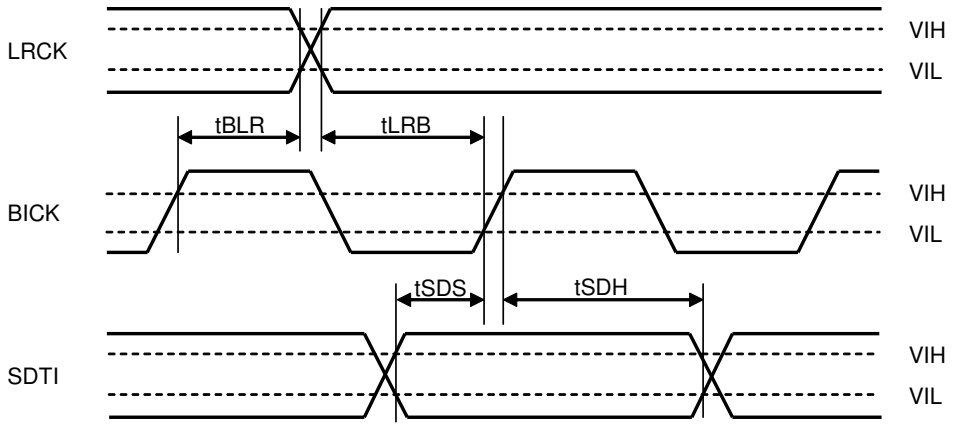

Figure 5. Audio Interface Timing (TDM1-0 bits = “00”)

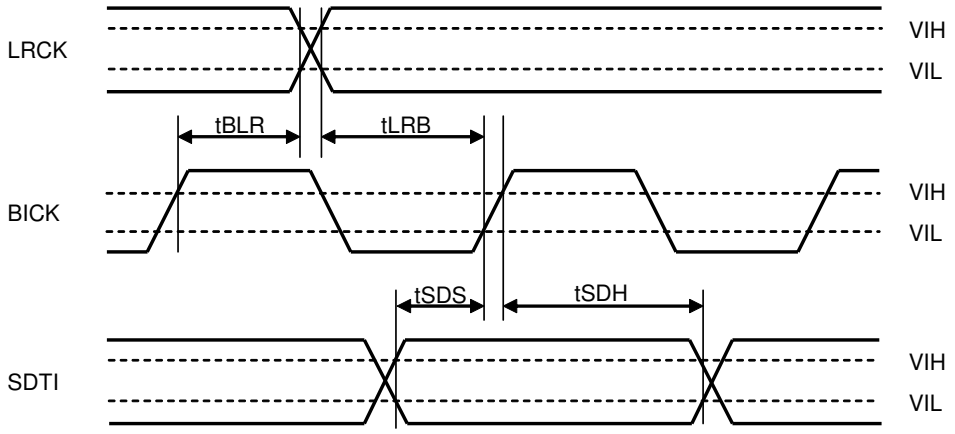

Figure 6. Audio Interface Timing (Except TDM1-0 bits = “00”)

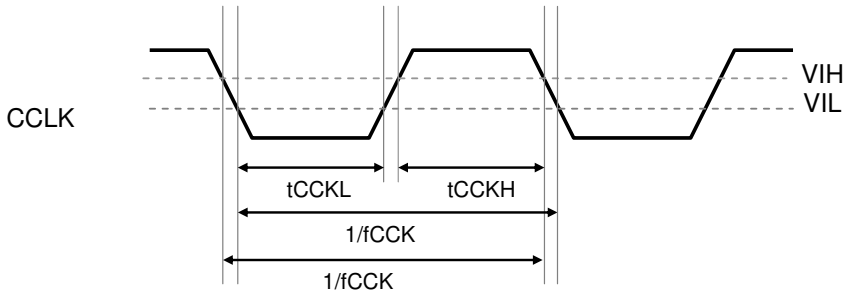

Figure 7. 3-wire Serial Mode Interface Timing

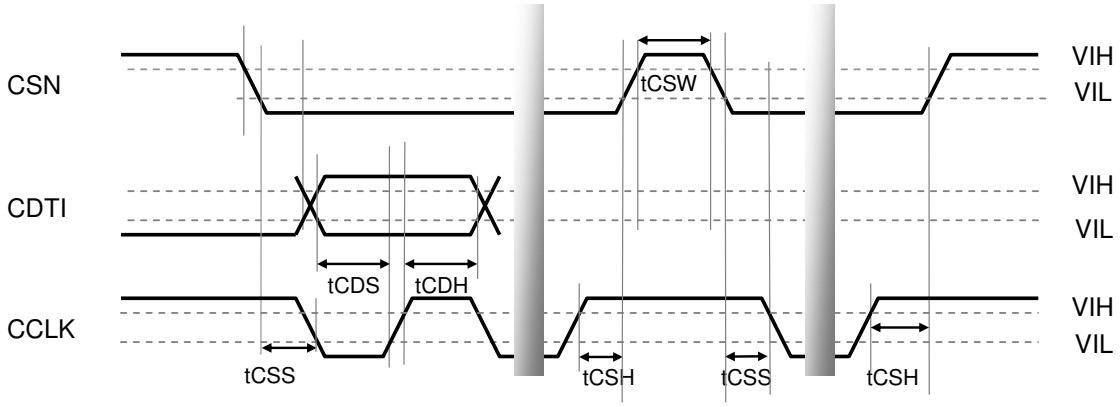

Figure 8. WRITE Data Input Timing (3-wire Serial mode)

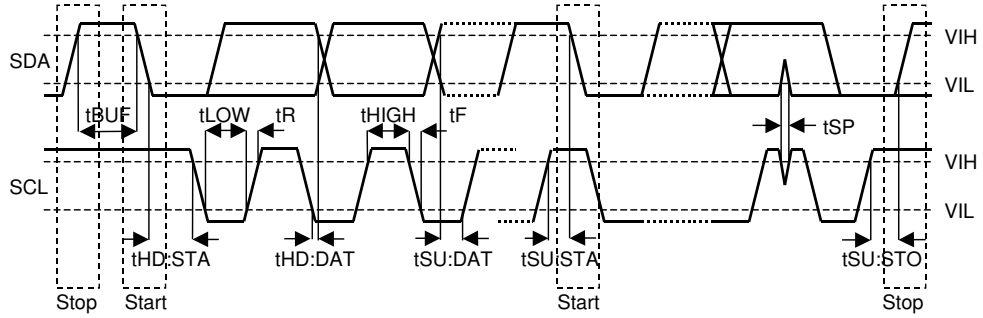

Figure 9. I^2C Bus Mode Timing

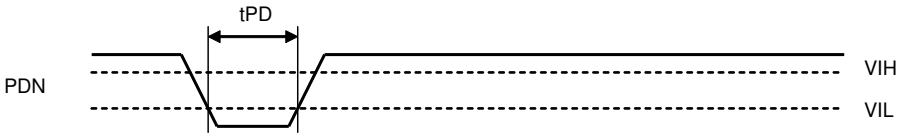

Figure 10. Power-down & Reset Timing

12. Functional Descriptions

■ System Clock

The external clocks which are required to operate the AK4432 are MCLK, LRCK and BICK. MCLK should be synchronized with LRCK and BICK but the phase is not critical. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit= “0”: Default), the sampling speed is set by DFS0, DFS1 (Table 1). The frequency of MCLK at each sampling speed is set automatically (Table 2, Table 3, Table 4). In Auto Setting Mode (ACKS bit= “1”), as MCLK frequency is detected automatically (Table 5) and the internal master clock attains the appropriate frequency (Table 6), so it is not necessary to set DFS bits.

The AK4432 exits system reset (power-down mode) by inputting MCLK and LRCK after the PDN pin=“H”.

If the clock is stopped, a click noise occurs when restarting the clock. Mute the digital output externally if the click noise affects system applications.

DFS1	DFS0	Sampling Speed Mode (fs)		
0	0	Normal Speed Mode	8kHz~48kHz	(default)
0	1	Double Speed Mode	48kHz~96kHz	
1	0	Quad Speed Mode	96kHz~192kHz	
1	1	N/A	-	

(N/A: Not available)

Table 1. Sampling Speed (Manual Setting Mode)

LRCK	MCLK (MHz)				BICK (MHz)
fs	256fs	384fs	512fs	768fs	64fs
8.0kHz	2.0480	3.0720	4.0960	6.1440	0.512
44.1kHz	11.2896	16.9344	22.5792	33.8688	2.8224
48.0kHz	12.2880	18.4320	24.5760	36.8640	3.0720

Table 2. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK (MHz)		BICK (MHz)
fs	256fs	384fs	64fs
88.2kHz	22.5792	33.8688	5.6448
96.0kHz	24.5760	36.8640	6.1440

Table 3. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK (MHz)		BICK (MHz)
fs	128fs	192fs	64fs
176.4kHz	22.5792	33.8688	11.2896
192.0kHz	24.5760	36.8640	12.2880

Table 4. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK		Sampling Speed Mode
512fs	768fs	Normal Speed Mode
256fs	384fs	Double Speed Mode
128fs	192fs	Quad Speed Mode

Table 5. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)						Sampling Speed Mode
fs	128fs	192fs	256fs	384fs	512fs	768fs	
8.0kHz	-	-	-	-	4.0960	6.1440	Normal Speed Mode
44.1kHz	-	-	-	-	22.5792	33.8688	
48.0kHz	-	-	-	-	24.5760	36.8640	
88.2kHz	-	-	22.5792	33.8688	-	-	Double Speed Mode
96.0kHz	-	-	24.5760	36.8640	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	Quad Speed Mode
192.0kHz	24.5760	36.8640	-	-	-	-	

Table 6. System Clock Example (Auto Setting Mode)

■ Audio Interface Format

TDM1-0 bits, DIF2-0 bits, SDS2-0 bits, TDM1-0 pins and DIF pin settings should not be changed during operation. MSB justified and I^2S formats are available but LSB justified format is not available when SYNCE bit = “1” (default).

Normal Mode (TDM1-0 bit=“00”)
Two channels audio data is shifted in via the SDTI pin using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF2-0 bits as shown in Table 7. In all formats the serial data is MSB first, 2's complement format and is latched on the rising edge of BICK. Input “0” data to unused bits if the data does not use maximum bits when MSB justified, I^2S format is selected. (e.g. Mode2 can be used in 16-bit MSB justified by zeroing the unused 8bits LSB).

TDM128 Mode (TDM1-0 bit=“01”)
Four channels audio data is shifted in via the SDTI pin using BICK and LRCK inputs. Data is selected by SDS1-0 bits. BICK is fixed to 128fs. Six data formats are supported and selected by the DIF2-0 bits as shown in Table 7. In all formats the serial data is MSB first, 2's complement format and is latched on the rising edge of BICK.

TDM256 Mode (TDM1-0 bit=“1X”)
Eight channels audio data is shifted in via the SDTI pin using BICK and LRCK inputs. Data is selected by SDS1-0 bits. BICK is fixed to 256fs. Six data formats are supported and selected by the DIF2-0 bits as shown in Table 7. In all formats the serial data is MSB first, 2's complement format and is latched on the rising edge of BICK.

Mode		TDM1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK
Normal (Note 15)	0	0	0	0	0	0	16-bit LSB justified	H/L	≥32fs
	1			0	0	1	20-bit LSB justified	H/L	≥40fs
	2			0	1	0	24-bit MSB justified	H/L	≥48fs
	3			0	1	1	16-bit I^{2}S compatible	L/H	32fs
							24-bit I^{2}S compatible	L/H	≥48fs
	4			1	0	0	24-bit LSB justified	H/L	≥48fs
	5			1	0	1	32-bit LSB justified	H/L	≥64fs
	6			1	1	0	32-bit MSB justified	H/L	≥64fs
	7			1	1	1	32-bit I^{2}S compatible	L/H	≥64fs
TDM128	-	0	1	0	0	0	N/A	↑	128fs
	-			0	0	1	N/A	↑	128fs
	8			0	1	0	24-bit MSB justified	↑	128fs
	9			0	1	1	24-bit I^{2}S compatible	↓	128fs
	10			1	0	0	24-bit LSB justified	↑	128fs
	11			1	0	1	32-bit LSB justified	↑	128fs
	12			1	1	0	32-bit MSB justified	↑	128fs
	13			1	1	1	32-bit I^{2}S compatible	↓	128fs
TDM256	-	1	0	0	0	0	N/A	↑	256fs
	-			0	0	1	N/A	↑	256fs
	14			0	1	0	24-bit MSB justified	↑	256fs
	15			0	1	1	24-bit I^{2}S compatible	↓	256fs
	16			1	0	0	24-bit LSB justified	↑	256fs
	17			1	0	1	32-bit LSB justified	↑	256fs
	18			1	1	0	32-bit MSB justified	↑	256fs
	19			1	1	1	32-bit I^{2}S compatible	↓	256fs

Note 15. BICK that is input to each channel must be longer than the bit length of setting format.

Table 7. Audio Data Format (N/A: Not available)

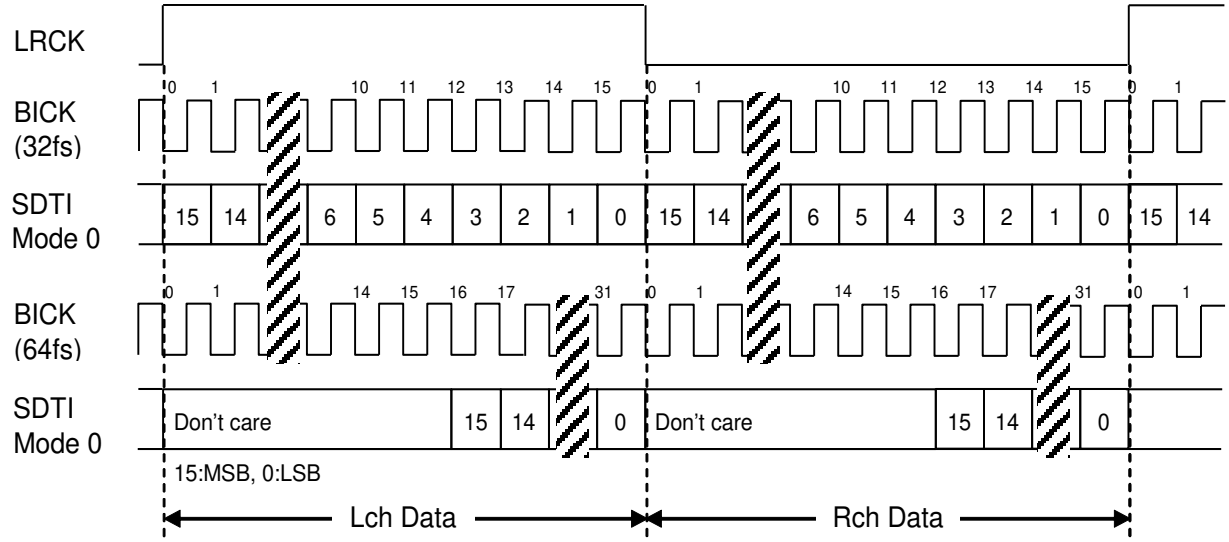

Figure 11. Mode 0 Timing

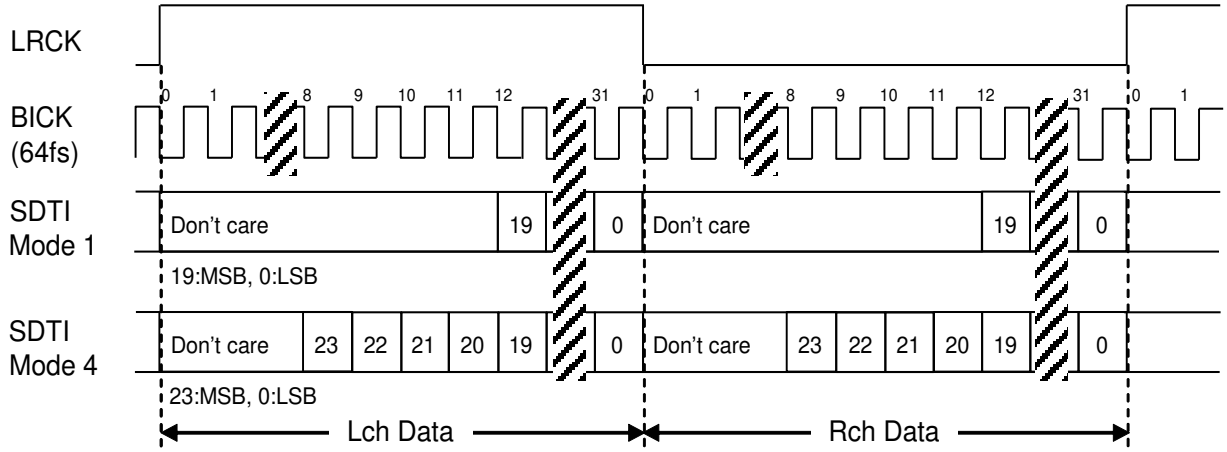

Figure 12. Mode 1/4 Timing

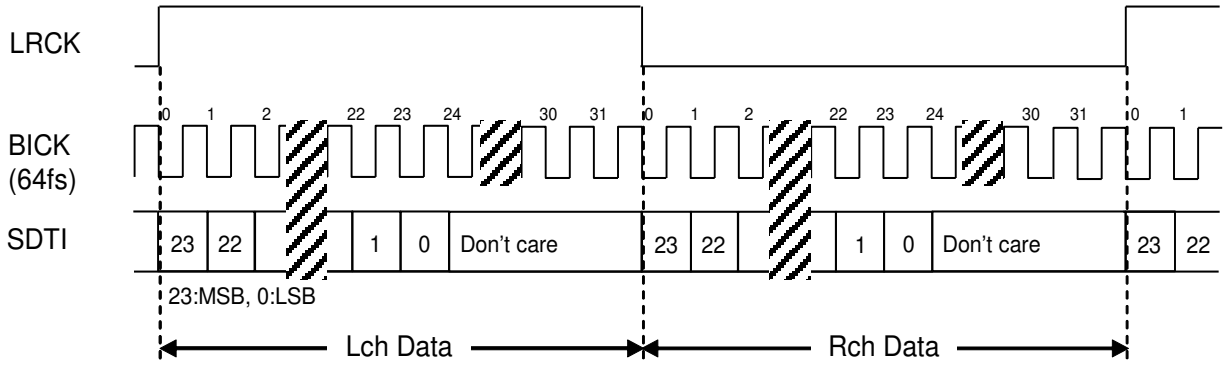

Figure 13. Mode 2 Timing