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AK4438

108dB 768kHz 32bit 8-Channel Audio DAC

1. General Description

The AK4438 is an 8-channel 32-bit DAC which corresponds to digital audio systems. An internal circuit includes newly developed 32-bit Digital Filter achieving short group delay and high quality sound. It corresponds to a 768kHz PCM input at maximum, suitable for play backing high resolution audio sources that are becoming widespread in network audios, USB-DACs and Car Audio Systems. In addition, "OSR-Doubler" technology is newly adopted, making the AK4438 capable of supporting wide range signals and achieving low out-of-band noise while realizing low power consumption. Moreover, the AK4438 has five types of 32-bit digital filters, realizing simple and flexible sound making in wide range of applications.

Application: AV Receivers, CD/SACD Players, Network Audios, USB DACs, USB Headphones, Sound Plate/Bars, Car Audios, Automotive External Amplifiers, Measuring Instruments and Control Systems.

2. Features

1. 8ch 32bit DAC
- **256 x Over sampling**
- **32-bit High Quality Sound Short Delay Digital Filter**
- **Single-ended Output, Smoothing Filter**
- **THD+N: 91dB**
- **DR, S/N: 108dB**
- **Channel Independent Digital Volume Control (0dB～-127dB, 0.5dB Step, Mute)**
- **Soft Mute**
- **De-emphasis Filter (supporting 32kHz, 44.1kHz and 48kHz)**
- **I/F Format: MSB justified, LSB justified, I^2S, TDM**
- **Zero Detection**

2. Sampling Frequency
- **Normal Speed Mode: 8kHz to 48kHz**
- **Double Speed Mode: 48kHz to 96kHz**
- **Quad Speed Mode: 96kHz to 192kHz**
- **Oct Speed Mode: 384kHz**
- **Hex Speed Mode: 768kHz**

3. Master Clock

256fs, 384fs or 512fs, 768fs	**(Normal Speed Mode: fs=8kHz ~ 48kHz)**
256fs, 384fs	**(Double Speed Mode: fs=48kHz ~ 96kHz)**
128fs, 192fs	**(Quad Speed Mode: fs=96kHz ~ 192kHz)**
64fs, 96fs	**(Oct Speed Mode: fs=384kHz)**
32fs, 48fs	**(Hex Speed Mode: fs=768kHz)**

4. μP Interface: 3-wire Serial/ I^2C bus (Ver 1.0, 400kHz mode)

5. Power Supply
- **Analog Supply: AVDD = 3.0 ~ 3.6V**
- **In/Output Buffer: TVDD = 1.7 ~ 3.6V**
- **Integrated LDO for Digital Power Supply**

8. Power Consumption: 31mA (fs=48kHz)

9. Operating Temperature: Ta = - 40 ~ 105℃

10. Package: 32-pin QFN(0.5mm pitch)

3. Table of Contents

4. Block Diagram and Functions

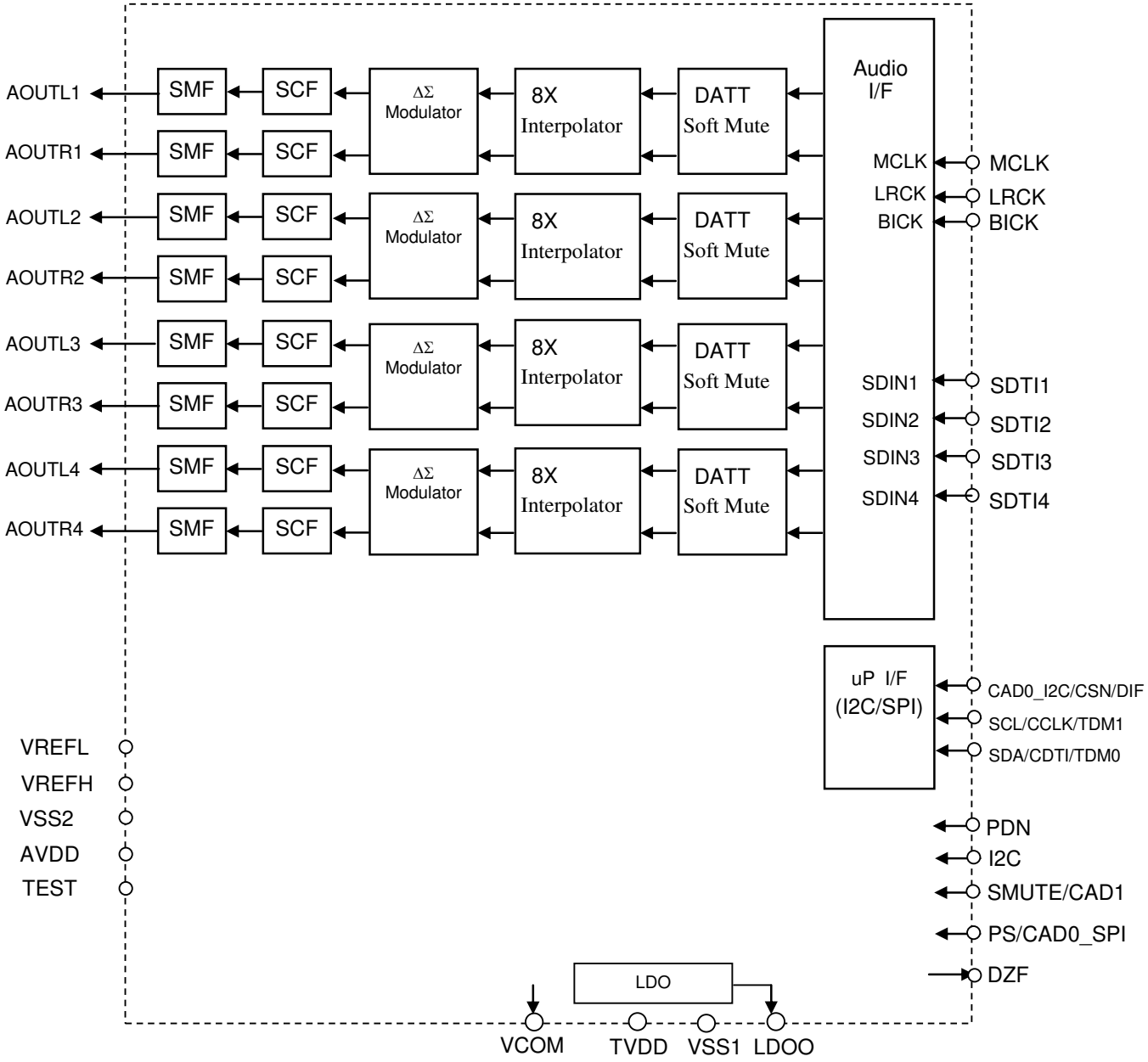

Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations

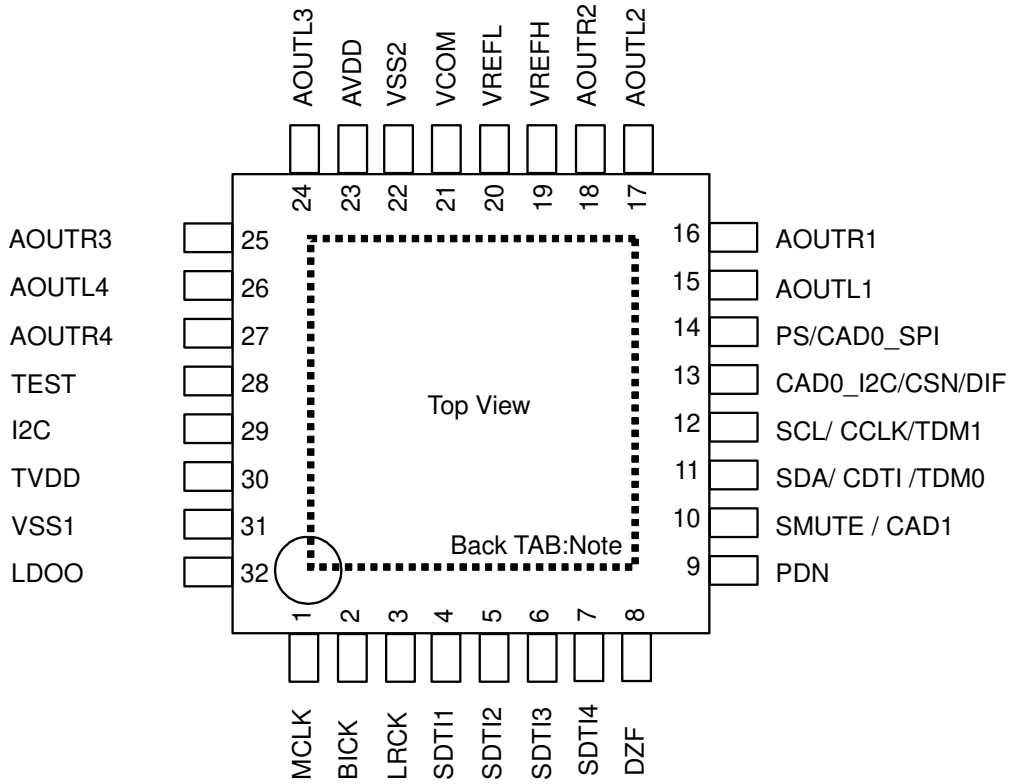

Figure 2. Pin Configurations

Note: The exposed pad on the bottom surface of the package must be open or connected to the analog ground.

■ **Pin Functions**

No.	Pin Name	I/O	PD state	Function
1	MCLK	I	Hi-z	External Master Clock Input Pin
2	BICK	I	Hi-z	Audio Serial Data Clock Pin
3	LRCK	I	Hi-z	Input Channel Clock Pin
4	SDTI1	I	Hi-z	Audio Serial Data Input
5	SDTI2	I	Hi-z	Audio Serial Data Input
6	SDTI3	I	Hi-z	Audio Serial Data Input
7	SDTI4	I	Hi-z	Audio Serial Data Input
8	DZF	O	50kΩ Pull-down	Zero Input Detect in I2C Bus or 3-wire serial control mode
9	PDN	I	Hi-z	Power-Down & Reset Pin. When "L", the AK4438 is powered-down and the control registers are reset to default state.
10	SMUTE	I	Hi-z	Soft Mute Pin in Parallel control mode. When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.
	CAD1	I		Chip Address 1 Pin in I^2C Bus or 3-wire serial control mode
11	SDA	I/O	Hi-z	Control Data Input Pin in I^2C Bus serial control mode
	CDTI	I		Control Data Input Pin in 3-wire serial control mode
	TDM0	I		TDM Mode select pin in Parallel control mode.
12	SCL	I	Hi-z	Control Data Clock Pin in I^2C Bus serial control mode
	CCLK	I		Control Data Clock Pin in 3-wire serial control mode
	TDM1	I		TDM Mode select pin in Parallel control mode.
13	CAD0_I2C	I	Hi-z	Chip Address 0 Pin in I^2C Bus serial control mode
	CSN	I		Chip Select Pin in 3-wire serial control mode
	DIF	I		Audio Data Format Select in Parallel control mode. "L": 32bit MSB, "H": 32bit I2S
14	PS	I	Hi-z	(I2C pin = "H") Control Mode Select Pin "L": I^2C Bus serial control mode, "H": Parallel control mode.
	CAD0_SPI	I		(I2C pin = "L") Chip Address 0 Pin in 3-wire serial control mode
15	AOUTL1	O	Hi-z	Lch Analog Output Pin
16	AOUTR1	O	Hi-z	Rch Analog Output Pin
17	AOUTL2	O	Hi-z	Lch Analog Output Pin
18	AOUTR2	O	Hi-z	Rch Analog Output Pin
19	VREFH	-	Hi-z	Positive Voltage Reference Input Pin, AVDD
20	VREFL	-	Hi-z	Negative Voltage Reference Input Pin, VSS2
21	VCOM	O	500Ω Pull-down	Common Voltage Output Pin, AVDDx1/2 Large external capacitor around 2.2μF is used to reduce power-supply noise.
22	VSS2	-	-	Analog Ground Pin
23	AVDD	-	-	Analog Power Supply Pin, 3.0V~3.6V
24	AOUTL3	O	Hi-z	Lch Analog Output Pin
25	AOUTR3	O	Hi-z	Rch Analog Output Pin
26	AOUTL4	O	Hi-z	Lch Analog Output Pin
27	AOUTR4	O	Hi-z	Rch Analog Output Pin
28	TEST	-	25kΩ Pull-down	This pin must be connected to VSS1.
29	I2C	I	Hi-z	Control Mode Select Pin "L": 3-wire serial control mode "H": I^2C Bus serial control mode or Parallel control mode.
30	TVDD	-	-	Digital Power Supply Pin, 1.7V~3.6V
31	VSS1	-	-	Digital Ground Pin
32	LDOO	O	580Ω Pull-down	LDO Output Pin. This pin must be connected to ground with 2.2uF ±50%.

Note 1. All digital input pins must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	AOUTL1-4, AOUTR1-4	Open
Digital	DZF	Open
	SDTI1-4	Connect to VSS1

6. Absolute Maximum Ratings

(VSS1=VSS2=0V; Note 2)

Parameter	Symbol	Min.	Max.	Unit
Power Supplies				
Analog	AVDD	-0.3	4.3	V
Digital	TVDD	-0.3	4.3	V
Difference (VSS1 ~ 2)	ΔGND	-0.3	0.3	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Digital Input Voltage	VIND	-0.3	TVDD+0.3	V
Ambient Temperature (power applied)	Ta	-40	105	°C
Storage Temperature	Tstg	-65	150	°C

Note 2. All voltages with respect to ground. VSS1 and VSS2 must be connected to the same analog ground plane.

Note 3. The maximum Digital input voltage is smaller value between (LVDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(VSS1=VSS2=0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog	AVDD	3.0	3.3	3.6	V
	Digital	TVDD	1.7	3.3	3.6	V
Voltage Reference (Note 5)	"H" voltage reference	VREFH	AVDD−0.5	-	AVDD	V
	"L" voltage reference	VREFL	-	VSS2	-	V

Note 4. The power up sequence between AVDD and TVDD is not critical.

Note 5. The VREFL pin must be connected to VSS2.

Note 6. Do not turn off the power supply of the AK4438 with the power supply of the peripheral device turned on. When using the I^2C interface, pull-up resistors of SDA and SCL pins should be connected to TVDD or less voltage.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

(Ta=25°C; AVDD =TVDD=3.3V; VSS1=VSS2 =0V; VREFH=AVDD; fs=48kHz; BICK=64fs; Signal Frequency=1kHz; 32bit Data; Measurement Frequency=20Hz~20kHz at 48kHz, 20Hz~40kHz at fs=96kHz, 20Hz~40kHz at fs=192kHz, unless otherwise specified.)

Parameter		Min.	Typ.	Max.	Unit
DAC Analog Output Characteristics					
Resolution				32	bit
Output Voltage (Note 7)		2.55	2.83	3.11	Vpp
S/(N+D) (0dBFS)	fs=48kHz	80	91		dB
	fs=96kHz	-	89		dB
	fs=192kHz	-	89		dB
Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	104	108		dB
	fs=96kHz	-	101		dB
	fs=192kHz	-	101		dB
S/N	fs=48kHz (A-weighted)	104	108		dB
	fs=96kHz	-	101		dB
	fs=192kHz	-	101		dB
Interchannel Isolation		90	110		dB
Interchannel Gain Mismatch			0	0.7	dB
Load Resistance (Note 8)		10			kΩ
Load Capacitance				30	pF
Power Supply Rejection (Note 9)		-	50	-	dB

Note 7. Full-scale output voltage. The output voltage is always proportional to AVDD (AVDD x 0.86).
Note 8. AC Load
Note 9. This is a value when applying a 1kHz 50mVpp sine wave to AVDD.

Parameter		Min.	Typ.	Max.	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")					
AVDD	fs=48kHz, 96kHz, 192kHz		27	36	mA
TVDD	fs=48kHz		3.4	4.5	mA
TVDD	fs=96kHz		4.9	6.4	mA
TVDD	fs=192kHz		8.0	10.4	mA
Power-down mode (PDN pin = "L") (Note 10)					
AVDD+TVDD			10	200	μA

Note 10. Quiescent Current. All digital input pins including clock pins are fixed to VSS.

9. Filter Characteristics (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD =3.0~ 3.6V, TVDD=1.7~ 3.6V; DEM=OFF)

■ **Sharp Roll-Off Filter (SD bit = "0", SLOW bit = "0")**

fs=44.1kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05dB	PB	0		20.0	kHz
	−3.0dB	PB		21.5		kHz
Passband Ripple (Note 12)		PR	-0.0032		0.0032	dB
Stopband (Note 11)		SB	24.1			kHz
Stopband Attenuation (Note 14)		SA	80			dB
Group Delay (Note 13)		GD	-	26.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-0.26		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Passband Ripple (Note 12)		PR	-0.0032		0.0032	dB
Stopband (Note 11)		SB	52.5	0		kHz
Stopband Attenuation (Note 14)		SA	80			dB
Group Delay (Note 13)		GD	-	26.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-0.53		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05dB	PB	0		87.0	kHz
	−3.0dB	PB		93.6		kHz
Passband Ripple (Note 12)		PR	-0.0032		0.0032	dB
Stopband (Note 11)		SB	105			kHz
Stopband Attenuation (Note 14)		SA	80			dB
Group Delay (Note 13)		GD	-	26.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-1.9		0.1	dB

Note 11. The pass band and stop band frequencies scale with fs. For example, PB=0.4535×fs, SB=0.546×fs.

Note 12. It is the pass band gain amplitude of the double over sampling filter at the first step of the Interpolator.

Note 13. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32bit data of both channels to input register to the output of analog signal.

Note 14. The output level is assumed as 0dB when inputting a 1kHz 0dB sine wave.

*Digital filter characteristics are based on simulation results.

■ **Slow Roll-Off Filter (SD bit = "0", SLOW bit = "1")**

fs=44.1kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 15)	±0.05dB	PB	0		8.1	kHz
	−3.0dB	PB		18.2		kHz
Passband Ripple (Note 12)		PR	-0.043		0.0032	dB
Stopband (Note 15)		SB	39.2			kHz
Stopband Attenuation (Note 14)		SA	73			dB
Group Delay (Note 13)		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-5.06		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 15)	±0.05dB	PB	0		17.7	kHz
	−3.0dB	PB		39.5		kHz
Passband Ripple (Note 12)		PR	-0.043		0.043	dB
Stopband (Note 15)		SB	85.3			kHz
Stopband Attenuation (Note 14)		SA	73			dB
Group Delay (Note 13)		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-5.23		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 15)	±0.05dB	PB	0		35.5	kHz
	−3.0dB	PB		79.0		kHz
Passband Ripple (Note 12)		PR	-0.043		0.043	dB
Stopband (Note 15)		SB	171			kHz
Stopband Attenuation (Note 14)		SA	73			dB
Group Delay (Note 13)		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-5.90		0.1	dB

Note 15. The pass band and stop band frequencies scale with fs. For example, PB=0.185×fs, SB=0.888×fs.

■ **Short Delay Sharp Roll-Off Filter (SD bit = "1", SLOW bit = "0")**

fs=44.1kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05dB	PB	0		20.0	kHz
	−3.0dB	PB		21.5		kHz
Passband Ripple (Note 12)		PR	-0.0031		0.0031	dB
Stopband (Note 11)		SB	24.1			kHz
Stopband Attenuation (Note 14)		SA	80			dB
Group Delay (Note 13)		GD	-	5.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-0.26		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Passband Ripple (Note 12)		PR	-0.0031		0.0031	dB
Stopband (Note 11)		SB	52.5	0		kHz
Stopband Attenuation (Note 14)		SA	80			dB
Group Delay (Note 13)		GD	-	5.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-0.53		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 11)	±0.05dB	PB	0		87.0	kHz
	−3.0dB	PB		93.6		kHz
Passband Ripple (Note 12)		PR	-0.0031		0.0031	dB
Stopband (Note 11)		SB	105			kHz
Stopband Attenuation (Note 14)		SA	80			dB
Group Delay (Note 13)		GD	-	5.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-1.9		0.1	dB

■ **Short Delay Slow Roll-Off Filter (SD bit = "1", SLOW bit = "1")**

fs=44.1kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 16)	±0.05dB	PB	0		11.1	kHz
	−3.0dB	PB		19.4		kHz
Passband Ripple (Note 12)		PR	-0.05		0.05	dB
Stopband (Note 16)		SB	38.1			kHz
Stopband Attenuation (Note 14)		SA	82			dB
Group Delay (Note 13)		GD	-	4.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-5.06		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 16)	±0.05dB	PB	0		24.2	kHz
	−3.0dB	PB		42.1		kHz
Passband Ripple (Note 12)		PR	-0.05		0.05	dB
Stopband (Note 16)		SB	83.0			kHz
Stopband Attenuation (Note 14)		SA	82			dB
Group Delay (Note 13)		GD	-	4.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-5.23		0.1	dB

fs=192kH

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 16)	±0.05dB	PB	0		48.4	kHz
	−3.0dB	PB		84.3		kHz
Passband Ripple (Note 12)		PR	-0.05		0.05	dB
Stopband (Note 16)		SB	165.9			kHz
Stopband Attenuation (Note 14)		SA	82			dB
Group Delay (Note 13)		GD	-	4.8	-	1/fs
Digital Filter + SCF + SMF (Note 14)						
Frequency Response : 0 ~ 20.0kHz			-5.90		0.1	dB

Note 16. The pass band and stop band frequencies scale with fs. For example, PB=0.252×fs, SB=0.864×fs.

10. DC Characteristics

(Ta= -40 ~ +105°C; AVDD =3.0~ 3.6V, TVDD=1.7~ 3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
TVDD=1.7V ~ 3.0V					
High-Level Input Voltage	VIH1	80%TVDD	-	-	V
Low-Level Input Voltage	VIL1	-	-	20%TVDD	V
TVDD=3.0V ~ 3.6V					
High-Level Input Voltage	VIH2	70%TVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	30%TVDD	V
High-Level Output Voltage (DZF pins: Iout= -100μA)	VOH	TVDD−0.5	-	-	V
Low-Level Output Voltage (DZF pin : Iout= 100μA)	VOL1	-	-	0.5	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout= 3mA)	VOL2	-	-	0.4	V
(SDA pin, 1.7V ≤ TVDD ≤ 2.0V: Iout= 3mA)	VOL3	-		20%TVDD	V
Input Leakage Current	Iin	-	-	±10	μA

11. Switching Characteristics

(Ta=-40 ~ 105°C; AVDD=3.0 ~ 3.6V, TVDD=1.7 ~ 3.6V; C_L=20pF, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
External Clock					
256fsn:	fCLK	2.048		12.288	MHz
Pulse Width Low	tCLKL	32			ns
Pulse Width High	tCLKH	32			ns
384fsn:	fCLK	3.072		18.432	MHz
Pulse Width Low	tCLKL	22			ns
Pulse Width High	tCLKH	22			ns
512fsn, 256fsd, 128fsq, 64fso, 32fsh:	fCLK	4.096		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
768fsn, 384fsd, 192fsq, 96fso, 48fsh:	fCLK	6.144		36.864	MHz
Pulse Width Low	tCLKL	11			ns
Pulse Width High	tCLKH	11			ns
LRCK Timing (Slave mode)					
Stereo mode (TDM1-0 bits = "00")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	48		96	kHz
Quad Speed Mode	fsq	96		192	kHz
Oct speed mode	fso		384		kHz
Hex speed mode	fsh		768		kHz
Duty Cycle	Duty	45		55	%
TDM128 mode (TDM1-0 bits = "01")					
LRCK frequency	fsn	8		48	kHz
	fsd	48		96	kHz
	fsq	96		192	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns
TDM256 mode (TDM1-0 bits = "10")					
LRCK frequency	fsn	8		48	kHz
	fsd	48		96	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
TDM512 mode (TDM1-0 bits = "11")					
LRCK frequency	fsn	8		48	kHz
"H" time	tLRH	1/512fs			ns
"L" time	tLRL	1/512fs			ns

Parameter		Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing						
Stereo mode (TDM1-0 bits = "00")						
BICK Period						
Normal Speed Mode		tBCK	1/256fsn			ns
Double Speed Mode		tBCK	1/128fsd			ns
Quad Speed Mode		tBCK	1/64fsq			ns
Oct Speed Mode		tBCK	1/64fso			ns
Hex Speed Mode		tBCK	1/64fsh			ns
BICK Pulse Width Low		tBCKL	9			ns
BICK Pulse Width High		tBCKH	9			ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	5			ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	5			ns
SDTI Hold Time		tSDH	5			
SDTI Setup Time		tSDS	5			
TDM128 mode (TDM1-0 bits = "01")						
BICK Period						
Normal Speed Mode		tBCK	1/128fsn			ns
Double Speed Mode		tBCK	1/128fsd			ns
Quad Speed Mode		tBCK	1/128fsq			ns
BICK Pulse Width Low		tBCKL	16			ns
BICK Pulse Width High		tBCKH	16			ns
LRCK Edge to BICK "↑"	(Note 17)	tBLR	5			ns
BICK "↑" to LRCK Edge	(Note 17)	tLRB	5			ns
SDTI Hold Time		tSDH	5			ns
SDTI Setup Time		tSDS	5			ns
TDM256 mode (TDM1-0 bits = "10")						
BICK Period						
Normal Speed Mode		tBCK	1/256fsn			ns
Double Speed Mode		tBCK	1/256fsd			ns
BICK Pulse Width Low		tBCKL	16			ns
BICK Pulse Width High		tBCKH	16			ns
LRCK Edge to BICK "↑"	(Note 17)	tBLR	5			ns
BICK "↑" to LRCK Edge	(Note 17)	tLRB	5			ns
SDTI Hold Time		tSDH	5			ns
SDTI Setup Time		tSDS	5			ns
TDM512 mode (TDM1-0 bits = "11")						
BICK Period						
Normal Speed Mode		tBCK	1/512fsn			ns
BICK Pulse Width Low		tBCKL	16			ns
BICK Pulse Width High		tBCKH	16			ns
LRCK Edge to BICK "↑"	(Note 17)	tBLR	5			ns
BICK "↑" to LRCK Edge	(Note 17)	tLRB	5			ns
SDTI Hold Time		tSDH	5			ns
SDTI Setup Time		tSDS	5			ns

Note 17. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (3-wire Serial mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 18)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 19)	tAPD	800			ns
PDN Reject Pulse Width	tRPD			50	ns

Note 18. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 19. The AK4438 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 800ns for a certain reset. The AK4438 is not reset by the "L" pulse less than 50ns.

Note 20. I^2C-bus is a trademark of NXP B.V.

■ Timing Diagram

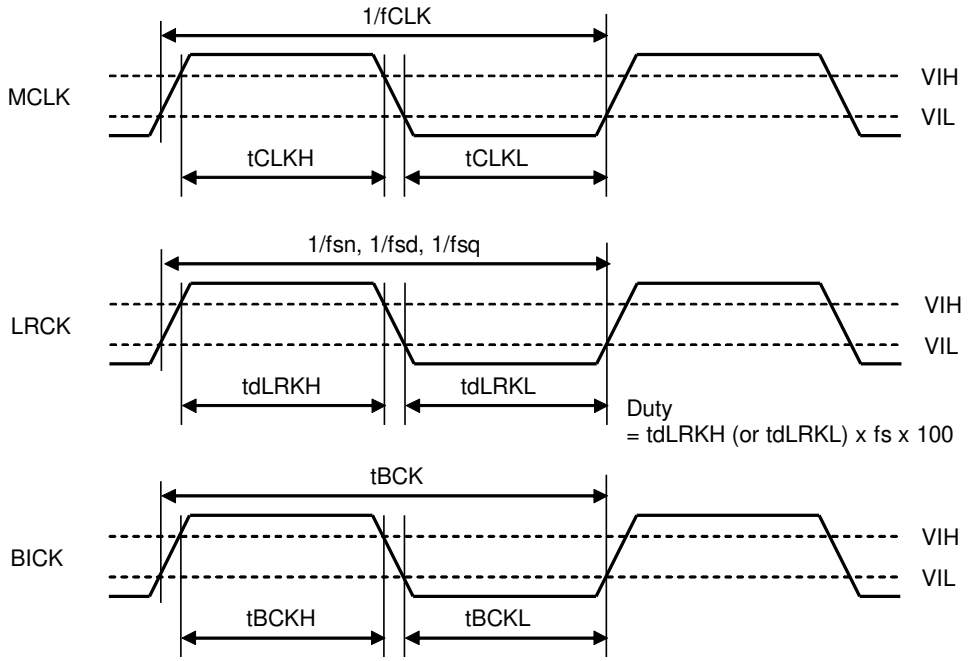

Figure 3. Clock Timing (TDM1-0 bits = “00”)

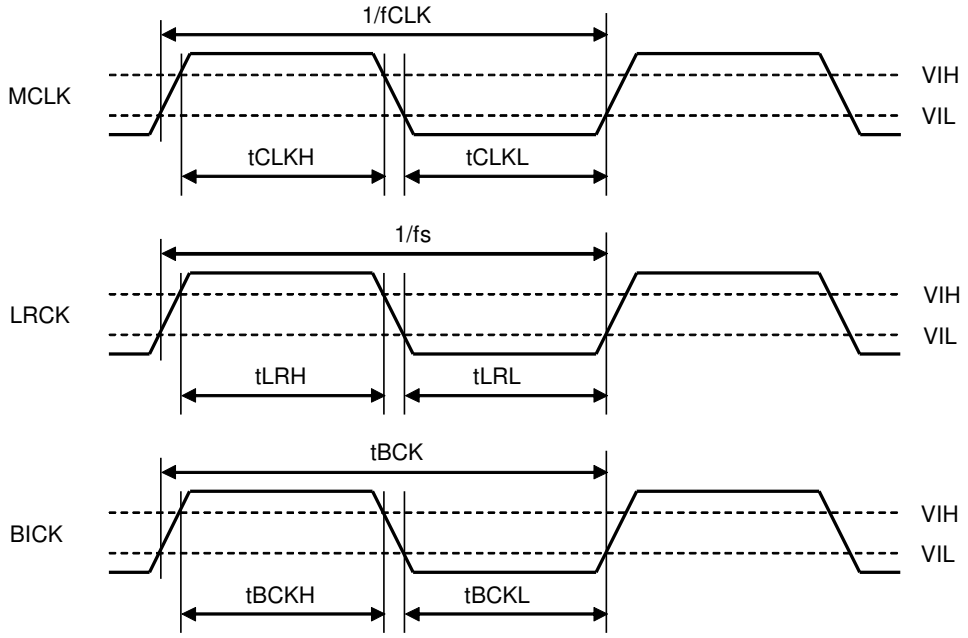

Figure 4. Clock Timing (Except TDM1-0 bits = “00”)

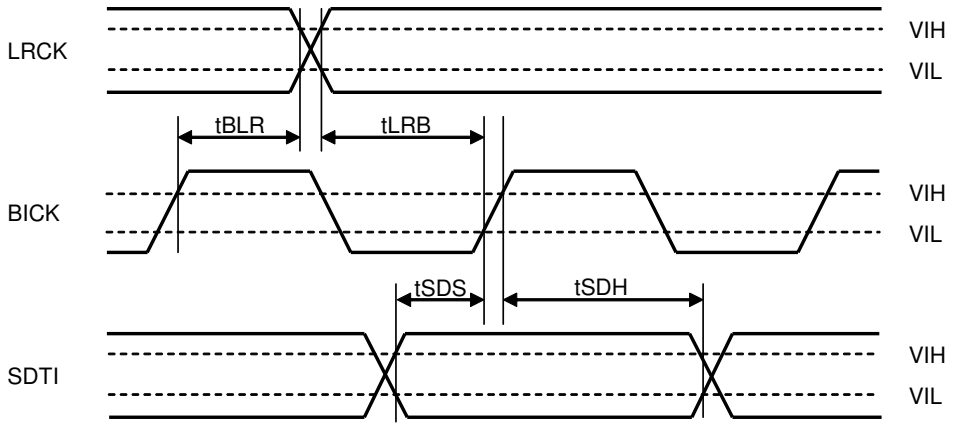

Figure 5. Audio Interface Timing (TDM1-0 bits = “00”)

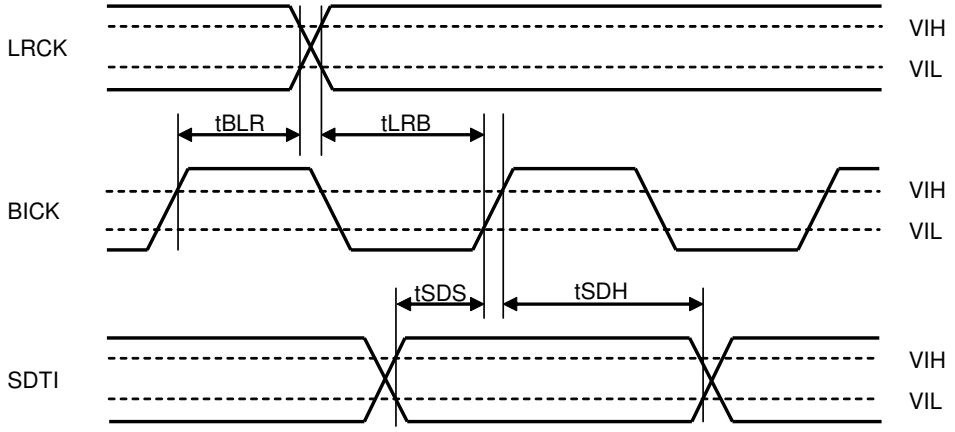

Figure 6. Audio Interface Timing (Except TDM1-0 bits = “00”)

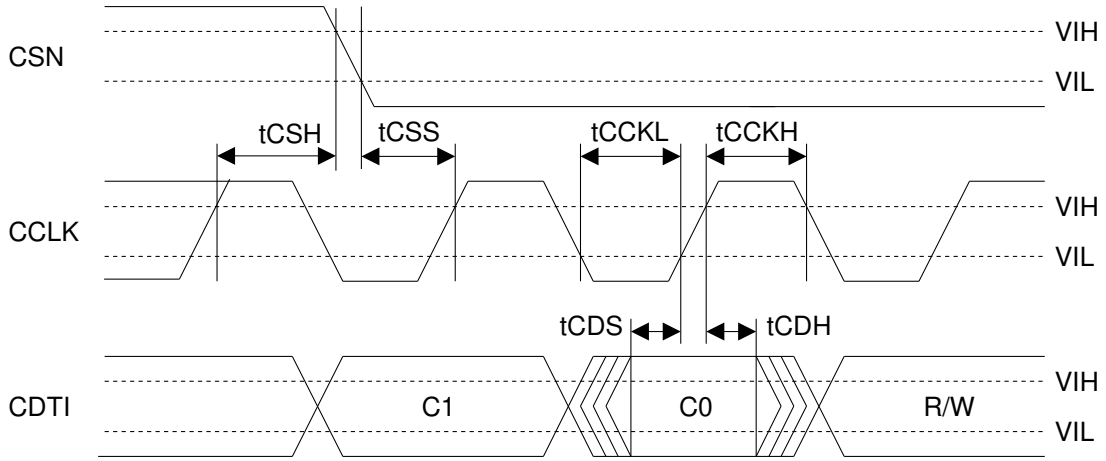

Figure 7. WRITE Command Input Timing (3-wire Serial mode)

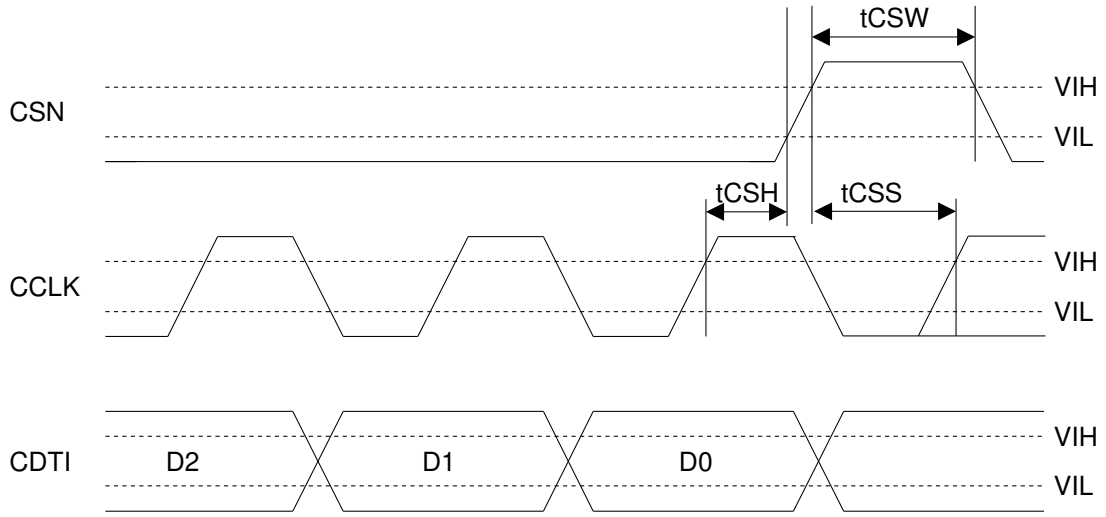

Figure 8. WRITE Data Input Timing (3-wire Serial mode)

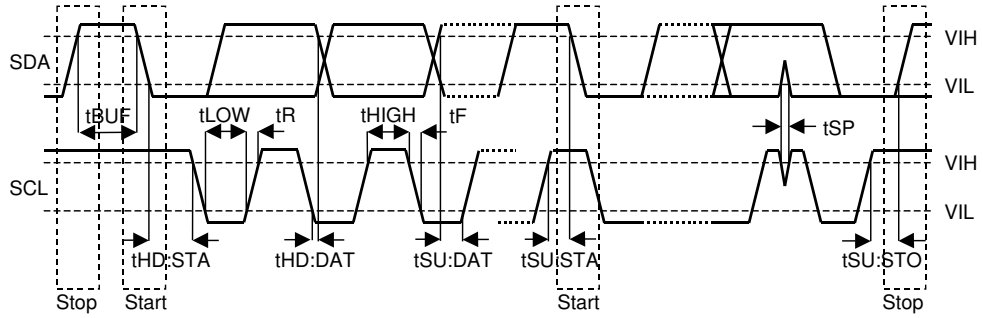

Figure 9. I^2C Bus mode Timing

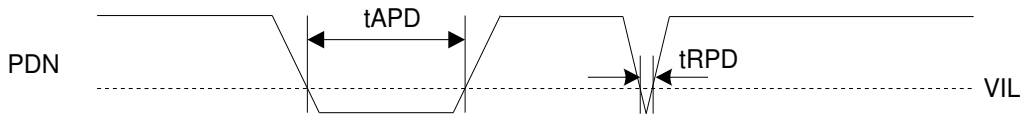

Figure 10. Power-down & Reset Timing

12. Functional Descriptions

■ System Clock

The external clocks which are required to operate the AK4438 are MCLK, LRCK and BICK. MCLK should be synchronized with LRCK and BICK but the phase is not critical. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit= “0”: Default), the sampling speed is set by DFS2-0 bit (Table 1). The frequency of MCLK at each sampling speed is set automatically (Table 2, Table 3). In Auto Setting Mode (ACKS bit= “1”), as MCLK frequency is detected automatically (Table 4) and the internal master clock attains the appropriate frequency (Table 5), so it is not necessary to set DFS2-0 bits.

After exiting reset at power-up (PDN pin = “L” →“H”), the AK4438 is in power-down mode until MCLK and LRCK are input. The AK4438 is set to Manual Setting Mode at power-up (PDN pin = “L” →“H”). When changing the clock, the AK4438 must be reset by the PDN pin or RSTN bit.

If the clock is stopped, a click noise occurs when restarting the clock. Mute the digital output externally if the click noise affects system applications.

1. Manual Setting Mode (ACKS bit = "0")

MCLK frequency is detected automatically and the sampling rate is set by DFS2-0 bits (Table 1). The MCLK frequency corresponding to each sampling speed should be provided externally (Table 2, Table 3). The AK4438 is set to Manual Setting Mode at power-up (PDN pin = "L" →"H"). When DFS2-0 bits are changed, the AK4438 should be reset by RSTN bit.

DFS2	DFS1	DFS0	Sampling Speed Mode (fs)		
0	0	0	Normal Speed Mode	8kHz~48kHz	(default)
0	0	1	Double Speed Mode	48kHz~96kHz	
0	1	0	Quad Speed Mode	96kHz~192kHz	
0	1	1	N/A	N/A	
1	0	0	Oct Speed Mode	384kHz	
1	0	1	Hex Speed Mode	768kHz	
1	1	0	N/A	N/A	
1	1	1	N/A	N/A	

(N/A: Not Available)

Table 1. Sampling Speed (Manual Setting Mode)

LRCK	MCLK(MHz)				Sampling Speed
fs	32fs	48fs	64fs	96fs	
8.0kHz	N/A	N/A	N/A	N/A	Normal
44.1kHz	N/A	N/A	N/A	N/A	
48.0kHz	N/A	N/A	N/A	N/A	
88.2kHz	N/A	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	Quad
192.0kHz	N/A	N/A	N/A	N/A	
384.0kHz	N/A	N/A	24.576	36.864	Oct
768.0kHz	24.576	36.864	N/A	N/A	Hex

Table 2. System Clock Example (Manual Setting Mode)

LRCK	MCLK(MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
8.0kHz	N/A	N/A	2.0480	3.0720	4.0960	6.1440	Normal
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	
88.2kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	Double
96.0kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Quad
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	
384.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex

Table 3. System Clock Example (Manual Setting Mode)

2. Auto Setting Mode (ACKS bit = “1”)

MCLK frequency and the sampling speed are detected automatically (Table 4) and DFS2-0 bits are ignored. The MCLK frequency corresponding to each sampling speed should be provided externally (Table 5, Table 6).

MCLK		Sampling Speed Mode
512fs/256fs	768fs/384fs	Normal Speed Mode
256fs	384fs	Double Speed Mode
128fs	192fs	Quad Speed Mode
64fs	96fs	Oct Speed Mode
32fs	48fs	Hex Speed Mode

Table 4. Sampling Speed (Auto Setting Mode)

LRCK	MCLK(MHz)				Sampling Speed
fs	32fs	48fs	64fs	96fs	
8.0kHz	N/A	N/A	N/A	N/A	Normal
44.1kHz	N/A	N/A	N/A	N/A	
48.0kHz	N/A	N/A	N/A	N/A	
88.2kHz	N/A	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	Quad
192.0kHz	N/A	N/A	N/A	N/A	
384.0kHz	N/A	N/A	24.576	36.864	Oct
768.0kHz	24.576	36.864	N/A	N/A	Hex

Table 5. System Clock Example (Auto Setting Mode)

LRCK	MCLK(MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
8.0kHz	N/A	N/A	2.0480	3.0720	4.0960	6.1440	Normal
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	
88.2kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	Double
96.0kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Quad
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	
384.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex

Table 6. System Clock Example (Auto Setting Mode)

MCLK= 256fs/384fs supports sampling rate of 8kHz~96kHz (Table 7). However, when the sampling rate is 8kHz~48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

ACKS bit	MCLK	DR,S/N
L	256fs/384fs/512fs/768fs	108dB
H	256fs/384fs	105dB
H	512fs/768fs	108dB

Table 7. Relationship of DR, S/N and MCLK frequency (fs = 44.1kHz)

■ De-emphasis Filter

The AK4438 has a digital de-emphasis filter (tc=50/15μs) by an IIR filter. The de-emphasis filter only supports Normal Speed Mode. This filter corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz). De-emphasis of each DAC can be set individually for DAC1(SDTI1), DAC2(SDTI2), DAC3(SDTI3) and DAC4(SDTI4) by register settings.

Mode	Sampling Speed Mode	DEM11 (DEM41-21)	DEM10 (DEM40-20)	DEM	
0	Normal Speed Mode	0	0	44.1kHz	
1	Normal Speed Mode	0	1	OFF	(default)
2	Normal Speed Mode	1	0	48kHz	
3	Normal Speed Mode	1	1	32kHz	

Table 8. De-emphasis Control

■ Audio Interface Format

TDM1-0 bits, DIF2-0 bits, SDS2-0 bits, TDM1-0 pins and DIF pin settings should not be changed during operation.

[1] PCM Mode

Normal Mode (TDM1-0 bit="00")
Eight channels audio data is shifted in via the SDTI1-4 pins using BICK and LRCK inputs. Data is selected by SDS2-0 bits. Eight data formats are supported and selected by the DIF2-0 bits as shown in Table 9. In all formats the serial data is MSB first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used in 16-bit and 20-bit MSB justified and Mode 6 can be used in 16-bit, 20-bit and 24-bit MSB justified formats by zeroing the unused LSBs.

TDM128 Mode (TDM1-0 bit="01")
Eight channels audio data is shifted in via the SDTI1-2 pins using BICK and LRCK inputs. Data is selected by SDS2-0 bits. The data input to the SDTI3-4 pins are ignored. BICK is fixed to 128fs. Six data formats are supported and selected by the DIF2-0 bits as shown in Table 9. In all formats the serial data is MSB first, 2's compliment format and is latched on the rising edge of BICK.

TDM256 Mode (TDM1-0 bit="10")
Sixteen channels audio data is shifted in via the SDTI1-2 pins using BICK and LRCK inputs. Data is selected by SDS2-0 bits. The data input to the SDTI3-4 pins are ignored. BICK is fixed to 256fs. Six data formats are supported and selected by the DIF2-0 bits as shown in Table 9. In all formats the serial data is MSB first, 2's compliment format and is latched on the rising edge of BICK.

TDM512 Mode (TDM1-0 bit="11")
Sixteen channels audio data is shifted in via the SDTI1 pin using BICK and LRCK inputs. Data is selected by SDS2-0 bits. The data input to the SDTI2-4 pins are ignored. BICK is fixed to 512fs. Six data formats are supported and selected by the DIF2-0 bits as shown in Table 9. In all formats the serial data is MSB first, 2's compliment format and is latched on the rising edge of BICK.