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AK4458

115dB 768kHz 32-bit 8ch Premium DAC

1. General Description

The AK4458 is a 32-bit 8ch Premium DAC, which achieves industry's best low distortion characteristics by a newly developed low distortion technology. It corresponds to a 768kHz PCM input and an 11.2MHz DSD input at maximum, suitable for play backing high resolution audio sources that are becoming widespread in network audios, USB-DACs and Car Audio Systems. In addition, "OSR-Doubler" technology is newly adopted, making the AK4458 capable of supporting wide range signals and achieving low out-of-band noise while realizing low power consumption. Moreover, the AK4458 has five types of 32-bit digital filters, realizing simple and flexible sound making in wide range of applications.

Application: AV Receivers, CD/SACD Players, Network Audios, USB DACs, USB Headphones, Sound Plate/Bars, Car Audios, Automotive External Amplifiers, Measuring Instruments and Control Systems.

2. Features

(1) DR, S/N: 115dB
(2) THD+N: -107dB
(3) 256x Over sampling (OSR - Doubler)
(4) Sampling Rate: 8kHz ~ 768kHz
(5) 32Bit 8x Digital Filter
- **Ripple: ±0.0032dB, Attenuation: 80dB (Sharp Roll-Off Filter Setting)**
- **Five Types of High Quality Sound Filter Option**
- **Sharp Roll-Off Filter**
- **Slow Roll-Off Filter**
- **Short Delay Sharp Roll-Off Filter (GD=5.8/fs)**
- **Short Delay Slow Roll-Off Filter (GD=4.8/fs)**
- **Super Slow Roll-Off Filter**

(6) High Tolerance to Clock Jitter
(7) Low Distortion Differential Output
(8) DSD data input
(9) Daisy Chain
(10) Digital De-emphasis for 32, 44.1, 48kHz sampling
(11) Soft Mute
(12) Digital Attenuator (255 levels and 0.5dB step)
(13) I/F Format:
- **24/32bit MSB justified**
- **16/20/24/32bit**
- **LSB justified**
- **I^2S**
- **DSD**
- **TDM**

(14) 3-wire Serial and I^2C µP I/F
(15) Master Clock:
- **30kHz ~ 32kHz: 1152fs**
- **30kHz ~ 54kHz: 512fs or 768fs**
- **30kHz ~ 108kHz: 256fs or 384fs**
- **108kHz ~ 216kHz: 128fs or 192fs**
  ~ 384kHz: 64fs or 128fs
  ~ 768kHz: 64fs

(16) Digital Input Level: CMOS
(17) Power Supply:
- TVDD= 1.7 ~ 3.6V
- AVDD=3.0 ~ 5.5V
(18) Supporting 105°C Temperature (Exposed pad is connected to ground)
(19) Package: 48-pin QFN

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4. Block Diagram and Functions

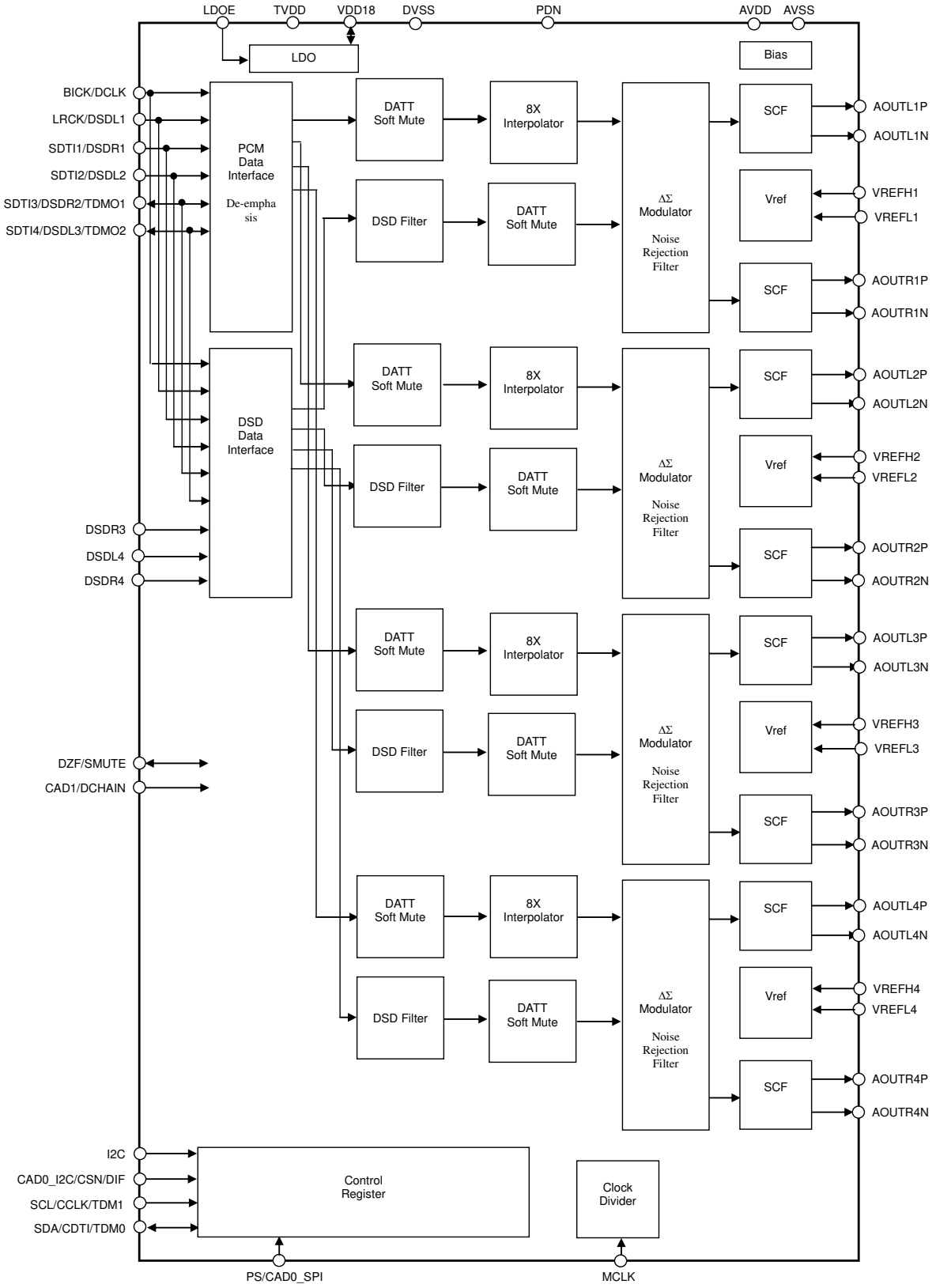


Figure 1. Block Diagram

■ Functions

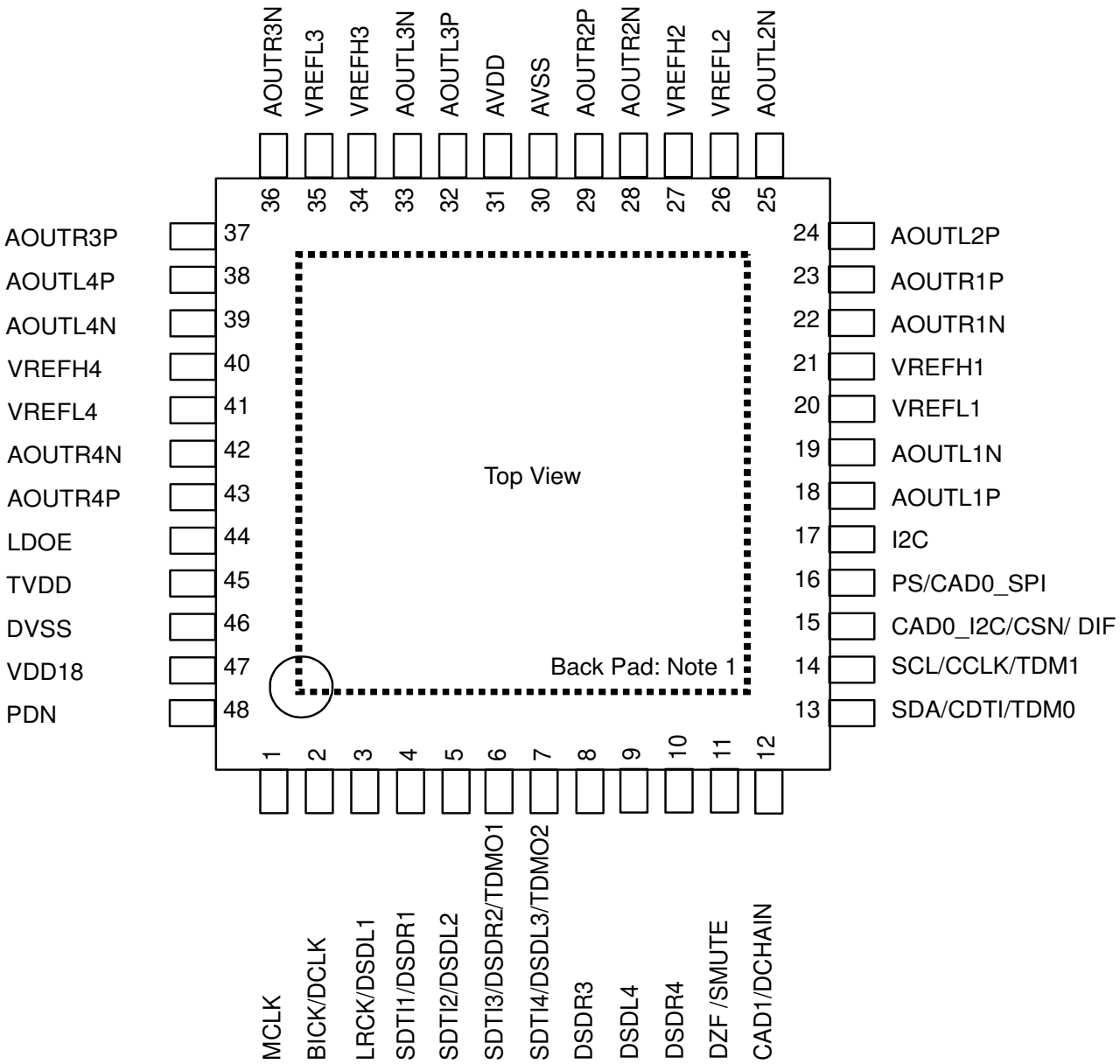
Block	Functions
PCM Data Interface	This block executes serial/parallel conversion of SDTI input 32bit data by synchronizing with LRCK and BICK.
DSD Data Interface	1-bit data that is input from DSDL1-4 and DSDR1-4 pins is received by synchronizing with DCLK.
DATT、Soft Mute	Apply DATT and Soft Mute process to input data.
De-emphasis	Apply De-emphasis process to input data.
8x Interpolator	FIR filters that over sample 1fs rate data to 8fs rate.
ΔΣ Modulator	Output multi-bit data to SCF. This block consists of a third-order digital delta-sigma modulator.
Noise Rejection Filter	Attenuate out of band noise to prevent degradation of analog characteristics.
SCF	A primary switched capacitor filter that converts a multi-bit output of delta-sigma modulator to an analog signal.
LDO	Generate power for internal digital circuit (1.8V typ.).
Control Register	Keep register settings for each mode.
Clock Divider	Divide Master Clock In PCM mode, master clock is divided automatically by fs rate auto detection function. In DSD mode, the master clock frequency is set by DCKS bit.

5. Pin Configurations and Functions

■ Ordering Guide

AK4458VN	–40 ~ +105°C (Exposed pad is connected to ground) –40 ~ +85°C (Exposed pad is open) 48-pin QFN (0.5mm pitch)
AKD4458	Evaluation Board for AK4458

■ Pin Configurations



Note 1. The exposed pad at back face of the package must be open or connected to the ground of the board.

■ Pin Functions

No.	Pin Name	I/O	Function	PD State
1	MCLK	I	External Master Clock Input Pin	Hi-Z
2	BICK	I	Audio Serial Data Clock Pin in PCM mode	Hi-z
	DCLK	I	DSD Clock Pin in DSD mode	
3	LRCK	I	Input Channel Clock Pin in PCM mode	Hi-Z
	DSDL1	I	Audio Serial Data Input in DSD mode	
4	SDTI1	I	Audio Serial Data Input in PCM mode	Hi-Z
	DSDR1	I	Audio Serial Data Input in DSD mode	
5	SDTI2	I	Audio Serial Data Input in PCM mode	Hi-Z
	DSDL2	I	Audio Serial Data Input in DSD mode	
6	SDTI3	I	Audio Serial Data Input in PCM mode	100kΩ Pull down
	DSDR2	I	Audio Serial Data Input in DSD mode	
	TDMO1	O	Audio Serial Data Output in Daisy Chain mode	
7	SDTI4	I	Audio Serial Data Input in PCM mode	100kΩ Pull down
	DSDL3	I	Audio Serial Data Input in DSD mode	
	TDMO2	O	Audio Serial Data Output in Daisy Chain mode	
8	DSDR3	I	Audio Serial Data Input in DSD mode	Hi-Z
9	DSDL4	I	Audio Serial Data Input in DSD mode	Hi-Z
10	DSDR4	I	Audio Serial Data Input in DSD mode	Hi-Z
11	DZF	O	Zero Input Detect in I^2C Bus or 3-wire serial control mode	100kΩ Pull down
	SMUTE	I	Soft Mute Pin in Parallel control mode. When this pin is changed to "H", soft mute cycle is initiated. When it is returning to "L", the output mute is released.	
12	CAD1	I	Chip Address 0 Pin in I^2C Bus or 3-wire serial control mode	Hi-Z
	DCHAIN	I	Daisy Chain Mode select pin in Parallel control mode.	
13	SDA	I/O	Control Data Pin in I^2C Bus serial control mode	Hi-Z
	CDTI	I	Control Data Input Pin in 3-wire serial control mode	
	TDM0	I	TDM Mode select pin in Parallel control mode.	
14	SCL	I	Control Data Clock Pin in I^2C Bus serial control mode	Hi-Z
	CCLK	I	Control Data Clock Pin in 3-wire serial control mode	
	TDM1	I	TDM Mode select pin in Parallel control mode.	
15	CAD0_I2C	I	Chip Address 0 Pin in I^2C Bus serial control mode	Hi-Z
	CSN	I	Chip Select Pin in 3-wire serial control mode	
	DIF	I	Audio Data Format Select in Parallel control mode. "L": 32-bit MSB, "H": 32-bit I^2S	
16	PS	I	(I2C pin = "H") Control Mode Select Pin "L": I^2C Bus serial control mode, "H": Parallel control mode.	Hi-Z
	CAD0_SPI	I	(I2C pin = "L") Chip Address 0 Pin in 3-wire serial control mode	
17	I2C	I	Control Mode Select Pin "L": 3-wire serial control mode "H": I^2C Bus serial control mode or Parallel control mode.	Hi-Z
18	AOUTL1P	O	Lch Positive Analog Output 1 Pin	Hi-Z
19	AOUTL1N	O	Lch Negative Analog Output 1 Pin	Hi-Z
20	VREFL1	I	Negative Voltage Reference Input Pin, AVSS	Hi-Z
21	VREFH1	I	Positive Voltage Reference Input Pin, AVDD	Hi-Z

No.	Pin Name	I/O	Function	PD State
22	AOUTR1N	O	Rch Negative Analog Output 1 Pin	Hi-Z
23	AOUTR1P	O	Rch Positive Analog Output 1 Pin	Hi-Z
24	AOUTL2P	O	Lch Positive Analog Output 2 Pin	Hi-Z
25	AOUTL2N	O	Lch Negative Analog Output 2 Pin	Hi-Z
26	VREFL2	I	Negative Voltage Reference Input Pin, AVSS	Hi-Z
27	VREFH2	I	Positive Voltage Reference Input Pin, AVDD	Hi-Z
28	AOUTR2N	O	Rch Negative Analog Output 2 Pin	Hi-Z
29	AOUTR2P	O	Rch Positive Analog Output 2 Pin	Hi-Z
30	AVSS	-	Analog Ground Pin	—
31	AVDD	-	Analog Power Supply Pin, 3.0V~5.5V	—
32	AOUTL3P	O	Lch Positive Analog Output 3 Pin	Hi-Z
33	AOUTL3N	O	Lch Negative Analog Output 3 Pin	Hi-Z
34	VREFH3	I	Positive Voltage Reference Input Pin, AVDD	Hi-Z
35	VREFL3	I	Negative Voltage Reference Input Pin, AVSS	Hi-Z
36	AOUTR3N	O	Rch Negative Analog Output 3 Pin	Hi-Z
37	AOUTR3P	O	Rch Positive Analog Output 3Pin	Hi-Z
38	AOUTL4P	O	Lch Positive Analog Output 4 Pin	Hi-Z
39	AOUTL4N	O	Lch Negative Analog Output 4 Pin	Hi-Z
40	VREFH4	I	Positive Voltage Reference Input Pin, AVDD	Hi-Z
41	VREFL4	I	Negative Voltage Reference Input Pin, AVSS	Hi-Z
42	AOUTR4N	O	Rch Negative Analog Output 4 Pin	Hi-Z
43	AOUTR4P	O	Rch Positive Analog Output 4 Pin	Hi-Z
44	LDOE	I	Internal LDO Enable Pin. “L”: Disable, “H”: Enable	Hi-Z
45	TVDD	-	Digital Power Supply Pin, 3.0V~3.6V	—
46	DVSS	-	Digital Ground Pin	—
47	VDD18	O	LDO Output Pin (LDOE pin = “H”) This pin should be connected to DVSS with 1.0µF.	(Note 4)
		I	1.8V Power Input Pin (LDOE pin = “L”)	
48	PDN	I	Power-Down & Reset Pin When this pin is “L”, the AK4458 is powered-down and the control registers are reset to default state.	Hi-Z

Note 2. All input pins except internal pull-up/down pins should not be left floating.
Note 3. PCM mode and DSD mode are controlled by registers. Daisy Chain mode is controlled by both registers and pins.
Note 4. This pin outputs DVSS when the LDOE pin = “H” and Hi-z when the LDOE pin = “L”.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	AOUTL1P/N, AOUTR1P/N AOUTL2P/N, AOUTR2P/N AOUTL3P/N, AOUTR3P/N AOUTL4P/N, AOUTR4P/N	These pins must be open.
Digital	DZF	This pin must be open.
	SDTI1-4, DSDR3, DSDL4, DSDR4	These pins must be connected to DVSS

6. Absolute Maximum Ratings

(AVSS =DVSS =0V; Note 5)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital I/O	TVDD	–0.3	4.0	V
	Digital Core	VDD18	–0.3	2.5	V
	|AVSS – DVSS|	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	–0.3	TVDD+0.3	V
Ambient Temperature (Power applied)					
When the back pad is connected to ground		Ta	–40	105	°C
When the back pad is open		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 5. All voltages with respect to ground.
Note 6. AVSS and DVSS must be connected to the same potential.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(AVSS =DVSS =0V; Note 5)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog	AVDD	3.0	5.0	5.5	V
	(LDOE pin= "L") (Note 7)					
	Digital I/O	TVDD	VDD18	1.8	3.6	V
	Digital Core	VDD18	1.7	1.8	1.98	V
	(LDOE pin = "H")(Note 8)					
	Digital I/O	TVDD	3.0	3.3	3.6	V
Voltage Reference	"H" voltage reference "L"	VREFH1-4	AVDD–0.5	-	AVDD	V
	voltage reference	VREFL1-4	-	AVSS	-	V

Note 7. TVDD must be powered up before VDD18 when the LDOE pin = "L". The power up sequence between AVDD and TVDD or AVDD and VDD18 is not critical.
Note 8. When LDOE pin = "H", the internal LDO supplies 1.8V (typ). The power up sequences between AVDD and TVDD, AVDD and VDD18 are not critical.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

■ Analog Characteristics

(1) AVDD = 5.0V

(Ta=25°C: TVDD=3.3V, AVDD=5.0V: AVSS= DVSS=0V: VREFH1/2/3/4=AVDD, VREFL1/2/3/4= AVSS: fs=44.1kHz: BICK=64fs: Signal Frequency=1kHz: 24-bit Input Data: $R_L \geq 2k\Omega$: measurement bandwidth = 20Hz ~ 20kHz: External Circuit: (Figure 75), unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Resolution			-	-	32	bit
Dynamic Characteristics (Note 9)						
THD+N	fs=44.1kHz	0dBFS	-	-107	-100	dB
	BW=20kHz	–60dBFS	-	-52	-	dB
	fs=96kHz	0dBFS	-	-104	-	dB
	BW=40kHz	–60dBFS	-	-48	-	dB
	fs=192kHz	0dBFS		-104	-	dB
	BW=40kHz	–60dBFS		-48	-	dB
	BW=80kHz	–60dBFS		-44	-	dB
Dynamic Range (–60dBFS with A-weighted) (Note 10)			110	115	-	dB
S/N (A-weighted) (Note 11)			110	115	-	dB
Interchannel Isolation (1kHz)			100	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0	0.3	dB
Gain Drift (Note 12)			-	20	-	ppm/°C
Output Voltage (Note 13)			±2.65	±2.8	±2.95	Vpp
Load Resistance (Note 14)			2	-	-	kΩ
Load Capacitance (Note 14)			-	-	30	pF
Power Supplies						
Power Supply Current						
Normal operation (PDN pin = "H")						
AVDD			-	31	41	mA
TVDD (fs = 44.1kHz)			-	8	11	mA
TVDD (fs = 96kHz)			-	13	17	mA
TVDD (fs = 192kHz)			-	20	26	mA
Power down (PDN pin = "L") (Note 15)						
AVDD+TVDD			-	1	100	μA

(2) AVDD = 3.3V

(Ta=25°C: TVDD=3.3V, AVDD=3.3V: AVSS= DVSS=0V: VREFH1/2/3/4=AVDD, VREFL1/2/3/4= AVSS: fs=44.1kHz: BICK=64fs: Signal Frequency=1kHz: 24-bit Input Data: $R_L \geq 2k\Omega$: measurement bandwidth = 20Hz ~ 20kHz: External Circuit: (Figure 75), unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Resolution					32	bit
Dynamic Characteristics		(Note 9)				
THD+N	fs=44.1kHz	0dBFS	-	-93	-86	dB
	BW=20kHz	–60dBFS	-	-48	-	dB
	fs=96kHz	0dBFS	-	-92	-	dB
	BW=40kHz	–60dBFS	-	-45	-	dB
	fs=192kHz	0dBFS		-92	-	dB
	BW=40kHz	–60dBFS		-45	-	dB
	BW=80kHz	–60dBFS		-41	-	dB
Dynamic Range(–60dBFS with A-weighted)		(Note 10)	106	111	-	dB
S/N (A-weighted)		(Note 11)	106	111	-	dB
Inter channel Isolation (1kHz)			100	110	-	dB
DC Accuracy						
Inter channel Gain Mismatch				0	0.3	dB
Gain Drift		(Note 12)	-	20	-	ppm/°C
Output Voltage		(Note 13)	±1.66	±1.85	±2.04	Vpp
Load Resistance		(Note 14)	2	-	-	kΩ
Load Capacitance		(Note 14)	-	-	30	pF
Power Supplies						
Power Supply Current						
Normal operation (PDN pin = "H", input opposite phase to each Lch and Rch)						
AVDD			-	24	-	mA
TVDD (fs = 44.1kHz)			-	8	-	mA
TVDD (fs = 96kHz)			-	13	-	mA
TVDD (fs = 192kHz)			-	20	-	mA
Power down (PDN pin = "L")		(Note 15)				
AVDD+TVDD				1	100	μA

Note 9. Measured by Audio Precision, System Two. Averaging mode.

Note 10. Figure 75 External LPF Circuit Example 1. 100dB for 16-bit data.

Note 11. Figure 75 External LPF Circuit Example 1. S/N does not depend on input data size.

Note 12. The voltage on (VREFH1/2/3/4 – VREFL1/2/3/4) is held +5V externally.

Note 13. The full scale voltage when applying a 1kHz sine wave (0dB) in PCM mode, or when applying a 1kHz sine wave (25~75% duty) in DSD mode. Output voltage scales with the voltage of (VREFH1/2/3/4 – VREFL1/2/3/4).

DAC1: AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFH1 – VREFL1)/5

DAC2: AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFH2 – VREFL2)/5

DAC3: AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFH3 – VREFL3)/5

DAC4: AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFH4 – VREFL4)/5

Note 14. Regarding Load Resistance, AC load is 2kΩ (min) with a DC cut capacitor (Figure 75). DC load is 3.5kΩ (min) without a DC cut capacitor (Figure 75). The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore the capacitive load must be minimized.

Note 15. In the power down mode. All other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.

■ Sharp Roll-Off Filter Characteristics

Sharp Roll-Off Filter Characteristics (fs= 44.1kHz)
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		20.0	kHz
	−3.0dB	PB		21.5		kHz
Pass band Ripple (Note 17)		PR	-0.0032		0.0032	dB
Stop band (Note 16)		SB	24.1			kHz
Stop band Attenuation (Note 19)		SA	80			dB
Group Delay (Note 18)		GD	-	26.8	-	1/fs
Frequency Response (Note 19)	±0.07dB	-	0		20.0	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 20.0kHz			-0.2		0.1	dB

Sharp Roll-Off Filter Characteristics **(fs= 96kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Pass band Ripple (Note 17)		PR	-0.0032		0.0032	dB
Stop band (Note 16)		SB	52.5	0		43.5
Stop band Attenuation (Note 19)		SA	80			dB
Group Delay (Note 18)		GD	-	26.8	-	1/fs
Frequency Response (Note 19)	±0.07dB	-	0		43.5	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 40.0kHz			-0.3		0.1	dB

Sharp Roll-Off Filter Characteristics **(fs= 192kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		87.0	kHz
	−3.0dB	PB		93.6		kHz
Pass band Ripple (Note 17)		PR	-0.0032		0.0032	dB
Stop band (Note 16)		SB	105			kHz
Stop band Attenuation (Note 19)		SA	80			dB
Group Delay (Note 18)		GD	-	26.8	-	1/fs
Frequency Response (Note 19)	±0.07dB	-	0		87.0	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 80.0kHz			-1		0.1	dB

Note 16. The pass band and stop band frequencies scale with fs. For example, PB=0.4535×fs, SB=0.546×fs.
Note 17. It is the pass band gain amplitude of the double over sampling filter at the first step of the Interpolator.
Note 18. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32bit data of both channels to input register to the output of analog signal.
Note 19. The output level is assumed as 0dB when inputting a 1kHz 0dB sine wave.
*Digital filter characteristics are based on simulation results.

■ Slow Roll-Off Filter Characteristics

Slow Roll-Off Filter Characteristics **(fs = 44.1kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 20)	±0.05dB	PB	0		8.1	kHz
	−3.0dB	PB		18.2		kHz
Pass band Ripple (Note 17)		PR	-0.043		0.043	dB
Stop band (Note 20)		SB	39.2			
Stop band Attenuation (Note 19)		SA	73			dB
Group Delay (Note 18)		GD	-	6.3	-	1/fs
Frequency Response (Note 19)	±0.05dB	-	0		8.1	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 20.0kHz			-5		0.1	dB

Slow Roll-Off Filter Characteristics **(fs = 96kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 20)	±0.05dB	PB	0		17.7	kHz
	−3.0dB	PB		39.5		kHz
Pass band Ripple (Note 17)		PR	-0.043		0.043	dB
Stop band (Note 20)		SB	85.3			
Stop band Attenuation (Note 19)		SA	73			dB
Group Delay (Note 18)		GD	-	6.3	-	1/fs
Frequency Response (Note 19)	±0.05dB	PB	0		17.7	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 40.0kHz			-5		0.1	dB

Slow Roll-Off Filter Characteristics **(fs = 192kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 20)	±0.05dB	PB	0		35.5	kHz
	−3.0dB	PB		79.0		kHz
Pass band Ripple (Note 17)		PR	-0.043		0.043	dB
Stop band (Note 20)		SB	171			kHz
Stop band Attenuation (Note 19)		SA	73			dB
Group Delay (Note 18)		GD	-	6.3	-	1/fs
Frequency Response (Note 19)	±0.05dB	PB	0		35.5	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 80.0kHz			-5		0.1	dB

Note 20. The pass band and stop band frequencies scale with fs. For example, PB=0.185×fs, SB=0.888×fs.

■ Short Delay Sharp Roll-Off Filter Characteristics

Short Delay Sharp Roll-Off Filter Characteristics **(fs= 44.1kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		20.0	kHz
	−3.0dB	PB		21.5		kHz
Pass band Ripple (Note 17)		PR	-0.0031		0.0031	dB
Stop band (Note 16)		SB	24.1			kHz
Stop band Attenuation (Note 19)		SA	80			dB
Group Delay (Note 18)		GD	-	5.8	-	1/fs
Frequency Response (Note 19)	±0.07dB	-	0		20.0	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 20.0kHz			-0.2		0.1	dB

Short Delay Sharp Roll-Off Filter Characteristics **(fs= 96kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Pass band Ripple (Note 17)		PR	-0.0031		0.0031	dB
Stop band (Note 16)		SB	52.5	0		43.5
Stop band Attenuation (Note 19)		SA	80			dB
Group Delay (Note 18)		GD	-	5.8	-	1/fs
Frequency Response (Note 19)	±0.07dB	-	0		43.5	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 40.0kHz			-0.3		0.1	dB

Short Delay Sharp Roll-Off Filter Characteristics **(fs= 192kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		87.0	kHz
	−3.0dB	PB		93.6		kHz
Pass band Ripple (Note 17)		PR	-0.0031		0.0031	dB
Stop band (Note 16)		SB	105			kHz
Stop band Attenuation (Note 19)		SA	80			dB
Group Delay (Note 18)		GD	-	5.8	-	1/fs
Frequency Response (Note 19)	±0.07dB	-	0		87.0	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 80.0kHz			-1		0.1	dB

■ Short Delay Slow Roll-Off Filter Characteristics

Short Delay Slow Roll-Off Filter Characteristics **(fs= 44.1kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 21)	±0.05dB	PB	0		11.1	kHz
	−3.0dB	PB		19.4		kHz
Pass band Ripple (Note 17)		PR	-0.05		0.05	dB
Stop band (Note 21)		SB	38.1			kHz
Stop band Attenuation (Note 19)		SA	82			dB
Group Delay (Note 18)		GD	-	4.8	-	1/fs
Frequency Response (Note 19)	±0.05dB	-	0		11.1	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 20.0kHz			-5		0.1	dB

Short Delay Slow Roll-Off Filter Characteristics **(fs= 96kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 21)	±0.05dB	PB	0		24.2	kHz
	−3.0dB	PB		42.1		kHz
Pass band Ripple (Note 17)		PR	-0.05		0.05	dB
Stop band (Note 21)		SB	83.0			43.5
Stop band Attenuation (Note 19)		SA	82			dB
Group Delay (Note 18)		GD	-	4.8	-	1/fs
Frequency Response (Note 19)	±0.05dB	-	0		24.2	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 40.0kHz			-5		0.1	dB

Short Delay Slow Roll-Off Filter Characteristics **(fs= 192kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 21)	±0.05dB	PB	0		48.4	kHz
	−3.0dB	PB		84.3		kHz
Pass band Ripple (Note 17)		PR	-0.05		0.05	dB
Stop band (Note 21)		SB	165.9			kHz
Stop band Attenuation (Note 19)		SA	82			dB
Group Delay (Note 18)		GD	-	4.8	-	1/fs
Frequency Response (Note 19)	±0.05dB	-	0		48.4	kHz
Digital Filter + SCF (Note 19)						
Frequency Response: 0 ~ 80.0kHz			-5		0.1	dB

Note 21. The pass band and stop band frequencies scale with fs. For example, PB=0.252×fs, SB=0.864×fs.

■ DSD Mode Characteristics

(1) DSDF bit= "0"

(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; fs=44.1kHz; D/P bit="1", DSDF bit="0")

Parameter			Min.	Typ.	Max.	Unit
Digital Filter Response						
Frequency Response (Note 22)	DSDSEL[1:0]					
	"00"	20kHz 50kHz 100kHz		-0.8 -5.5 -19.9		dB
	"01"	40kHz 200kHz 400kHz		-0.8 -5.5 -19.9		dB
	"10"	80kHz 400kHz 800kHz		-0.8 -5.5 -19.9		dB

(2) DSDF bit= "1"

(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; fs=44.1kHz; D/P bit="1", DSDF bit="1")

Parameter			Min.	Typ.	Max.	Unit
Digital Filter Response						
Frequency Response (Note 22)	DSDSEL[1:0]					
	"00"	20kHz 100kHz 200kHz		-0.2 -6.3 -23.7		dB
	"01"	40kHz 200kHz 400kHz		-0.2 -6.3 -23.7		dB
	"10"	80kHz 400kHz 800kHz		-0.2 -6.3 -23.7		dB

Note 22. In DSD mode, the signal level is ranging from 25% to 75%. Peak levels of DSD signal above this duty are not recommended by SACD format book (Scarlet Book).

Note 23. It is assumed that the output level is 0dB when the input signal is 1kHz and the duty range is between 25 ~ 75%.The output level is assumed as 0dB when applying a 1kHz sine wave in 25~ 75% duty.

*Digital filter characteristics are based on simulation results.

■ DC Characteristics

(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
TVDD=1.7 ~ 3.0V					
High-Level Input Voltage	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	20%TVDD	V
TVDD=3.0V ~ 3.6V					
High-Level Input Voltage	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD	V
High-Level Output Voltage (LRCK, BICK pins: Iout=-100μA)	VOH	TVDD−0.5	-	-	V
Low-Level Output Voltage					
(excpt SDA pin : Iout= 100μA)	VOL	-	-	0.5	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout= 3mA)	VOL	-	-	0.4	V
(SDA pin, 1.7V ≤ TVDD ≤ 2.0V: Iout= 3mA)	VOL	-		20%TVDD	V
Input Leakage Current	Iin	-	-	±10	μA

■ Switching Characteristics

(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V, C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
Frequency	fCLK	2.048		49.152	MHz
Duty Cycle	dCLK	40		60	%
Minimum Pulse Width	tCLKH	9.155			ns
	tCLKL	9.155			ns
LRCK Frequency (Note 24)					
Normal Mode (TDM1-0 bits = "00")					
Normal Speed Mode	fsn	8		54	kHz
Double Speed Mode	fsd	54		108	kHz
Quad Speed Mode	fsq	108		216	kHz
Oct speed mode	fso		384		kHz
Hex speed mode	fsh		768		kHz
Duty Cycle	Duty	45		55	%
TDM128 mode (TDM1-0 bits = "01")					
Normal Speed Mode	fsn	8		54	kHz
Double Speed Mode	fsd	54		108	kHz
Quad Speed Mode	fsq	108		216	kHz
High time	tLRH	1/128fs			nsec
Low time	tLRL	1/128fs			ns
TDM256 mode (TDM1-0 bits = "10")					
Normal Speed Mode High time	fsn	8		54	kHz
Double Speed Mode	fsd	54		108	kHz
High time	tLRH	1/256fs			nsec
Low time	tLRL	1/256fs			nsec
TDM512 mode (TDM1-0 bits = "11")					
Normal Speed Mode	fsn	8		54	kHz
High time	tLRH	1/512fs			nsec
Low time	tLRL	1/512fs			nsec
PCM Audio Interface Timing					
Normal Mode (TDM1-0 bits = "00")					
BICK Period					
Normal Speed Mode	tBCK	1/256fsn			nsec
Double Speed Mode	tBCK	1/128fsd			nsec
Quad Speed Mode	tBCK	1/64fsq			nsec
Oct speed mode	tBCK	1/64fso			nsec
Hex speed mode	tBCK	1/64fsh			nsec
BICK Pulse Width Low	tBCKL	9			nsec
BICK Pulse Width High	tBCKH	9			nsec
BICK "↑" to LRCK Edge (Note 25)	tBLR	5			nsec
LRCK Edge to BICK "↑" (Note 25)	tLRB	5			nsec
SDTI1/2/3/4 Hold Time	tSDH	5			nsec
SDTI1/2/3/4 Setup Time	tSDS	5			nsec

Parameter	Symbol	Min.	Typ.	Max.	Unit
TDM128 mode (TDM1-0 bits = "01")					
BICK Period					
Normal Speed Mode	tBCK	1/128fsn			nsec
Double Speed Mode	tBCK	1/128fsd			nsec
Quad Speed Mode	tBCK	1/128fsq			nsec
BICK Pulse Width Low	tBCKL	14			nsec
BICK Pulse Width High	tBCKH	14			nsec
BICK "↑" to LRCK Edge (Note 25)	tBLR	14			nsec
LRCK Edge to BICK "↑" (Note 25)	tLRB	14			nsec
SDTI1/2 Hold Time	tSDH	5			nsec
SDTI1/2 Setup Time	tSDS	5			nsec
TDM256 mode (TDM1-0 bits = "10")					
BICK Period					
Normal Speed Mode	tBCK	1/256fsn			nsec
Double Speed Mode (Note 26)	tBCK	1/256fsd			nsec
BICK Pulse Width Low	tBCKL	14			nsec
BICK Pulse Width High	tBCKH	14			nsec
BICK "↑" to LRCK Edge (Note 25)	tBLR	14			nsec
LRCK Edge to BICK "↑" (Note 25)	tLRB	14			nsec
TDMO1/2 Setup time BICK "↑"	tBSS	5			nsec
TDMO1/2 Hold time BICK "↑" (Note 28)	tBSH	5			nsec
SDTI1/2 Hold Time	tSDH	5			nsec
SDTI1/2 Setup Time	tSDS	5			nsec
TDM512 mode (TDM1-0 bits = "11")					
BICK Period					
Normal Speed Mode (Note 27)	tBCK	1/512fsn			nsec
BICK Pulse Width Low	tBCKL	14			nsec
BICK Pulse Width High	tBCKH	14			nsec
BICK "↑" to LRCK Edge (Note 25)	tBLR	14			nsec
LRCK Edge to BICK "↑" (Note 25)	tLRB	14			nsec
TDMO1 Setup time BICK "↑"	tBSS	5			nsec
TDMO1 Hold time BICK "↑" (Note 28)	tBSH	5			nsec
SDTI1 Hold Time	tSDH	5			nsec
SDTI1 Setup Time	tSDS	5			nsec

Parameter	Symbol	Min.	Typ.	Max.	Unit
DSD Audio Interface Timing					
(64 mode, DSDSEL 1-0 bits = "00")					
DCLK Period	tDCK		1/64fs		nsec
DCLK Pulse Width Low	tDCKL	144			nsec
DCLK Pulse Width High	tDCKH	144			nsec
DCLK Edge to DSDL/R (Note 29)	tDDD	−20		20	nsec
(128 mode, DSDSEL 1-0 bits = "01")					
DCLK Period	tDCK		1/128fs		nsec
DCLK Pulse Width Low	tDCKL	72			nsec
DCLK Pulse Width High	tDCKH	72			nsec
DCLK Edge to DSDL/R (Note 29)	tDDD	−10		10	nsec
(256 mode, DSDSEL 1-0 bits = "10")					
DCLK Period	tDCK		1/256fs		nsec
DCLK Pulse Width Low	tDCKL	36			nsec
DCLK Pulse Width High	tDCKH	36			nsec
DCLK Edge to DSDL/R (Note 29)	tDDD	−5		5	nsec

Note 24. When the 1152fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK4458 should be reset by the PDN pin or RSTN bit.

Note 25. BICK rising edge must not occur at the same time as LRCK edge.

Note 26. fsd (max) = 96kHz when TVDD < 3.0V in Daisy Chain mode.

Note 27. fsd (max) = 48kHz when TVDD < 3.0V in Daisy Chain mode.

Note 28. tBSH (min) = 4 nsec when TVDD < 2.6V and the LDOE pin = "L".

Note 29. DSD data transmitting device must meet this time.
tDDD is defined from a falling edge of DCLK "↓" to a DSDL/R edge when DCKB bit = "0" and it is defined from a rising edge of DCLK "↑" to a DSDL/R edge when DCKB bit = "1".

(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.62 ~ 1.98V / 3.0 ~ 3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (3-wire Serial mode):					
CCLK Period	tCCK	200			nsec
CCLK Pulse Width Low	tCCKL	80			nsec
Pulse Width High	tCCKH	80			nsec
CDTI Setup Time	tCDS	40			nsec
CDTI Hold Time	tCDH	40			nsec
CSN "H" Time	tCSW	150			nsec
CSN "↓" to CCLK "↑"	tCSS	50			nsec
CCLK "↑" to CSN "↑"	tCSH	50			nsec
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µsec
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µsec
Clock Low Time	tLOW	1.3		-	µsec
Clock High Time	tHIGH	0.6		-	µsec
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µsec
SDA Hold Time from SCL Falling (Note 30)	tHD:DAT	0		-	µsec
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µsec
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µsec
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µsec
Setup Time for Stop Condition	tSU:STO	0.6		-	µsec
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	nsec
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing (Note 31)					
PDN Accept Pulse Width	tAPD	150			nsec
PDN Reject Pulse Width	tRPD			30	nsec

Note 30. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 31.The AK4458 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 150ns for a certain reset. The AK4458 is not reset by the "L" pulse less than 30ns.

Note 32. I^2C is a trademark of NXP B.V.

■ Timing Diagram

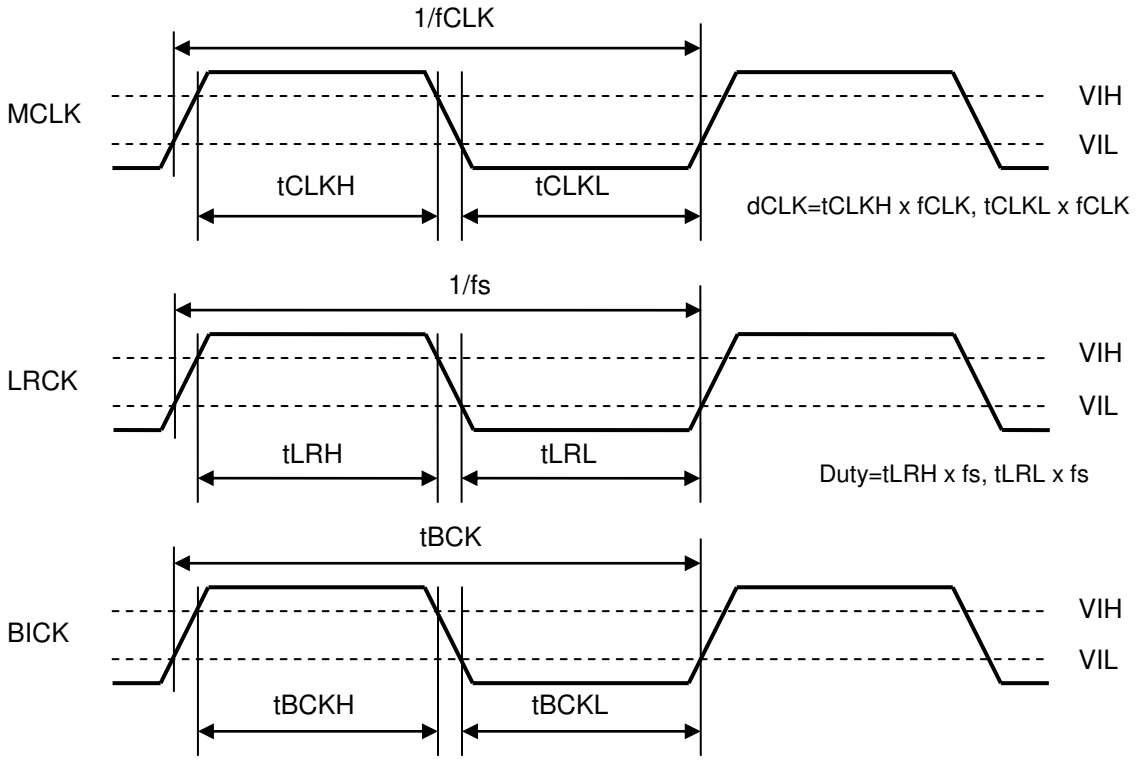


Figure 2. Clock Timing

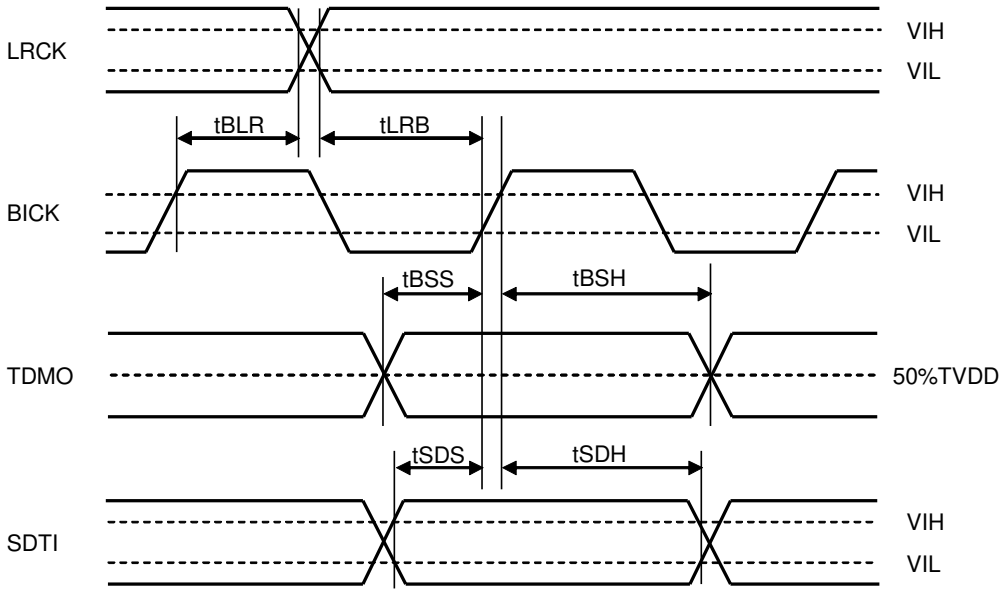


Figure 3. Audio Interface Timing (PCM mode)

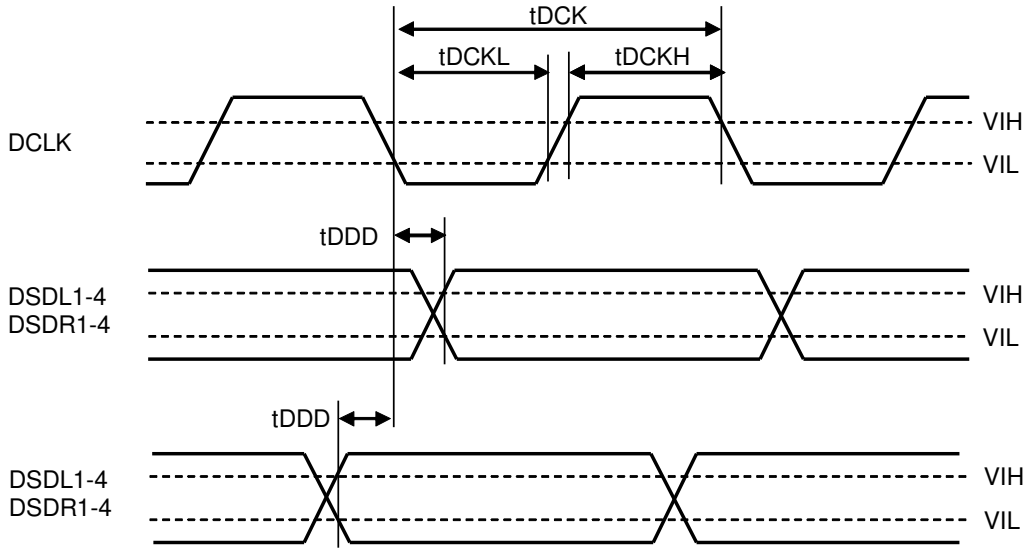


Figure 4. Audio Serial Interface Timing (DSD Normal Mode, DCKB bit = "0")

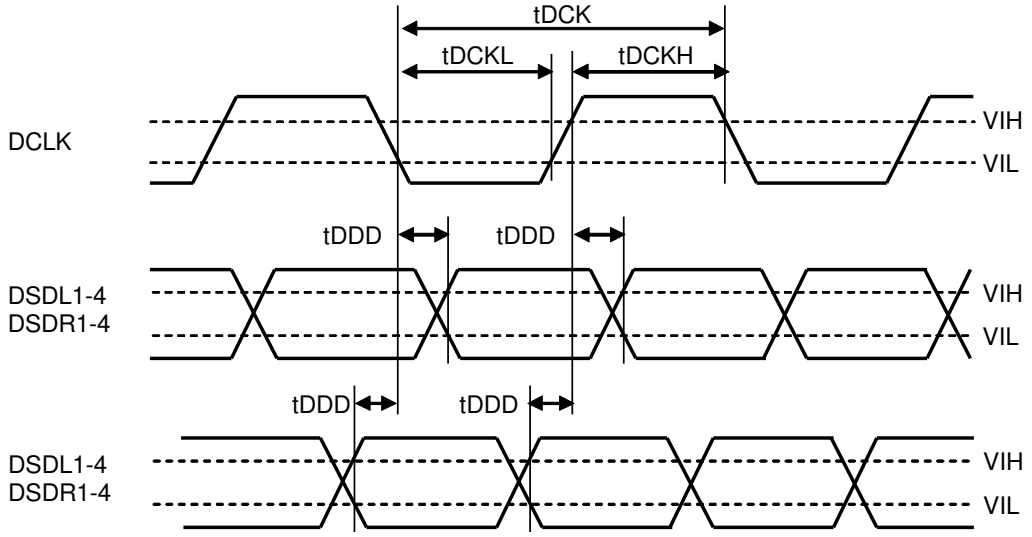


Figure 5. Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB bit = "0")

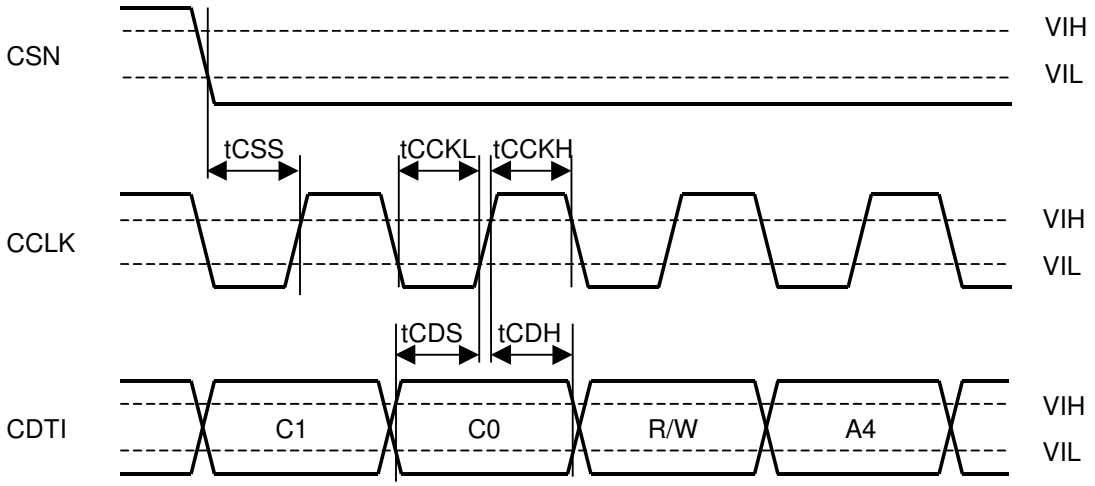


Figure 6. WRITE Command Input Timing (3-wire Serial mode)

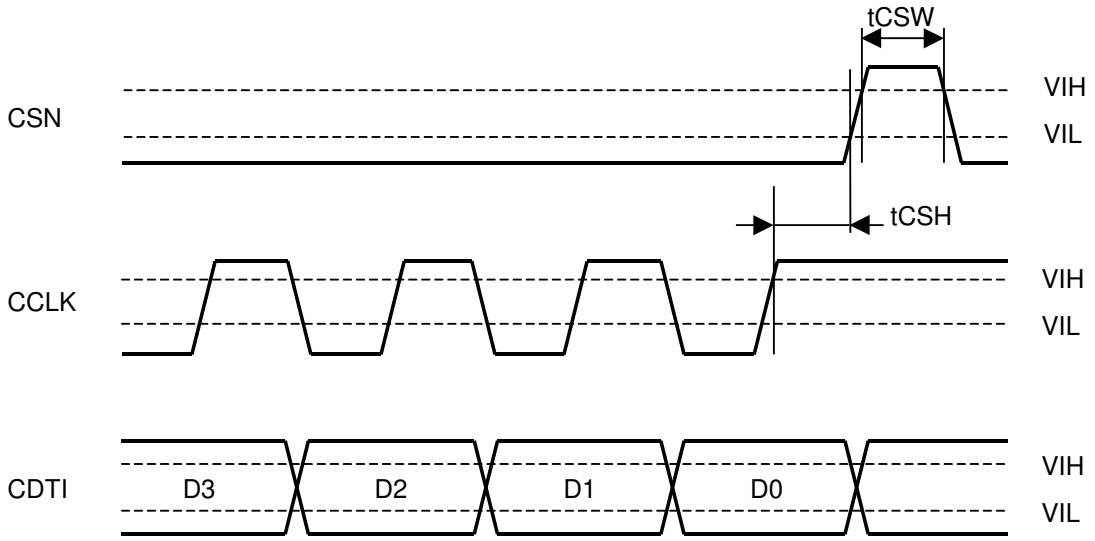


Figure 7. WRITE Data Input Timing (3-wire Serial mode)

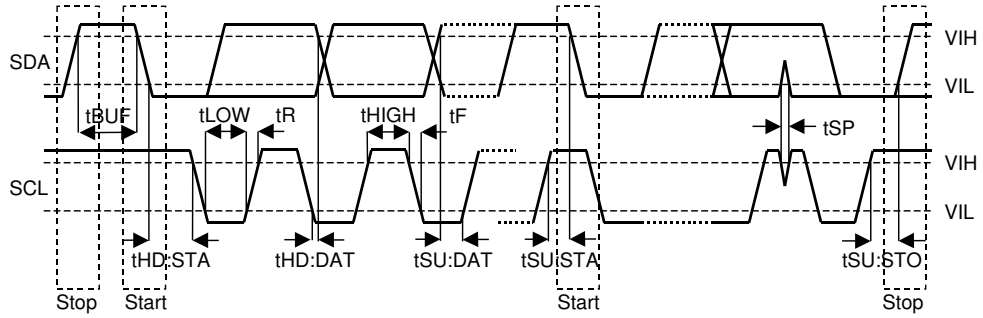


Figure 8. I^{2}C Bus mode Timing

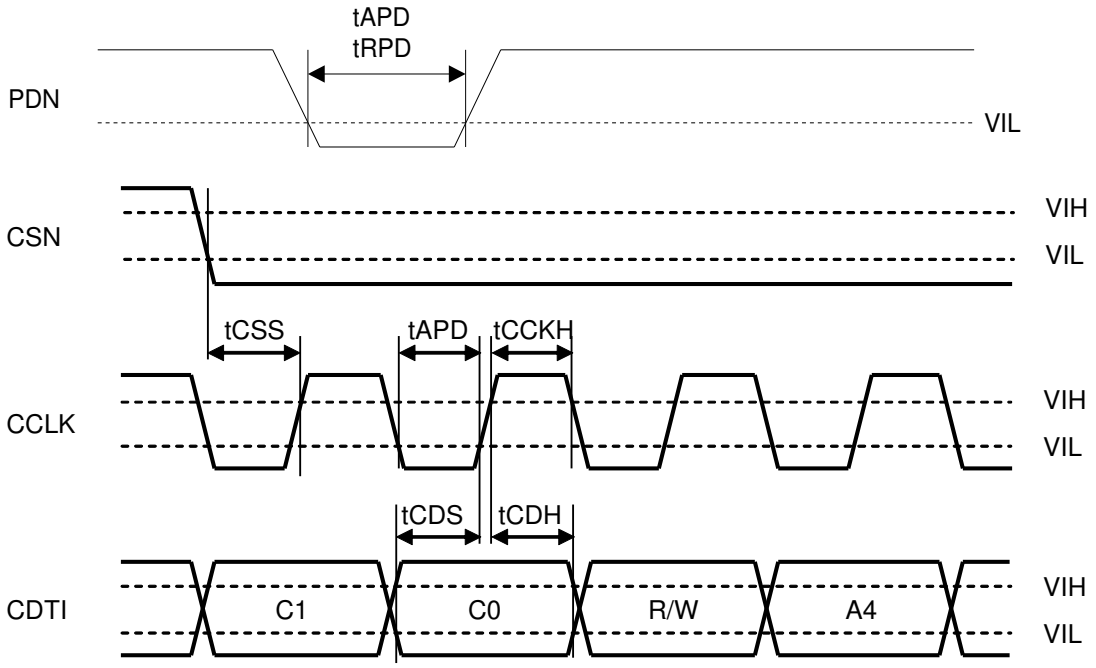


Figure 9. Power-down & Reset Timing