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AK4480

High Performance 114dB 32-Bit DAC

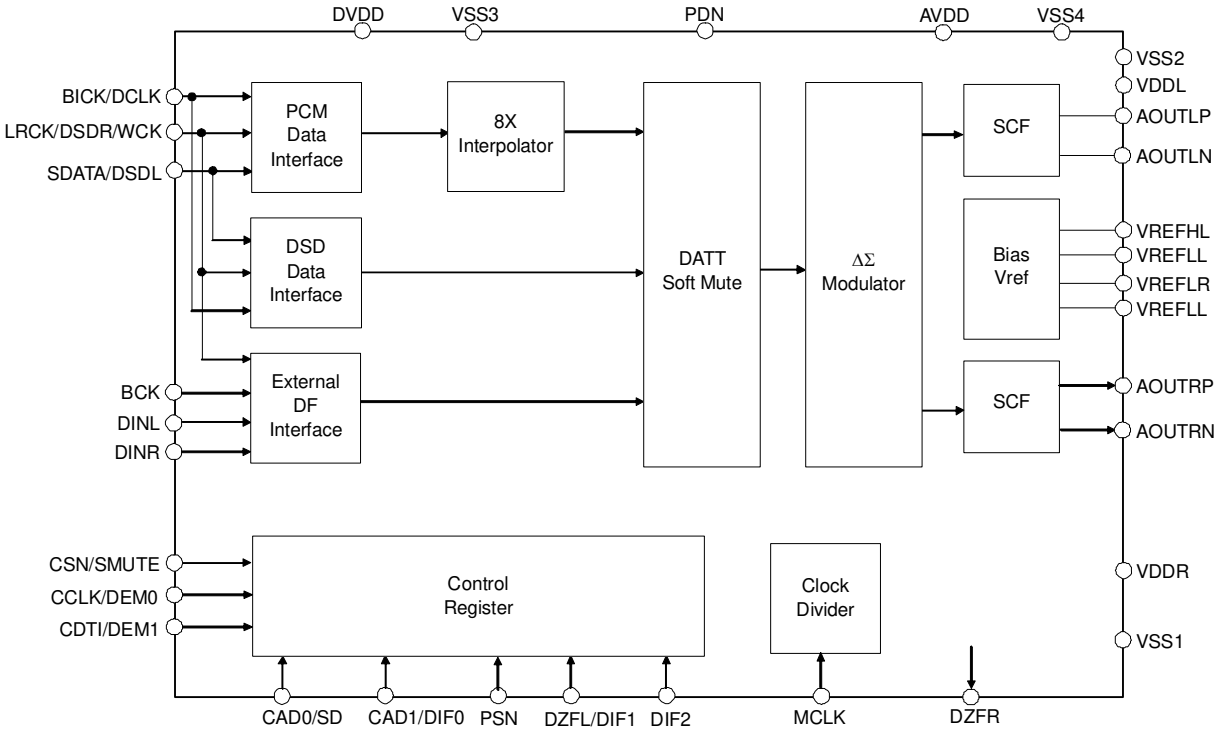
GENERAL DESCRIPTION

The AK4480 is a 32-bit DAC, which corresponds to Blu-ray Disc systems. An internal circuit includes newly developed 32bit Digital Filter for better sound quality achieving low distortion characteristics and wide dynamic range. The AK4480 has full differential SCF outputs, removing the need for AC coupling capacitors and increasing performance for systems with excessive clock jitter. The AK4480 accepts 216kHz PCM data and 1-bit DSD data, ideal for a wide range of applications including Blu-ray Discs and SACDs.

FEATURES

- **128x Over Sampling**
- **Sampling Rate: 30kHz ~ 216kHz**
- **32Bit 8x Digital Filter**
  - **Ripple: ±0.005dB, Attenuation: 70dB**
  - **Minimum delay option GD=7/fs**
  - **Sharp Roll-off Filter**
  - **Slow Roll-off Filter**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **DSD Data Input**
- **Digital De-emphasis for 32, 44.1, 48kHz Sampling**
- **Soft Mute**
- **Digital Attenuator (Linear 256 steps)**
- **Mono Mode**
- **External Digital Filter Mode**
- **THD+N: -100dB**
- **DR, S/N: 114dB (117dB when Mono mode)**
- **I/F Format: 24/32bit MSB justified, 16/20/24/32bit LSB justified, I^2S, DSD**
- **Master Clock:**
  - **30kHz ~ 32kHz: 1152fs**
  - **30kHz ~ 54kHz: 512fs or 768fs**
  - **30kHz ~ 108kHz: 256fs or 384fs**
  - **108kHz ~ 216kHz: 128fs or 192fs**
- **Power Supply: 4.75 ~ 5.25V**
- **Digital Input Level: TTL**
- **Package: 30pin VSOP**

■ Block Diagram

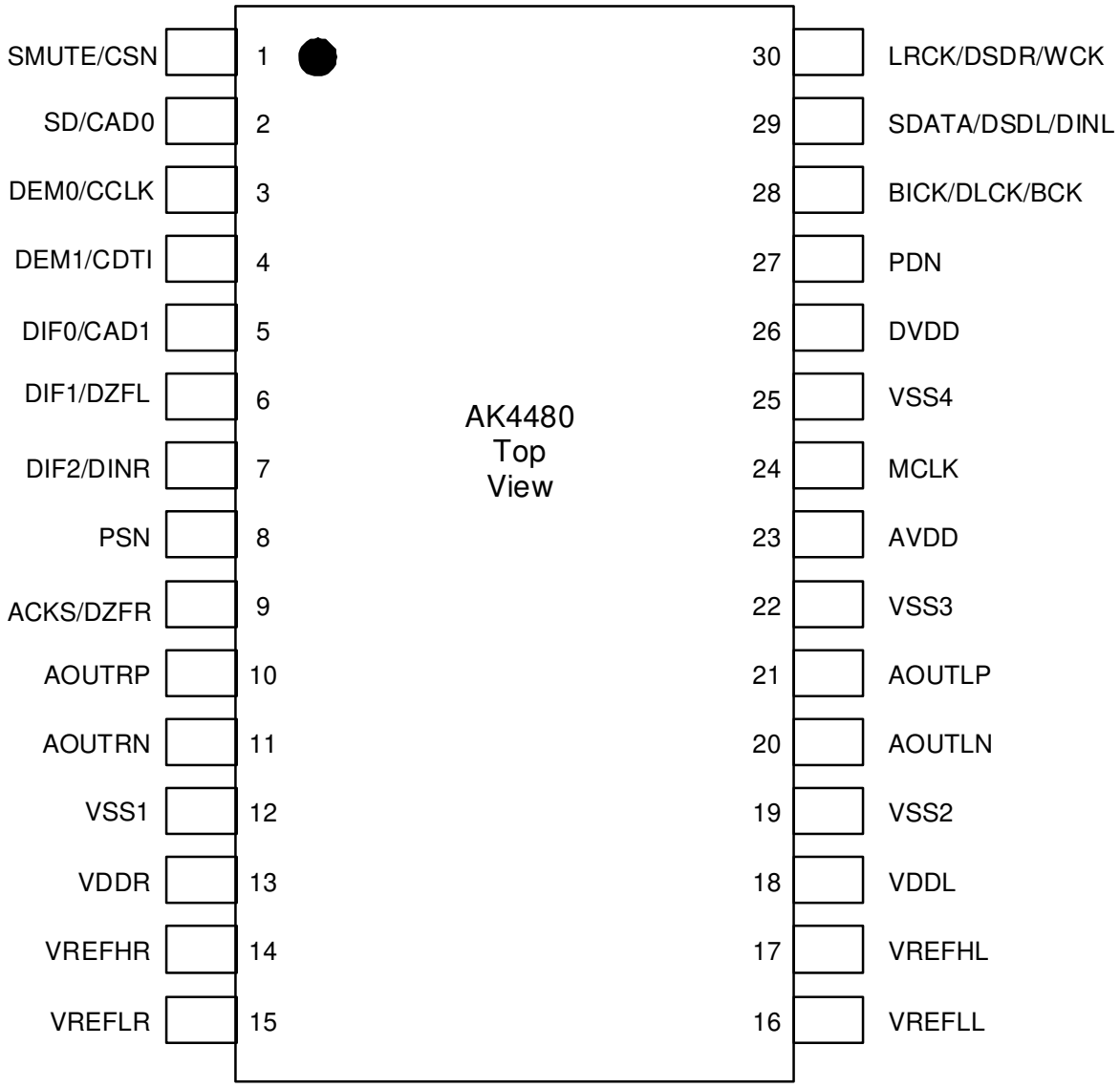


Block Diagram

■ Ordering Guide

AK4480EF	–10 ~ +70°C	30pin VSOP (0.65mm pitch)
AKD4480	Evaluation Board for AK4480	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	SMUTE	I	Soft Mute in Parallel Control Mode When this pin goes to "H", soft mute cycle is initiated. When returning to "L", the output mute releases.
	CSN	I	Chip Select in Serial Control Mode
2	SD	I	Digital Filter Select Pin
	CAD0	I	Chip Address 0 in Serial Control Mode
3	DEM0	I	De-emphasis Enable 0 in Parallel Control Mode
	CCLK	I	Control Data Clock in Serial Control Mode
4	DEM1	I	De-emphasis Enable 1 in Parallel Control Mode
	CDTI	I	Control Data Input in Serial Control Mode
5	DIF0	I	Digital Input Format 0 in PCM Mode
	CAD1	I	Chip Address 1 in Serial Control Mode
6	DIF1	I	Digital Input Format 1 in PCM Mode
	DZFL	O	Left Channel Zero Input Detect in Serial Control Mode
7	DIF2	I	Digital Input Format 2 in PCM Mode
	DINR	I	Rch Audio Serial Data Input in External DF Mode.
8	PSN	I	Parallel/Serial Select (Internal pull-up pin) "L": Serial Control Mode, "H": Parallel Control Mode
9	ACKS	I	Clock Auto Setting Mode Pin
	DZFR	O	Rch Zero Input Detect in Serial Control Mode
10	AOUTRP	O	Right Channel Positive Analog Output
11	AOUTRN	O	Right Channel Negative Analog Output
12	VSS1	-	Connected to VSS2/3/4 Ground
13	VDDR	-	Right Channel Analog Power Supply, 4.75~5.25V
14	VREFHR	I	Right Channel High Level Voltage Reference Input
15	VREFLR	I	Right Channel Low Level Voltage Reference Input
16	VREFLL	I	Left Channel Low Level Voltage Reference Input
17	VREFHL	I	Left Channel High Level Voltage Reference Input
18	VDDL	-	Left Channel Analog Power Supply, 4.75~5.25V
19	VSS2	-	Ground (connected to VSS1/3/4 ground)
20	AOUTLN	O	Left Channel Negative Analog Output
21	AOUTLP	O	Left Channel Positive Analog Output
22	VSS3	-	Ground (connected to VSS1/2/4 ground)
23	AVDD	-	Analog Power Supply, 4.75 to 5.25V
24	MCLK	I	Master Clock Input
25	VSS4	-	Connected to VSS1/2/3 Ground
26	DVDD	-	Digital Power Supply, 4.75 ~ 5.25V
27	PDN	I	Power-Down Mode When at "L", the AK4480 is in power-down mode and is held in reset. The AK4480 should always be reset upon power-up.

Note: All input pins except internal pull-up/down pins must not be left floating.

PIN/FUNCTION (Continued)

No.	Pin Name	I/O	Function
28	BICK	I	Audio Serial Data Clock in PCM Mode
	DCLK	I	Audio Serial Data Clock in DSD Mode
	BCK	I	Audio Serial Data Clock in EXDF Mode
29	SDATA	I	Audio Serial Data Input in PCM Mode
	DSDL	I	Lch Audio Serial Data Clock in DSD Mode
	DINL	I	Lch Audio Serial Data Clock in EXDF Mode
30	LRCK	I	L/R Clock in PCM Mode
	DSDR	I	Rch Audio Serial Data Input Pin in DSD Mode
	WCK	I	Word Clock Pin in EXDF Mode

Note: All input pins except internal pull-up/down pins must not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

(1) Parallel Mode (PCM Mode only)

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.

(2) Serial Mode

1. PCM Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	DIF2, PSN	These pins must be connected to VSS4.
	DZFL, DZFR	These pins must be open.

2. DSD Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	DIF2, PSN	These pins must be connected to VSS4.
	DZFL, DZFR	These pins must be open.

3. Ex DF Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	DIF2, PSN	These pins must be connected to VSS4.
	DZFL, DZFR	These pins must be open.

ABSOLUTE MAXIMUM RATINGS

(VSS1-4 =0V; Note 1)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Analog	VDDL/R	–0.3	6.0	V
	Digital	DVDD	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	–10	70	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. VSS1-4 must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1-4 =0V; Note 1)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 3)	Analog	AVDD	4.75	5.0	5.25	V
	Analog	VDDL/R	4.75	5.0	5.25	V
	Digital	DVDD	4.75	5.0	5.25	V
Voltage Reference (Note 4)	VREFHL/R	VREFHL/R	AVDD–0.5	-	AVDD	V
	VREFLL/R	VREFLL/R	-	VSS	-	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD, VDDL/R and DVDD is not critical.
Note 4. The VREFLL/R pin must be the same voltage as VSS.
The analog output voltage scales with the voltage of (VREFH – VREFL).
AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.4Vpp × (VREFHL/R – VREFLL/R)/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=VDDL/R=DVDD=5.0V; VSS1-4 =0V; VREFHL/R=AVDD, VREFLL/R= VSS;
Input data = 24bit; $R_L \geq 1k\Omega$; BICK=64fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz;
Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: Figure 20; unless otherwise specified.)

Parameter			min	typ	max	Unit
Resolution			-	-	32	Bits
Dynamic Characteristics (Note 5)						
THD+N	fs=44.1kHz	0dBFS	-	-100	-93	dB
	BW=20kHz	–60dBFS	-	-51	-	dB
	fs=96kHz	0dBFS	-	97	-	dB
	BW=40kHz	–60dBFS	-	-48	-	dB
	fs=192kHz	0dBFS		97	-	dB
	BW=40kHz	–60dBFS		-48	-	dB
	BW=80kHz	–60dBFS		-45	-	dB
Dynamic Range (–60dBFS with A-weighted) (Note 6)			108	114		dB
S/N (A-weighted) (Note 7)			108	114		dB
Interchannel Isolation (1kHz)			100	110		dB
DC Accuracy						
Interchannel Gain Mismatch			-	0	0.3	dB
Gain Drift (Note 8)			-	20	-	ppm/°C
Output Voltage (Note 9)			±2.25	±2.4	±2.55	Vpp
Load Capacitance			-	-	25	pF
Load Resistance (Note 10)			2	-	-	kΩ
Power Supplies						
Power Supply Current						
Normal operation (PDN pin = "H")						
AVDD + VDDL/R			-	30	45	mA
DVDD (fs ≤ 96kHz)			-	15	-	mA
DVDD (fs = 192kHz)			-	24	36	mA
Power down (PDN pin = "L") (Note 11)						
AVDD+VDDL/R+DVDD			-	10	100	μA

Note 5. Measured by Audio Precision, System Two. Averaging mode. Refer to the evaluation board manual.
Note 6. Figure 20 External LPF Circuit Example 2. 100dB for 16-bit data.
Note 7. Figure 20 External LPF Circuit Example 2. S/N does not depend on input data size.
Note 8. The voltage on (VREFH – VREFL) is held +5V externally.
Note 9. Full-scale voltage(0dB). Output voltage scales with the voltage of (VREFHL/R – VREFLL/R).
AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.4Vpp × (VREFHL/R – VREFLL/R)/5.
Note 10. Regarding Load Resistance, AC load is 2kΩ (min) with a DC cut capacitor. Please refer to Figure 20. The load resistance is 4k ohm (min) to ground when without a DC cut capacitor. Please refer to Figure 19. Load Resistance is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected output pin. Therefore the capacitive load must be minimized.
Note 11. In the power down mode. P/S pin = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held VSS4.

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Normal Speed Mode; DEM=OFF; SLOW bit ="0", SD bit="0")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)		PB	0	-	20.0	kHz
Frequency Response	±0.05dB	PB	0		20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 12)		SB	24.1			kHz
Passband Ripple		PR	-0.005		+0.0001	dB
Stopband Attenuation		SA	70			dB
Group Delay (Note 13)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-0.2	-	+0.2	dB

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Double Speed Mode; DEM=OFF; SLOW bit ="0", SD bit="0")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)		PB	0	-	43.5	kHz
Frequency Response	±0.05dB		0	-	43.5	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 12)		SB	52.5	-		kHz
Passband Ripple		PR	-0.005	-	+0.0001	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 13)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-0.3	-	+0.3	dB

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Quad Speed Mode; DEM=OFF; SLOW bit ="0", SD bit="0")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)		PB	0	-	87.0	kHz
Frequency Response	±0.05dB		0		87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 12)		SB	105			kHz
Passband Ripple		PR	-0.005	-	+0.0001	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 13)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-1	-	+0.1	dB

Note 12. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

Note 13. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32bit data of both channels to input register to the output of analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Normal Speed Mode; DEM=OFF; SLOW bit="1", SD bit = "0")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 14)		PB	0	-	8.1	kHz
Frequency Response	±0.07dB		0	-	8.1	kHz
	−3.0dB		-	18.2	-	kHz
Stopband (Note 14)		SB	39.2	-	-	kHz
Passband Ripple		PR	-0.07	-	+0.02	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 13)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-5	-	+0.1	dB

SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Double Speed Mode DEM=OFF; SLOW bit="1", SD bit = "0")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 14)		PB	0	-	17.7	kHz
Frequency Response	±0.07dB		0	-	17.7	kHz
	−3.0dB		-	39.6	-	kHz
Stopband (Note 14)		SB	85.3	-	-	kHz
Passband Ripple		PR	-0.07	-	+0.02	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 13)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-4	-	+0.1	dB

SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Quad Speed Mode; DEM=OFF; SLOW bit="1", SD bit = "0")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 14)		PB	0	-	35.5	kHz
Frequency Response	±0.07dB		0	-	35.5	kHz
	−3.0dB		-	79.1	-	kHz
Stopband (Note 14)		SB	171	-	-	kHz
Passband Ripple		PR	-0.07	-	+0.02	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 13)		GD	-	27	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-5	-	+0.1	dB

Note 14. The passband and stopband frequencies scale with fs. For example, PB=0.185×fs (@±0.04dB), SB=0.888×fs.

MINIMUM DELAY FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Normal Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 14)	±0.01dB	PB	0	-	20.0	kHz
Frequency Response	±0.06dB		0	-	20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 14)		SB	24.1	-	-	kHz
Passband Ripple		PR	-0.0052	-	+0.0006	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 13)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-0.2	-	+0.2	dB

MINIMUM DELAY FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Double Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 14)	±0.01dB	PB	0	-	43.5	kHz
Frequency Response	±0.06dB		0	-	43.5	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 14)		SB	52.5	-	-	kHz
Passband Ripple		PR	-0.0052	-	+0.0006	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 13)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-0.3	-	+0.3	dB

MINIMUM DELAY FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Quad Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 14)	±0.01dB	PB	0	-	87.0	kHz
Frequency Response	±0.06dB		0	-	87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 14)		SB	105	-	-	kHz
Passband Ripple		PR	-0.0052	-	+0.0006	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 13)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-1	-	+0.1	dB

DC CHARACTERISTICS

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V)

Parameter		Symbol	min	typ	max	Unit
High-Level Input Voltage		VIH	2.2	-	-	V
Low-Level Input Voltage		VIL	-	-	0.8	V
High-Level Output Voltage	(Iout=–100μA)	VOH	DVDD–0.5	-	-	V
Low-Level Output Voltage	(Iout=100μA)	VOL	-	-	0.5	V
Input Leakage Current	(Note 15)	Iin	-	-	±10	μA

Note 15. The TEST1/CAD0 pin is an internal pull-down pin, and the P/S pin is an internal pull-up pin, nominally 100kΩ. Therefore TEST1/CAD0 pin and P/S pin are not included.

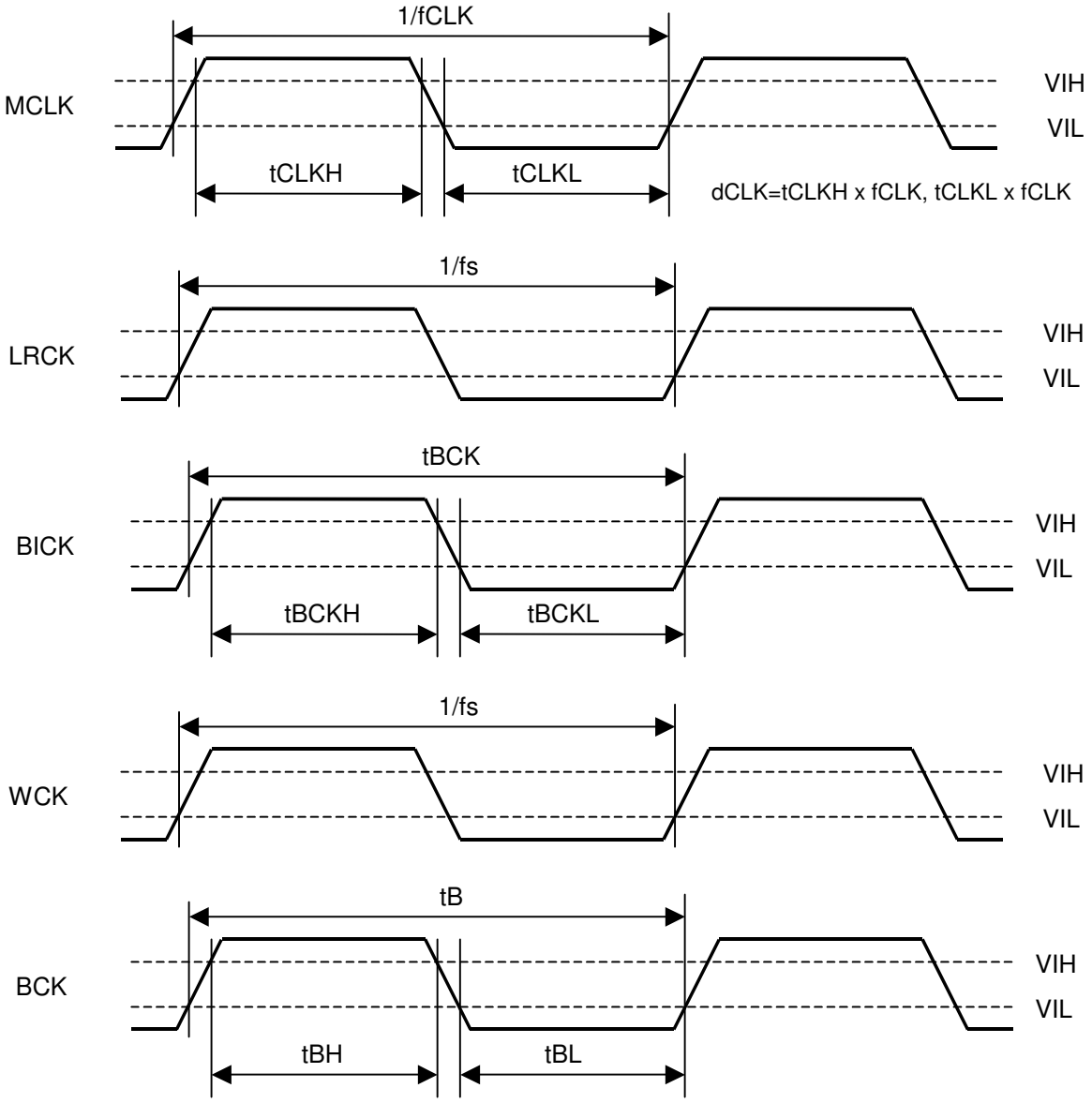
SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V)

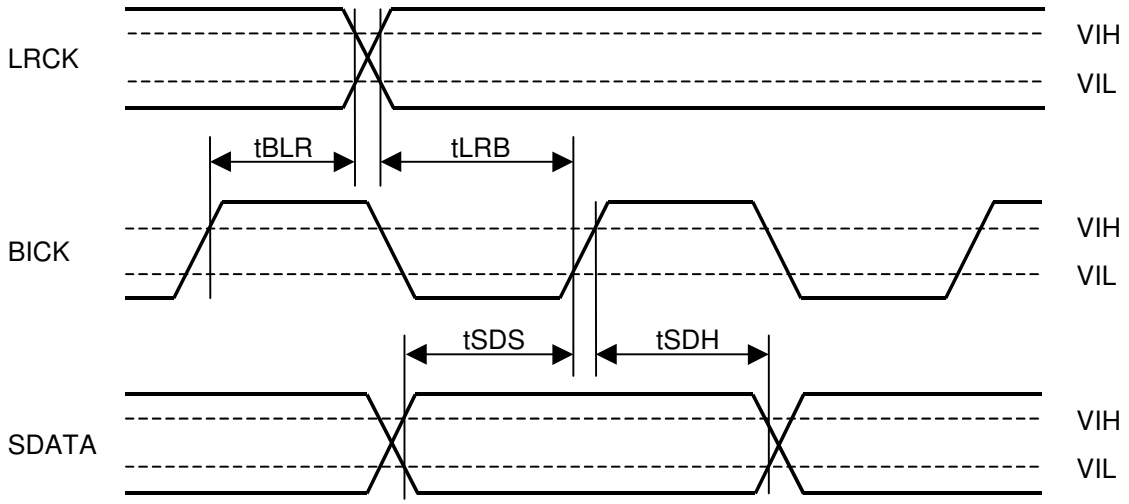
Parameter		Symbol	min	typ	max	Unit
Master Clock Timing						
Frequency		fCLK	7.7		41.472	MHz
Duty Cycle		dCLK	40		60	%
LRCK Frequency	(Note 16)					
1152fs, 512fs or 768fs		fsn	30		54	kHz
256fs or 384fs		fsd	54		108	kHz
128fs or 192fs		fsq	108		216	kHz
Duty Cycle		Duty	45		55	%
PCM Audio Interface Timing						
BICK Period						
1152fs, 512fs or 768fs		tBCK	1/128fsn			ns
256fs or 384fs		tBCK	1/64fsd			ns
128fs or 192fs		tBCK	1/64fsq			ns
BICK Pulse Width Low		tBCKL	30			ns
BICK Pulse Width High		tBCKH	30			ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	20			ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	20			ns
SDATA Hold Time		tSDH	20			ns
SDATA Setup Time		tSDS	20			ns
External Digital Filter Mode						
BICK Period		tB	27			ns
BCK Pulse Width Low		tBL	10			ns
BCK Pulse Width High		tBH	10			ns
BCK "↑" to WCK Edge		tBW	5			ns
WCK Edge to BCK "↑"		tWB	5			ns
WCK Pulse Width Low		tWCK	54			ns
WCK Pulse Width High		tWCH	54			ns
DATA Hold Time		tDH	5			ns
DATA Setup Time		tDS	5			ns
DSD Audio Interface Timing						
DCLK Period		tDCK	-	1/64fs		ns
DCLK Pulse Width Low		tDCKL	160			ns
DCLK Pulse Width High		tDCKH	160			ns
DCLK Edge to DSDL/R	(Note 18)	tDDD	–20		20	ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	50			ns
CDTI Hold Time		tCDH	50			ns
CSN High Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Reset Timing						
PDN Pulse Width	(Note 19)	tPD	150			ns

Note 16. When the 1152fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK4480 should be reset by the PDN pin or RSTN bit.
Note 17. BICK rising edge must not occur at the same time as LRCK edge.
Note 18. DSD data transmitting device must meet this time.
Note 19. The AK4480 can be reset by bringing the PDN pin "L" to "H" upon power-up.

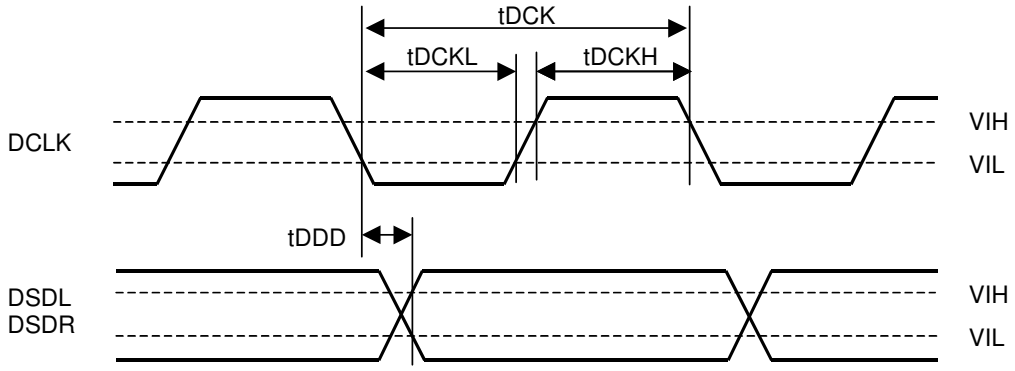
■ Timing Diagram



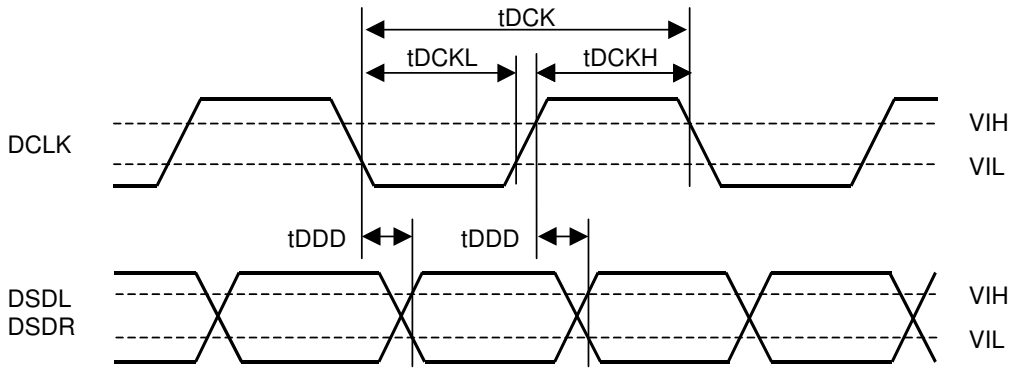
Clock Timing



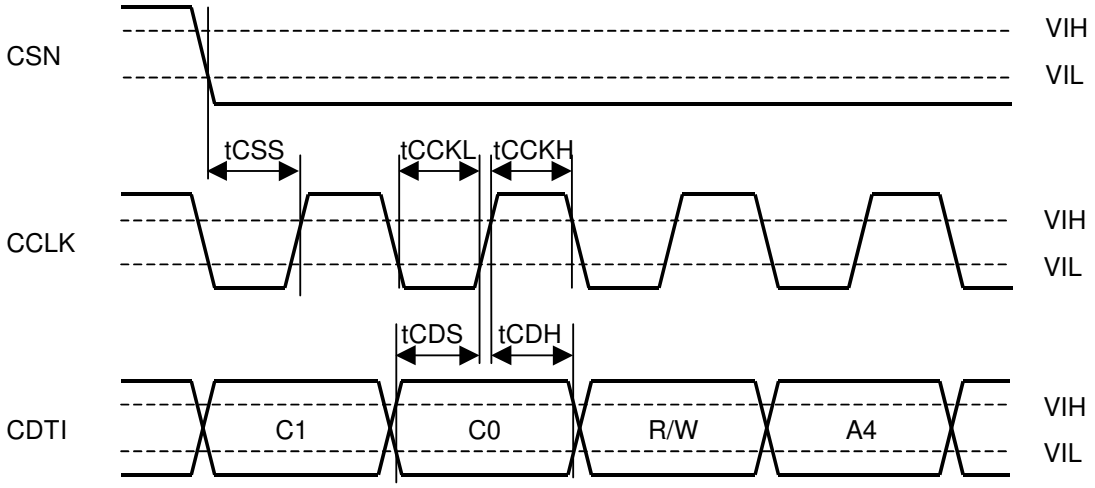
Audio Interface Timing (PCM Mode)



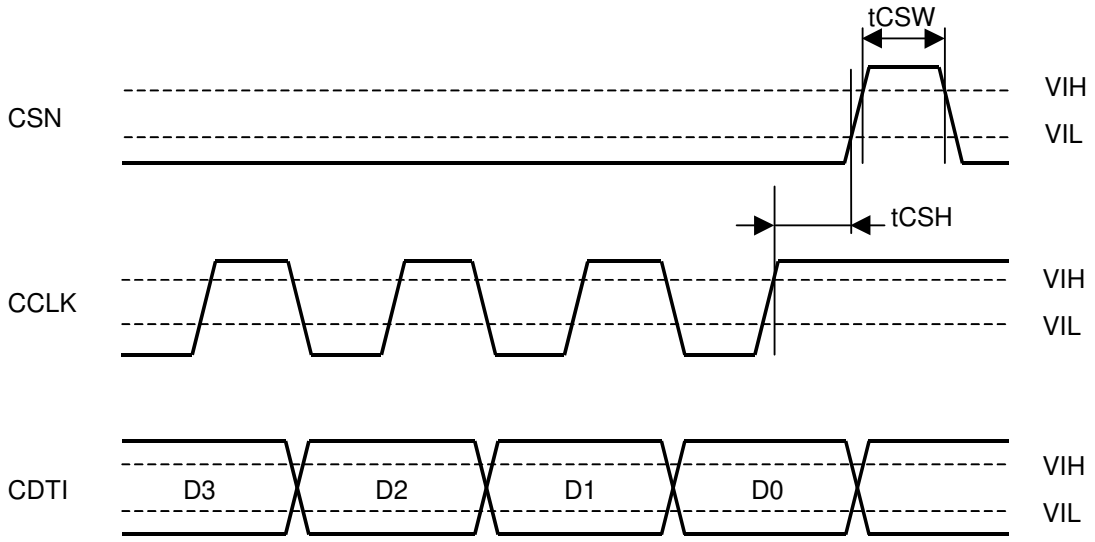
Audio Serial Interface Timing (DSD Normal Mode, DCKB bit = "0")



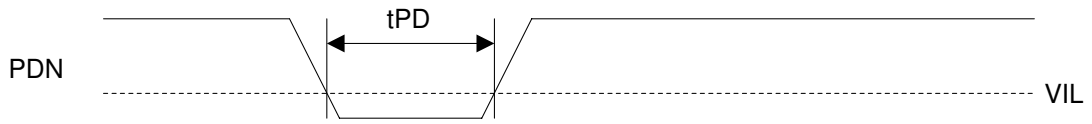
Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB bit = "0")



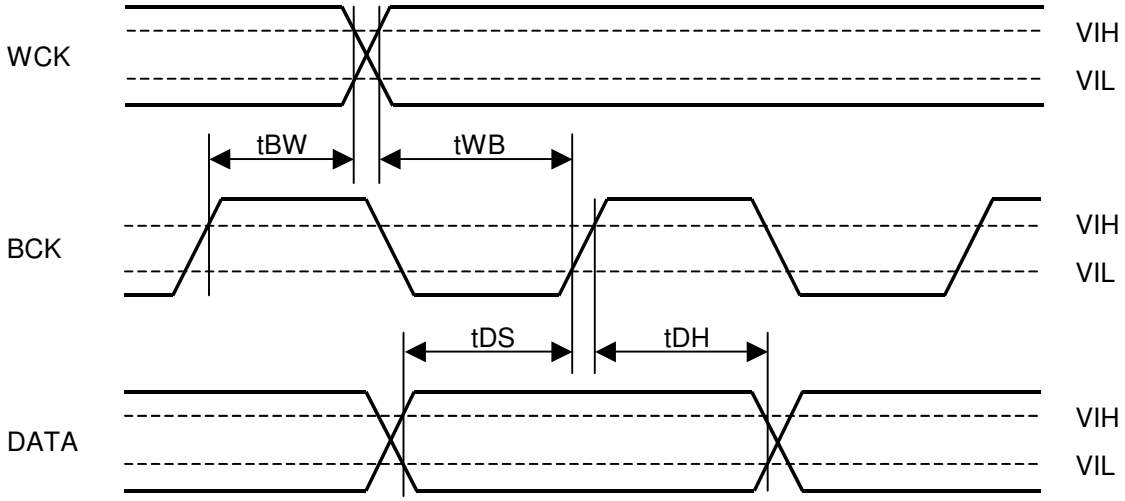
WRITE Command Input Timing



WRITE Data Input Timing



Power Down & Reset Timing



External Digital Filter I/F mode

OPERATION OVERVIEW

■ D/A Conversion Mode

In serial mode, the AK4480 can covert both PCM and DSD data. The D/P bit controls PCM/DSD mode. When DSD mode, DSD data can be input from DCLK, DSDL and DSDR pins. When PCM mode, PCM data can be input from BICK, LRCK and SDATA pins. When PCM/DSD mode is changed by D/P bit, the AK4480 should be reset by RSTN bit. It takes about 2/fs ~ 3/fs to change the mode. In parallel mode, the AK4480 can only convert PCM data.

D/P bit	Interface
0	PCM
1	DSD

Table 1. PCM/DSD Mode Control

When DP bit= "0", an internal digital filter or external digital filter can be selected. When using an external digital filter (EX DF I/F mode), data is input to each MCLK, BCK, WCK, DINL and DINR pin. EXD bit controls the modes. When switching internal and external digital filters, the AK4480 must be reset by RSTN bit. A Digital filter switching takes 2~3k/fs.

Ex DF bit	Interface
0	PCM
1	EX DF I/F

Table 2. Digital Filter Control (DP bit = "0")

■ System Clock

[1] PCM Mode

The external clocks, which are required to operate the AK4480, are MCLK, BICK and LRCK. MCLK should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two modes for setting MCLK frequency, Manual Setting Mode and Auto Setting Mode. In auto setting mode, sampling speed and MCLK frequency are detected automatically and then the initial master clock is set to the appropriate frequency (Table 3). When external clocks are changed, the AK4480 should be reset by the PDN pin or RSTN bit.

The AK4480 is automatically placed in power saving mode when MCLK or LRCK is stopped during normal operation mode, and the analog output goes to AVDD/2 (typ). When MCLK and LRCK are input again, the AK4480 is powered up. After exiting reset following power-up, the AK4480 is not fully operational until MCLK and LRCK are input.

The MCLK frequency corresponding to each sampling speed should be provided (Table 3).

(1) Parallel Mode (P/S pin = "H")

1. Manual Setting Mode (ACKS pin = "L")

The MCLK frequency corresponding to each sampling speed should be provided (Table 3). DFS1 bit is fixed to "0". Quad speed mode is not supported in this mode.

LRCK	MCLK (MHz)							BICK
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	64fs
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	2.0480MHz
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	2.8224MHz
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	3.0720MHz
88.2kHz	11.2896	16.9344	22.5792	33.8688	N/A	N/A	N/A	5.6448MHz
96.0kHz	12.2880	18.4320	24.5760	36.8640	N/A	N/A	N/A	6.1440MHz

Table 3. System Clock Example (Manual Setting Mode @Parallel Mode)(N/A: Not available)

32kHz ~ 96kHz sampling rates are supported (Table 4). However, when the sampling rate is 32kHz ~ 48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

ACKS pin	MCLK	DR,S/N
L	256fs/384fs/512fs/768fs	114dB
H	256fs/384fs	111dB
H	512fs/768fs	114dB

Table 4. Relationship between MCLK Frequency and DR, S/N (fs = 44.1kHz)

2. Auto Setting Mode (ACKS pin = "H")

MCLK frequency and the sampling speed are detected automatically (Table 5). MCLK with appropriate frequency should be input externally for each speed (Table 6).

MCLK		Sampling Speed
1152fs		Normal (fs≤32kHz)
512fs/256fs	768fs/384fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 5. Sampling Speed (Auto Setting Mode @Parallel Mode)

LRCK	MCLK (MHz)							Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	Normal
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	
88.2kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	N/A	
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A	

Table 6. System Clock Example (Auto Setting Mode @Parallel Mode) (N/A: Not available)

MCLK= 256fs/384fs supports sampling rate of 32kHz ~ 96kHz (Table 7). However, when the sampling rate is 32kHz ~ 48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

ACKS pin	MCLK	DR,S/N
L	256fs/384fs/512fs/768fs	114dB
H	256fs/384fs	111dB
H	512fs/768fs	114dB

Table 7. Relationship between MCLK Frequency and DR, S/N (fs = 44.1kHz)

(2) Serial Mode (P/S pin = "L")

1. Manual Setting Mode (ACKS bit = "0")

MCLK frequency is detected automatically and the sampling speed is set by DFS1-0 bits (Table 8). The MCLK frequency corresponding to each sampling speed should be provided (Table 9). The AK4480 is set to Manual Setting Mode at power-up (PDN pin = "L" → "H"). When DFS1-0 bits are changed, the AK4480 should be reset by RSTN bit.

DFS1 bit	DFS0 bit	Sampling Rate (fs)		
0	0	Normal Speed Mode	30kHz ~ 54kHz	(default)
0	1	Double Speed Mode	54kHz ~ 108kHz	
1	0	Quad Speed Mode	120kHz ~ 216kHz	

Table 8. Sampling Speed (Manual Setting Mode @Serial Mode)

LRCK	MCLK (MHz)							BICK
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	64fs
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	2.0480MHz
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	2.8224MHz
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	3.0720MHz
88.2kHz	11.2896	16.9344	22.5792	33.8688	N/A	N/A	N/A	5.6448MHz
96.0kHz	12.2880	18.4320	24.5760	36.8640	N/A	N/A	N/A	6.1440MHz
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	11.2896MHz
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A	12.2880MHz

Table 9. System Clock Example (Manual Setting Mode @Serial Mode)

2. Auto Setting Mode (ACKS bit = "1")

MCLK frequency and the sampling speed are detected automatically (Table 10) and DFS1-0 bits are ignored. The MCLK frequency corresponding to each sampling speed should be provided (Table 11).

MCLK		Sampling Speed
1152fs		Normal (fs≤32kHz)
512fs/256fs	768fs/384fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 10. Sampling Speed (Auto Setting Mode @Serial Mode)

LRCK	MCLK (MHz)							Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	Normal
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	
88.2kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	N/A	
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A	

Table 11. System Clock Example (Auto Setting Mode @Serial Mode)

MCLK= 256fs/384fs supports sampling rate of 32kHz ~ 96kHz (Table 12). However, when the sampling rate is 32kHz ~ 48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

ACKS bit	MCLK	DR,S/N
0	256fs/384fs/512fs/768fs	114dB
1	256fs/384fs	111dB
1	512fs/768fs	114dB

Table 12. Relationship between MCLK Frequency and DR, S/N (fs = 44.1kHz)

[2] DSD Mode

The external clocks, which are required to operate the AK4480, are MCLK and DCLK. MCLK should be synchronized with DCLK but the phase is not critical. The frequency of MCLK is set by DCKS bit.

The AK4480 is automatically placed in reset state when MCLK is stopped during a normal operation, and the analog output becomes AVDD/2 (typ).

DCKS bit	MCLK Frequency	DCLK Frequency	
0	512fs	64fs	(default)
1	768fs	64fs	

Table 13. System Clock (DSD Mode)

■ Audio Interface Format

[1] PCM Mode

Data is shifted in via the SDATA pin using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF2-0 pins (Parallel control mode) or DIF2-0 bits (Serial control mode) as shown in Table 14. In all formats the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20-bit and 16-bit MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	Input Format	BICK	Figure	
0	0	0	0	16bit LSB justified	≥ 32fs	Figure 1	
1	0	0	1	20bit LSB justified	≥ 48fs	Figure 2	
2	0	1	0	24bit MSB justified	≥ 48fs	Figure 3	(default)
3	0	1	1	24bit I^{2}S Compatible	≥ 48fs	Figure 4	
4	1	0	0	24bit LSB justified	≥ 48fs	Figure 2	
5	1	0	1	32bit LSB justified	≥ 64fs	Figure 5	
6	1	1	0	32bit MSB justified	≥64fs	Figure 6	
7	1	1	1	32bit I^{2}S Compatible	≥ 64fs	Figure 7	

Table 14. Audio Interface Format

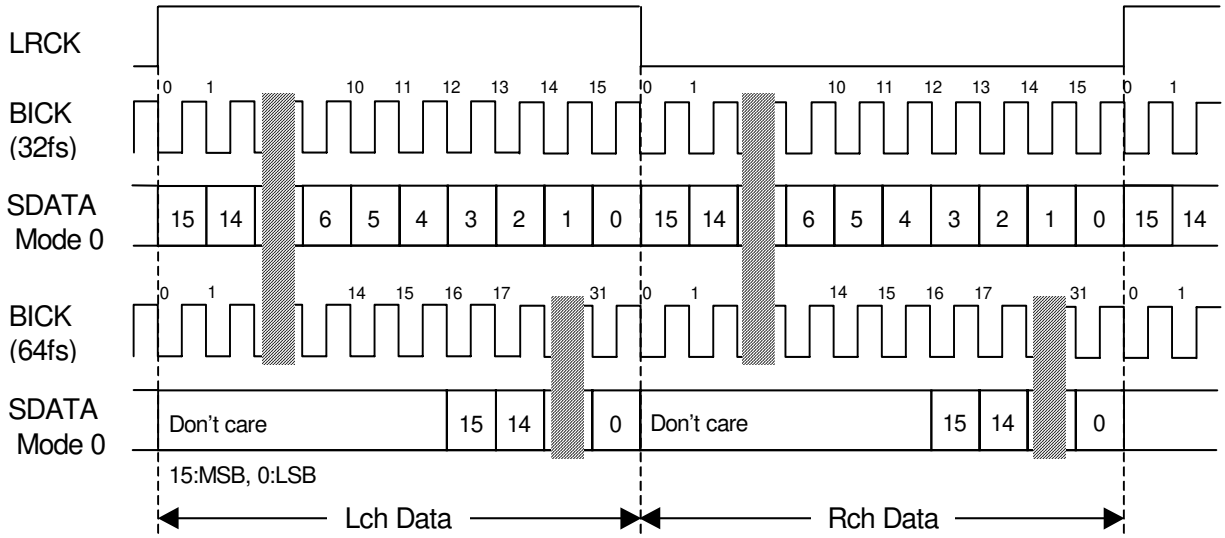


Figure 1. Mode 0 Timing

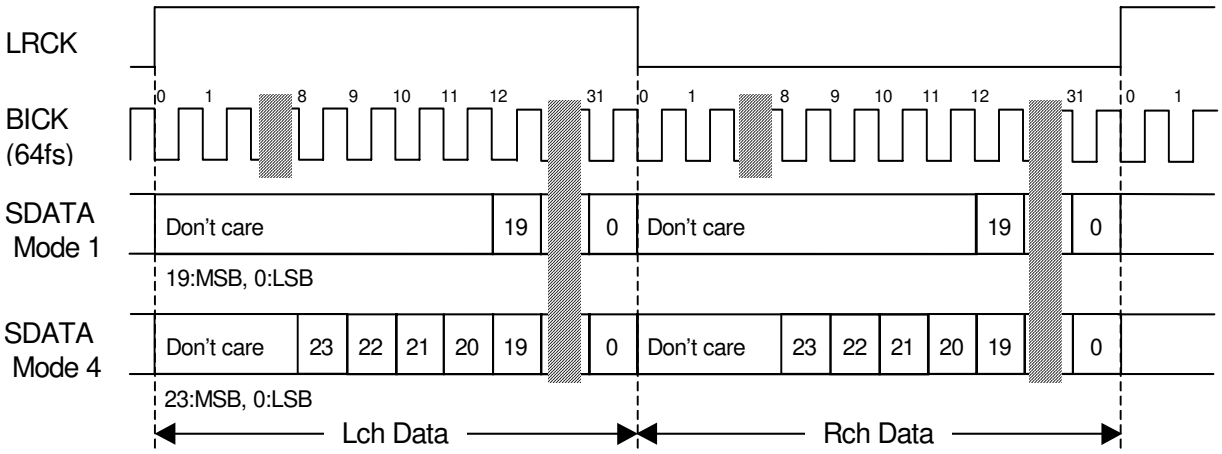


Figure 2. Mode 1/4 Timing

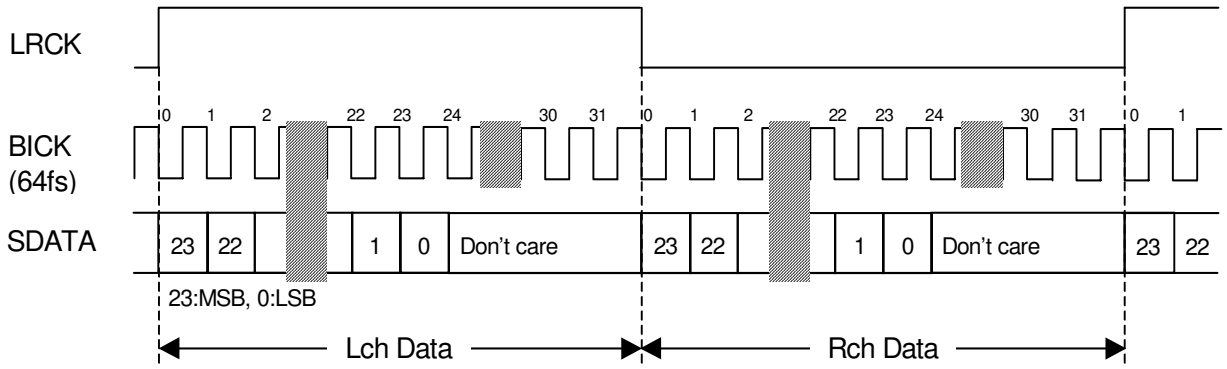


Figure 3. Mode 2 Timing

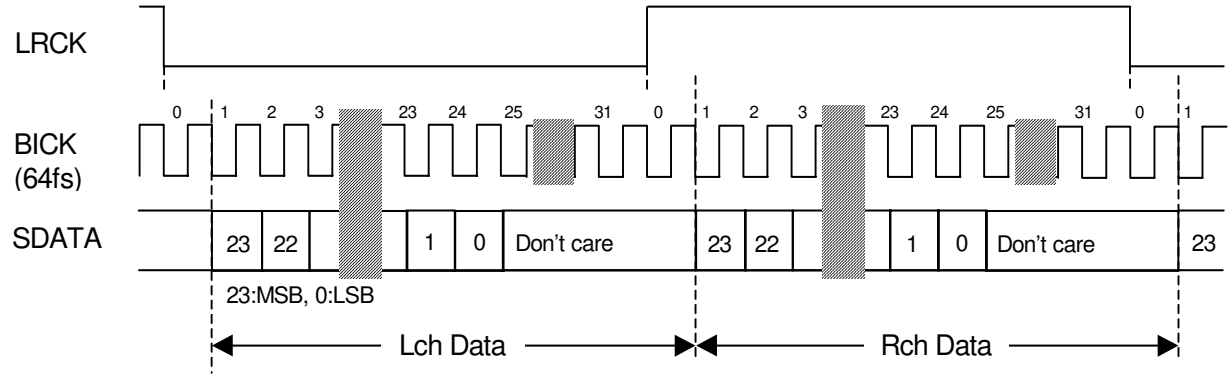


Figure 4. Mode 3 Timing

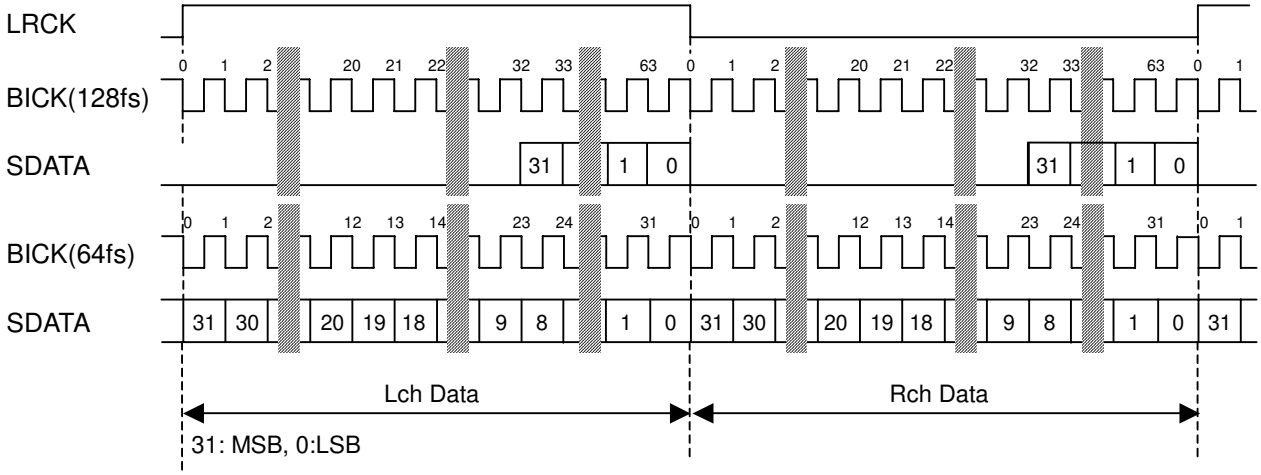


Figure 5. Mode 5 Timing

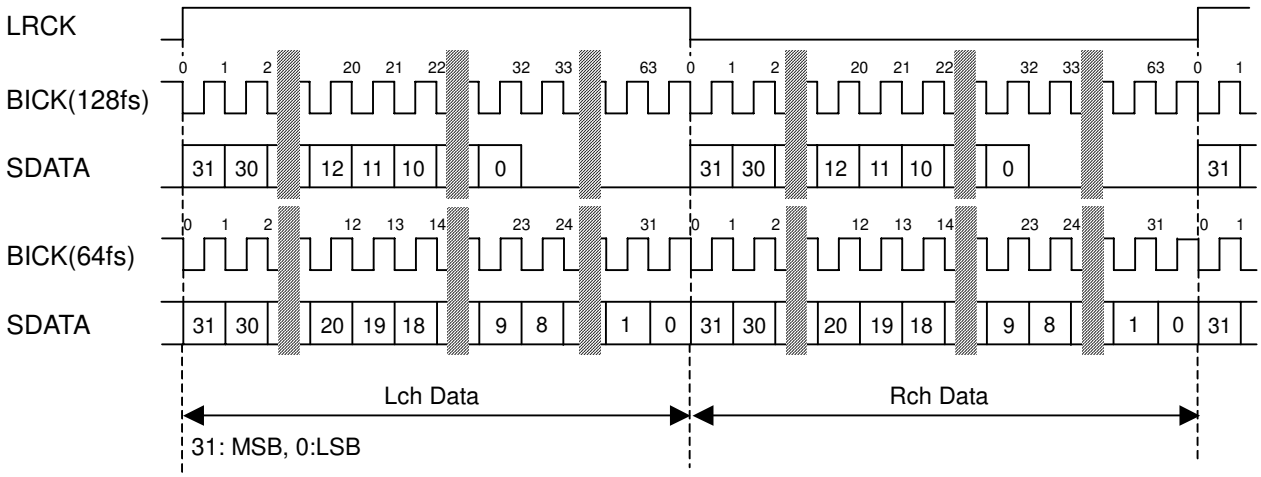


Figure 6. Mode 6 Timing

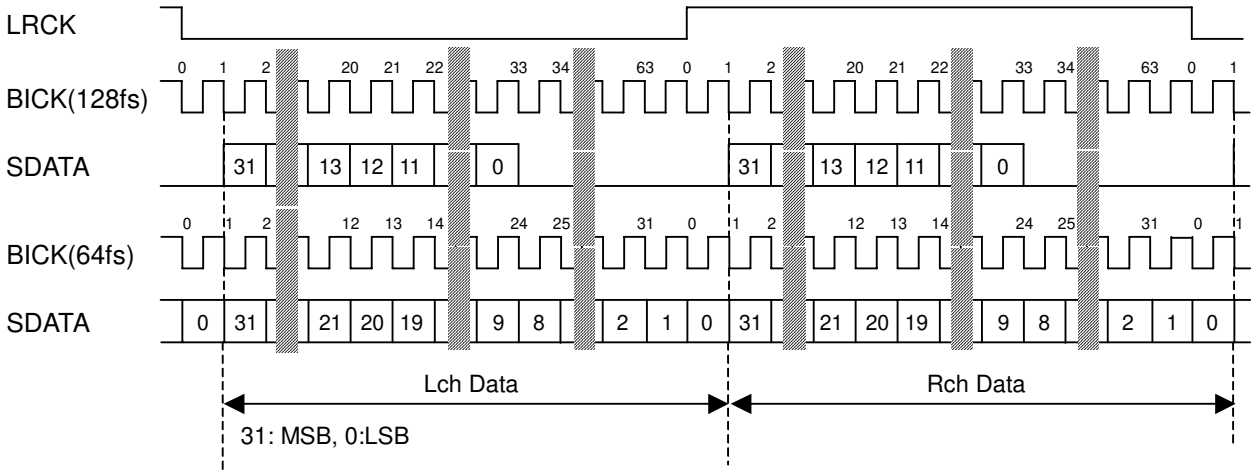


Figure 7. Mode 7 Timing

[2] DSD Mode

In case of DSD mode, DIF2-0 pins and DIF2-0 bits are ignored. The frequency of DCLK is fixed to 64fs. DCKB bit can invert the polarity of DCLK.

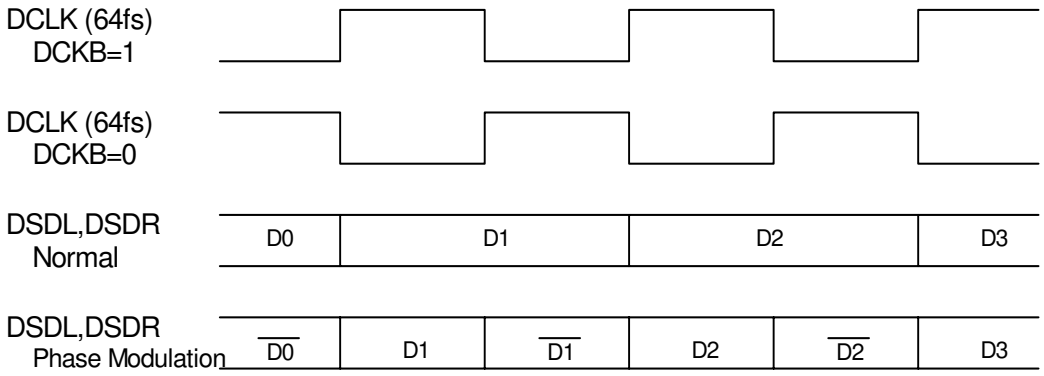


Figure 8. DSD Mode Timing

[3] External Digital Filter Mode (EX DF I/F Mode)

DW indicates the number of BCK in one WCK cycle. The audio data is input by MCLK, BCK and WCK from the DINL and DINR pins. Three formats are available (Table 16) by DIF2-0 bits setting. The data is latched on the rising edge of BCK. The BCK and MCLK clocks must be the same frequency and must not burst. BCK and MCLK frequencies for each sampling speed are shown in Table 15.

Sampling Speed[kHz]	MCLK&BCK [MHz]						WCK	ECS
	128fs	192fs	256fs	384fs	512fs	768fs		
44.1(30~54)	N/A	N/A	N/A	N/A	22.5792	33.8688	16fs	0
					32	48	DW	
44.1(30~54)	N/A	N/A	11.2896	16.9344	N/A	33.8688	8fs	1
			32	48		96	DW	
96(54~108)	N/A	N/A	24.576	36.864	N/A	N/A	8fs	0
			32	48			DW	
96(54~108)	12.288	18.432	N/A	36.864	N/A	N/A	4fs	1
	32	48		96			DW	
192(108~216)	24.576	36.864	N/A	N/A	N/A	N/A	4fs	0
	32	48					DW	
192(108~216)	N/A	36.864	N/A	N/A	N/A	N/A	2fs	1
		96					DW	

(default)

Table 15. System Clock Example (EX DF I/F mode) (N/A: Not available)

Mode	DIF2	DIF1	DIF0	Input Format	
0	0	0	0	16bit LSB justified	
1	0	0	1	N/A	
2	0	1	0	N/A	
3	0	1	1	N/A	
4	1	0	0	24bit LSB justified	
5	1	0	1	32bit LSB justified	(default)
6	1	1	0	N/A	
7	1	1	1	N/A	

Table 16. Audio Interface Format (EX DF I/F mode) (N/A: Not available)

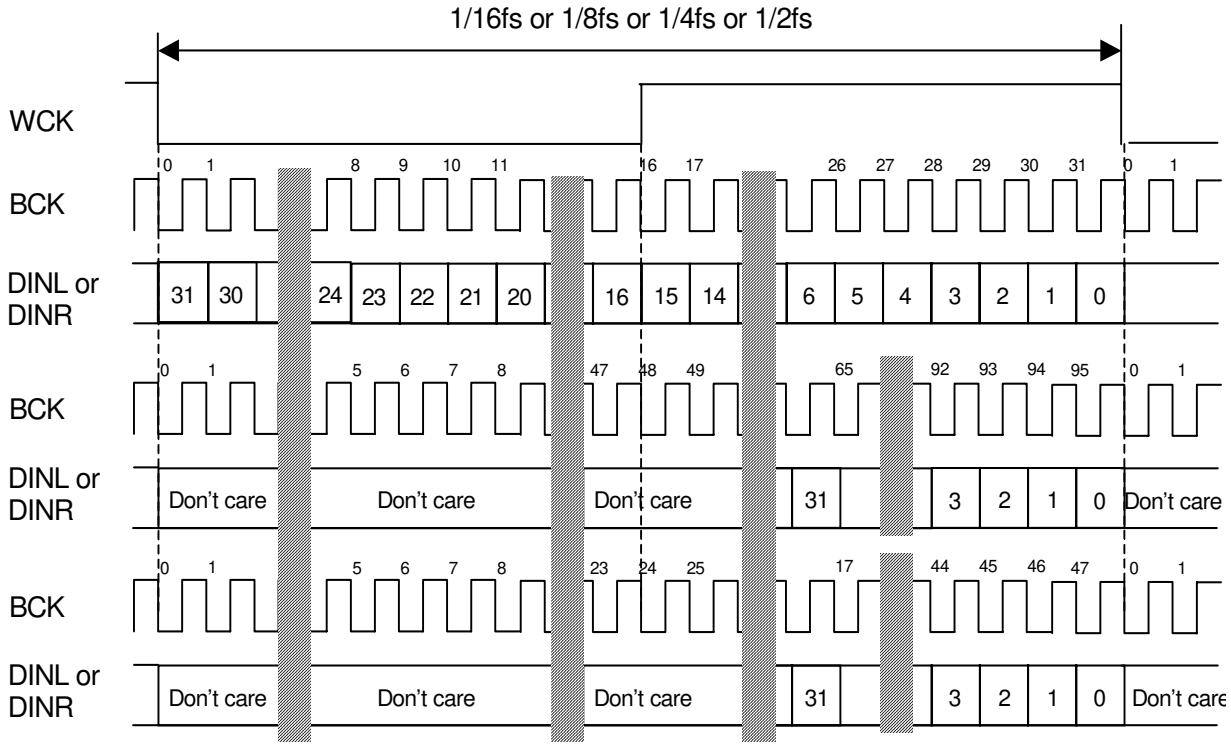


Figure 9. EX DF I/F Mode Timing