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AK4490EN

Premium 32-Bit 2ch DAC

1. General Description

The AK4490EN is a new generation Premium 32-bit 2ch DAC with new technologies, achieving industry's leading level low distortion characteristics and wide dynamic range. The AK4490EN integrates a newly developed switched capacitor filter "OSR Doubler", making it capable of supporting wide range signals and achieving low out-of-band noise while realizing low power consumption. Moreover, the AK4490EN has five types of 32-bit digital filters, realizing simple and flexible sound tuning in wide range of applications. The AK4490EN accepts up to 768kHz PCM data and 11.2MHz DSD data, ideal for a high-resolution audio source playback that are becoming widespread in network audios and USB-DACs.

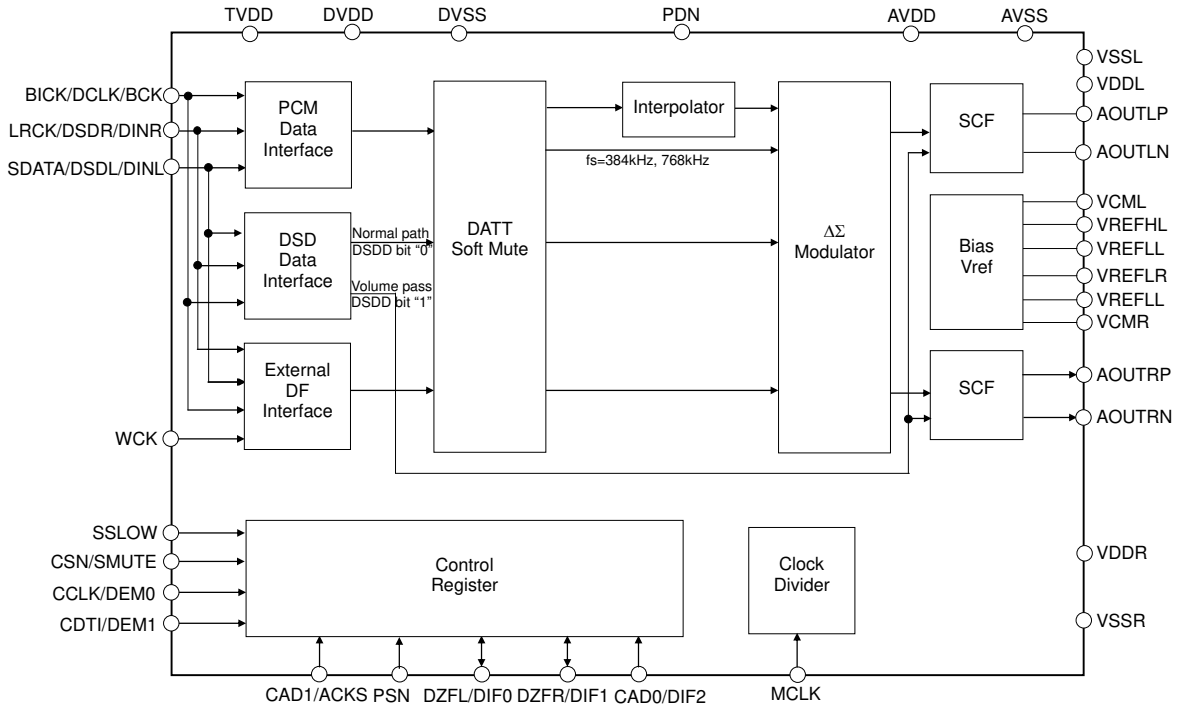
Application: AV Receivers, CD/SACD player, Network Audios, USB DACs, USB Headphones, Sound Plates/Bars, Measurement Equipment, Control Systems, Public Audios (PA), Smart Cellular Phones, IC-Recorders, Bluetooth Headphones, HD Audio/Voice Conference Systems

2. Features

- **256x Over sampling**
- **Sampling Rate: 30kHz ~ 768kHz**
- **32-bit 8x Digital Filter**
  - **Ripple: ±0.005dB, Attenuation: 100dB**
  - **Short Delay Sharp Roll-off, GD=6.25/fs**
  - **Short Delay Slow Roll-off, GD=5.3/fs**
  - **Sharp Roll-off**
  - **Slow Roll-off**
  - **Super Slow Roll-off**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **2.8MHz, 5.6MHz and 11.2MHz DSD Input Support**
  - **Filter (fc=50kHz, fc=150kHz, 2.8MHz mode)**
- **Digital De-emphasis for 32, 44.1, 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (255 levels and 0.5dB step + Mute)**
- **Mono Mode**
- **External Digital Filter Mode**
- **THD+N: -112dB**
- **DR, S/N: 120dB (Mono mode: 123dB)**
- **I/F Format: 24/32bit MSB justified, 16/20/24/32bit LSB justified, I^2S, DSD**
- **Master Clock:**
  - **30kHz ~ 32kHz: 256fs, 384fs, 512fs, 768fs, 1024fs or 1152fs**
  - **30kHz ~ 54kHz: 256fs, 384fs, 512fs or 768fs**
  - **30kHz ~ 96kHz: 256fs, 384fs or 512fs**
  - **30kHz ~ 108kHz: 256fs or 384fs**
  - **108kHz ~ 192kHz: 128fs, 192fs or 256fs**
  - **108kHz ~ 216kHz: 128fs or 192fs**
  - **384kHz: 32fs, 48fs, 64fs or 96fs**
  - **768kHz: 16fs, 32fs, 48fs or 64fs**
- **Power Supply: DVDD=AVDD=3.0 ~ 3.6V, TVDD=1.6V ~ DVDD, VDDL/R= VREFHL/VREFHR=4.75 ~ 5.25V**
- **Digital Input Level: CMOS**
- **Package: 48-pin QFN**

3. Table of Contents

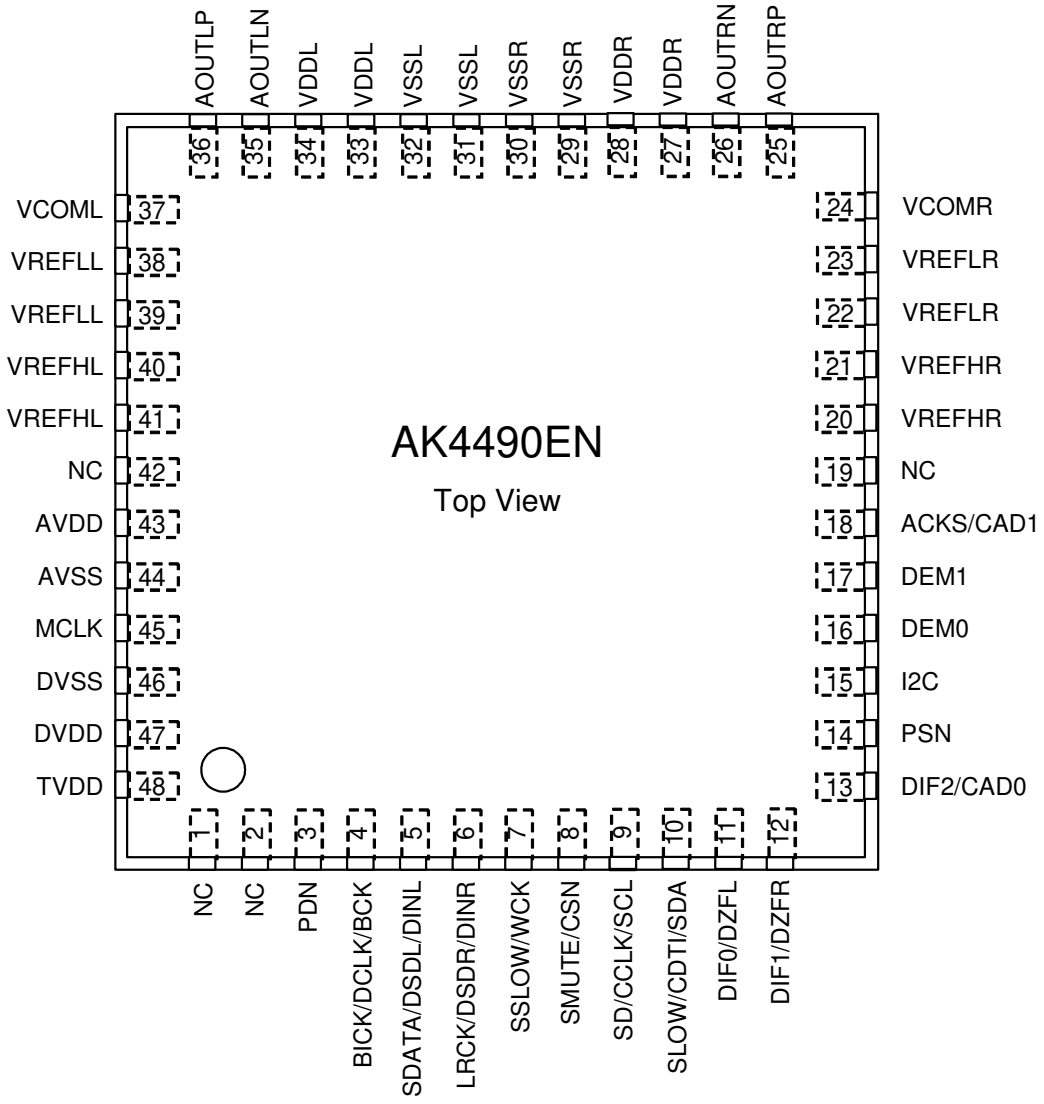
4. Block Diagram



Block Diagram

5. Pin Configurations and Functions

■ Pin Layout



■ Pin Functions

No.	Pin Name	I/O	Function
1	NC	-	No internal bonding. Connect to GND.
2	NC	-	No internal bonding. Connect to GND.
3	PDN	I	Power-Down Mode Pin When at "L", the AK4490EN is in power-down mode and is held in reset. The AK4490EN must always be reset upon power-up.
4	BICK	I	Audio Serial Data Clock Pin in PCM Mode
	DCLK	I	DSD Clock Pin in DSD Mode
	BCK	I	Audio Serial Data Clock Pin in External DF Mode
5	SDATA	I	Audio Serial Data Input Pin in PCM Mode
	DSDL	I	DSD Lch Data Input Pin in DSD Mode
	DINL	I	Lch Audio Serial Data Input Pin in External DF Mode
6	LRCK	I	L/R Clock Pin in PCM Mode
	DSDR	I	DSD Rch Data Input Pin in DSD Mode in Serial Control Mode
	DINR	I	Rch Audio Serial Data Input Pin in External DF Mode
7	SSLOW	I	Digital Filter Setting Pin in Parallel Control Mode (PSN="H")
	WCK	I	Word Clock input pin in External DF Mode (PSN="L")
8	SMUTE	I	Soft Mute Pin in Parallel Control Mode (PSN="H") When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.
	CSN	I	Chip Select Pin in Serial Control Mode (PSN="L", I2C="L") When this pin is PSN="L", I2C="H", it should be connected to TVDD or DVSS.
9	SD	I	Digital Filter Setting Pin in Parallel Control Mode (PSN="H")
	CCLK	I	Control Data Clock Pin in Serial Control Mode (PSN="L", I2C="L")
	SCL	I	Control Data Clock Pin in Serial Control Mode (PSN="L", I2C="H")
10	SLOW	I	Digital Filter Setting Pin in Parallel Control Mode (PSN="H")
	CDTI	I	Control Data Input Pin in Serial Control Mode (PSN="L", I2C="L")
	SDA	I/O	Control Data Input Pin in Serial Control Mode (PSN="L", I2C="H")
11	DIF0	I	Digital Input Format 0 Pin in PCM Mode (PSN="H")
	DZFL	O	Lch Zero Input Detect Pin in Serial Control Mode (PSN="L")
12	DIF1	I	Digital Input Format 1 Pin in PCM Mode (PSN="H")
	DZFR	O	Rch Zero Input Detect Pin in Serial Control Mode (PSN="L")
13	DIF2	I	Digital Input Format 2 Pin in PCM Mode (PSN="H")
	CAD0	I	Chip Address 0 Pin in Serial Control Mode (PSN="L")
14	PSN	I	Parallel or Serial Select Pin (Internal pull-up pin) "L": Serial Control Mode, "H": Parallel Control Mode
15	I2C	I	I2C mode select pin in Serial mode (Internal pull-down pin) "L": 3 Wire Serial Mode, "H": I2C-Bus Mode
16	DEM0	I	De-emphasis Enable 0 Pin in Parallel Control Mode (PSN="H") (Internal pull-up pin)

Note 1. All input pins except internal pull-up/down pins must not be left floating.

17	DEM1	I	De-emphasis Enable 1 Pin in Parallel Control Mode (PSN="H") (Internal pull-down pin)
18	ACKS	I	Master Clock Auto Setting Mode Pin in Parallel Mode (PSN="H") "L": Manual Setting Mode, "H": Auto Setting Mode (Internal pull-down pin)
	CAD1	I	Chip Address 1 Pin in Serial Control Mode (PSN="L") (Internal pull-down pin)
19	NC	-	No internal bonding. Connect to GND.
20	VREFHR	I	Rch High Level Voltage Reference Input Pin
21	VREFHR	I	Rch High Level Voltage Reference Input Pin
22	VREFLR	I	Rch Low Level Voltage Reference Input Pin
23	VREFLR	I	Rch Low Level Voltage Reference Input Pin
24	VCOMR	-	Right channel Common Voltage Pin, Normally connected to VSS with a 10μF electrolytic cap.
25	AOUTRP	O	Rch Positive Analog Output Pin
26	AOUTRN	O	Rch Negative Analog Output Pin
27	VDDR	-	Rch Analog Power Supply Pin, 4.75 ~ 5.25V
28	VDDR	-	Rch Analog Power Supply Pin, 4.75 ~ 5.25V
29	VSSR	-	Ground Pin
30	VSSR	-	Ground Pin
31	VSSL	-	Ground Pin
32	VSSL	-	Ground Pin
33	VDDL	-	Lch Analog Power Supply Pin, 4.75 ~ 5.25V
34	VDDL	-	Lch Analog Power Supply Pin, 4.75 ~ 5.25V
35	AOUTLN	O	Lch Negative Analog Output Pin
36	AOUTLP	O	Lch Positive Analog Output Pin
37	VCOML	-	Left channel Common Voltage Pin, Normally connected to VSS with a 10μF electrolytic cap.
38	VREFLL	I	Lch Low Level Voltage Reference Input Pin
39	VREFLL	I	Lch Low Level Voltage Reference Input Pin
40	VREFHL	I	Lch High Level Voltage Reference Input Pin
41	VREFHL	I	Lch High Level Voltage Reference Input Pin
42	NC	-	No internal bonding. Connect to GND.
43	AVDD	-	Analog Power Supply Pin, 3.0 ~ 3.6V
44	AVSS	-	Ground Pin
45	MCLK	I	Master Clock Input Pin
46	DVSS	-	Ground Pin
47	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V
48	TVDD	I	Input Buffer Power Supply Pin, 1.6V ~ DVDD
	Exposed Pad	-	The exposed pad on the bottom surface of the package must be connected to the ground.

Note 1. All input pins except internal pull-up/down pins must not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

(1) Parallel Mode (PCM Mode only)

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	I2C	This pin must be connected to DVSS or open.

(2) Serial Mode

1. PCM Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	DEM1	This pin must be connected to DVSS or open.
	DEM0	This pin must be connected to TVDD or open.
	SMUTE/CSN	This pin must be connected to TVDD or DVSS, when this pin is I2C="H".
	DZFL, DZFR	These pins must be open.

2. DSD Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	DEM1	This pin must be connected to DVSS or open.
	DEM0	This pin must be connected to TVDD or open.
	SMUTE/CSN	This pin must be connected to TVDD or DVSS, when this pin is I2C="H".
	DZFL, DZFR	These pins must be open.

3. EXDF Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	DEM1	This pin must be connected to DVSS or open.
	DEM0	This pin must be connected to TVDD or open.
	SMUTE/CSN	This pin must be connected to TVDD or DVSS, when this pin is I2C="H".
	DZFL, DZFR	These pins must be open.

pull-up pin List

pull-up pin	14, 16

pull-down pin List

pull-down pin	15, 17, 18

6. Absolute Maximum Ratings

(AVSS=DVSS=VSSL=VSSR=VREFLL=VREFLR=0V; Note 2)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Analog	AVDD	−0.3	4.6	V
	Analog	VDDL/R	−0.3	6.0	V
	Digital	DVDD	−0.3	4.6	V
	Input Buffer	TVDD	−0.3	4.6	V
	|AVSS − DVSS| (Note 3)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	−0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 2. All voltages with respect to ground.
Note 3. AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane.
Note 4. Connect at least 0.1μF or more decoupling capacitors between VDDL/VDDR and VSSL/VSSR to suppress affections by a static electricity noise or an over voltage (includes over shooting) that exceeds absolute maximum ratings.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS=VSSL=VSSR=VREFLL=VREFLR=0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 5)	Analog	AVDD	3.0	3.3	3.6	V
	Analog	VDDL/R	4.75	5.0	5.25	V
	Digital	DVDD	3.0	3.3	3.6	V
	Input Buffer	TVDD	1.6	1.8	DVDD	
Voltage Reference (Note 6)	"H" voltage reference	VREFHL/R	VDDL/R−0.5	-	VDDL/R	V
	"L" voltage reference	VREFLL/R		VSSL/R	-	V

Note 2. All voltages with respect to ground.
Note 5. Each power-up/down sequence is shown below.

<Power-Up>
1. PDN pin = "L"
2. TVDD (1.8V) power-up
3. AVDD, DVDD (3V) power-up
4. VREFHL/R and VDDL/R (5V) power-up
5. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

otherwise power up the 1.8V power supply, the 3.3V power supplies and the 5V power supplies at the same time.

<Power-down>
1. PDN pin = "L"
2. VREFHL/R and VDDL/R (5V) power-down
3. AVDD, DVDD (3V) power-down
4. TVDD (1.8V) power-down

Note 6. The analog output voltage scales with the voltage of (VREFH − VREFL).
AOUT (typ.@0dB) = (AOUT+) − (AOUT−) = ±2.8Vpp × (VREFHL/R − VREFLL/R)/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

■ Analog Characteristics

(Ta=25°C; AVDD=DVDD=3.3V; TVDD=1.8V; AVSS=DVSS=VSSL/R=0V; VREFHL/R=VDDL/R=5V, VREFLL/R= VSSL/R=0V; Input data = 24bit; $R_L \geq 1k\Omega$; BICK=64fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: Figure 41; unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Resolution			-	-	32	Bits
Dynamic Characteristics (Note 7)						
THD+N	fs=44.1kHz BW=20kHz	0dBFS −60dBFS	- -	-112 -57	-105 -49	dB dB
	fs=96kHz BW=40kHz	0dBFS −60dBFS	- -	-109 -54	-100 -44	dB dB
	fs=192kHz BW=40kHz BW=80kHz	0dBFS −60dBFS −60dBFS		-106 -54 -51	-100 -44 -41	dB dB dB
Dynamic Range (−60dBFS with A-weighted) (Note 8)			115	120	-	dB
S/N (A-weighted) (Note 9)			115	120	-	dB
S/N (Mono mode, A-weighted)			118	123	-	dB
Interchannel Isolation (1kHz)			110	120	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.15	0.3	dB
Gain Drift (Note 10)			-	-	20	ppm/°C
Output Voltage (Note 11)			±2.65	±2.8	±2.95	Vpp
Load Capacitance			-	-	25	pF
Load Resistance (Note 12)			1	-	-	kΩ
Power Supplies						
Power Supply Current						
	Normal operation (PDN pin = “H”)					
	VDDL/R			22	32	mA
	AVDD			0.6	1.2	mA
	TVDD		-	0.5	1	mA
	DVDD (fs= 44.1kHz)		-	10	14	mA
	DVDD (fs= 96kHz)		-	15	20	mA
	DVDD (fs = 192kHz)		-	17	23	mA
	Power down (PDN pin = “L”) (Note 13)					
	AVDD+VDDL/R+DVDD+TVDD		-	0	10	μA

Note 7. Measured by Audio Precision, System Two. Averaging mode. Refer to the evaluation board manual.

Note 8. Figure 41 External LPF Circuit Example 2. 101dB for 16-bit data and 118dB for 20-bit data.

Note 9. Figure 41 External LPF Circuit Example 2. S/N does not depend on input data size.

Note 10. The voltage on (VREFH − VREFL) is held +5V externally.

Note 11. Full-scale voltage(0dB). Output voltage scales with the voltage of (VREFHL/R − VREFLL/R).
AOUT (typ.@0dB) = (AOUT+) − (AOUT−) = ±2.8Vpp × (VREFHL/R − VREFLL/R)/5.

Note 12. Regarding Load Resistance, AC load is 1kΩ (min) with a DC cut capacitor (Figure 41). DC load is 1.5k ohm (min) without a DC cut capacitor (Figure 40). The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore the capacitive load must be minimized.

Note 13. In the power down mode. The PSN pin = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.

■ Sharp Roll-Off Filter Characteristics (fs=44.1kHz)

(Ta=25°C; AVDD=DVDD=3.0~3.6V, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; Normal Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 14)	±0.01dB −6.0dB	PB	0 -	 22.05	20.0 -	kHz kHz
Stopband (Note 14)		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 15)		GD	-	29.4	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-	+0.1/-0.2	-	dB

■ Sharp Roll-Off Filter Characteristics (fs=96kHz)

Ta=25°C; AVDD=DVDD=3.0~3.6V, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; Double Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 14)	±0.01dB −6.0dB	PB	0 -	 48.0	43.5 -	kHz kHz
Stopband (Note 14)		SB	52.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 15)		GD	-	28.8	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-	+0.1/-0.6	-	dB

■ Sharp Roll-Off Filter Characteristics (fs=192kHz)

(Ta=25°C; AVDD=DVDD=3.0~3.6V, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; Quad Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 14)	±0.01dB −6.0dB	PB	0 -	 96.0	87.0 -	kHz kHz
Stopband (Note 14)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	92			dB
Group Delay (Note 15)		GD	-	28.8	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-	+0.1/-0.2	-	dB

Note 14. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

Note 15. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32 bit data of both channels to the output of analog signal.

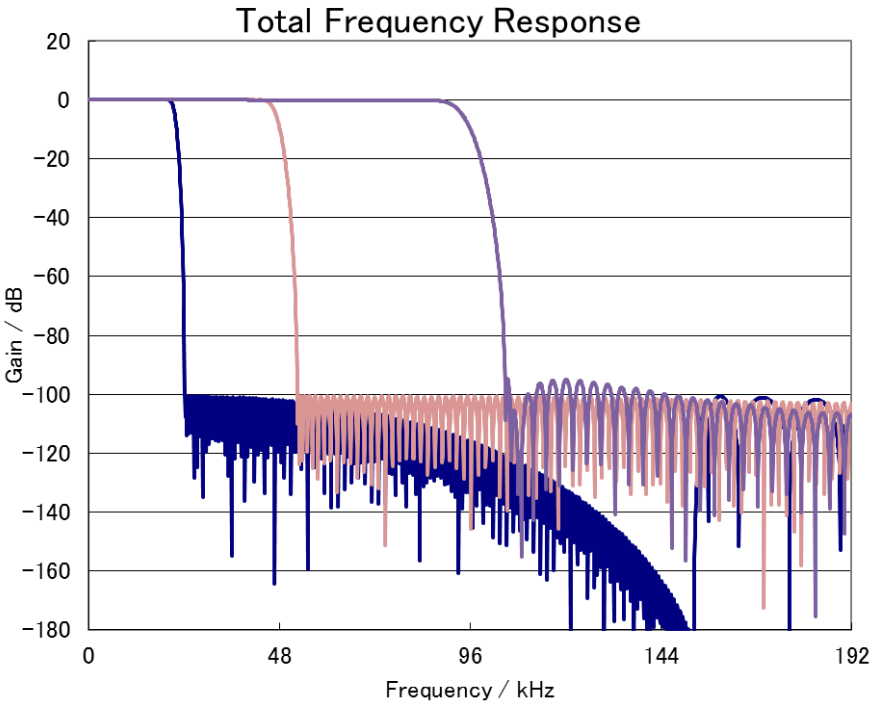


Figure 1. Sharp Roll-off Filter Frequency Response

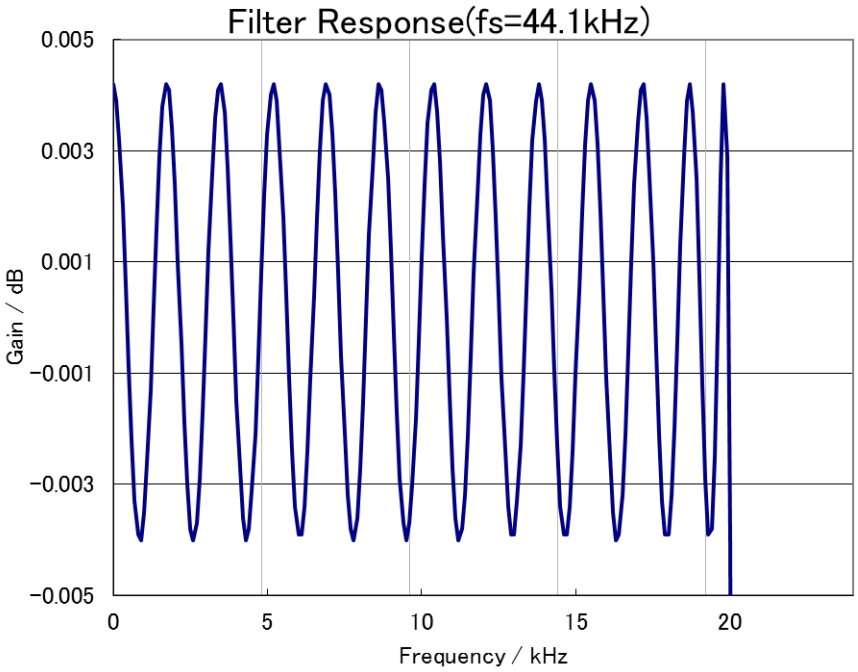


Figure 2. Sharp Roll-off Filter Passband Ripple

■ Short Delay Sharp Roll-Off Filter Characteristics (fs=44.1kHz)

(Ta=25°C; AVDD=DVDD=3.0~3.6V, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; Normal Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 14)	±0.01dB −6.0dB	PB	0 -	 22.05	20.0 -	kHz kHz
Stopband (Note 14)		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 15)		GD	-	6.25	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-	+0.1/-0.2	-	dB

■ Short Delay Sharp Roll-Off Filter Characteristics (fs=96kHz)

(Ta=25°C; AVDD=DVDD=3.0~3.6V, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; Double Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 14)	±0.01dB −6.0dB	PB	0 -	 48.0	43.5 -	kHz kHz
Stopband (Note 14)		SB	52.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 15)		GD	-	5.63	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-	+0.1/-0.6	-	dB

■ Short Delay Sharp Roll-Off Filter Characteristics (fs=192kHz)

(Ta=25°C; AVDD=DVDD=3.0~3.6V, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; Quad Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 14)	±0.01dB −6.0dB	PB	0 -	 96.0	87.0 -	kHz kHz
Stopband (Note 14)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	92			dB
Group Delay (Note 15)		GD	-	5.63	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-	+0.1/-2.0	-	dB

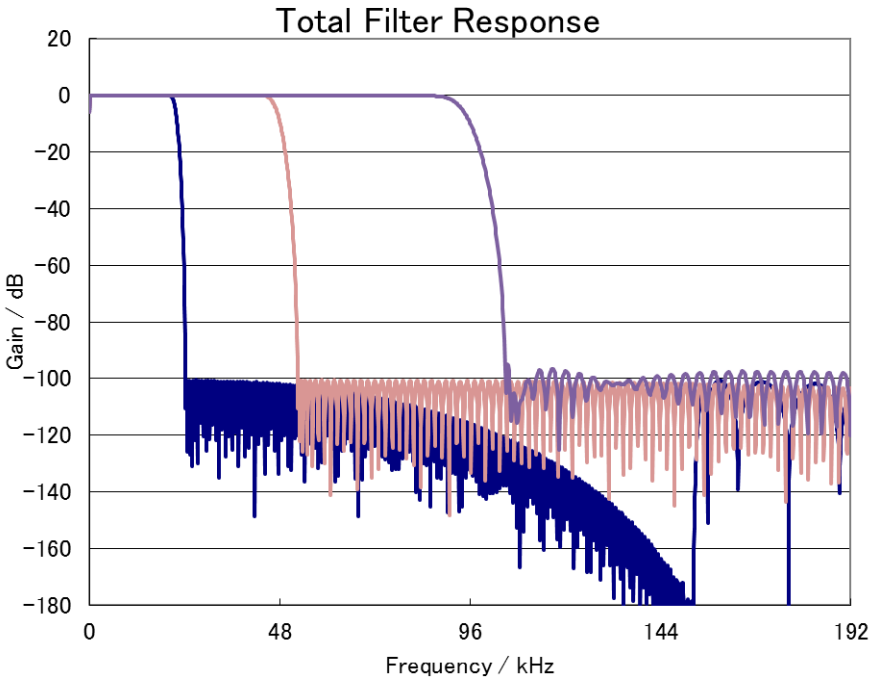


Figure 3. Short delay Sharp Roll-off Filter Frequency Response

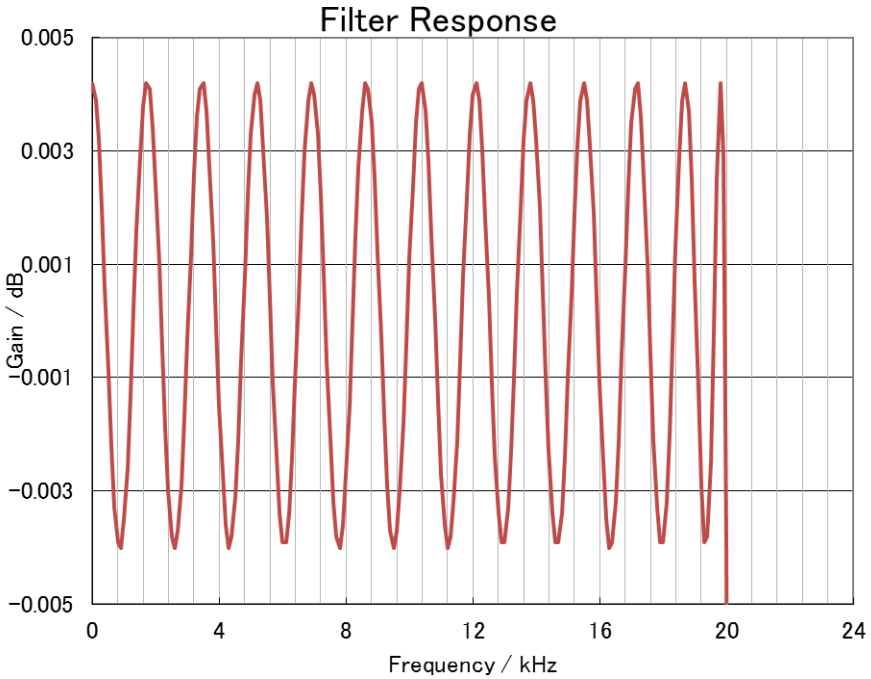


Figure 4. Short delay Sharp Roll-off Filter Passband Ripple

■ Slow Roll-Off Filter Characteristics (fs=44.1kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; Normal Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 16)	±0.01dB −6.0dB	PB	0 -	 18.2	4.4 -	kHz kHz
Stopband (Note 16)		SB	39.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	94			dB
Group Delay (Note 17)		GD	-	6.63	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-	+0.1/-4.5	-	dB

■ Slow Roll-Off Filter Characteristics (fs=96kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; Double Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 16)	±0.01dB −6.0dB	PB	0 -	 45.6	18.1 -	kHz kHz
Stopband (Note 16)		SB	85.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 17)		GD	-	6.00	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-	+0.1/-4.0	-	dB

■ Slow Roll-Off Filter Characteristics (fs=192kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; Quad Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 16)	±0.01dB −6.0dB	PB	0 -	 90.4	32.9 -	kHz kHz
Stopband (Note 16)		SB	171			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	97			dB
Group Delay (Note 17)		GD	-	6.00	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-	+0.1/-5.5	-	dB

Note 16. The passband and stopband frequencies scale with fs. For example, PB=0.1836×fs (@±0.01dB), SB=0.8889×fs.

Note 17. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32 bit data of both channels to the output of analog signal.

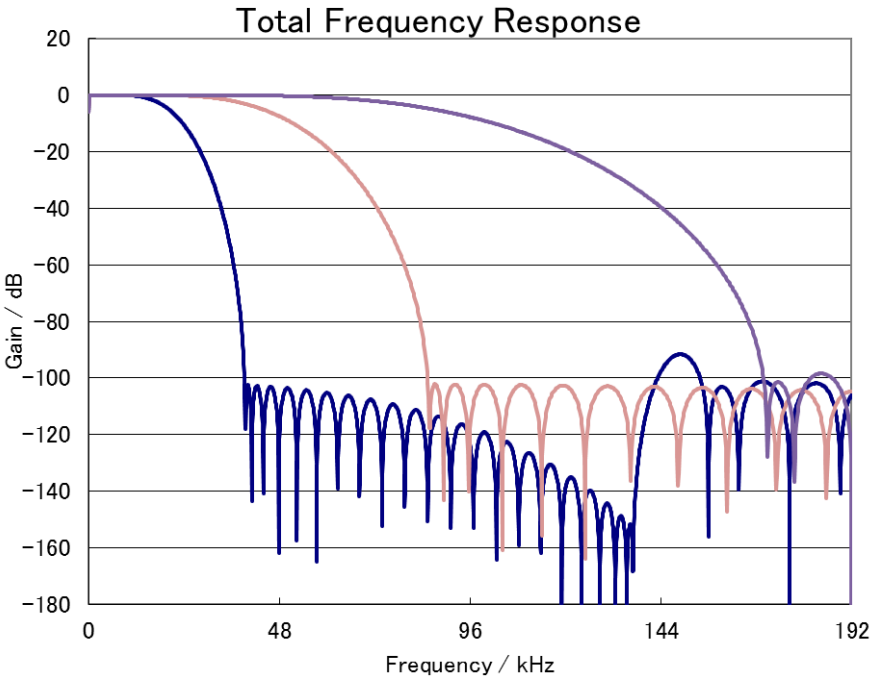


Figure 5. Slow Roll-off Filter Frequency Response

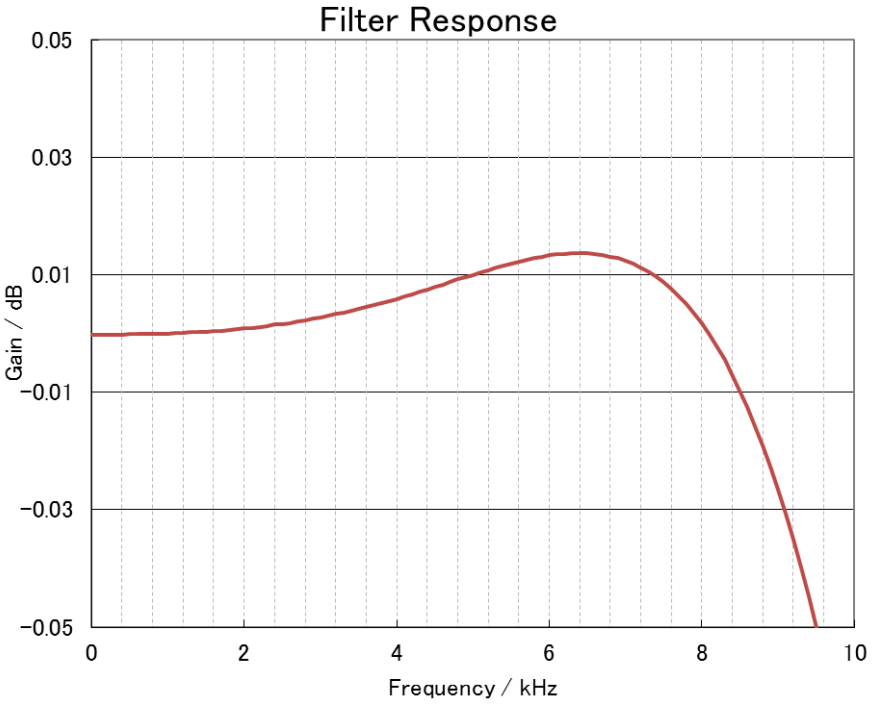


Figure 6. Slow Roll-off Filter Passband Ripple

■ Short Delay Slow Roll-Off Filter Characteristics (fs=44.1kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, TVDD=1.6V ~ DVDD , VREFHL/R=VDDL/R=4.75 ~ 5.25V; Normal Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 18)	±0.01dB −6.0dB	PB	0 -	 18.2	4.4 -	kHz kHz
Stopband (Note 18)		SB	39.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	94			dB
Group Delay (Note 19)		GD	-	5.3	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-	+0.1/-4.5	-	dB

■ Short Delay Slow Roll-Off Filter Characteristics (fs=96kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; Double Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 18)	±0.01dB −6.0dB	PB	0 -	 45.6	18.1 -	kHz kHz
Stopband (Note 18)		SB	85.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 19)		GD	-	4.68	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-	+0.1/-0.4	-	dB

■ Short Delay Slow Roll-Off Filter Characteristics (fs=192kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; Quad Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Passband (Note 18)	±0.01dB −6.0dB	PB	0 -	 96.0	32.9 -	kHz kHz
Stopband (Note 18)		SB	170			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	97			dB
Group Delay (Note 19)		GD	-	4.68	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-	+0.1/-5.5	-	dB

Note 18. The passband and stopband frequencies scale with fs. For example, PB=0.1836×fs (@±0.01dB), SB=0.8866×fs.

Note 19. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32 bit data of both channels to the output of analog signal.

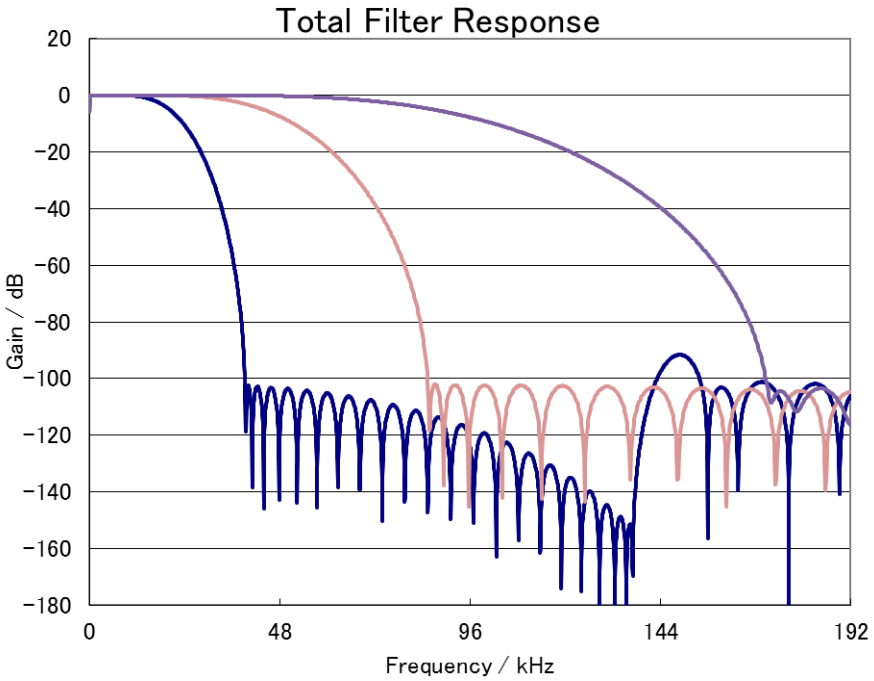


Figure 7. Short Delay Slow Roll-off Filter Frequency Response

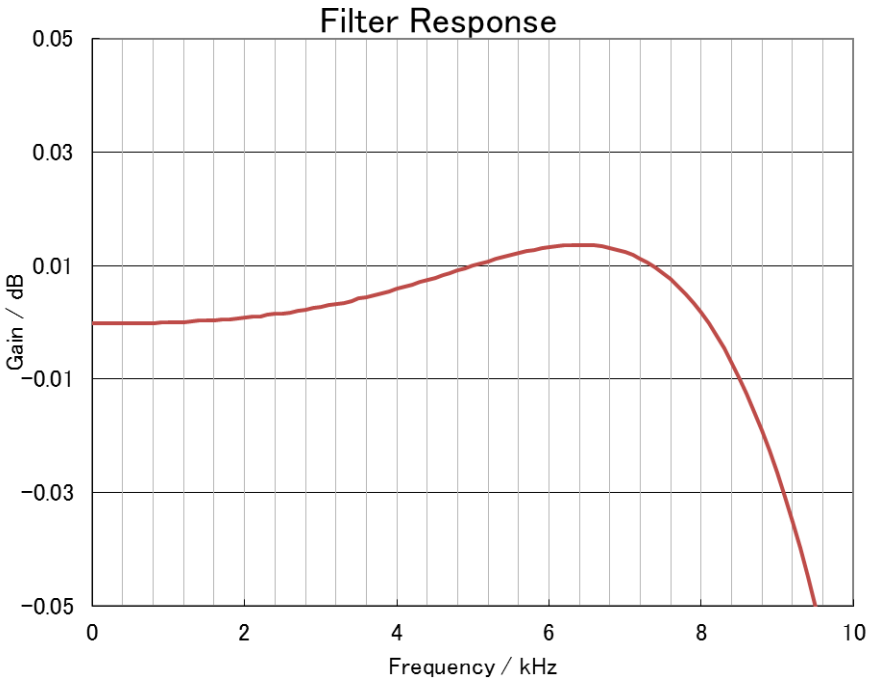


Figure 8. Short Delay Slow Roll-off Filter Passband Ripple

■ DSD Mode Characteristics

(Ta=-40~85°C; AVDD=DVDD=3.0 ~ 3.6, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; fs=44.1kHz; DP bit="1", DSDF bit="0")

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response					
Frequency Response (Note 21)	20kHz	-	-0.4	-	dB
	50kHz	-	-2.8	-	dB
	100kHz	-	-15.5	-	dB

(Ta=-40~85°C; AVDD=DVDD=3.0 ~ 3.6, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V; fs=44.1kHz; DP bit="1", DSDF bit="1", DSDD bit="1")

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response					
Frequency Response (Note 21)	20kHz	-	-0.05	-	dB
	50kHz	-	-0.29	-	dB
	100kHz	-	-1.16	-	dB
	150kHz	-	-2.8	-	dB

Note 20. The peak level of DSD signal should be in the range of 25% ~ 75% duty according to the SACD format book (Scarlet Book).

Note 21. The output level is assumed as 0dB when a 1kHz 25% ~ 75% duty sine wave is input.

■ DC Characteristics

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
TVDD=1.6 ~ 3.0V					
High-Level Input Voltage	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	20%TVDD	V
TVDD=3.0 ~ DVDD					
High-Level Input Voltage	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD	V
High-Level Output Voltage (DZFL/R pins: Iout=-100μA)	VOH	DVDD−0.5	-	-	V
Low-Level Output Voltage					
(except SDA pin : Iout= 100μA)	VOL	-	-	0.5	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout= 3mA)	VOL	-	-	0.4	V
(SDA pin, 1.6V ≤ TVDD ≤ 2.0V: Iout= 3mA)	VOL	-		20%DVDD	V
Input Leakage Current (Note 22)	Iin	-	-	±10	μA

Note 22. The DEM1, I2C and ACKS/CAD1 pins have internal pull-down and DEM0 and PSN pins have internal pull-up devices, nominally 100kΩ. Therefore the DEM1, I2C, ACKS/CAD1, DEM0 and PSN pins are not included.

■ Switching Characteristics

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, TVDD=1.6V ~ DVDD, VREFHL/R=VDDL/R=4.75 ~ 5.25V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
Frequency	fCLK	7.7		49.152	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency (Note 23)					
1152fs, 512fs or 768fs	fsn	30		54	kHz
256fs or 384fs	fsd	54		108	kHz
128fs or 192fs	fsq	108		216	kHz
64fs	fsoc		384		kHz
64fs	fssd		768		kHz
Duty Cycle	Duty	45		55	%
PCM Audio Interface Timing					
BICK Period					
1152fs, 512fs or 768fs	tBCK	1/128fsn			ns
256fs or 384fs	tBCK	1/64fsd			ns
128fs or 192fs	tBCK	1/64fsq			ns
64fs	tBCK	1/64fso			ns
64fs	tBCK	1/64fsh			ns
BICK Pulse Width Low	tBCKL	9			ns
BICK Pulse Width High	tBCKH	9			ns
BICK "↑" to LRCK Edge (Note 24)	tBLR	5			ns
LRCK Edge to BICK "↑" (Note 24)	tLRB	5			ns
SDATA Hold Time	tSDH	5			ns
SDATA Setup Time	tSDS	5			ns
External Digital Filter Mode					
BICK Period	tB	27			ns
BCK Pulse Width Low	tBL	10			ns
BCK Pulse Width High	tBH	10			ns
BCK "↑" to WCK Edge	tBW	5			ns
WCK Edge to BCK "↑"	tWB	5			ns
WCK Pulse Width Low	tWCK	54			ns
WCK Pulse Width High	tWCH	54			ns
DATA Hold Time	tDH	5			ns
DATA Setup Time	tDS	5			ns
DSD Audio Interface Timing (64 mode, DSDSEL 1-0 bits = "00")					
DCLK Period	tDCK		1/64fs		ns
DCLK Pulse Width Low	tDCKL	160			ns
DCLK Pulse Width High	tDCKH	160			ns
DCLK Edge to DSDL/R (Note 25)	tDDD	−20		20	ns
DSD Audio Interface Timing (128 mode, DSDSEL 1-0 bits = "01")					
DCLK Period	tDCK		1/128fs		ns
DCLK Pulse Width Low	tDCKL	80			ns
DCLK Pulse Width High	tDCKH	80			ns
DCLK Edge to DSDL/R (Note 25)	tDDD	−10		10	ns

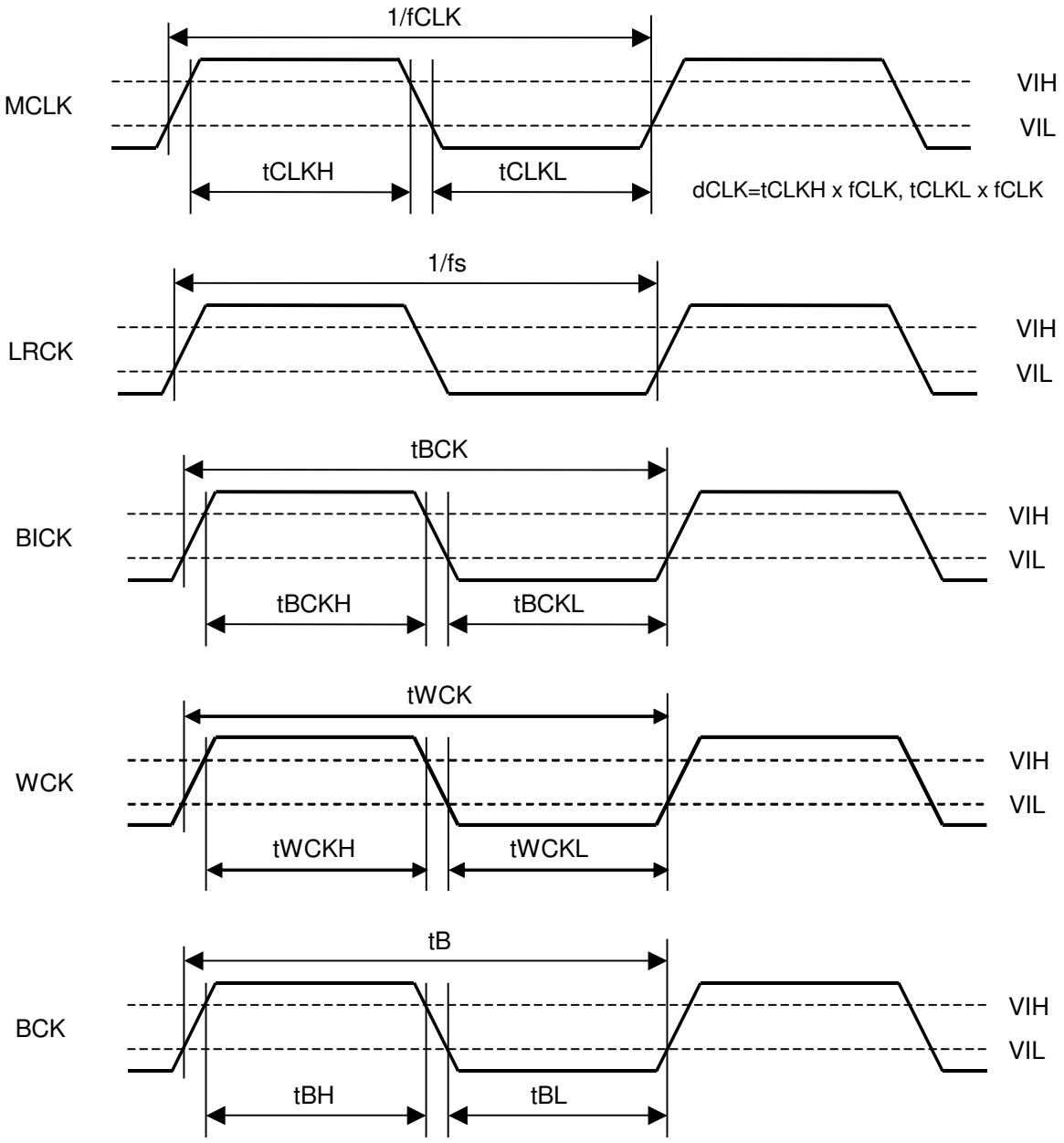
DSD Audio Interface Timing (256 mode, DSDSEL 1-0 bit = "10")					
DCLK Period	tDCK		1/256fs		ns
DCLK Pulse Width Low	tDCKL	40			ns
DCLK Pulse Width High	tDCKH	40			ns
DCLK Edge to DSDL/R (Note 25)	tDDD	–5		5	ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN High Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 26)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Reset Timing					
PDN Pulse Width (Note 27)	tPD	150			ns

Note 23. When the 1152fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK4490EN should be reset by the PDN pin or RSTN bit.
Note 24. BICK rising edge must not occur at the same time as LRCK edge.
Note 25. DSD data transmitting device must meet this time.
Note 26. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 27. The AK4490EN can be reset by bringing the PDN pin to "L".

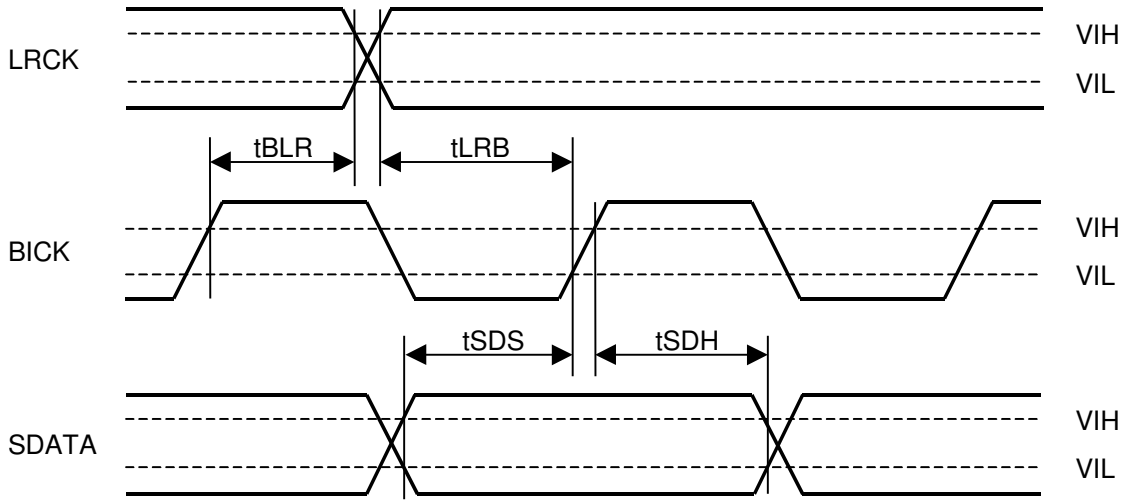
When the AK8157A is used for MCLK, Minimum Pulse Width is specified as below.

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
Frequency1 (CKSEL= "00")	fCLK		16.384		MHz
Frequency2 (CKSEL= "01")	fCLK		22.5792		MHz
Frequency3 (CKSEL= "10" / "11")	fCLK		24.576		MHz
Minimum Pulse Width	tCLKH / tCLKL	9.155			ns

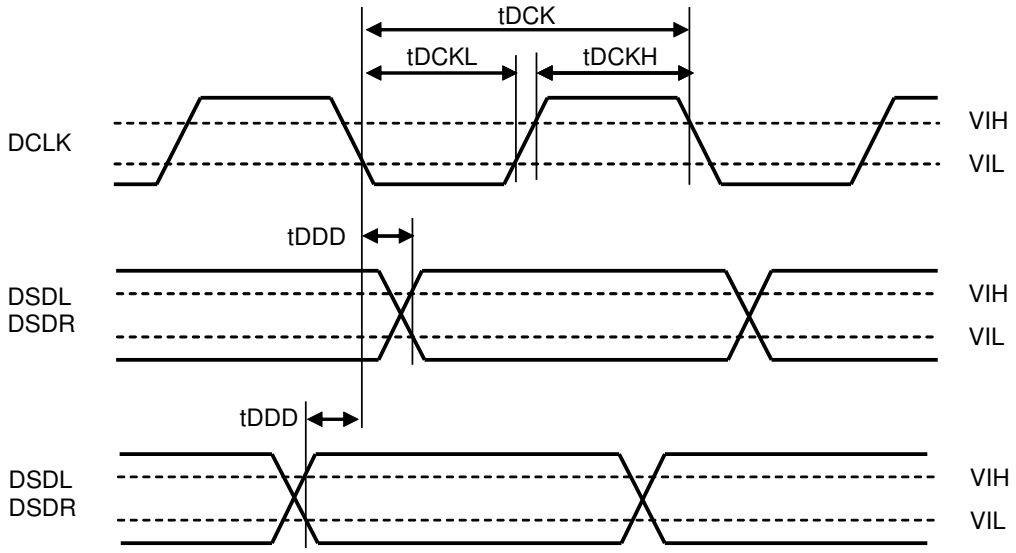
■ **Timing Diagram**



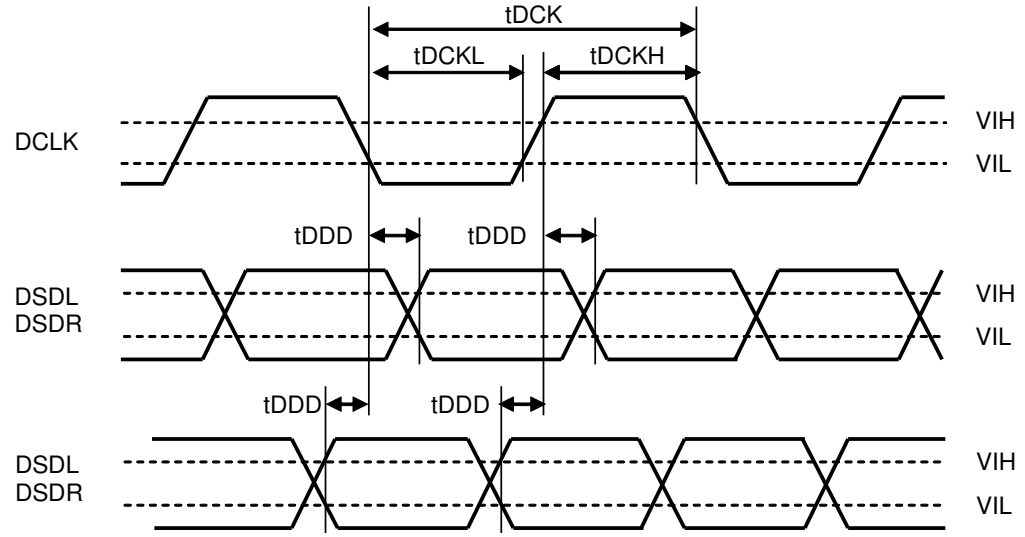
Clock Timing



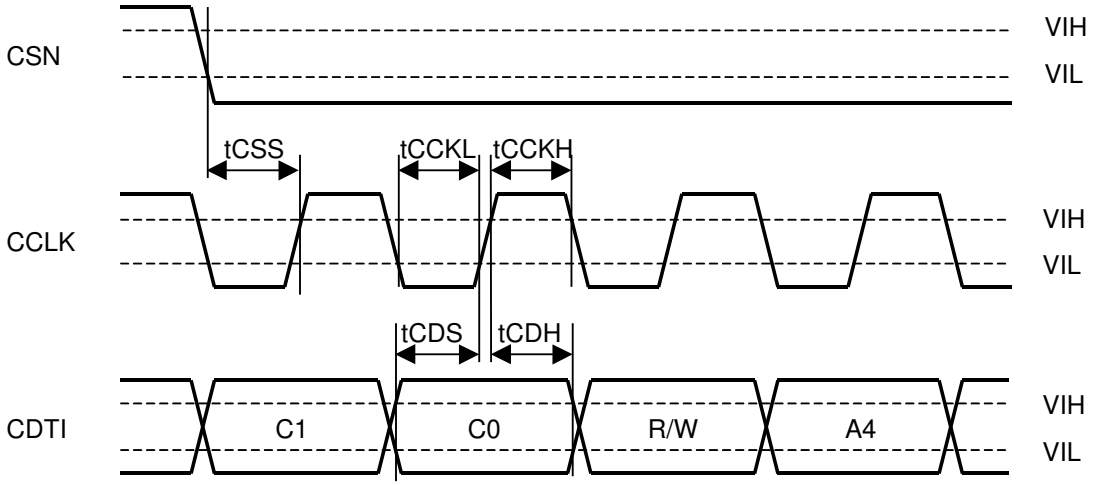
Audio Interface Timing (PCM Mode)



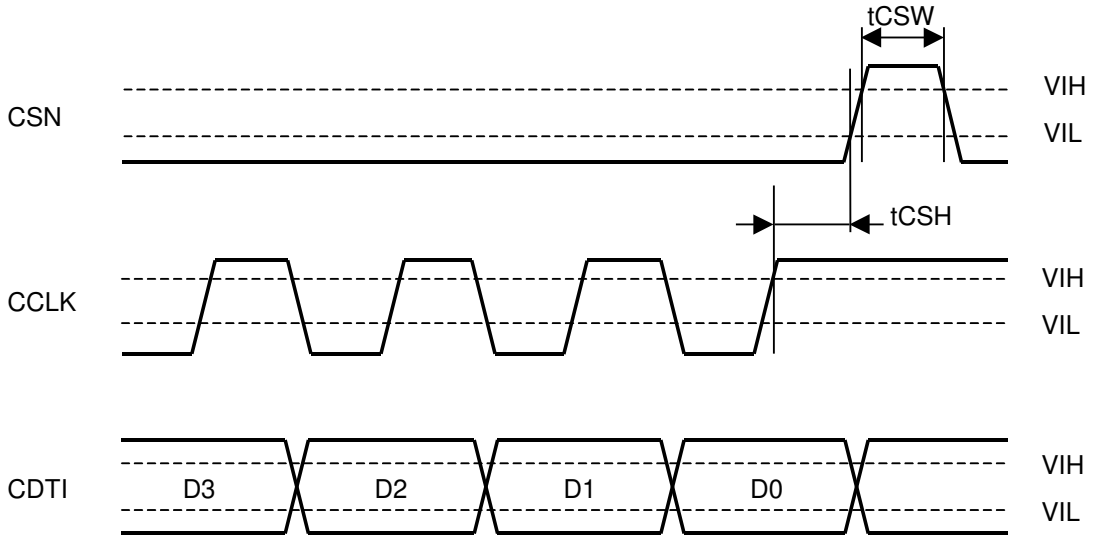
Audio Serial Interface Timing (DSD Normal Mode, DCKB bit = “0”)



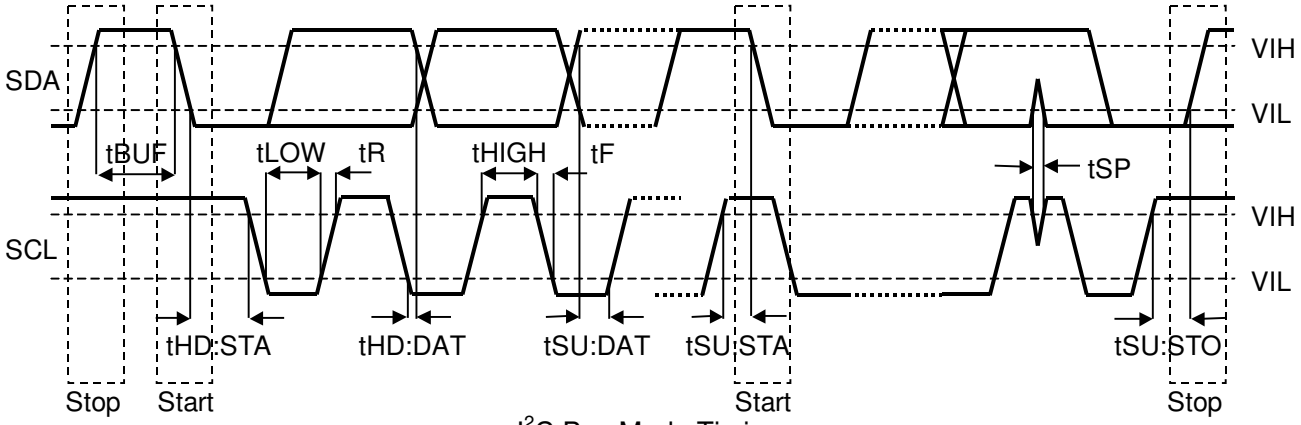
Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB bit = "0")



3 Wire Serial Mode WRITE Command Input Timing



3 Wire Serial Mode WRITE Data Input Timing



I^2C Bus Mode Timing