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AK4490

Premium 32-Bit 2ch DAC

1. General Description

AK4490 is a new generation Premium 32-bit 2ch DAC with new technologies, achieving industry's leading level low distortion characteristics and wide dynamic range. The AK4490 integrates a newly developed switched capacitor filter "OSR Doubler", making it capable of supporting wide range signals and achieving low out-of-band noise while realizing low power consumption. Moreover, the AK4490 has five types of 32-bit digital filters, realizing simple and flexible sound tuning in wide range of applications. The AK4490 accepts up to 768kHz PCM data and 11.2MHz DSD data, ideal for a high-resolution audio source playback that are becoming widespread in network audios, USB-DACs and Car Audio Systems.

Application: AV Receivers, CD/SACD player, Network Audios, USB DACs, USB Headphones, Sound Plates/Bars, Car Audios, Automotive External Amplifiers, Measurement Equipment, Control Systems, Public Audios (PA), Smart Cellular Phones, IC-Recorders, Bluetooth Headphones, HD Audio/Voice Conference Systems

2. Features

- **256x Over sampling**
- **Sampling Rate: 30kHz ~ 768kHz**
- **32-bit 8x Digital Filter**
 - **Ripple: $\pm 0.005\text{dB}$, Attenuation: 100dB**
 - **Short Delay Sharp Roll-off, $\text{GD}=6.25/\text{fs}$**
 - **Short Delay Slow Roll-off, $\text{GD}=5.3/\text{fs}$**
 - **Sharp Roll-off**
 - **Slow Roll-off**
 - **Super Slow Roll-off**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **2.8MHz, 5.6MHz and 11.2MHz DSD Input Support**
 - **Filter ($f_c=50\text{kHz}$, $f_c=150\text{kHz}$, 2.8MHz mode)**
- **Digital De-emphasis for 32, 44.1, 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (255 levels and 0.5dB step)**
- **Mono Mode**
- **External Digital Filter Mode**
- **THD+N: -112dB**
- **DR, S/N: 120dB (Mono mode: 123dB)**
- **I/F Format: 24/32bit MSB justified, 16/20/24/32bit LSB justified, I²S, DSD**
- **Master Clock:**
 - 30kHz ~ 32kHz: 1152fs**
 - 30kHz ~ 54kHz: 512fs or 768fs**
 - 30kHz ~ 108kHz: 256fs or 384fs**
 - 108kHz ~ 216kHz: 128fs or 192fs**
 - ~ 384kHz: 64fs or 128fs**
 - ~ 768kHz: 64fs**
- **Power Supply: DVDD=AVDD=3.0 ~ 3.6V, VDD1/2=4.75 ~ 7.2V**
- **Digital Input Level: CMOS**
- **Package: 48-pin LQFP**



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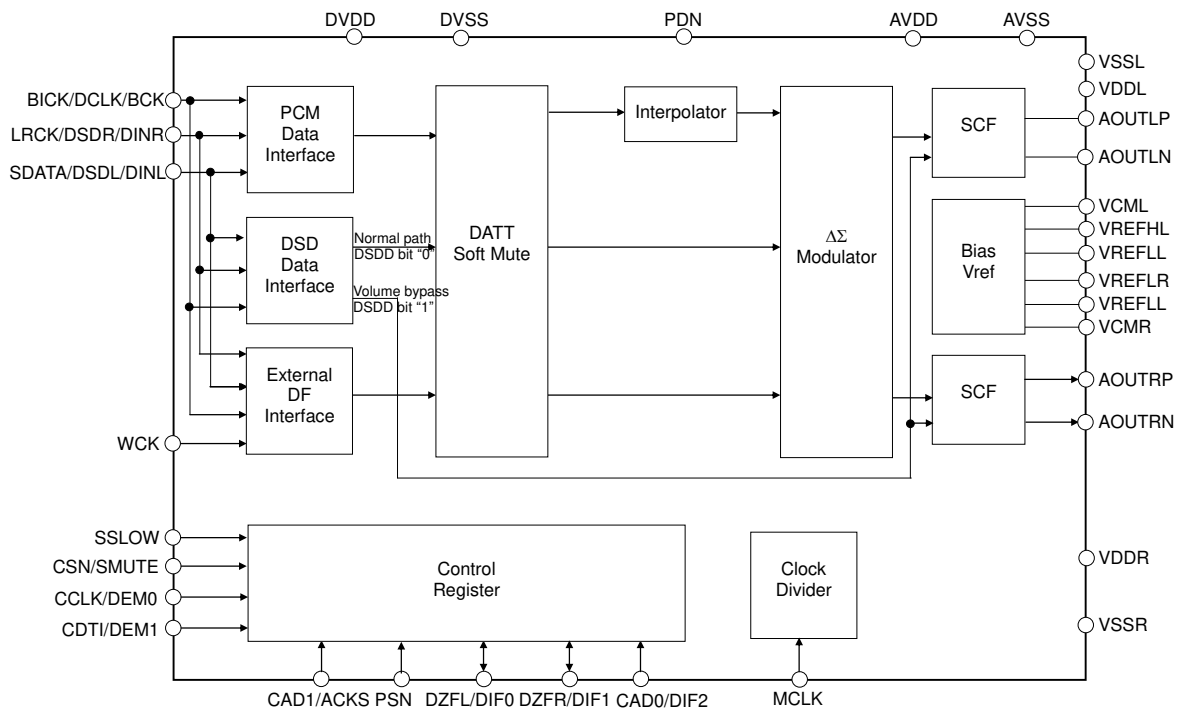
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4. Block Diagram



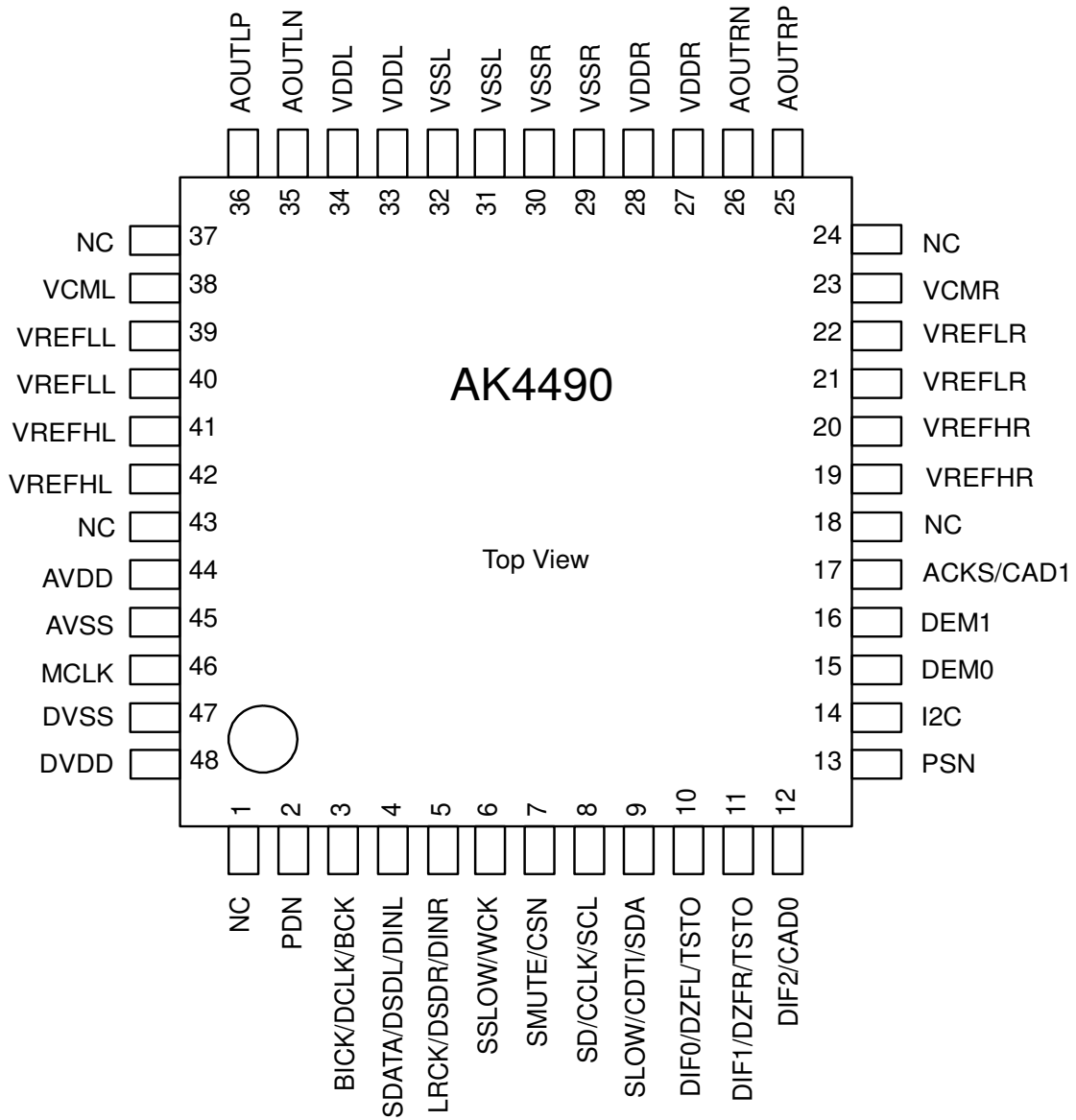
Block Diagram

5. Pin Configurations and Functions

■ Ordering Guide

AK4490EQ -40 ~ +85°C 48pin LQFP (0.5mm pitch)
 AKD4490 Evaluation Board for AK4490

■ Pin Layout



■ Pin Functions

No.	Pin Name	I/O	Function
1	NC	-	No internal bonding. Connect to GND.
2	PDN	I	Power-Down Mode Pin When at “L”, the AK4490 is in power-down mode and is held in reset. The AK4490 must always be reset upon power-up.
3	BICK	I	Audio Serial Data Clock Pin in PCM Mode
	DCLK	I	DSD Clock Pin in DSD Mode
	BCK	I	Audio Serial Data Clock Pin
4	SDATA	I	Audio Serial Data Input Pin in PCM Mode
	DSDL	I	DSD Lch Data Input Pin in DSD Mode
	DINL	I	Lch Audio Serial Data Input Pin
5	LRCK	I	L/R Clock Pin in PCM Mode
	DSDR	I	DSD Rch Data Input Pin in DSD Mode in Serial Control Mode
	DINR	I	Rch Audio Serial Data Input Pin in Serial Control Mode
6	SSLOW	I	Digital Filter Setting in Parallel Control Mode
	WCK	I	Word Clock input pin in Serial Control Mode
7	SMUTE	I	Soft Mute Pin in Parallel Control Mode When this pin is changed to “H”, soft mute cycle is initiated. When returning “L”, the output mute releases.
	CSN	I	Chip Select Pin in Serial Control Mode, I2C= “L”
8	SD	I	Digital Filter Setting Pin in Parallel Control Mode
	CCLK	I	Control Data Clock Pin in Serial Control Mode, I2C= “L”
	SCL	I	Control Data Clock Input Pin in Serial Control Mode, I2C= “H”
9	SLOW	I	Digital Filter Setting Pin in Parallel Control Mode
	CDTI	I	Control Data Input Pin in Serial Control Mode, I2C= “L”
	SDA	I/O	I2C= “H”: Control Data Input Pin in Serial Control Mode, I2C= “H”
10	DIF0	I	Digital Input Format 0 Pin in PCM Mode
	DZFL	O	Lch Zero Input Detect Pin in Serial Control Mode
11	DIF1	I	Digital Input Format 1 Pin in PCM Mode
	DZFR	O	Rch Zero Input Detect Pin in Serial Control Mode
12	DIF2	I	Digital Input Format 2 Pin in PCM Control Mode
	CAD0	I	Chip Address 0 Pin in Serial Control Mode
13	PSN	I	Parallel or Serial Select Pin (Internal pull-up pin) “L”: Serial Control Mode, “H”: Parallel Control Mode
14	I2C	I	I2C mode select pin in Serial mode (Internal pull-down pin)
15	DEM0	I	De-emphasis Enable 0 Pin in Parallel Control Mode (Internal pull-up pin)

Note: All input pins except internal pull-up/down pins must not be left floating.

16	DEMI	I	De-emphasis Enable 1 Pin in Parallel Control Mode (Internal pull-down pin)
17	ACKS	I	Master Clock Auto Setting Mode Pin in Parallel Mode (Internal pull-down pin)
	CAD1	I	Chip Address 1 Pin in Serial Control Mode
18	NC	-	No internal bonding. Connect to GND.
19	VREFHR	I	Rch High Level Voltage Reference Input Pin
20	VREFHR	I	Rch High Level Voltage Reference Input Pin
21	VREFLR	I	Rch Low Level Voltage Reference Input Pin
22	VREFLR	I	Rch Low Level Voltage Reference Input Pin
23	VCMR	-	Right channel Common Voltage Pin, Normally connected to VREFLR with a 10uF electrolytic cap.
24	NC	-	No internal bonding. Connect to GND.
25	AOUTRP	O	Rch Positive Analog Output Pin
26	AOUTRN	O	Rch Negative Analog Output Pin
27	VDDR	-	Rch Analog Power Supply Pin, 4.75 ~ 7.2V
28	VDDR	-	Rch Analog Power Supply Pin, 4.75 ~ 7.2V
29	VSSR	-	Ground Pin
30	VSSR	-	Ground Pin
31	VSSL		Ground Pin
32	VSSL		Ground Pin
33	VDDL	-	Lch Analog Power Supply Pin, 4.75 ~ 7.2V
34	VDDL	-	Lch Analog Power Supply Pin, 4.75 ~ 7.2V
35	AOUTLN	O	Lch Negative Analog Output Pin
36	AOUTLP	O	Lch Positive Analog Output Pin
37	NC	-	No internal bonding. Connect to GND.
38	VCML	-	Left channel Common Voltage Pin, Normally connected to VREFLL with a 10uF electrolytic cap.
39	VREFLL	I	Lch Low Level Voltage Reference Input Pin
40	VREFLL	I	Lch Low Level Voltage Reference Input Pin
41	VREFHL	I	Lch High Level Voltage Reference Input Pin
42	VREFHL	I	Lch High Level Voltage Reference Input Pin
43	NC	-	No internal bonding. Connect to GND.
44	AVDD	-	Analog Power Supply Pin, 3.0 ~ 3.6V
45	AVSS	-	Ground Pin
46	MCLK	I	Master Clock Input Pin
47	DVSS	-	Ground Pin
48	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V

Note. All input pins except internal pull-up/down pins must not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

(1) Parallel Mode (PCM Mode only)

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	I2C	This pin must be connected to DVSS or open.

(2) Serial Mode

1. PCM Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	PSN, DEM1	These pins must be connected to DVSS
	DEM0	This pin must be connected to DVDD.

2. DSD Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	PSN, DEM1	These pins must be connected to DVSS
	DEM0	This pin must be connected to DVDD.

pull-up pin List

pull-up pin	13, 15
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pull-down pin List

pull-down pin	14, 16, 17
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6. Absolute Maximum Ratings

(AVSS=DVSS=VSSL=VSSR=VREFLL=VREFLR=0V; Note 1)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	-0.3	4.6	V
	Analog	VDDL/R	-0.3	7.5	V
	Digital	DVDD	-0.3	4.6	V
	AVSS – DVSS (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

Note 2. AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane.

Note 3. Connect at least 0.1μF or more decoupling capacitors between VDDL/VDDR and VSSL/VSSR to suppress affections by a static electricity noise or an over voltage (includes over shooting) that exceeds absolute maximum ratings.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS=VSSL=VSSR=0V; Note 1)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 4)	Analog	AVDD	3.0	3.3	3.6	V
	Analog	VDDL/R	4.75	5.0	7.2	V
	Digital	DVDD	3.0	3.3	3.6	V
Voltage Reference (Note 5)	“H” voltage reference	VREFHL/R	VDDL/R-0.5	-	VDDL/R	V
	“L” voltage reference	VREFLL/R		VSSL/R	-	V

Note 1. All voltages with respect to ground.

Note 4. The power up sequence between AVDD, VDDL/R and DVDD is not critical.

Note 5. The analog output voltage scales with the voltage of (VREFH – VREFL).

$$AOUT(\text{typ.}@0\text{dB}) = (AOUT+) - (AOUT-) = \pm 2.8V_{pp} \times (VREFHL/R - VREFLL/R)/5.$$

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

■ Analog Characteristics

($T_a=25^{\circ}\text{C}$; $AVDD=DVDD=3.3\text{V}$; $AVSS=DVSS=VSSL/R=0\text{V}$; $VREFHL/R=VDDL/R=5\text{V}$, $VREFLL/R=VSSL/R=0\text{V}$; Input data = 24bit; $R_L \geq 1\text{k}\Omega$; BICK=64fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: [Figure 41](#); unless otherwise specified.)

Parameter		min	typ	max	Unit	
Resolution		-	-	32	Bits	
Dynamic Characteristics (Note 6)						
THD+N	$f_s=44.1\text{kHz}$	0dBFS	-	-112	-105	dB
	$BW=20\text{kHz}$	-60dBFS	-	-57	-49	dB
	$f_s=96\text{kHz}$	0dBFS	-	-109	-100	dB
	$BW=40\text{kHz}$	-60dBFS	-	-54	-44	dB
	$f_s=192\text{kHz}$	0dBFS		-106	-100	dB
	$BW=40\text{kHz}$	-60dBFS		-54	-44	dB
	$BW=80\text{kHz}$	-60dBFS		-51	-41	dB
Dynamic Range (-60dBFS with A-weighted)		(Note 7)	115	120	-	dB
S/N (A-weighted)		(Note 8)	115	120	-	dB
S/N (Mono mode, A-weighted)			118	123	-	dB
Interchannel Isolation (1kHz)			110	120	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.15	0.3	dB
Gain Drift		(Note 9)	-	-	20	ppm/ $^{\circ}\text{C}$
Output Voltage		(Note 10)	± 2.65	± 2.8	± 2.95	V _{pp}
Load Capacitance			-	-	25	pF
Load Resistance		(Note 11)	1	-	-	k Ω
Power Supplies						
Power Supply Current						
Normal operation (PDN pin = "H")	VDDL/R			22	32	mA
	AVDD			0.6	1.2	mA
	DVDD ($f_s=44.1\text{kHz}$)	-		10	14	mA
	DVDD ($f_s=96\text{kHz}$)	-		15	20	mA
	DVDD ($f_s=192\text{kHz}$)	-		17	23	mA
	Power down (PDN pin = "L")	(Note 12)				
AVDD+VDDL/R+DVDD			-	10	100	μA

Note 6. Measured by Audio Precision, System Two. Averaging mode. Refer to the evaluation board manual.

Note 7. [Figure 41](#) External LPF Circuit Example 2. 101dB for 16-bit data and 118dB for 20-bit data.

Note 8. [Figure 41](#) External LPF Circuit Example 2. S/N does not depend on input data size.

Note 9. The voltage on (VREFH – VREFL) is held +5V externally.

Note 10. Full-scale voltage(0dB). Output voltage scales with the voltage of (VREFHL/R – VREFLL/R).

$$A_{\text{OUT}} (\text{typ. @0dB}) = (A_{\text{OUT}+}) - (A_{\text{OUT}-}) = \pm 2.8V_{\text{pp}} \times (V_{\text{REFHL/R}} - V_{\text{REFLL/R}})/5.$$

Note 11. Regarding Load Resistance, AC load is 1k Ω (min) with a DC cut capacitor ([Figure 41](#)). DC load is 1.5k ohm (min) without a DC cut capacitor ([Figure 40](#)). The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin.

Therefore the capacitive load must be minimized.

Note 12. In the power down mode. The PSN pin = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.

■ Sharp Roll-Off Filter Characteristics (fs=44.1kHz)

(Ta=25°C; AVDD=DVDD=3.0~3.6V, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Normal Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0	20.0	kHz
			-	22.05	kHz
Stopband (Note 13)		SB	24.1		kHz
Passband Ripple		PR		±0.005	dB
Stopband Attenuation		SA	100		dB
Group Delay (Note 14)		GD	-	29.4	1/fs
Digital Filter + SCF					
Frequency Response: 0 ~ 20.0kHz			-	+0.1/-0.2	dB

■ Sharp Roll-Off Filter Characteristics (fs=96kHz)

Ta=25°C; AVDD=DVDD=3.0~3.6V, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Double Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0	43.5	kHz
			-	48.0	kHz
Stopband (Note 13)		SB	52.5		kHz
Passband Ripple		PR		±0.005	dB
Stopband Attenuation		SA	100		dB
Group Delay (Note 14)		GD	-	28.8	1/fs
Digital Filter + SCF					
Frequency Response: 0 ~ 40.0kHz			-	+0.1/-0.6	dB

■ Sharp Roll-Off Filter Characteristics (fs=192kHz)

(Ta=25°C; AVDD=DVDD=3.0~3.6V, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Quad Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0	87.0	kHz
			-	96.0	kHz
Stopband (Note 13)		SB	105		kHz
Passband Ripple		PR		±0.005	dB
Stopband Attenuation		SA	92		dB
Group Delay (Note 14)		GD	-	28.8	1/fs
Digital Filter + SCF					
Frequency Response: 0 ~ 80.0kHz			-	+0.1/-0.2	dB

Note 13. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

Note 14. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32 bit data of both channels to the output of analog signal.

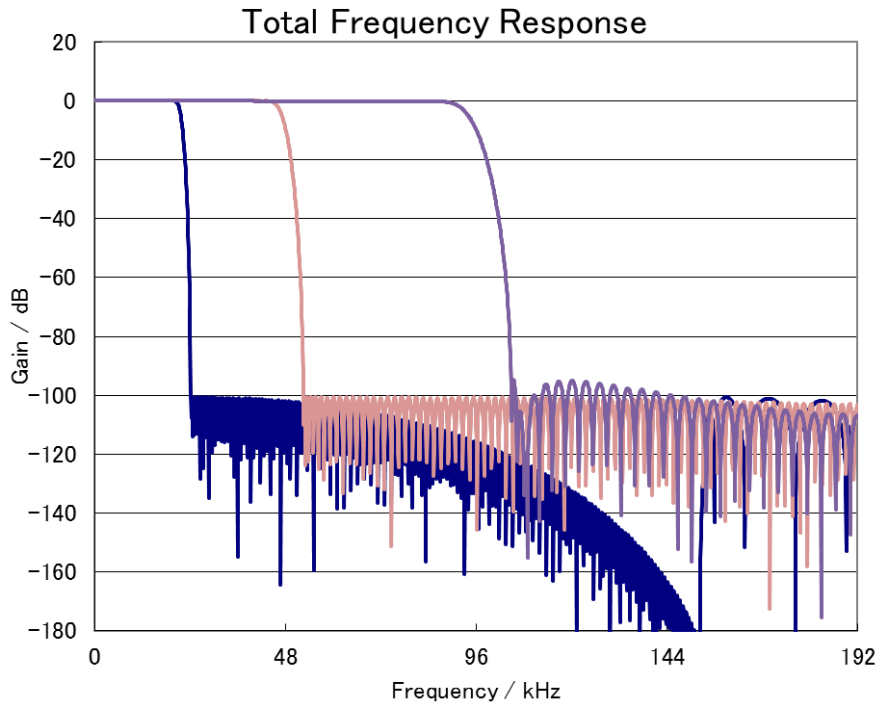


Figure 1. Sharp Roll-off Filter Frequency Response

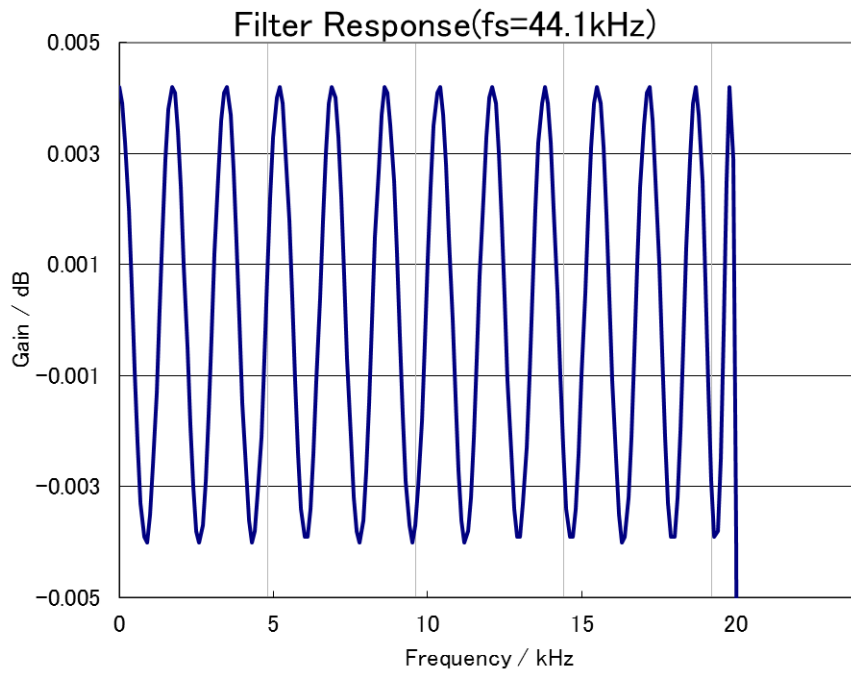


Figure 2. Sharp Roll-off Filter Passband Ripple

■ Short Delay Sharp Roll-Off Filter Characteristics (fs=44.1kHz)

(Ta=25°C; AVDD=DVDD=3.0~3.6V, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Normal Speed Mode;
DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0		kHz
			-	22.05	kHz
Stopband (Note 13)	SB	24.1			kHz
Passband Ripple	PR			±0.005	dB
Stopband Attenuation	SA	100			dB
Group Delay (Note 14)	GD	-	6.25	-	1/fs
Digital Filter + SCF					
Frequency Response : 0 ~ 20.0kHz		-	-0.1/-0.2	-	dB

■ Short Delay Sharp Roll-Off Filter Characteristics (fs=96kHz)

(Ta=25°C; AVDD=DVDD=3.0~3.6V, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Double Speed Mode;
DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0		kHz
			-	48.0	kHz
Stopband (Note 13)	SB	52.5			kHz
Passband Ripple	PR			±0.005	dB
Stopband Attenuation	SA	100			dB
Group Delay (Note 14)	GD	-	5.63	-	1/fs
Digital Filter + SCF					
Frequency Response : 0 ~ 40.0kHz		-	+0.1/-0.6	-	dB

■ Short Delay Sharp Roll-Off Filter Characteristics (fs=192kHz)

(Ta=25°C; AVDD=DVDD=3.0~3.6V, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Quad Speed Mode; DEM=OFF;
SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0		kHz
			-	96.0	kHz
Stopband (Note 13)	SB	105			kHz
Passband Ripple	PR			±0.005	dB
Stopband Attenuation	SA	92			dB
Group Delay (Note 14)	GD	-	5.63	-	1/fs
Digital Filter + SCF					
Frequency Response : 0 ~ 80.0kHz		-	+0.1/-2.0	-	dB

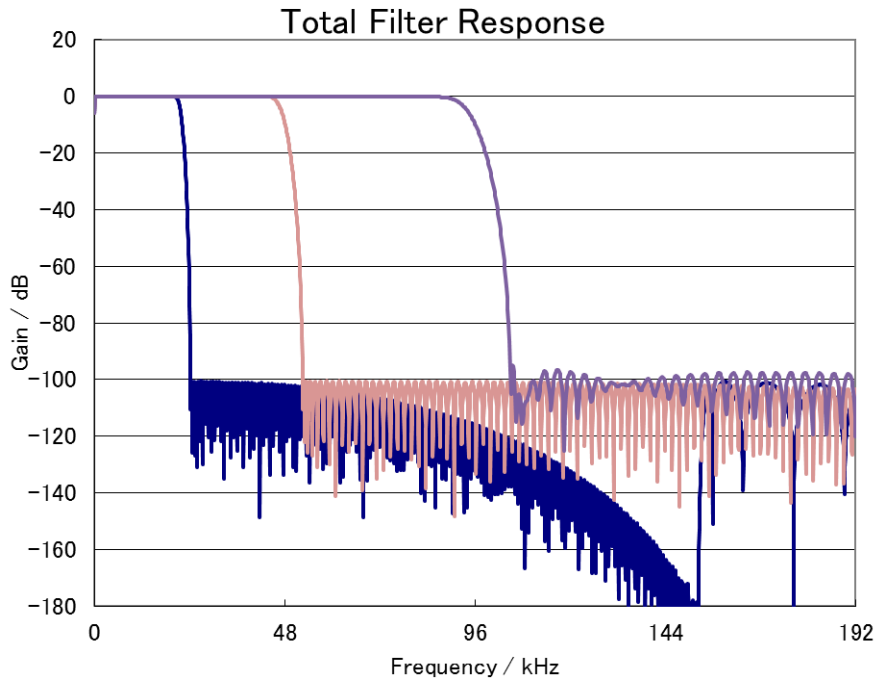


Figure 3. Short delay Sharp Roll-off Filter Frequency Response

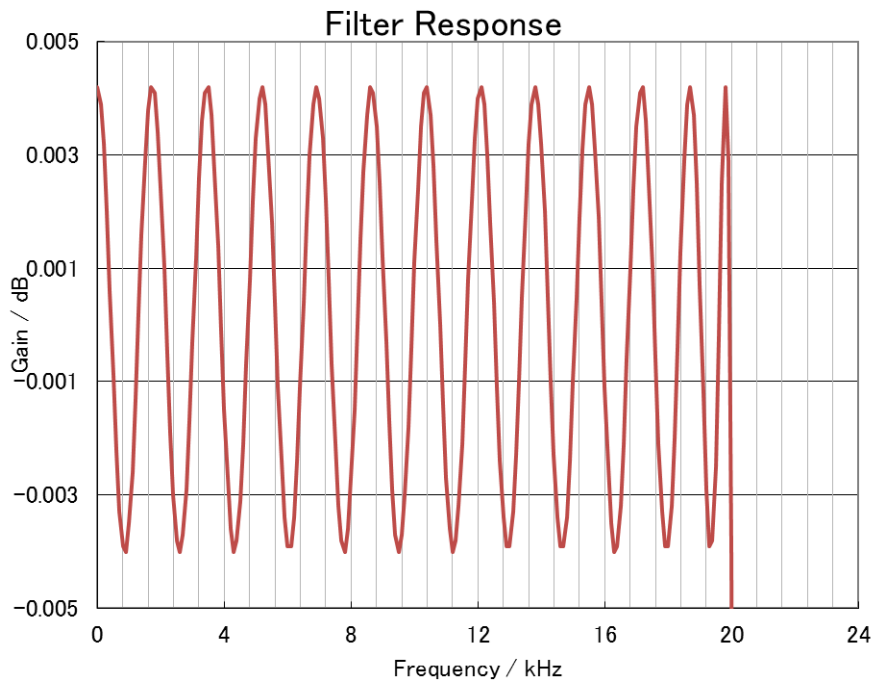


Figure 4. Short delay Sharp Roll-off Filter Passband Ripple

■ Slow Roll-Off Filter Characteristics (fs=44.1kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Normal Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0	4.4	kHz
			-	18.2	kHz
Stopband (Note 13)	SB	39.1			kHz
Passband Ripple	PR			±0.005	dB
Stopband Attenuation	SA	94			dB
Group Delay (Note 14)	GD	-	6.63	-	1/fs
Digital Filter + SCF					
Frequency Response: 0 ~ 20.0kHz		-	+0.1/-4.5	-	dB

■ Slow Roll-Off Filter Characteristics (fs=96kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Double Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0	18.1	kHz
			-	45.6	kHz
Stopband (Note 13)	SB	85.0			kHz
Passband Ripple	PR			±0.005	dB
Stopband Attenuation	SA	100			dB
Group Delay (Note 14)	GD	-	6.00	-	1/fs
Digital Filter + SCF					
Frequency Response: 0 ~ 40.0kHz		-	+0.1/-4.0	-	dB

■ Slow Roll-Off Filter Characteristics (fs=192kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Quad Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0	32.9	kHz
			-	90.4	kHz
Stopband (Note 13)	SB	171			kHz
Passband Ripple	PR			±0.005	dB
Stopband Attenuation	SA	97			dB
Group Delay (Note 14)	GD	-	6.00	-	1/fs
Digital Filter + SCF					
Frequency Response: 0 ~ 80.0kHz		-	+0.1/-5.5	-	dB

Note 15. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

Note 16. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32 bit data of both channels to the output of analog signal.

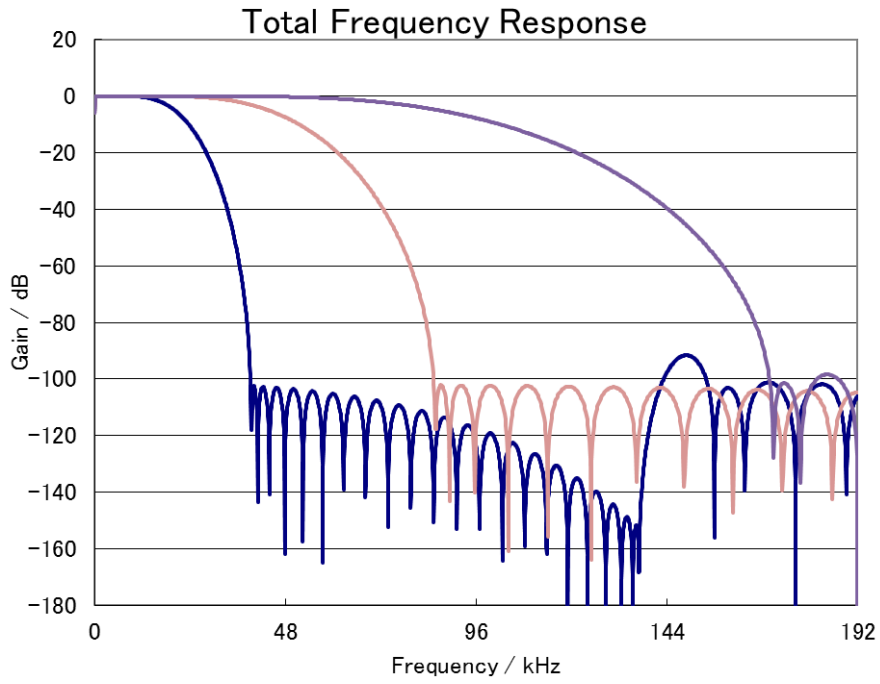


Figure 5. Slow Roll-off Filter Frequency Response

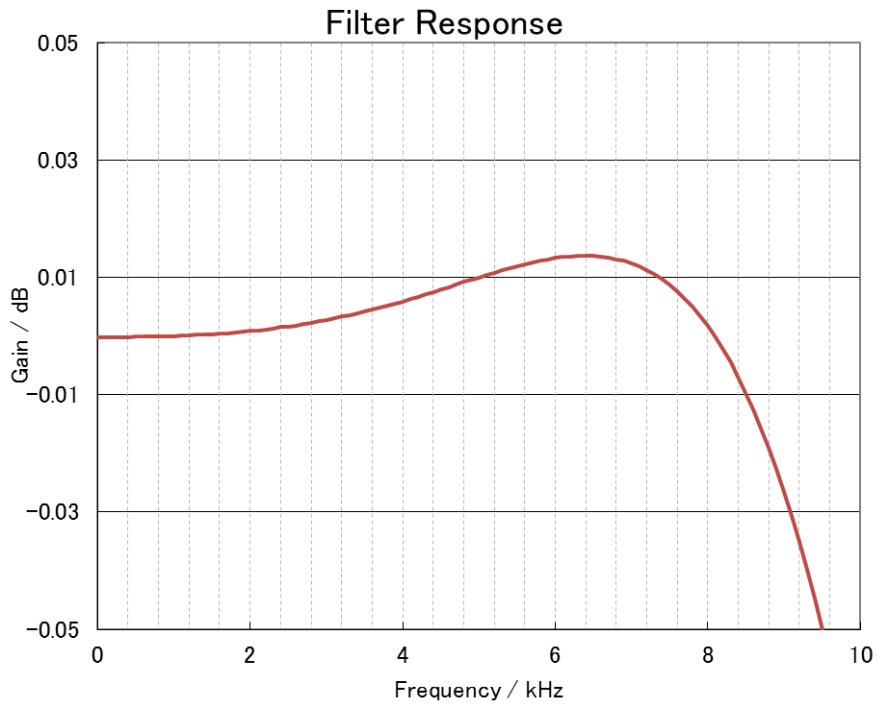


Figure 6. Slow Roll-off Filter Passband Ripple

■ Short Delay Slow Roll-Off Filter Characteristics (fs=44.1kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Normal Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="1" or SLOW pin = "H")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0	4.4	kHz
			-	18.2	kHz
Stopband (Note 13)	SB	39.1			kHz
Passband Ripple	PR			±0.005	dB
Stopband Attenuation	SA	94			dB
Group Delay (Note 14)	GD	-	5.3	-	1/fs
Digital Filter + SCF					
Frequency Response : 0 ~ 20.0kHz		-	+0.1/-4.5	-	dB

■ Short Delay Slow Roll-Off Filter Characteristics (fs=96kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Double Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0	18.1	kHz
			-	45.6	kHz
Stopband (Note 13)	SB	85.0			kHz
Passband Ripple	PR			±0.005	dB
Stopband Attenuation	SA	100			dB
Group Delay (Note 14)	GD	-	4.68	-	1/fs
Digital Filter + SCF					
Frequency Response : 0 ~ 40.0kHz		-	+0.1/-0.4	-	dB

■ Short Delay Slow Roll-Off Filter Characteristics (fs=192kHz)

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, VREFHL/R=VDDL/R=4.75 ~ 7.2V; Quad Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H")

Parameter	Symbol	min	typ	max	Unit
Digital Filter					
Passband (Note 13)	±0.01dB -6.0dB	PB	0	32.9	kHz
			-	96.0	kHz
Stopband (Note 13)	SB	170			kHz
Passband Ripple	PR			±0.005	dB
Stopband Attenuation	SA	97			dB
Group Delay (Note 14)	GD	-	4.68	-	1/fs
Digital Filter + SCF					
Frequency Response : 0 ~ 80.0kHz		-	+0.1/-5.5	-	dB

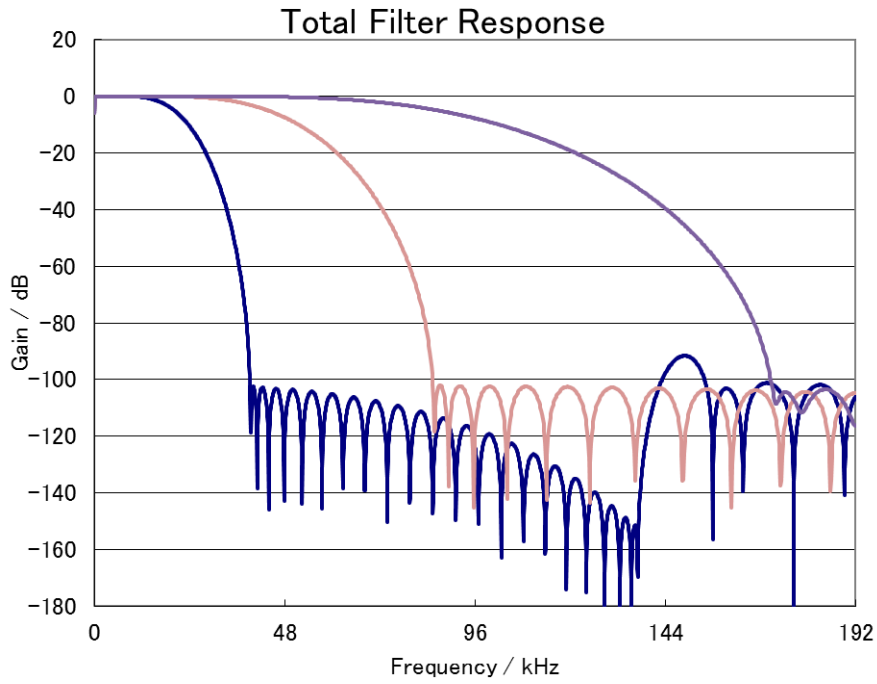


Figure 7. Short Delay Slow Roll-off Filter Frequency Response

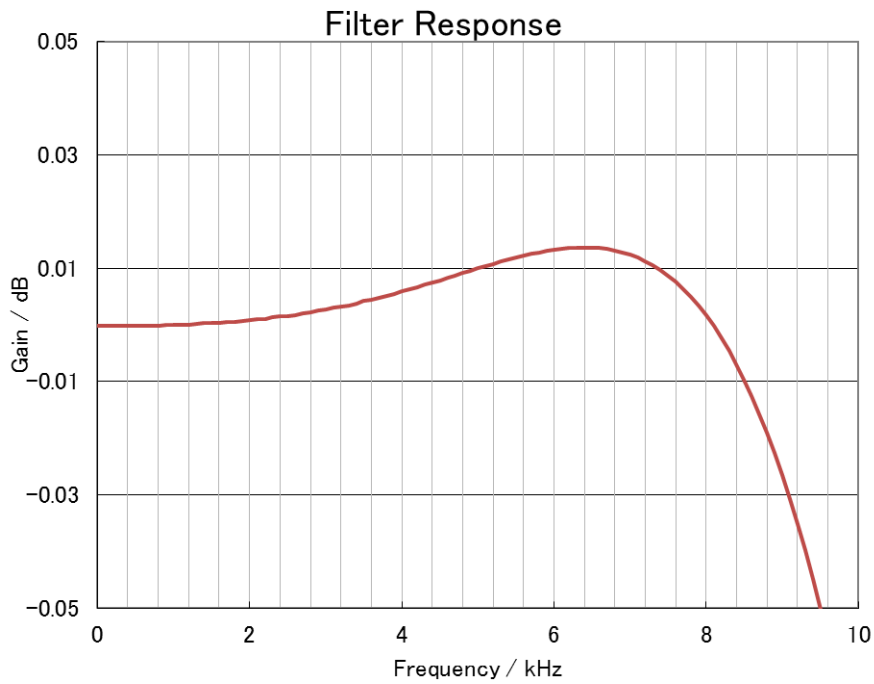


Figure 8. Short Delay Slow Roll-off Filter Passband Ripple

■ DSD Mode Characteristics

($T_a = -40 \sim 85^\circ\text{C}$; $V_{DDL/R} = 4.75 \sim 7.2\text{V}$, $A_{VDD} = DV_{DD} = 3.0 \sim 3.6\text{V}$; $f_s = 44.1\text{kHz}$; D/P bit="1", DSDF bit="0")

Parameter		min	typ	max	Unit
Digital Filter Response					
Frequency Response (Note 18)	20kHz		-0.4		dB
	50kHz		-2.8		dB
	100kHz		-15.5		dB

($T_a = -40 \sim 85^\circ\text{C}$; $V_{DDL/R} = 4.75 \sim 7.2\text{V}$, $A_{VDD} = DV_{DD} = 3.0 \sim 3.6\text{V}$; $f_s = 44.1\text{kHz}$; D/P bit="1", DSDF bit="1", DSDD bit="1")

Parameter		min	typ	max	Unit
Digital Filter Response					
Frequency Response (Note 18)	20kHz		-0.05		dB
	50kHz		-0.29		dB
	100kHz		-1.16		dB
	150kHz		-2.8		dB

Note 17. The peak level of DSD signal should be in the range of 25% ~ 75% Duty according to the SACD format book (Scarlet Book).

Note 18. The output level is assumed as 0dB when a 1kHz 25% ~ 75% Duty sine wave is input.

■ DC Characteristics

($T_a = 25^\circ\text{C}$; $A_{VDD} = DV_{DD} = 3.0 \sim 3.6$, $V_{REFHL/R} = V_{DDL/R} = 4.75 \sim 7.2\text{V}$)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage	V_{IH}	70% DV_{DD}	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30% DV_{DD}	V
High-Level Output Voltage ($I_{out} = -100\mu\text{A}$)	V_{OH}	$DV_{DD} - 0.5$	-	-	V
Low-Level Output Voltage (DZFL, DZFR pins: $I_{out} = 100\mu\text{A}$)	V_{OL}	-	-	0.5	V
(SDA pin: $I_{out} = 3\text{mA}$)	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 19)	I_{in}	-	-	± 10	μA

Note 19. The DEM1, I2C and ACKS pins have internal pull-down and DEM0 and PSN pins have internal pull-up devices, nominally 100k Ω . Therefore the DEM1, I2C, ACKS, DEM0 and PSN pins are not included.

■ Switching Characteristics

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, VREFHL/R=VDDL/R=4.75 ~ 7.2V))

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
Frequency	fCLK	7.7		49.152	MHz
Duty Cycle	dCLK	40		60	%
Minimum Pulse Width	tCLKH	9.155			ns
	tCLKL	9.155			ns
LRCK Frequency (Note 20)					
1152fs, 512fs or 768fs	fsn	30		54	kHz
256fs or 384fs	fsd	54		108	kHz
128fs or 192fs	fsq	108		216	kHz
64fs	fsoc		384		kHz
64fs	fssd		768		kHz
Duty Cycle	Duty	45		55	%
PCM Audio Interface Timing					
BICK Period					
1152fs, 512fs or 768fs	tBCK	1/128fsn			ns
256fs or 384fs	tBCK	1/64fsd			ns
128fs or 192fs	tBCK	1/64fsq			ns
64fs	tBCK	1/64fso			ns
64fs	tBCK	1/64fsh			ns
BICK Pulse Width Low	tBCKL	9			ns
BICK Pulse Width High	tBCKH	9			ns
BICK “↑” to LRCK Edge (Note 21)	tBLR	5			ns
LRCK Edge to BICK “↑” (Note 21)	tLRB	5			ns
SDATA Hold Time	tSDH	5			ns
SDATA Setup Time	tSDS	5			ns
External Digital Filter Mode					
BICK Period	tB	27			ns
BCK Pulse Width Low	tBL	10			ns
BCK Pulse Width High	tBH	10			ns
BCK “↑” to WCK Edge	tBW	5			ns
WCK Period	tWCK	1.3			μs
WCK Edge to BCK “↑”	tWB	5			ns
WCK Pulse Width Low	tWCK	54			ns
WCK Pulse Width High	tWCH	54			ns
DATA Hold Time	tDH	5			ns
DATA Setup Time	tDS	5			ns
DSD Audio Interface Timing (64 mode, DSDSEL 1-0 bits = “00”)					
DCLK Period	tDCK		1/64fs		ns
DCLK Pulse Width Low	tDCKL	160			ns
DCLK Pulse Width High	tDCKH	160			ns
DCLK Edge to DSDL/R (Note 22)	tDDD	-20		20	ns

DSD Audio Interface Timing (128 mode, DSDSEL 1-0 bits = "01")					
DCLK Period	tDCK		1/128fs		ns
DCLK Pulse Width Low	tDCKL	80			ns
DCLK Pulse Width High	tDCKH	80			ns
DCLK Edge to DSDL/R (Note 22)	tDDD	-10		10	ns
DSD Audio Interface Timing (256 mode, DSDSEL 1-0 bit = "10")					
DCLK Period	tDCK		1/256fs		ns
DCLK Pulse Width Low	tDCKL	40			ns
DCLK Pulse Width High	tDCKH	40			ns
DCLK Edge to DSDL/R (Note 22)	tDDD	-5		5	ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
CCLK Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN High Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I²C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	μs
Clock Low Time	tLOW	1.3		-	μs
Clock High Time	tHIGH	0.6		-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	μs
SDA Hold Time from SCL Falling (Note 23)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	μs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6		-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Reset Timing					
PDN Pulse Width (Note 24)	tPD	150			ns

Note 20. When the 1152fs, 512fs or 768fs /256fs or 384fs/128fs or 192fs are switched, the AK4490 should be reset by the PDN pin or RSTN bit.

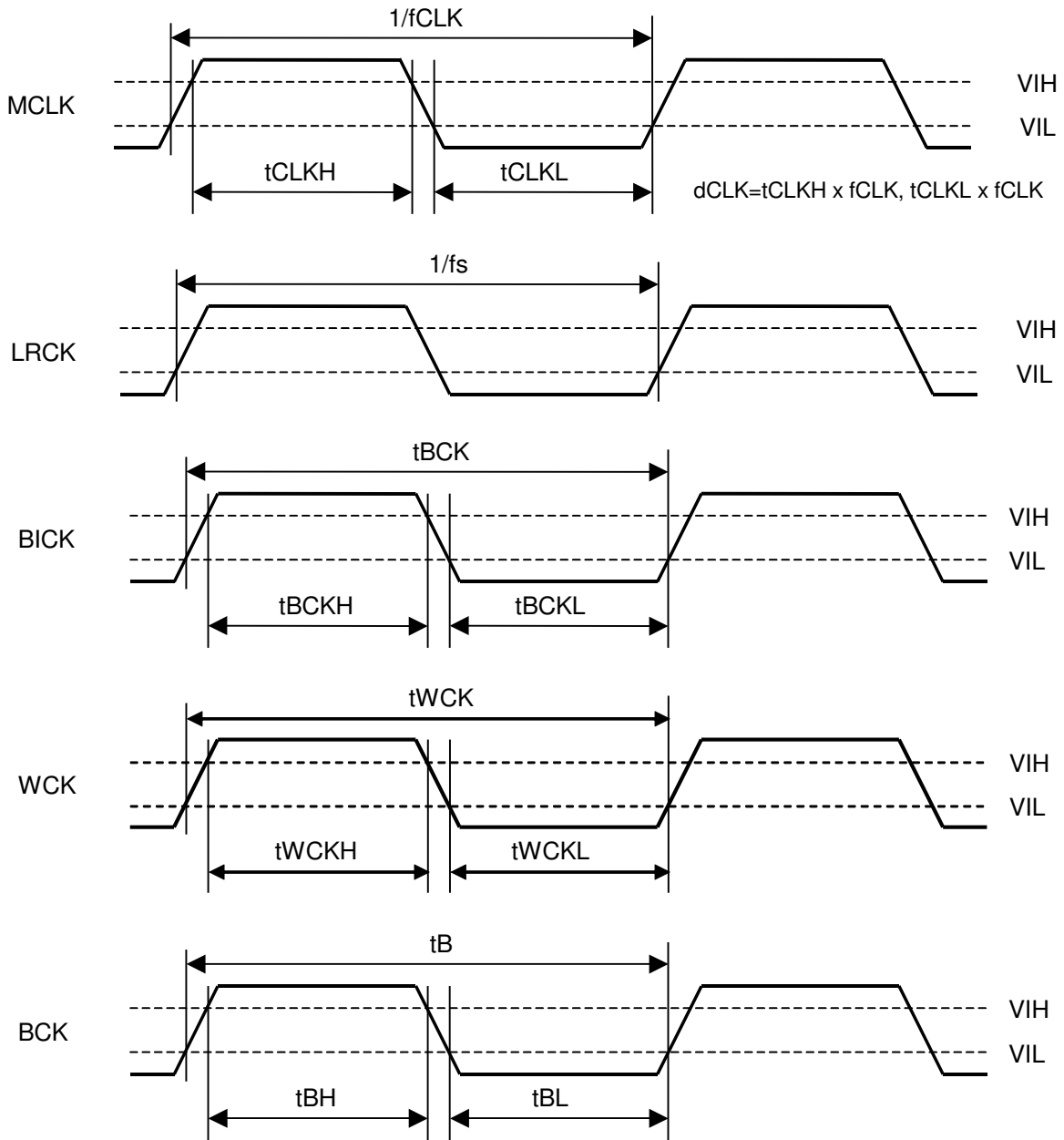
Note 21. BICK rising edge must not occur at the same time as LRCK edge.

Note 22. DSD data transmitting device must meet this time.

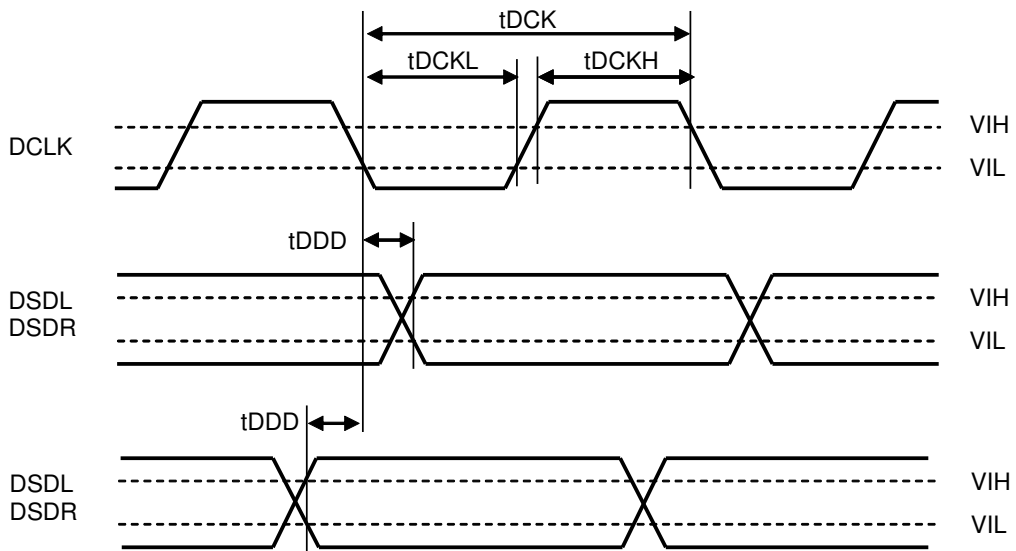
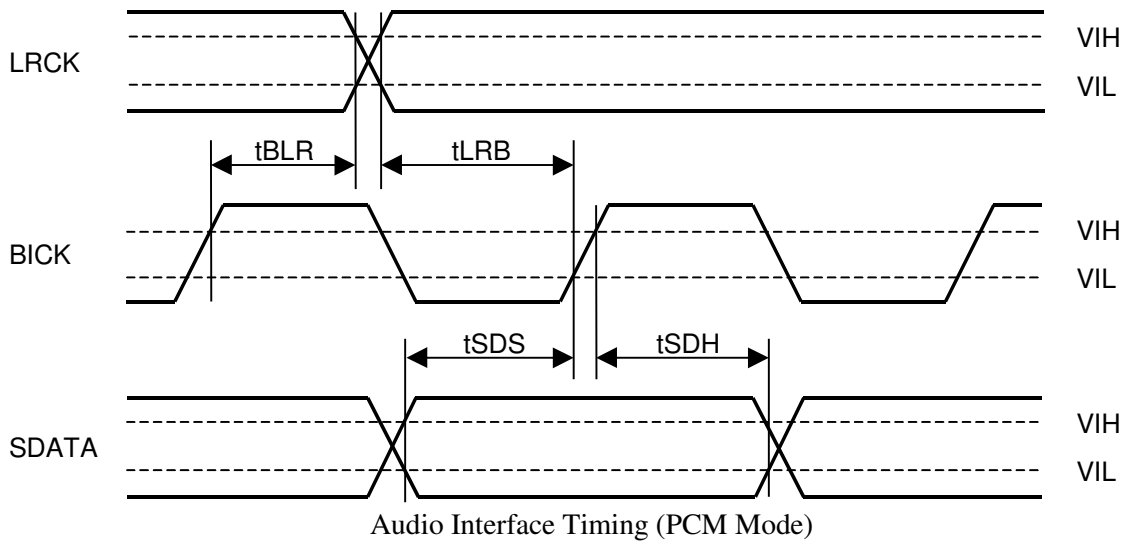
Note 23. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

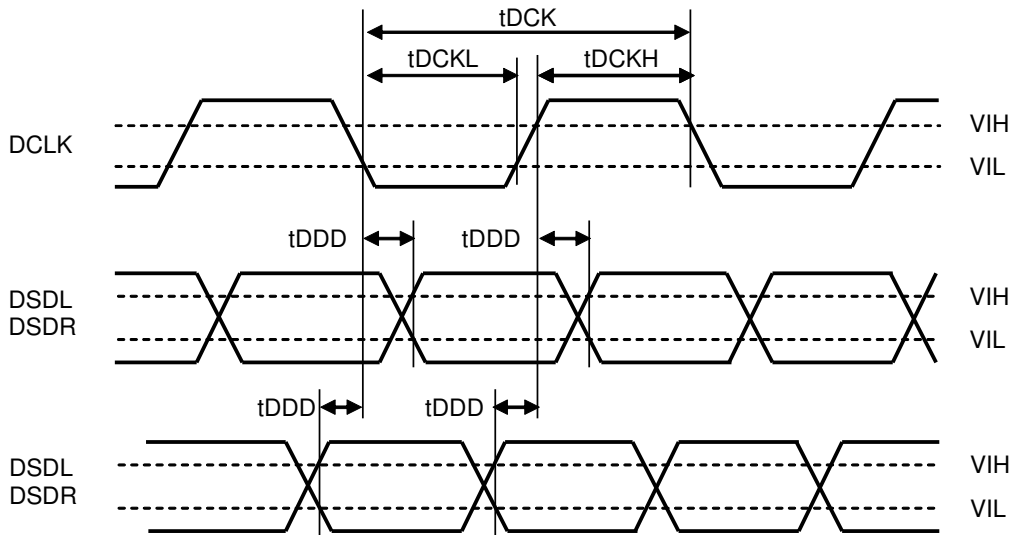
Note 24. The AK4490 can be reset by bringing the PDN pin to "L".

■ Timing Diagram

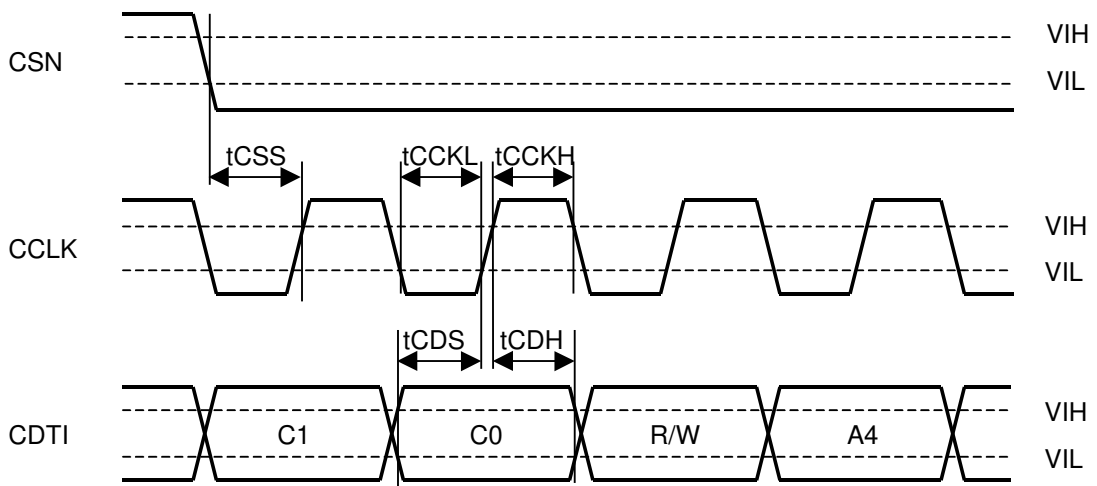


Clock Timing

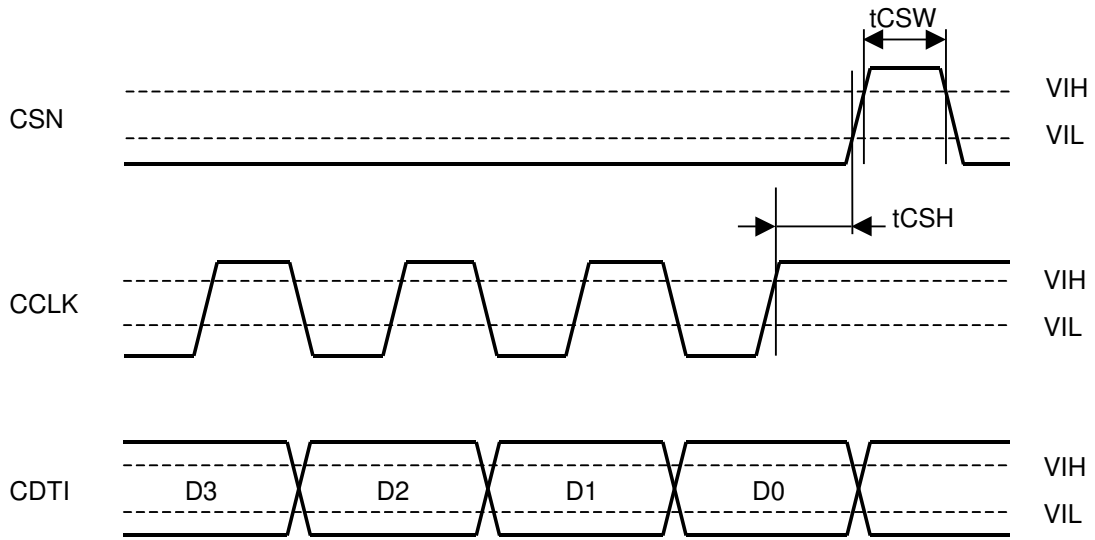




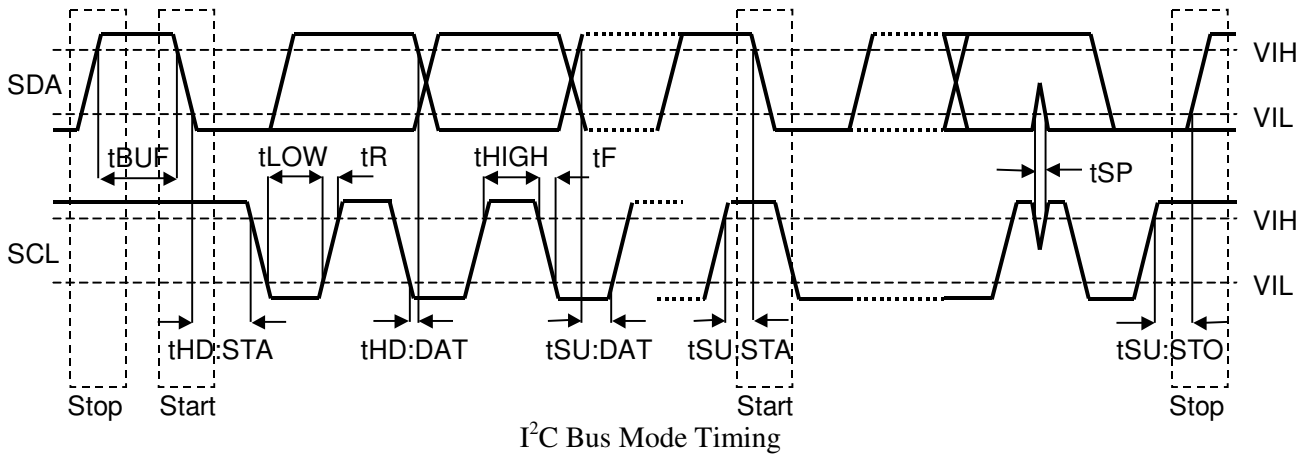
Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB bit = "0")



WRITE Command Input Timing



WRITE Data Input Timing



I²C Bus Mode Timing