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AK4492

Quality Oriented 32-Bit 2ch DAC

1. General Description

The AK4492 is a new generation Premium 32-bit 2ch DAC with VELVET SOUND™ technology, achieving industry's leading level low distortion characteristics. The OSR-Doubler technology establishes low power consumption and low distortion characteristics. Moreover, the AK4492 has six types of 32-bit digital filters, realizing simple and flexible sound tuning in wide range of applications. The AK4492 accepts up to 768kHz PCM data and 11.2MHz DSD data, ideal for a high-resolution audio source playback that are becoming widespread in smartphone, portable audio player etc.

Application: Smart Cellular Phones, IC-Recorders, Bluetooth Headphones, CD/SACD Players, Network Audios, USB DACs, USB Headphones, Sound Plates/Bars, HD Audio/Voice Conference Systems, AV Receivers

2. Features

- **THD+N: -115 dB**
- **DR, S/N: 127 dB (2 Vrms Output)**
- **128 Times Over Sampling**
- **Sampling Rate: 8kHz ~ 768 kHz**
- **32-bit 8x Digital Filter**
  - **Short Delay Sharp Roll-off, GD=6.0/fs, Ripple: ±0.005dB, Attenuation: 100dB**
  - **Short Delay Slow Roll-off, GD=5.0/fs**
  - **Sharp Roll-off**
  - **Slow Roll-off**
  - **Low-dispersion Short Delay Filter**
  - **Super Slow Roll-off**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **2.8 MHz, 5.6 MHz, 11.2 MHz DSD Input Support**
  - **Filter1 (fc = 39 kHz, 2.8 MHz mode)**
  - **Filter2 (fc = 76 kHz, 2.8 MHz mode)**
- **Digital De-emphasis for 32, 44.1and 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (255 levels and 0.5dB step + mute)**
- **Mono Mode**
- **External Digital Filter Interface**
- **Audio I/F Format: 24/32 bit MSB justified, 16/20/24/32 bit LSB justified, I²S, DSD, TDM**
- **Master Clock**
  - **8 kHz ~ 32 kHz: 256 fs or 384 fs or 512 fs or 768 fs or 1024 fs or 1152 fs**
  - **8 kHz ~ 54 kHz: 256 fs or 384 fs or 512 fs or 768 fs**
  - **8 kHz ~ 108 kHz: 256 fs or 384 fs**
  - **108 kHz ~ 216 kHz: 128 fs or 192 fs**
  - **~384 kHz: 32 fs or 48 fs or 64 fs or 96 fs**
  - **~768 kHz: 16 fs or 32 fs or 48 fs or 64 fs**
- **3-wire, I²C-bus Interface**

- **Power Supply:**
  (by Internal LDO)TVDD=AVDD= 3.0 ~ 3.6V, VDDL/R= 4.75 ~ 5.25V
  (by external supply)TVDD=AVDD= (DVDD) ~ 3.6V, DVDD=1.7 ~ 1.98V,
  VDDL/R= 4.75 ~ 5.25V
- **Operational Temperature Rnage: −40 ~ 85 °C**
- **Digital Input Level: CMOS**
- **Package: 96-pin WLCSP**

3. Table of Contents

4. Block Diagram

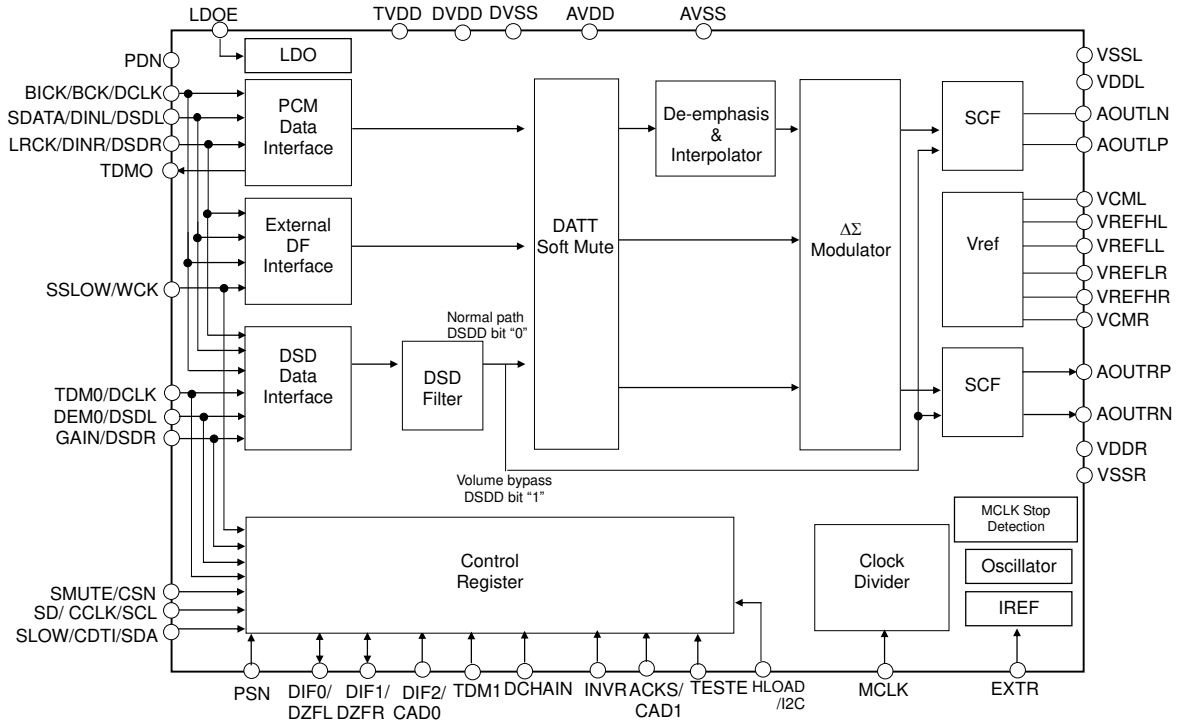
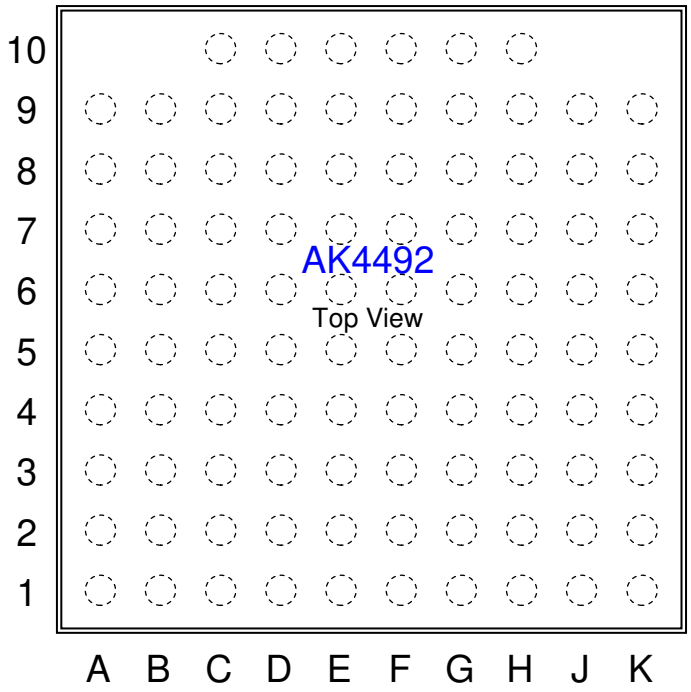


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations



10			VDDR	VSSR	VSSR	VSSL	VSSL	VDDL		
9	AOUTRN	AOUTRP	VDDR	VDDR	VSSR	VSSL	VDDL	VDDL	AOUTLP	AOUTLN
8	VREFLR	VCMR	NC	NC	NC	NC	NC	NC	VCML	VREFLL
7	VREFLR	NC	NC	NC	NC	NC	NC	NC	NC	VREFLL
6	VREFHR	NC	NC	NC	NC	NC	NC	NC	NC	VREFHL
5	VREFHR	TESTE	NC	NC	NC	NC	NC	NC	EXTR	VREFHL
4	INVR	DCHAIN	NC	NC	NC	NC	NC	NC	AVSS	AVDD
3	TDM0/ DCLK	TDM1	NC	PSN	NC	NC	NC	LDOE	MCLK	DVDD
2	ACKS/ CAD1	GAIN/ DSDR	HLOAD/ I2C	DIF2/ CAD0	SD/ CCLK/ SCL	TDMO	SSLOW/ WCK	PDN	TVDD	DVSS
1	NC	DEM0/ DSDL	DIF1/ DZFR	DIF0/ DZFL	SLOW/ CDTI/ SDA	SMUTE/ CSN	LRCK/ DINR/ DSDR	SDATA/ DINL/ DSDL	BICK/ BCK/ DCLK	NC
	A	B	C	D	E	F	G	H	J	K

Figure 2. Pin Configurations

The exposed pad on the bottom surface of the package must be connected to VSS.

■ **Pin Functions**

No.	Pin Name	I/O	Protection Diode	Function
A2	ACKS	I	TVDD/DVSS	Auto Setting Mode Select Pin in Pin Control Mode (PSN pin = "H") "L": Manual Setting Mode, "H": Auto Setting Mode
	CAD1	I		Chip Address 1 Pin in Register Control Mode (PSN pin = "L")
A3	TDM0	I	TVDD/DVSS	TDM Mode Select Pin in Pin Control mode (PSN pin="H")
	DCLK	I		DSD Clock Pin in DSD Mode (PSN pin="L", DSDPATH bit ="0")
A4	INVR	I	TVDD/DVSS	Rch signal Invert pin in Pin Control Mode
A5	VREFHR	I	VDDR/VSSR	Rch High Level Voltage Reference Input Pin
A6	VREFHR	I	VDDR/VSSR	Rch High Level Voltage Reference Input Pin
A7	VREFLR	I	VDDR/VSSR	Rch Low Level Voltage Reference Input Pin
A8	VREFLR	I	VDDR/VSSR	Rch Low Level Voltage Reference Input Pin
A9	AOUTRN	O	VDDR/VSSR	Rch Negative Analog Output Pin
B1	DEM0	I	TVDD/DVSS	De-emphasis Enable 0 Pin in Pin Control Mode (PSN pin="H")
	DSDL	I		DSD Lch Data Input Pin in DSD Mode (PSN pin = "L", DSDPATH bit = "0")
B2	GAIN	I	TVDD/DVSS	Output Gain Control Pin in Pin Control Mode (PSN pin = "H") "L":Output Level 2.8 Vpp, "H": Output Level 3.75 Vpp
	DSDR	I		DSD Rch Data Input Pin in DSD Mode (PSN pin = "L", DSDPATH bit = "0")
B3	TDM1	I	TVDD/DVSS	TDM Mode Select Pin in Pin Control Mode
B4	DCHAIN	I	TVDD/DVSS	Daisy Chain Mode Select Pin in Pin Control Mode
B5	TESTE	I	TVDD/DVSS	Test mode Enable Pin(Internal pull-down pin)
B8	VCMR	I	VDDR/VSSR	Right channel Common Voltage Pin, Normally connected to VREFLR with a 1uF electrolytic cap. This pin is inhibited to connect other devices.
B9	AOUTRP	O	VDDR/VSSR	Rch Positive Analog Output Pin
C1	DIF1	I	TVDD/DVSS	Digital Input Format 1 Pin in Pin Control Mode (PSN pin = "H")
	DZFR	O		Rch Zero Input Detect Pin in Register Control Mode (PSN pin = "L") (Internal pull-down pin)
C2	HLOAD	I	TVDD/DVSS	Heavy Load Mode Enable Pin in Pin Control Mode (PSN pin = "H") "L":Normal Drive Mode, "H": Heavy Load Drive Mode
	I2C	I		Resister Control Interface Pin in Register Control Mode (PSN pin = "L") "L": 3 Wire Serial Mode, "H": I^2C-Bus Mode
C9	VDDR	-	-	Rch Analog Power Supply Pin
C10	VDDR	-	-	Rch Analog Power Supply Pin
D1	DIF0	I	TVDD/DVSS	Digital Input Format 0 Pin in Pin Control Mode (PSN pin = "H")
	DZFL	O		Lch Zero Input Detect Pin in Register Control Mode (PSN pin="L")(Internal pull-down pin)
D2	DIF2	I	TVDD/DVSS	Digital Input Format 2 Pin in Pin Control Mode (PSN pin = "H")
	CAD0	I		Chip Address 0 Pin in Register Control Mode (PSN pin = "L")
D3	PSN	I	TVDD/DVSS	Pin Control Mode or Register Control Mode Select Pin (Internal pull-down pin) "L": Register Control Mode, "H": Pin Control Mode
D9	VDDR	-	-	Rch Analog Power Supply Pin
D10	VSSR	-	-	Analog Ground Pin

No.	Pin Name	I/O	Protection Diode	Function
E1	SLOW	I	― /DVSS	Digital Filter Select Pin in Pin Control Mode (PSN pin = “H”)
	CDTI	I		Control Data Input Pin in Register Control Mode (PSN pin = “L”, I2C pin = “L”)
	SDA	I/O		Control Data Input Pin (PSN pin = “L”, I2C pin = “H”)
E2	SD	I	― /DVSS	Digital Filter Select Pin in Pin Control Mode (PSN pin = “H”)
	CCLK	I		Control Data Clock Pin in Register Control Mode (PSN pin = “L”, I2C pin = “L”)
	SCL	I		Control Data Clock Input Pin (PSN pin = “L”, I2C pin = “H”)
E9	VSSR	-	-	Analog Ground Pin
E10	VSSR	-	-	Analog Ground Pin
F1	SMUTE	I	TVDD/DVSS	Soft Mute Pin in Pin Control Mode (PSN pin = “H”) When this pin is changed to “H”, soft mute cycle is initiated. When returning “L”, the output mute releases.
	CSN	I		Chip Select Pin in Register Control Mode (PSN pin = “L”, I2C pin = “L”)
				This Pin should be connected to DVSS (PSN pin = “L”, I2C pin = “H”)
F2	TDMO	O	TVDD/DVSS	Audio Data Onput in Daisy Chain Mode (Internal pull-down pin)
F9	VSSL	-	-	Analog Ground Pin
F10	VSSL	-	-	Analog Ground Pin
G1	LRCK	I	TVDD/DVSS	L/R Clock Pin in PCM Mode
	DINR	I		Rch Audio Data Input Pin in EXDF Mode
	DSDR	I		DSD Rch Data Input Pin in DSD Mode (DSDPATH bit = “1”)
G2	SSLOW	I	TVDD/DVSS	Digital Filter Select Pin in Pin Control Mode (PSN pin= “H”)
	WCK	I		Word Clock input Pin in EXDF Mode (PSN pin = “L”)
G9	VDDL	-	-	Lch Analog Power Supply Pin
G10	VSSL	-	-	Analog Ground Pin
H1	SDATA	I	TVDD/DVSS	Audio Data Input Pin in PCM Mode
	DINL	I		Lch Audio Data Input Pin in EXDF Mode
	DSDL	I		DSD Lch Data Input Pin in DSD Mode (DSDPATH bit = “1”)
H2	PDN	I	TVDD/DVSS	Power-Up, Power-Down Pin When at “L”, the AK4492 is in power-down mode and is held in reset.The AK4492 must always be reset upon power-up.
H3	LDOE	I	TVDD/DVSS	Internal LDO Enable Pin. “L”: Disable, “H”: Enable
H9	VDDL	-	-	Lch Analog Power Supply Pin
H10	VDDL	-	-	Lch Analog Power Supply Pin
J1	BICK	I	TVDD/DVSS	Audio Data Clock Pin in PCM Mode
	BCK	I		Audio Data Clock Pin in EXDF Mode
	DCLK	I		DSD Clock Pin in DSD Mode (DSDPATH bit = “1”)
J2	TVDD	-	-	Digital Power Supply Pin. LDOE pin = “L”: (DVDD) ~ 3.6 V / LDOE pin = “H”: 3.0 ~ 3.6V
J3	MCLK	I	AVDD/AVSS	Master Clock Input Pin
J4	AVSS	-	-	Analog Ground Pin
J5	EXTR	I	VDDL/VSSL	External Resistor Connect Pin Rext=33 kΩ(±1 %, Note 1) toAVSS
J8	VCML	-	VDDL/VSSL	Left channel Common Voltage Pin, Normally connected to VREFLL with a 1 uF electrolytic cap. This pin is inhibited to connect other devices.
J9	AOUTLP	O	VDDL/VSSL	Lch Positive Analog Output Pin

No.	Pin Name	I/O	Protection Diode	Function
K2	DVSS	-	-	Digital Ground Pin
K3	DVDD	O	-	(LDOE pin = "H") LDO Output Pin, This pin should be connected to DVSS with 1.0 µF. This pin is inhibited to connect other devices.
		-		(LDOE pin = "L") 1.8 V Power Input Pin
K4	AVDD	-	-	Analog Power Supply Pin. LDOE pin = "L": (DVDD) ~ 3.6 V / LDOE pin = "H": 3.0 ~ 3.6 V
K5	VREFHL	I	VDDL/VSSL	Lch High Level Voltage Reference Input Pin
K6	VREFHL	I	VDDL/VSSL	Lch High Level Voltage Reference Input Pin
K7	VREFLL	I	VDDL/VSSL	Lch Low Level Voltage Reference Input Pin
K8	VREFLL	I	VDDL/VSSL	Lch Low Level Voltage Reference Input Pin
K9	AOUTLN	O	VDDL/VSSL	Lch Negative Analog Output Pin

Note 1. It is recommended to use a resistor with 0.1% absolute error in Fs Auto Detect Mode.
Note 2. All input pins except for internal pull-up/down pins must not be left floating.
Note 3. Reset by PDN pin when changing control mode(Pin Control ⇔ Register Control) by PSN pin.
Note 4. PCM mode, DSD mode and EXDF mode are controlled by register settings.

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

(1) Pin Control Mode (PCM mode only)

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN, AOUTRP, AOUTRN	Open
	TESTE	Connect to AVSS or Open

(2) Resister Control Mode

1. PCM Mode

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN, AOUTRP, AOUTRN	Open
	TESTE	Connect to AVSS or Open
Digital	DCLK, DSDL, DSDR, WCK, TDM1, DCHAIN, INVR	Connect to DVSS
	TDMO, DZFR, DZFL	Open
	CSN	Connect to DVSS (I2C pin = "H")

2. DSD Mode

DSDPATH bit = "0"

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN, AOUTRP, AOUTRN	Open
	TESTE	Connect to AVSS or Open
Digital	WCK, TDM1, DCHAIN, INVR	Connect to DVSS
	TDMO, DZFR, DZFL	Open
	CSN	Connect to DVSS (I2C pin = "H")

DSDPATH bit = "1"

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN, AOUTRP, AOUTRN	Open
	TESTE	Connect to AVSS or Open
Digital	DCLK, DSDL, DSDR, WCK, TDM1, DCHAIN, INVR	Connect to DVSS
	TDMO, DZFR, DZFL	Open
	CSN	Connect to DVSS (I2C pin = "H")

3. EXDF Mode

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN, AOUTRP, AOUTRN	Open
	TESTE	Connect to AVSS or Open
Digital	DCLK, DSDL, DSDR, TDM1, DCHAIN, INVR	Connect to DVSS
	TDMO, DZFR, DZFL	Open
	CSN	Connect to DVSS (I2C pin = "H")

4. Pull-up, Pull-down Pin List

Classification	Pin Name	Status
Pull-down pin (typ = 100 kΩ)	TDMO, DZFL, DZFR, PSN	DVSS
	TESTE	DVSS

6. Absolute Maximum Ratings

(AVSS = DVSS = VSSL = VSSR = VREFLL = VREFLR = 0 V; Note 5)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Digital I/O	TVDDam	−0.3	6.0	V
	Digital Core	DVDDam	−0.3	2.5	V
	Clock Ineterface	AVDDam	−0.3	6.0	V
	Analog	VDDL/Ram	−0.3	6.0	V
	|AVSS − DVSS| (Note 6)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 7)		VIND	−0.3	(TVDD+0.3) or 6.0	V
Ambient Temperature (Power supplied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 5. All voltages with respect to ground.
Note 6. AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane.
Note 7. Max value of VIND is lower either of (TVDD + 0.3) or 6.0V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS = DVSS = VSSL = VSSR = VREFLL = VREFLR = 0 V; Note 5)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	■ LDOE pin = "L"					
	Digital I/O	TVDD	DVDD	1.8	3.6	V
	Clock Ineterface	AVDD	DVDD	1.8	3.6	V
	Digital Core	DVDD	1.7	1.8	1.98	V
	Analog	VDDL/R	4.75	5.0	5.25	V
	■ LDOE pin = "H"					
	Digital I/O	TVDD	3.0	3.3	3.6	V
	Clock Ineterface	AVDD	3.0	3.3	3.6	V
	Analog	VDDL/R	4.75	5.0	5.25	V
Voltage Reference (Note 8)	"H" voltage reference	VREFHL/R	VDDL/R-0.5	-	VDDL/R	V
	"L" voltage reference	VREFLL/R	-	VSSL/R	-	V

Note 5. All voltages with respect to ground.
Note 8. The analog output voltage scales with the voltage of (VREFHL/R − VREFLL/R).
Note 9. TVDD and AVDD must be connected to the same ground plane and powered up at the same time. When not using the LDO (LDOE pin = "L"), all power supplies (DVDD (1.8V), TVDD and AVDD (3.3V) and VDDL/R (5V)) should be powered up at the same time or sequentially in the order of 3.3V (TVDD, AVDD), 1.8V (DVDD) and 5V (VDDL/R).
Note 10. The internal LDO outputs DVDD (1.8V) when the LDOE pin = "H". 3.3V (TVDD and AVDD) power supplies must be powered up before or at the same time with 5V (VDDL/R) power supplies when the LDOE pin = "H".

*** AKM assumes no responsibility for the usage beyond the conditions in this data sheet.**

8. Electrical Characteristics

■ Analog Characteristics

■ PCM Mode

(Ta = 25 °C; LDOE pin = "L", AVDD = TVDD = DVDD = 1.8 V, AVSS = DVSS = VSSL/R = 0 V; VREFHL/R = VDDL/R = 5.0 V, VREFLL/R= 0V; Input data = 24 bit; BICK = 64 fs; Signal Frequency = 1 kHz; Sampling Frequency = 44.1 kHz; Measurement bandwidth = 20 Hz ~ 20 kHz; 2 Vrms output mode (GC[2:0] bits = "000" or GAIN pin = "L"); Heavy load drive mode = off(HLOAD bit = "0" or HLOAD pin = "L"); unless otherwise specified.)

Parameter					Min.	Typ.	Max.	Unit
Resolution					-	-	32	Bit
Dynamic Characteristics (Note 11)								
THD+N	fs=44.1kHz	BW=20kHz	0dBFS	GC[2:0]= "000" or GAIN="L"	-	-115	-	dB
				GC[2:0]="100" or GAIN="H"	-	-111	-	dB
			−60dBFS		-	-61	-	dB
	fs=96kHz	BW=40kHz	0dBFS		-	-111	-	dB
			−60dBFS		-	-57	-	dB
	fs=192kHz	BW=40kHz	0dBFS		-	-111	-	dB
			−60dBFS		-	-57	-	dB
		BW=80kHz	−60dBFS		-	-52	-	dB
Dynamic Range (−60dBFS with A-weighted)					-	123	-	dB
				(Note 12)	-	127	-	dB
S/N (A-weighted)	GC[2:0]= "000" or GAIN="L"				-	123	-	dB
				(Note 12)	-	127	-	dB
	GC[2:0]= "100" or GAIN="H"				-	125	-	dB
				(Note 12)	-	129	-	dB
Interchannel Isolation (1kHz)					110	120	-	dB
DC Accuracy (Note 13)								
Interchannel Gain Mismatch					-	0.15	0.3	dB
Gain Drift					-	20	-	ppm/°C
Output Voltage	GC[2:0]="000" or GAIN pin="L" (Note 14)				±2.65	±2.8	±2.95	Vpp
	GC[2:0]="100" or GAIN pin="H" (Note 15)				±3.55	±3.75	±3.95	Vpp
Load Resistance (Note 16)	HLOAD="0" or HLOAD pin="L"				400	-	-	Ω
	HLOAD="1" or HLOAD pin="H"				300	-	-	Ω
Load Capacitance				(Note 17)	-	-	25	pF

Note 11. Measured by Audio Precision APx555. Averaging mode.

Note 12. The value of as IC single AK4492. It is a calculated value to remove the noise of External Circuit Figure 74 and the measuring instrument.

Note 13. The value of as IC single AK4492.

Note 14. The analog output voltage with 0dBFS input signal when GC[2:0] bits = "000" or the GAIN pin = "L" is calculated by the following formula.

AOUTL/R (typ.@0dB) = (AOUT+) − (AOUT−) = ±2.8Vpp × (VREFHL/R − VREFLL/R)/5.

Note 15. The analog output voltage with 0dBFS input signal when GC[2:0] bits = "100" or the GAIN pin = "H" is calculated by the following formula.

AOUTL/R (typ.@0dB) = (AOUT+) − (AOUT−) = ±3.75Vpp × (VREFHL/R − VREFLL/R)/5.

Note 16. The load resistance value with respect to ground. 10.3 System Design Analog Output shows the circuits and the calculataion example.

Note 17. The load capacitance value with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore the capacitive load must be minimized.

Note 18. It is recommended to use a resistor with 0.1% absolute error for the output stage of the adding circuit.

(Ta = 25 °C; LDOE pin = “L”, AVDD = TVDD = DVDD = 1.8 V, AVSS = DVSS = VSSL/R = 0 V; VREFHL/R = VDDL/R = 5.0 V, VREFLL/R = 0V; Input data = 24 bit; BICK = 64 fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; 2 Vrms output mode (GC[2:0] bits = “000” or GAIN pin = “L”); Heavy load drive mode = off(HLOAD bit=“0” or HLOAD pin=“L”); unless otherwise specified.)

Power Supplies					
Parameter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Supply Current				
Normal operation (PDN pin = “H”)				
VDDL+VDDR	-	27	40	mA
VREFHL+VREFHR	-	1.6	3	mA
AVDD	-	0.4	1.5	mA
TVDD				
LDOE pin = “H” fs = 44.1 kHz		6	9	mA
LDOE pin = “H” fs = 96 kHz	-	10	15	mA
LDOE pin = “H” fs = 192 kHz	-	18	27	mA
LDOE pin = “L”	-	0.3	1.5	mA
DVDD				
LDOE pin = “L” fs = 44.1 kHz	-	6	9	mA
LDOE pin = “L” fs = 96 kHz	-	10	15	mA
LDOE pin = “L” fs = 192 kHz	-	18	27	mA
Total Idd (fs = 44.1 kHz, LDOE pin = “L”)	-	35.4	55	mA
Power down (PDN pin = “L”) (Note 19) TVDD + AVDD + VDDL + VDDR + DVDD	-	0.4	100	μA

Note 19. In power down mode, the PSN pin = TVDD and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held to DVSS.

Note 20. The DVDD pin becomes an output pin when the LDOE pin = “H”.

■ DSD Mode

(Ta = 25 °C; LDOE pin = "L", AVDD = TVDD = DVDD = 1.8 V; AVSS = DVSS = VSSL/R = 0 V; VREFHL/R = VDDL/R = 5.0 V, VREFLL/R = 0 V; Signal Frequency = 1 kHz; Measurement bandwidth = 20 Hz ~ 20 kHz; External Circuit: Figure 74; 2 Vrms output mode (GC[2:0] bits = "000" or GAIN pin = "L"); unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Dynamic Characteristics						
THD+N (Note 21)	DSD data stream: 2.8224 MHz	0dB	-	-111	-	dB
	DSD data stream: 5.6448 MHz	0dB	-	-112	-	dB
	DSD data stream: 11.2896 MHz	0dB	-	-107	-	dB
S/N (A-weighted, Normal path) (Note 21)	DSD data stream: 2.8224 MHz	Digital"0" (Note 24)	-	123	-	dB
	DSD data stream: 5.6448 MHz	Digital"0" (Note 24)	-	123	-	dB
	DSD data stream: 11.2896 MHz	Digital"0" (Note 24)	-	123	-	dB
DC Accuracy						
Output Voltage (Normal path)		(Note 25)	±2.65	±2.8	±2.95	Vpp
Output Voltage (Volume Bypass)		(Note 25)	±2.38	±2.5	±2.63	Vpp

Note 21. References values in using AK4137 as the input source. This value does not change by increasimg the signal amplitude with gain adjustment function.

Note 22. The peak level of DSD signal should be in the range of 25% ~ 75% duty according to the SACD format book (Scarlet Book).

Note 23. The output level is assumed as 0dB when a 1kHz 25% ~ 75% duty sine wave is input. Click noise may occur if the input signal exceeds 0dB.

Note 24. Digital "0" is a digital zero code pattern ("01101001") according to the SACD format book (Scarlet Book).

Note 25. In case of GC[2:0] = "000" and DSDD bit = "1", the analog output voltage at input signal = 0dB is following equation.

AOUTL/R (typ.@0 dB) = (AOUTLP/RP) − (AOUTLN/RN) = ±2.5 Vpp × (VREFHL/R − VREFLL/R)/5

.

■ Sharp Roll-Off Filter Characteristics

Sharp Roll-Off Filter Characteristics (fs=44.1kHz)

(Ta = -40~85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7 ~ 1.98 V; Normal Speed Mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin ="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.01 dB −6.0 dB (Note 26)	- -	0 -	 22.05	20.0 -	kHz kHz
Passband	(Note 27)	PB	0		20.0	kHz
Stopband	(Note 27)	SB	24.1			kHz
Passband Ripple	(Note 28)	PR			±0.005	dB
Stopband Attenuation	(Note 26)	SA	100			dB
Group Delay	(Note 29)	GD	-	29.2	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 20.0 kHz			-0.7	-	+0.1	dB

Sharp Roll-Off Filter Characteristics (fs=96kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6V, DVDD = 1.7~1.98V; Double Speed Mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.01dB −6.0 dB (Note 26)	- -	0 -	 48.0	43.5 -	kHz kHz
Passband	(Note 27)	PB	0		43.5	kHz
Stopband	(Note 27)	SB	52.5			kHz
Passband Ripple	(Note 28)	PR			±0.005	dB
Stopband Attenuation	(Note 26)	SA	100			dB
Group Delay	(Note 29)	GD	-	29.2	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 40.0 kHz			-1.9	-	+0.1	dB

Sharp Roll-Off Filter Characteristics (fs=192kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Quad Speed Mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Responce	±0.01 dB −6.0 dB (Note 26)	- -	0 -	 96.0	87.0 -	kHz kHz
Passband	(Note 27)	PB	0		87.0	kHz
Stopband	(Note 27)	SB	104.9			kHz
Passband Ripple	(Note 28)	PR			±0.005	dB
Stopband Attenuation	(Note 26)	SA	100			dB
Group Delay	(Note 29)	GD	-	29.2	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 80.0kHz			-5.0	-	+0.1	dB

Note 26. Frequency response refers to the output level (0dB) of a 1kHz, 0dB sine wave input.

Note 27. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

Note 28. The first stage of the Interpolator. This is a passband gain amplitude of the 4 times oversampling filter.

Note 29. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32 bit data of both channels to the output of analog signal.

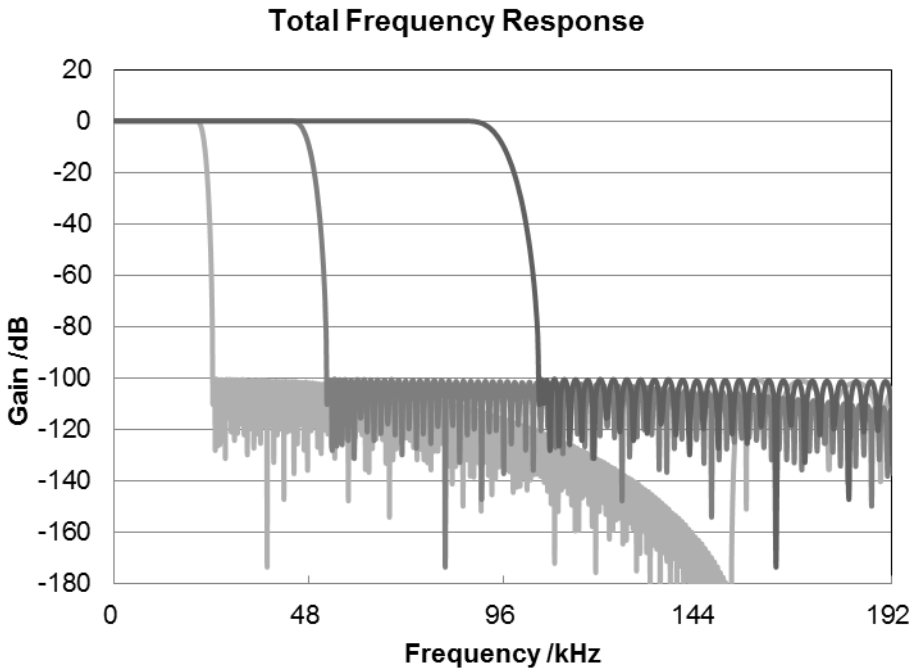


Figure 3. Sharp Roll-off Filter Frequency Response

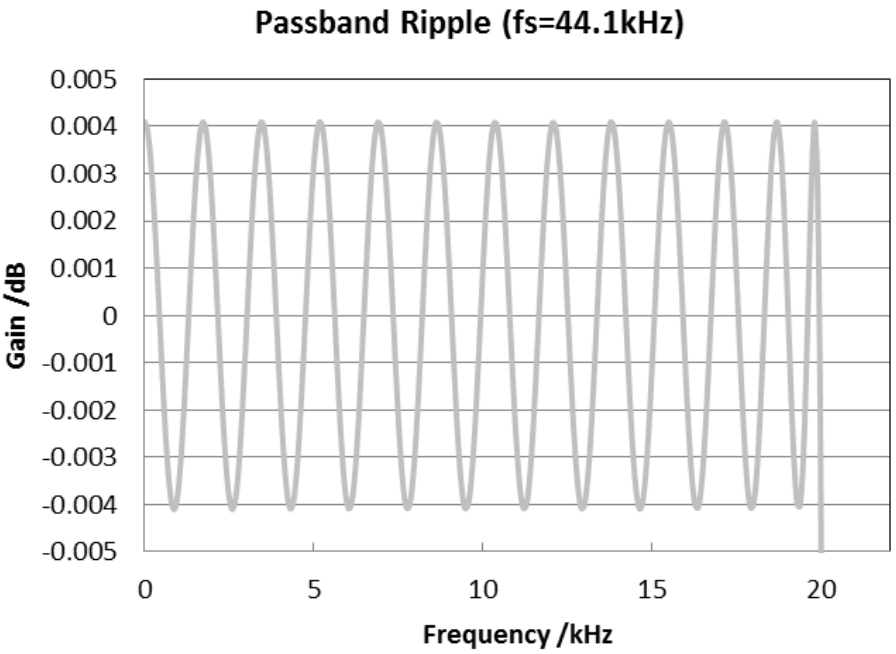


Figure 4. Sharp Roll-off Filter Passband Ripple

■ Slow Roll-Off Filter Characteristics

Slow Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta = -40 ~ 85° C; VDDL/R = 4.75 ~ 5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Normal Speed Mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.01dB −6.0dB (Note 26)	- -	0 -	 21.0	8.0 -	kHz kHz
Passband	(Note 30)	PB	0		8.0	kHz
Stopband	(Note 30)	SB	39.2			kHz
Passband Ripple	(Note 28)	PR			±0.007	dB
Stopband Attenuation	(Note 26)	SA	92			dB
Group Delay	(Note 29)	GD	-	6.5	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 20.0 kHz			-5.5	-	+0.1	dB

Slow Roll-Off Filter Characteristics (fs = 96kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Double Speed Mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Responce	±0.01 dB −6.0 dB (Note 26)	- -	0 -	 45.6	17.6 -	kHz kHz
Passband	(Note 30)	PB	0		17.6	kHz
Stopband	(Note 30)	SB	85.4			kHz
Passband Ripple	(Note 28)	PR			±0.007	dB
Stopband Attenuation	(Note 26)	SA	100			dB
Group Delay	(Note 29)	GD	-	6.5	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 40.0 kHz			-5.1	-	+0.1	dB

Slow Roll-Off Filter Characteristics (fs = 192kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Quad Speed Mode; DEM = OFF; SD bit or SD pin = "0", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Responce	±0.01 dB −6.0 dB (Note 26)	- -	0 -	 91.2	35.2 -	kHz kHz
Passband	(Note 30)	PB	0		35.2	kHz
Stopband	(Note 30)	SB	170.7			kHz
Passband Ripple	(Note 28)	PR			±0.007	dB
Stopband Attenuation	(Note 26)	SA	100			dB
Group Delay	(Note 29)	GD	-	6.5	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 80.0kHz			-8.0	-	+0.1	dB

Note 30. The passband and stopband frequencies scale with fs. For example, PB = 0.1836 × fs (@±0.01dB), SB = 0.8889 × fs.

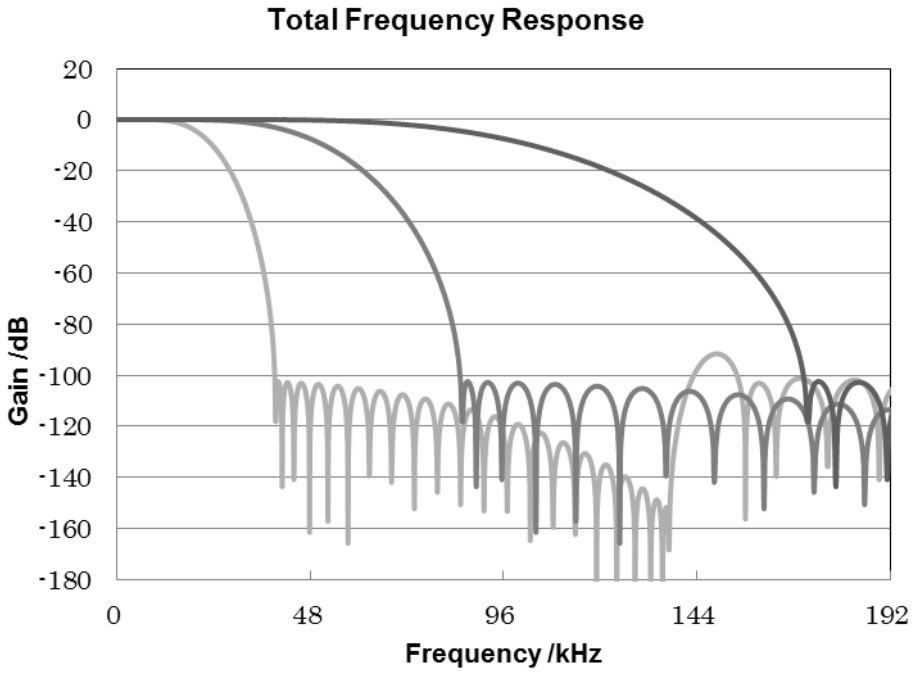


Figure 5. Slow Roll-off Filter Frequency Response

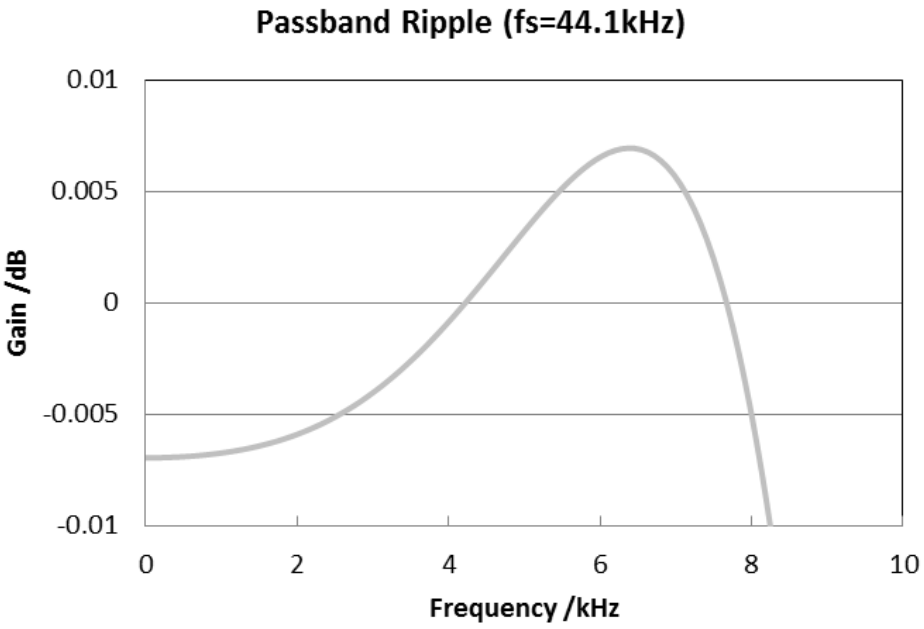


Figure 6. Slow Roll-off Filter Passband Ripple

■ Short Delay Sharp Roll-Off Filter Characteristics

Short Delay Sharp Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Normal Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency	±0.01 dB	-	0		20.0	kHz
Responce	−6.0 dB (Note 26)	-	-	22.05	-	kHz
Passband (Note 31)		PB	0		20.0	kHz
Stopband (Note 31)		SB	24.1			kHz
Passband Ripple (Note 30)		PR			±0.005	dB
Stopband Attenuation (Note 26)		SA	100			dB
Group Delay (Note 29)		GD	-	6.0	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 20.0 kHz			-0.7	-	+0.1	dB

Short Delay Sharp Roll-Off Filter Characteristics (fs = 96kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Double Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency	±0.01 dB	-	0		43.5	kHz
Responce	−6.0 dB (Note 26)	-	-	48.0	-	kHz
Passband (Note 31)		PB	0		43.5	kHz
Stopband (Note 31)		SB	52.5			kHz
Passband Ripple (Note 28)		PR			±0.005	dB
Stopband Attenuation (Note 26)		SA	100			dB
Group Delay (Note 29)		GD	-	6.0	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 40.0 kHz			-1.9	-	+0.1	dB

Short Delay Sharp Roll-Off Filter Characteristics (fs = 192kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Quad Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency	±0.01 dB	-	0		87.0	kHz
Responce	−6.0 dB (Note 26)	-	-	96.0	-	kHz
Passband (Note 31)		PB	0		87.0	kHz
Stopband (Note 31)		SB	104.9			kHz
Passband Ripple (Note 28)		PR			±0.005	dB
Stopband Attenuation (Note 26)		SA	100			dB
Group Delay (Note 29)		GD	-	6.0	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 80.0 kHz			-5.0	-	+0.1	dB

Note 31. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

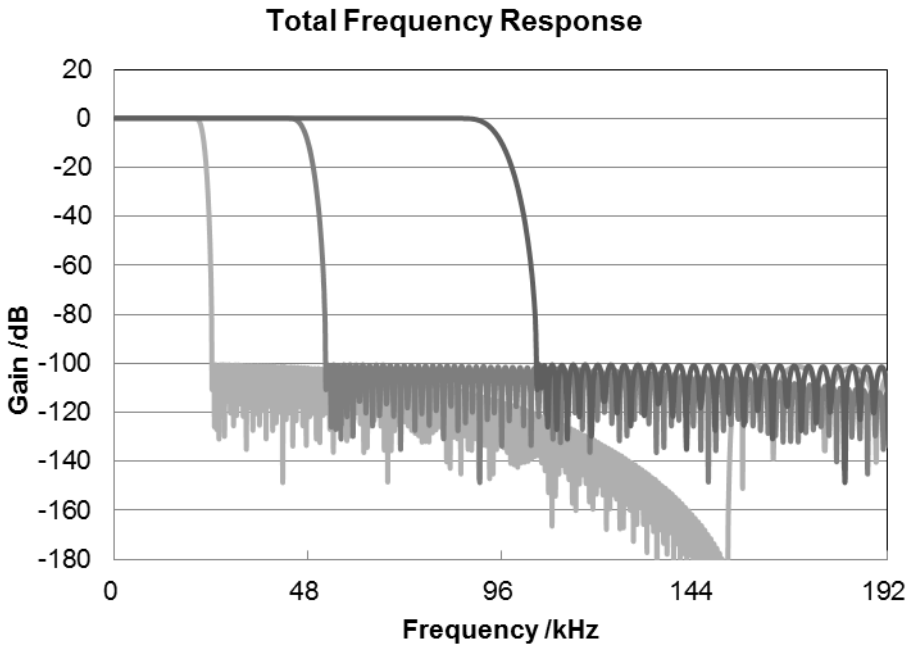


Figure 7. Short Delay Sharp Roll-off Filter Frequency Response

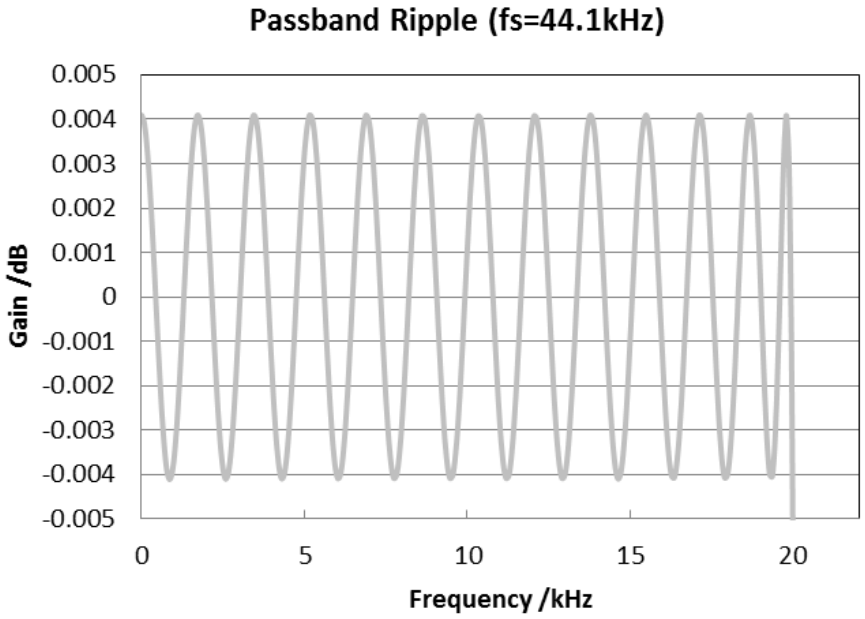


Figure 8. Short Delay Sharp Roll-off Filter Passband Ripple

■ Short Delay Slow Roll-Off Filter Characteristics

Short Delay Slow Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Normal Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency	±0.01 dB	-	0		8.0	kHz
Responce	−6.0 dB (Note 26)	-	-	21.0	-	kHz
Passband (Note 32)		PB	0		8.0	kHz
Stopband (Note 32)		SB	39.2			kHz
Passband Ripple (Note 28)		PR			±0.007	dB
Stopband Attenuation (Note 26)		SA	92			dB
Group Delay (Note 29)		GD	-	5.0	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 20.0 kHz			-5.5	-	+0.1	dB

Short Delay Slow Roll-Off Filter Characteristics (fs = 96kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Double Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency	±0.01 dB	-	0	-	17.6	kHz
Response	−6.0 dB (Note 26)	-	-	45.6	-	kHz
Passband (Note 32)		PB	0	-	17.6	kHz
Stopband (Note 32)		SB	85.4	-	-	kHz
Passband Ripple (Note 28)		PR	-	-	±0.007	dB
Stopband Attenuation (Note 26)		SA	100	-	-	dB
Group Delay (Note 29)		GD	-	5.0	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 40.0 kHz			-5.1	-	+0.1	dB

Short Delay Slow Roll-Off Filter Characteristics (fs = 192kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75 ~ 5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Quad Speed Mode; DEM = OFF; SD bit or SD pin = "1", SLOW bit or SLOW pin = "1", SSLOW bit or SSLOW pin = "0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency	±0.01 dB	-	0	-	35.2	kHz
Response	−6.0 dB (Note 26)	-	-	91.2	-	kHz
Passband (Note 32)		PB	0	-	35.2	kHz
Stopband (Note 32)		SB	170.7	-	-	kHz
Passband Ripple (Note 28)		PR	-	-	±0.007	dB
Stopband Attenuation (Note 26)		SA	100	-	-	dB
Group Delay (Note 29)		GD	-	5.0	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 80.0 kHz			-8.0	-	+0.1	dB

Note 32. The passband and stopband frequencies scale with fs. For example, PB = 0.1836 × fs (@±0.01dB), SB = 0.8866 × fs.

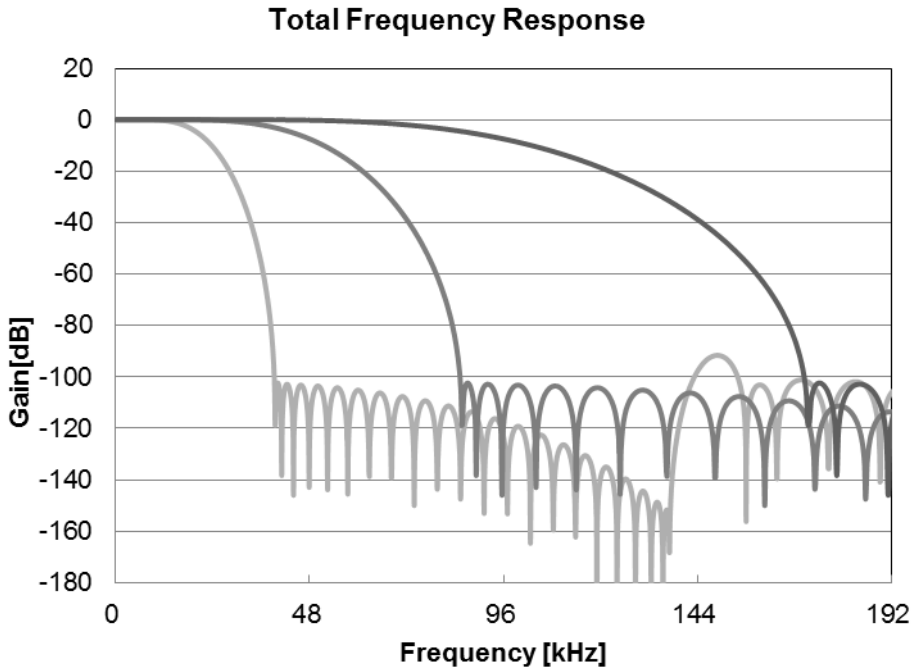


Figure 9. Short Delay Slow Roll-off Filter Frequency Response

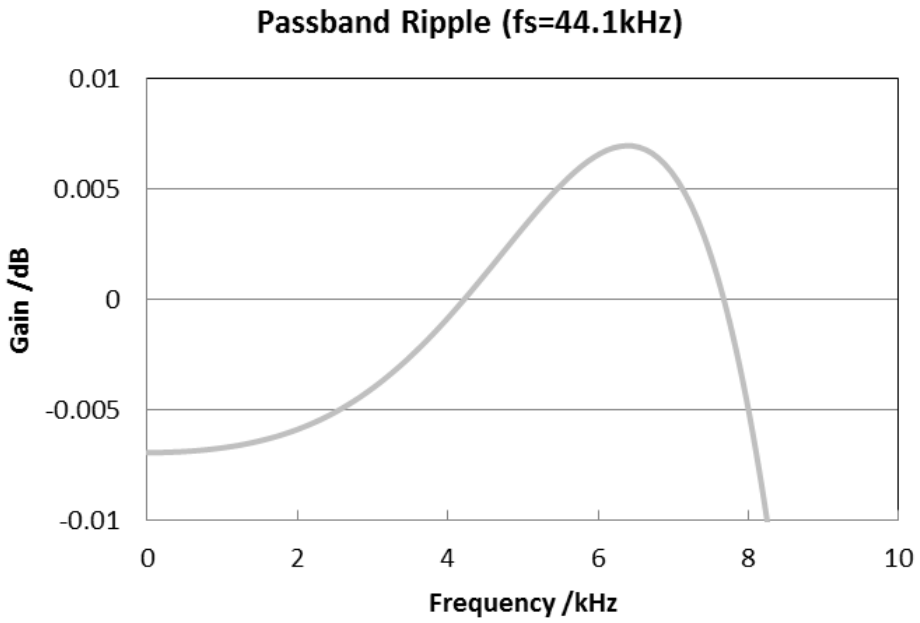


Figure 10. Short Delay Slow Roll-off Filter Passband Ripple

■ Low-dispersion Short Delay Filter Characteristics

Low-dispersion Short Delay Filter Characteristics (fs = 44.1kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Normal Speed Mode; DEM = OFF; SD bit pr SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.05 dB −6.0 dB (Note 26)	- -	0 -	- 22.05	18.4 -	kHz kHz
Passband	(Note 33)	PB	0	-	18.4	kHz
Stopband	(Note 33)	SB	25.7	-	-	kHz
Passband Ripple	(Note 33)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 26)	SA	80	-	-	dB
Group Delay	(Note 29)	GD	-	10.0	-	1/fs
Group Delay Distortion		ΔGD	-	±0.035	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 20.0 kHz			-1.2	-	+0.1	dB

Low-dispersion Short Delay Filter Characteristics (fs = 96kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75~5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Double Speed Mode; DEM = OFF; SD bit pr SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.05 dB −6.0 dB (Note 26)	- -	0 -	- 48.0	40.1 -	kHz kHz
Passband	(Note 33)	PB	0	-	40.1	kHz
Stopband	(Note 33)	SB	55.9	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 26)	SA	80	-	-	dB
Group Delay	(Note 29)	GD	-	10.0	-	1/fs
Group DelayDistortion		ΔGD	-	±0.035	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 40.0 kHz			-1.9	-	+0.1	dB

Low-dispersion Short Delay Filter Characteristics (fs = 192kHz)

(Ta = -40 ~ 85 °C; VDDL/R = 4.75 ~ 5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; Quad Speed Mode; DEM = OFF; SD bit pr SD pin = "1", SLOW bit or SLOW pin = "0", SSLOW bit or SSLOW pin = "1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.05 dB −6.0 dB (Note 26)	- -	0 -	- 96.0	80.2 -	kHz kHz
Passband	(Note 33)	PB	0	-	80.2	kHz
Stopband	(Note 33)	SB	111.8	-	-	kHz
Passband Ripple	(Note 28)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 26)	SA	80	-	-	dB
Group Delay	(Note 29)	GD	-	10.0	-	1/fs
Group Delay Distortion		ΔGD	-	±0.035	-	1/fs
Digital Filter + SCF (Note 26)						
Frequency Response: 0 ~ 80.0 kHz			-5.0	-	+0.1	dB

Note 33. The passband and stopband frequencies scale with fs. For example, PB = 0.418 × fs (@±0.05dB), SB = 0.582 × fs.

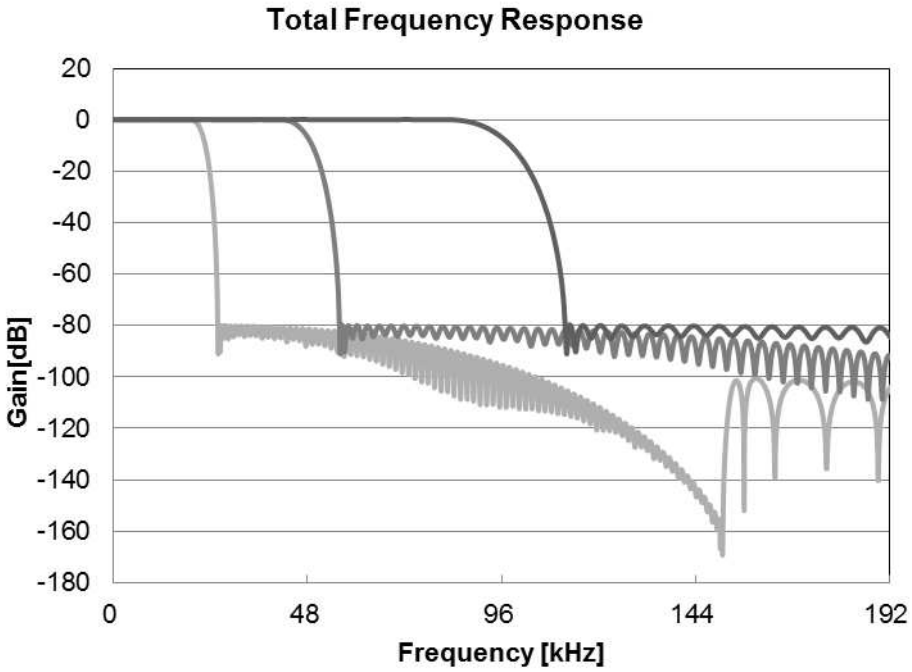


Figure 11. Low Dispersion Shortdelay Filter Frequency Responce

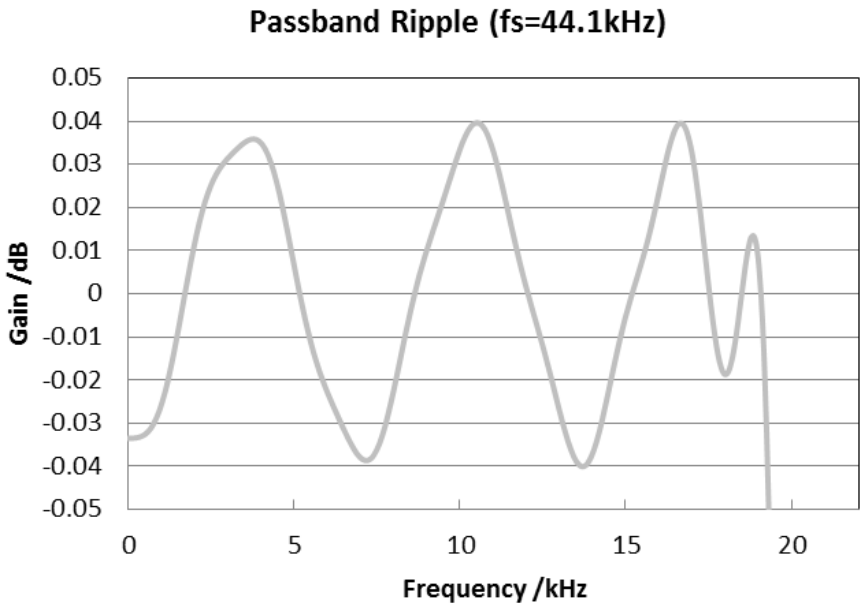


Figure 12. Low Dispersion Shortdelay Filter PassbandRipple

■ DSD Filter Characteristics

(Ta = -40 ~ 85 °C; VDDL/R = 4.75 ~ 5.25 V, AVDD = TVDD = (DVDD) ~ 3.6 V, DVDD = 1.7~1.98 V; fs = 44.1 kHz; DP bit = "1", DSDSEL[1:0] bits = "00")

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response (Note 34)					
DSDF bit = "0"	20 kHz	-	-0.77	-	dB
	50 kHz	-	-5.25	-	dB
	100 kHz	-	-18.80	-	dB
DSDF bit = "1"	20 kHz	-	-0.19	-	dB
	100 kHz	-	-5.29	-	dB
	150 kHz	-	-15.57	-	dB

Note 34. 0dB is the output level when a 1kHz 25% ~ 75% duty sibne wave is input.

Note 35. The frequency(20 k,100 k,150 kHz) is doubled in 128 fs(DSDSEL[1:0] bits = "01"), and it is four times in 256 fs(DSDSEL[1:0] bits = "10").

■ DC Characteristics

(Ta = -40 ~ 85 °C; VDDL/R = 4.75 ~ 5.25 V, AVDD = TVDD = 1.7~3.6 V, DVDD = 1.7~1.98 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
AVDD=TVDD=1.7 ~ 3.0 V					
High-Level Input Voltage	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	20%TVDD	V
AVDD=TVDD=3.0V ~ 3.6 V					
High-Level Input Voltage	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD	V
High-Level Output Voltage (TDMO, DZFL, DZFR pins: Iout = -100 µA)	VOH	TVDD−0.5	-	-	V
Low-Level Output Voltage (except SDA pin: Iout= 100µA)	VOL	-	-	0.5	V
(SDA pin, 2.0 V ≤ TVDD ≤ 3.6 V: Iout = 3mA)	VOL	-	-	0.4	V
(SDA pin, 1.7 V ≤ TVDD ≤ 2.0 V: Iout = 3mA)	VOL	-	-	20%TVDD	V
Input Leakage Current (Note 36)	Iin	-	-	±10	µA

Note 36. The TESTE, TDMO, PSN, DIF0 and DIF1 pins have internal pull-down. The value of resistance is 100 kohm(typical).Therefore the TESTE, TDMO, PSN, DIF0 and DIF1 pins are not included in this specification.