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AK4495S/95

Quality-oriented Premium 32-Bit 2ch DAC

1. General Description

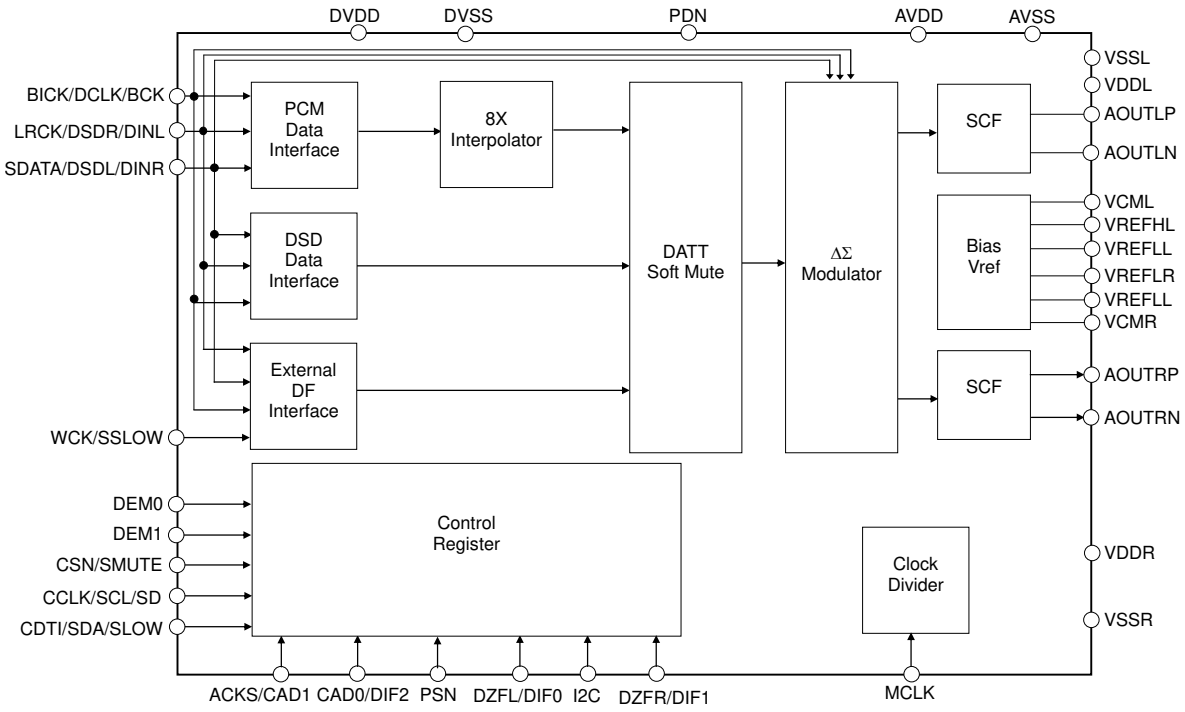
The AK4495S/95 is a 32-bit DAC, which corresponds to high-performance, high sound quality digital audio systems such as DVD-Audio and BD. An internal circuit includes newly developed 32-bit digital filters for better sound quality, achieving low distortion characteristics and wide dynamic range. The AK4495S/95 has full differential SCF outputs, removing the need for AC coupling capacitors and increasing performance for systems with excessive clock jitter. The AK4495S/95 accepts up to 768kHz PCM data and 5.6MHz DSD data, ideal for a wide range of applications including Network Audio and SACD.

2. Features

- **128x Over sampling**
- **Sampling Rate: 30kHz ~ 768kHz**
- **32-bit 8x Digital Filter**
  - **Ripple: ±0.005dB, Attenuation: 100dB**
  - **Short Delay Sharp Roll-off, GD=6.25/fs**
  - **Short Delay Slow Roll-off, GD=5.3/fs**
  - **Sharp Roll-off**
  - **Slow Roll-off**
  - **Super Slow Roll-off**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **2.8MHz, 5.6MHz DSD Input Support**
- **Digital De-emphasis for 32, 44.1, 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (255 levels and 0.5dB step)**
- **Mono Mode**
- **External Digital Filter Mode**
- **THD+N: -101dB, -105dB (Analog Block Power Supply 7V)**
- **DR, S/N: 120dB, 123dB (Mono mode: 126dB, Analog Block Power Supply 7V)**
- **I/F Format: 24/32bit MSB justified, 16/20/24/32bit LSB justified, I^2S, DSD**
- **Master Clock:**
  - **30kHz ~ 32kHz: 1152fs**
  - **30kHz ~ 54kHz: 512fs or 768fs**
  - **30kHz ~ 108kHz: 256fs or 384fs**
  - **108kHz ~ 216kHz: 128fs or 192fs**
  - **~ 384kHz: 64fs or 128fs**
  - **~ 768kHz: 64fs**
- **Power Supply: DVDD=AVDD=3.0~ 3.6V, VDD1/2=4.75 ~ 7.2V**
- **Digital Input Level: CMOS**
- **Package: 44-pin LQFP**

3. Table of Contents

4. Block Diagram and Functions



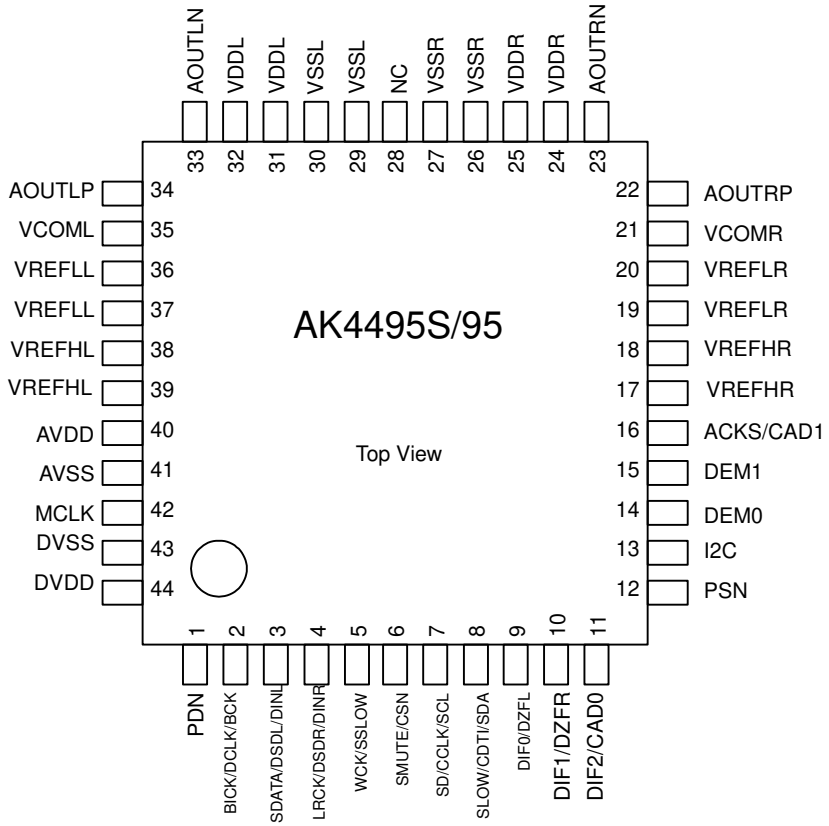
Block Diagram

5. Pin Configuration and Functions

■ Ordering Guide

AK4495EQ	–40 ~ +85°C	44-pin LQFP (0.8mm pitch)
AK4495SEQ	–40 ~ +85°C	44-pin LQFP (0.8mm pitch), Special Sound Quality Package
AKD4495	Evaluation Board for AK4495	
AKD4495S	Evaluation Board for AK4495S	

■ Pin Configuration



■ Functions

No.	Pin Name	I/O	Function
1	PDN	I	Power-Down Mode Pin When at "L", the AK4495S/95 is in power-down mode and is held in reset. The AK4495S/95 must always be reset upon power-up.
2	BICK	I	Audio Serial Data Clock Pin in PCM Mode
	DCLK	I	DSD Clock Pin in DSD Mode
	BCK	I	Audio Serial Data Clock Pin
3	SDATA	I	Audio Serial Data Input Pin in PCM Mode
	DSDL	I	DSD Lch Data Input Pin in DSD Mode
	DINL	I	Lch Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin in PCM Mode
	DSDR	I	DSD Rch Data Input Pin in DSD Mode in Serial Control Mode
	DINR	I	Rch Audio Serial Data Input Pin in Serial Control Mode
5	SSLOW	I	Digital filter setting in Parallel Control Mode
	WCK	I	Word Clock input pin in Serial Control Mode
6	SMUTE	I	Soft Mute Pin in Parallel Control Mode When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.
	CSN	I	Chip Select Pin in Serial Control Mode in Serial Control Mode, I2C="L"
7	SD	I	Digital filter setting in Parallel Control Mode
	CCLK	I	Control Data Clock Pin in Serial Control Mode in Serial Control Mode, I2C="L"
	SCL	I	Control Data Clock Pin in Serial Control Mode in Serial Control Mode, I2C="H"
8	SLOW	I	Digital filter setting in Parallel Control Mode
	CDTI	I	Control Data Input Pin in Serial Control Mode in Serial Control Mode, I2C="L"
	SDA	I/O	Control Data Clock Pin in Serial Control Mode in Serial Control Mode, I2C="H"
9	DIF0	I	Digital Input Format 0 Pin in PCM Mode
	DZFL	O	Lch Zero Input Detect Pin in Serial Control Mode
10	DIF1	I	Digital Input Format 1 Pin in PCM Mode
	DZFR	O	Rch Zero Input Detect Pin in Serial Control Mode
11	DIF2	I	Digital Input Format 2 Pin in PCM Mode
	CAD0	I	Chip Address 0 Pin in Serial Control Mode (Internal pull-down pin)
12	PSN	I	Parallel or Serial Select Pin (Internal pull-up pin) "L": Serial Control Mode, "H": Parallel Control Mode
13	I2C	I	I2C mode select pin in Serial mode (Internal pull-down pin)
14	DEM0	I	De-emphasis Enable 0 Pin in Parallel Control Mode (Internal pull-up pin)

Note: All input pins except internal pull-up/down pins must not be left floating.

15	DEM1	I	De-emphasis Enable 1 Pin in Parallel Control Mode (Internal pull-down pin)
16	ACKS	I	Master Clock Auto Setting Mode Pin in Parallel Mode (Internal pull-down pin)
	CAD1	I	Chip Address 1 Pin in Serial Control Mode
17	VREFHR	I	Rch High Level Voltage Reference Input Pin
18	VREFHR	I	Rch High Level Voltage Reference Input Pin
19	VREFLR	I	Rch Low Level Voltage Reference Input Pin
20	VREFLR	I	Rch Low Level Voltage Reference Input Pin
21	VCOMR	-	Right channel Common Voltage Pin, Normally connected to VREFLL with a 10uF electrolytic cap.
22	AOUTRP	O	Rch Positive Analog Output Pin
23	AOUTRN	O	Rch Negative Analog Output Pin
24	VDDR	-	Rch Analog Power Supply Pin, 4.75 ~ 7.2V
25	VDDR	-	Rch Analog Power Supply Pin, 4.75 ~ 7.2V
26	VSSR		Ground Pin
27	VSSR		Ground Pin
28	NC	-	No internal bonding. Connect to GND.
29	VSSL		Ground Pin
30	VSSL		Ground Pin
31	VDDL	-	Lch Analog Power Supply Pin, 4.75 ~ 7.2V
32	VDDL	-	Lch Analog Power Supply Pin, 4.75 ~ 7.2V
33	AOUTLN	O	Lch Negative Analog Output Pin
34	AOUTLP	O	Lch Positive Analog Output Pin
35	VCOML	-	Left channel Common Voltage Pin, Normally connected to VREFLR with a 10uF electrolytic cap.
36	VREFLL	I	Lch Low Level Voltage Reference Input Pin
37	VREFLL	I	Lch Low Level Voltage Reference Input Pin
38	VREFHL	I	Lch High Level Voltage Reference Input Pin
39	VREFHL	I	Lch High Level Voltage Reference Input Pin
40	AVDD	-	Analog Power Supply Pin, 3.0 ~ 3.6V
41	AVSS	-	Ground Pin
42	MCLK	I	Master Clock Input Pin
43	DVSS	-	Ground Pin
44	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V

Note: All input pins except internal pull-up/down pins must not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

(1) Parallel Mode (PCM Mode only)

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	SMUTE	This pin must be connected to DVSS.

(2) Serial Mode

1. PCM Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	DIF2	These pins must be connected to DVSS.
	DZFL, DZFR	These pins must be open.

2. DSD Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
	DZFL, DZFR	These pins must be open.

6. Absolute Maximum Ratings

(AVSS=DVSS=VSSL=VSSR=VREFLL=VREFLR=0V; Note 1)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	−0.3	4.6	V
	Analog	VDDL/R	−0.3	7.5	V
	Digital	DVDD	−0.3	4.6	V
	|AVSS − DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	−0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(AVSS=DVSS=VSSL=VSSR =0V; Note 1)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 3)	Analog	AVDD	3.0	3.3	3.6	V
	Analog	VDDL/R	4.75	5.0	7.2	V
	Digital	DVDD	3.0	3.3	3.6	V
Voltage Reference (Note 4)	"H" voltage reference	VREFHL/R	VDDL/R−0.5	-	VDDL/R	V
	"L" voltage reference	VREFLL/R		VSS	-	V
	VREFH − VREFL	ΔVREF	3.0	-	VDDL/R	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD, VDDL/R and DVDD is not critical.
Note 4. The analog output voltage scales with the voltage of (VREFH − VREFL).
AOUT (typ.@0dB) = (AOUT+) − (AOUT−) = ±2.8Vpp × (VREFHL/R − VREFLL/R)/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

■ Handling of Unused Pin

(Ta=25°C; AVDD=DVDD=3.3V; AVSS=DVSS=VSSL/R=0V; VREFHL/R=VDDL/R=5V, VREFLL/R= VSSL/R=0V; Input data = 24bit; $R_L \geq 1k\Omega$; BICK=64fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: Figure 39; unless otherwise specified.)

Parameter			min	typ	max	Unit
Resolution			-	-	32	Bits
Dynamic Characteristics (Note 5)						
THD+N	fs=44.1kHz BW=20kHz	0dBFS	-	-101	-93	dB
		0dBFS (VDDL/R=VREFHL/R=7.0V)	-	-105	-	dB
		–60dBFS	-	-57	-47	dB
	fs=96kHz BW=40kHz	0dBFS	-	-98	-88	dB
		–60dBFS	-	-54	-44	dB
	fs=192kHz BW=40kHz	0dBFS	-	-98	-88	dB
		–60dBFS	-	-54	-44	dB
	BW=80kHz	–60dBFS	-	-51	-41	dB
Dynamic Range (–60dBFS with A-weighted) (Note 6)			114	120	-	dB
S/N (A-weighted) (Note 7)			114	120	-	dB
S/N (A-weighted, VDDL/R=7.0V)			100	123	-	dB
S/N (Mono mode, A-weighted, VDDL/R=7.0V)			100	126	-	dB
Interchannel Isolation (1kHz)			110	120	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.15	0.3	dB
Gain Drift (Note 8)			-	-	20	ppm/°C
Output Voltage (Note 9)			±2.65	±2.8	±2.95	Vpp
Load Capacitance			-	-	25	pF
Load Resistance (Note 10)			1	-	-	kΩ
Power Supplies						
Power Supply Current						
	Normal operation (PDN pin = "H")					
		VDDL/R		33	42	mA
		AVDD		1	2	mA
		DVDD (fs= 44.1kHz)	-	8	12	mA
		DVDD (fs= 96kHz)	-	14	20	mA
		DVDD (fs = 192kHz)	-	15	23	mA
	Power down (PDN pin = "L") (Note 11)					
		AVDD+VDDL/R+DVDD	-	10	100	μA

Note 5. Measured by Audio Precision, System Two. Averaging mode. Refer to the evaluation board manual. When SC2:SC1:SC0 bit = "010".

Note 6. Figure 39 External LPF Circuit Example 2. 101dB for 16-bit data and 118dB for 20-bit data.

Note 7. Figure 39 External LPF Circuit Example 2. S/N does not depend on input data size.

Note 8. The voltage on (VREFH – VREFL) is held +5V externally.

Note 9. Full-scale voltage(0dB). Output voltage scales with the voltage of (VREFHL/R – VREFLL/R). AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFHL/R – VREFLL/R)/5.

Note 10. Regarding Load Resistance, AC load is 1kΩ (min) with a DC cut capacitor (Figure 39). DC load is 1.5k ohm (min) without a DC cut capacitor (Figure 38). The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore the capacitive load must be minimized.

Note 11. In the power down mode. The PSN pin = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.

■ Sharp Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Normal Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 12)		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	29.4	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-	±0.2	-	dB

■ Sharp Roll-Off Filter Characteristics (fs = 96kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Double Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		43.5	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 12)		SB	52.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	28.8	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-	±0.3	-	dB

■ Sharp Roll-Off Filter Characteristics (fs = 192kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Quad Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 12)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	92			dB
Group Delay (Note 13)		GD	-	28.8	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-	+0/−1	-	dB

Note 12. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

Note 13. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

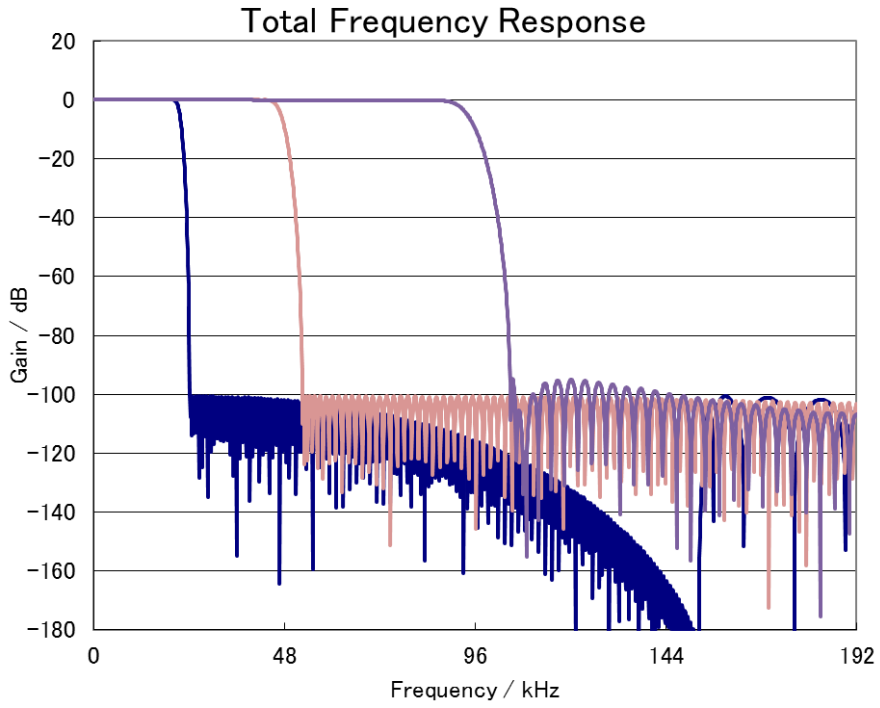


Figure 1. Sharp Roll-off Filter Frequency Response

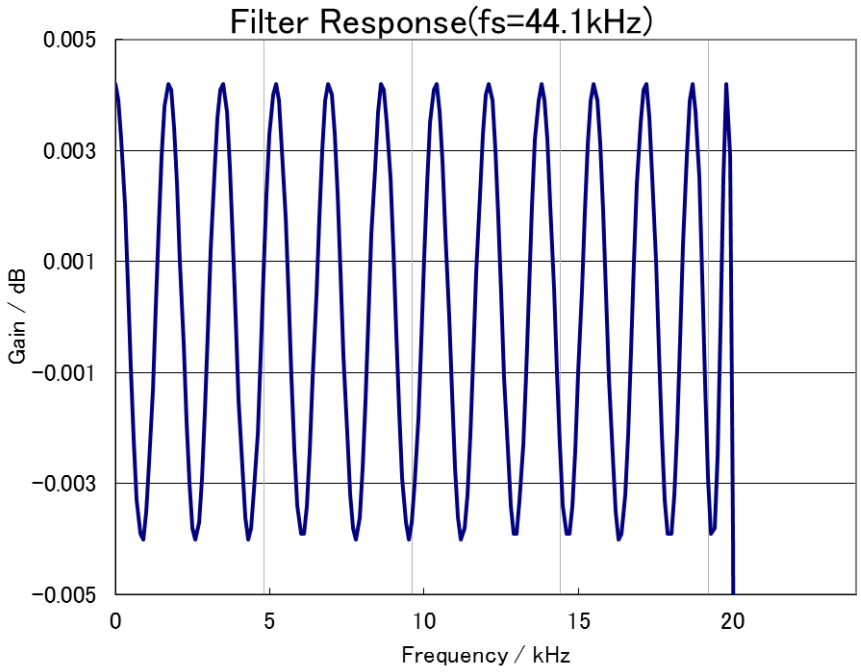


Figure 2. Sharp Roll-off Filter PassBand Ripple

■ Short Delay Sharp Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Normal Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 22.05	20.0 -	kHz kHz
Stopband (Note 12)		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	6.25	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-	±0.2	-	dB

■ Short Delay Sharp Roll-Off Filter Characteristics (fs = 96kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Double Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 48.0	43.5 -	kHz kHz
Stopband (Note 12)		SB	52.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	5.63	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-	±0.3	-	dB

■ Short Delay Sharp Roll-Off Filter Characteristics (fs = 192kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Quad Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 96.0	87.0 -	kHz kHz
Stopband (Note 12)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	92			dB
Group Delay (Note 13)		GD	-	5.63	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-	+0/−1	-	dB

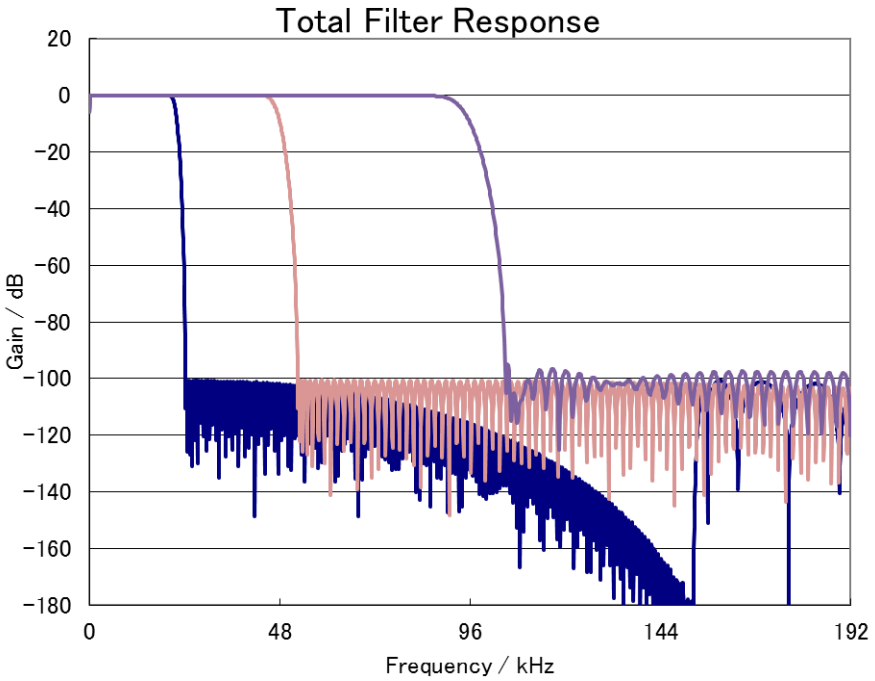


Figure 3. Short Delay Sharp Roll-off Filter Frequency Response

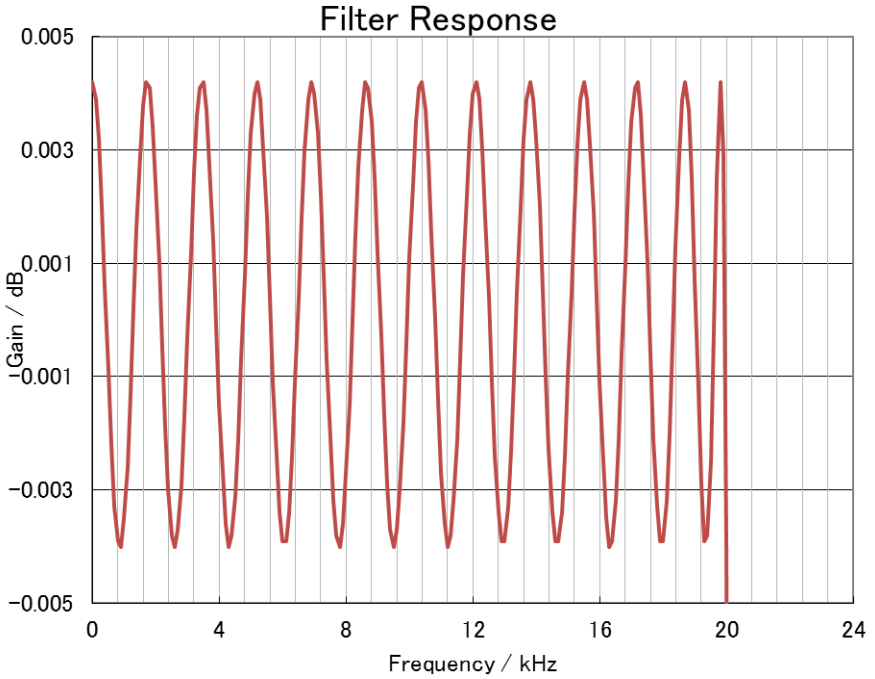


Figure 4. Short Delay Sharp Roll-off Filter Passband Ripple

■ Slow Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Normal Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 18.2	8.1 -	kHz kHz
Stopband (Note 12)		SB	39.2			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	94			dB
Group Delay (Note 13)		GD	-	6.63	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-	±0.2	-	dB

■ Slow Roll-Off Filter Characteristics (fs = 96kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Double Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 39.6	17.7 -	kHz kHz
Stopband (Note 12)		SB	85.3			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	6.00	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-	±0.3	-	dB

■ Slow Roll-Off Filter Characteristics (fs = 192kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Quad Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 79.1	35.5 -	kHz kHz
Stopband (Note 12)		SB	171			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	97			dB
Group Delay (Note 13)		GD	-	6.00	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-	+0/−1	-	dB

Note 14. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

Note 15. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

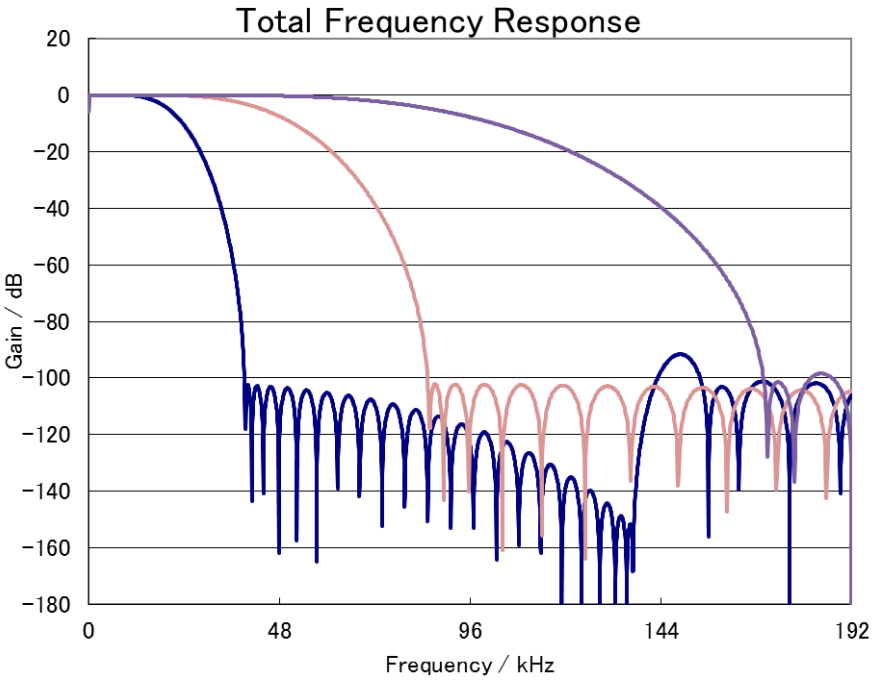


Figure 5. Slow Roll-off Filter Frequency Response

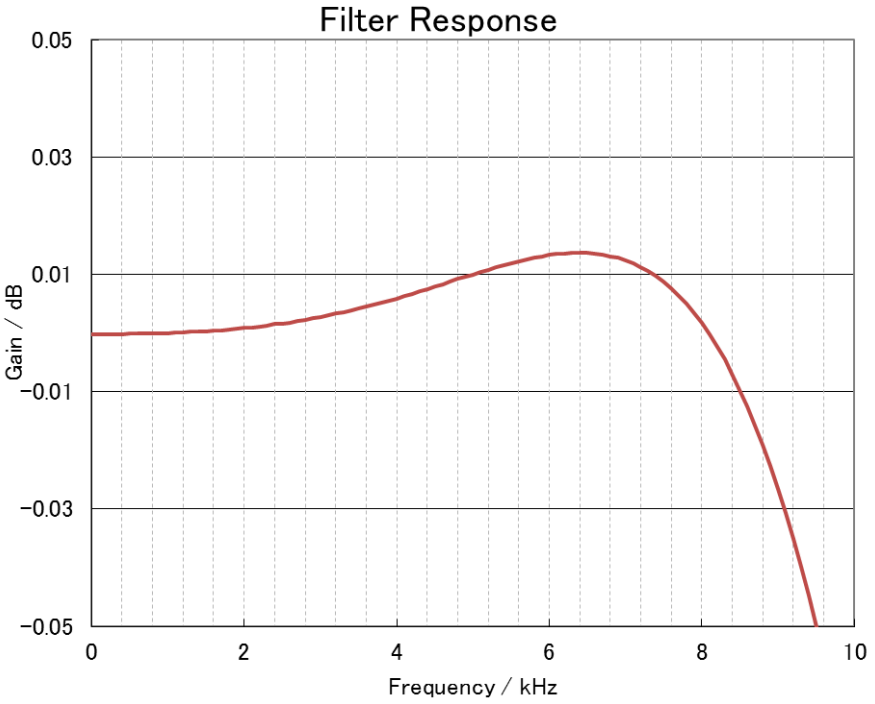


Figure 6. Slow Roll-off Filter Passband Ripple

■ Short Delay Slow Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta=25°C; AVDD= DVDD=3.0~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Normal Speed Mode;
DEM=OFF; SD bit="1" or SD pin = "H" , SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 18.2	8.1 -	kHz kHz
Stopband (Note 12)		SB	39.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	94			dB
Group Delay (Note 13)		GD	-	5.3	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-	±0.2	-	dB

■ Short Delay Slow Roll-Off Filter Characteristics (fs = 96kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Double Speed Mode;
DEM=OFF; SD bit="1" or SD pin = "H" , SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 48.0	43.5 -	kHz kHz
Stopband (Note 12)		SB	85.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	4.68	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-	±0.3	-	dB

■ Short Delay Slow Roll-Off Filter Characteristics (fs = 192kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Quad Speed Mode;
DEM=OFF; SD bit="1" or SD pin = "H" , SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 96.0	87.0 -	kHz kHz
Stopband (Note 12)		SB	170			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	97			dB
Group Delay (Note 13)		GD	-	4.68	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-	+0/−1	-	dB

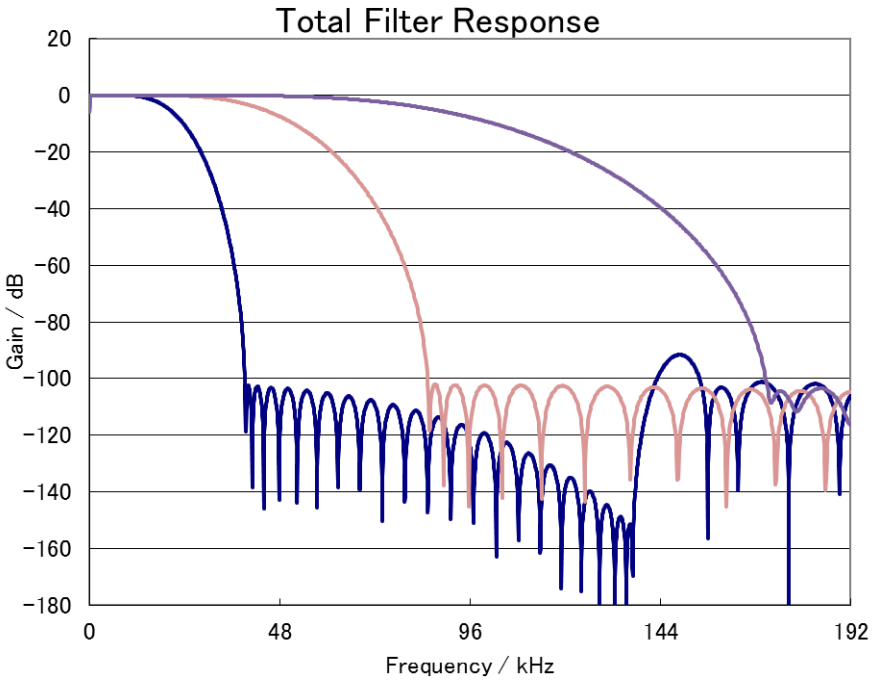


Figure 7. Short Delay Slow Roll-off Filter Frequency Response

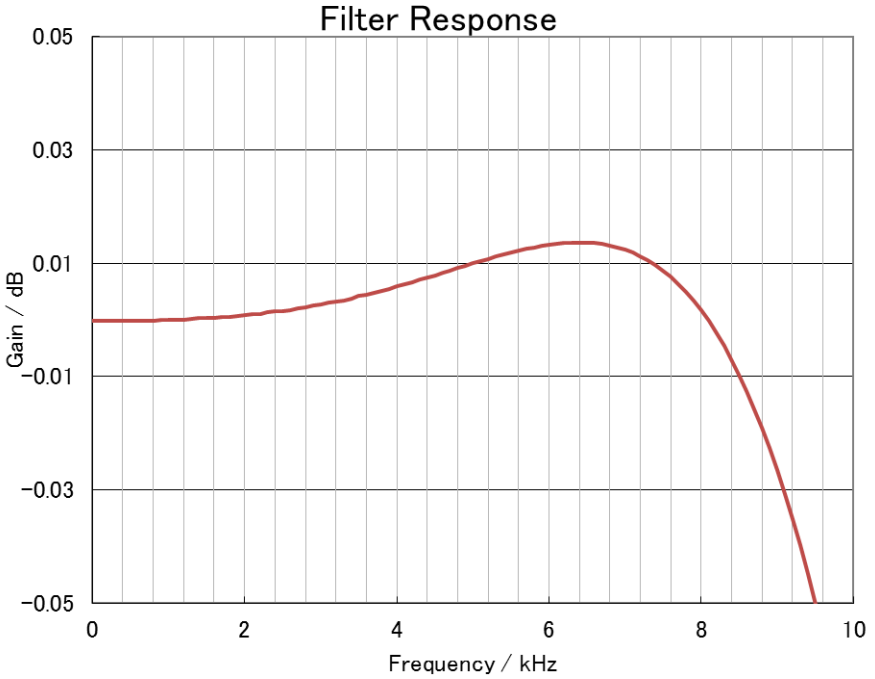


Figure 8. Short Delay Slow Roll-off Filter Passband Ripple

■ DC Characteristics

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, VREFHL/R=VDDL/R=4.75 ~ 7.2V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=−100μA)	VOH	DVDD−0.5	-	-	V
Low-Level Output Voltage					
(DZFL, DZFR pins: Iout=100μA)	VOL	-	-	0.5	V
(SDA pin: Iout=3mA)	VOL	-	-	0.5	V
Input Leakage Current (Note 16)	Iin	-	-	±10	μA

Note 16. The TST1/CAD0 and P/S pins have internal pull-up devices, nominally 100kΩ. Therefore The TST1/CAD0 and P/S pins are not included.

■ Switching Characteristics

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V, VREFHL/R= 4.75 ~ 7.2V)

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
Frequency	fCLK	7.7		49.152	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency (Note 17)					
1152fs, 512fs or 768fs	fsn	30		54	kHz
256fs or 384fs	fsd	54		108	kHz
128fs or 192fs	fsq	108		216	kHz
64fs	fsoc		384		kHz
64fs	fssd		768		kHz
Duty Cycle	Duty	45		55	%
PCM Audio Interface Timing					
BICK Period					
1152fs, 512fs or 768fs	tBCK	1/128fsn			ns
256fs or 384fs	tBCK	1/64fsd			ns
128fs or 192fs	tBCK	1/64fsq			ns
64fs	tBCK	1/64fso			ns
64fs	tBCK	1/64fsh			ns
BICK Pulse Width Low	tBCKL	10			ns
BICK Pulse Width High	tBCKH	10			ns
BICK "↑" to LRCK Edge (Note 18)	tBLR	5			ns
LRCK Edge to BICK "↑" (Note 18)	tLRB	5			ns
SDATA Hold Time	tSDH	5			ns
SDATA Setup Time	tSDS	5			ns
External Digital Filter Mode					
BICK Period	tB	27			ns
BCK Pulse Width Low	tBL	10			ns
BCK Pulse Width High	tBH	10			ns
BCK "↑" to WCK Edge	tBW	5			ns
WCK Edge to BCK "↑"	tWB	5			ns
WCK Pulse Width Low	tWCK	54			ns
WCK Pulse Width High	tWCH	54			ns
DATA Hold Time	tDH	5			ns
DATA Setup Time	tDS	5			ns
DSD Audio Interface Timing (64 mode, fs=44.1kHz)					
DCLK Period	tDCK		1/64fs		ns
DCLK Pulse Width Low	tDCKL	160			ns
DCLK Pulse Width High	tDCKH	160			ns
DCLK Edge to DSDL/R (Note 19)	tDDD	−20		20	ns
DSD Audio Interface Timing (128 mode, fs=44.1kHz)					
DCLK Period	tDCK		1/128fs		ns
DCLK Pulse Width Low	tDCKL	80			ns
DCLK Pulse Width High	tDCKH	80			ns
DCLK Edge to DSDL/R (Note 19)	tDDD	−10		10	ns

Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN High Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 20)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Reset Timing					
PDN Pulse Width (Note 21)	tPD	150			ns

Note 17. When the 1152fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK4495S/95 should be reset by the PDN pin or RSTN bit.

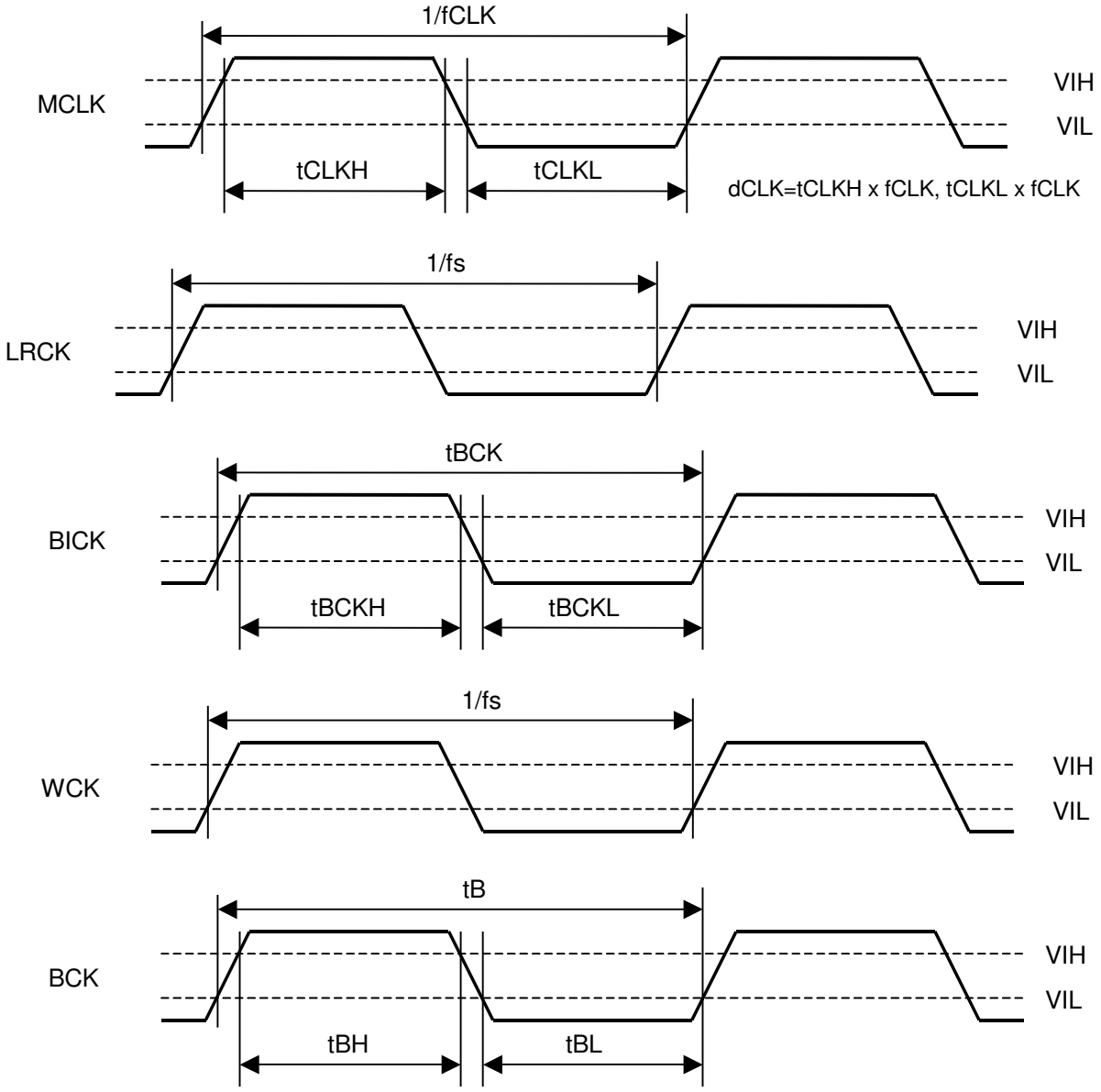
Note 18. BICK rising edge must not occur at the same time as LRCK edge.

Note 19. DSD data transmitting device must meet this time.

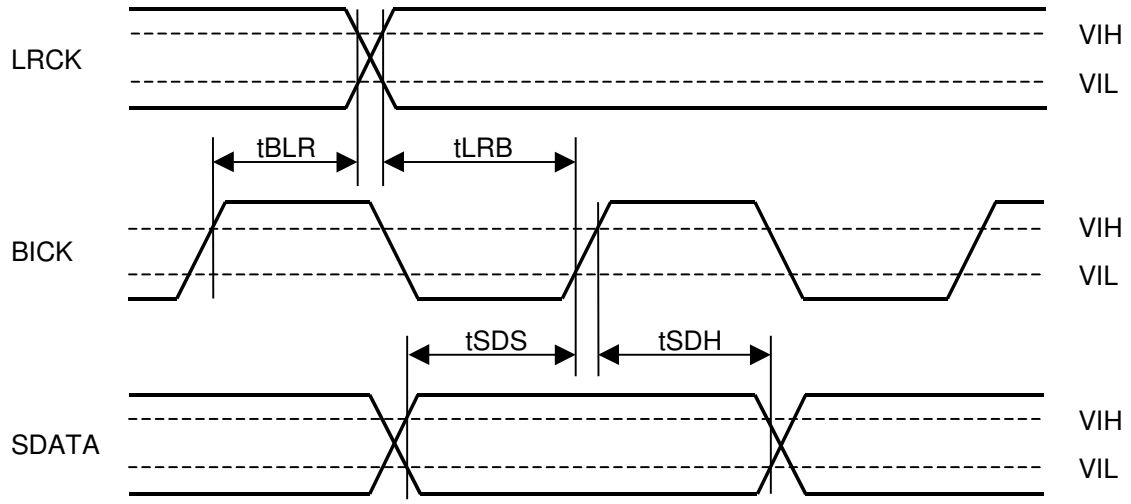
Note 20. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 21. The AK4495S/95 can be reset by bringing the PDN pin to "L".

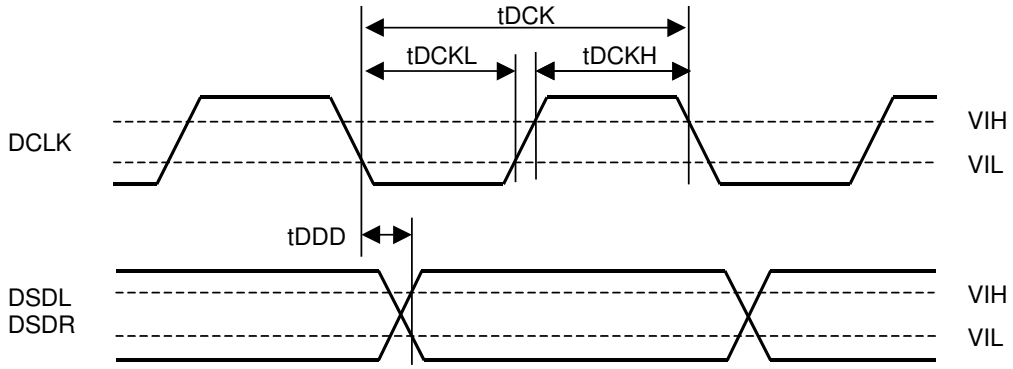
■ Timing Diagram



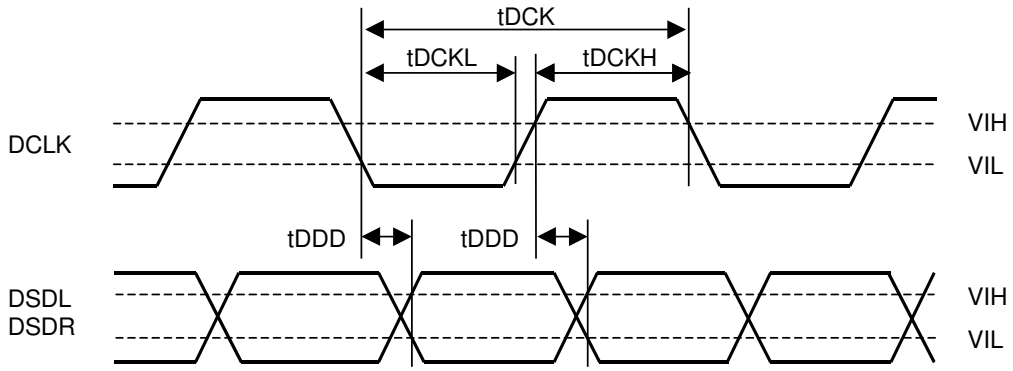
Clock Timing



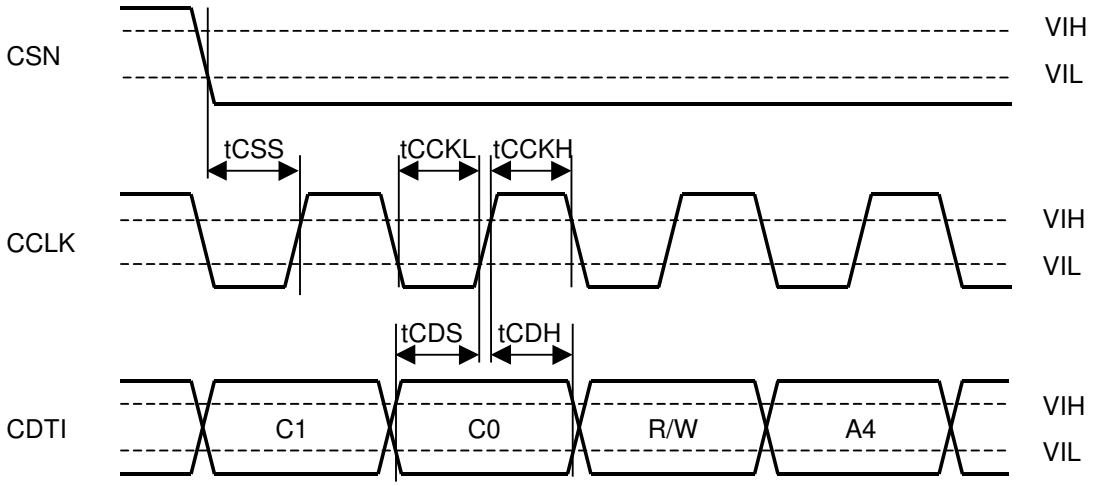
Audio Interface Timing (PCM Mode)



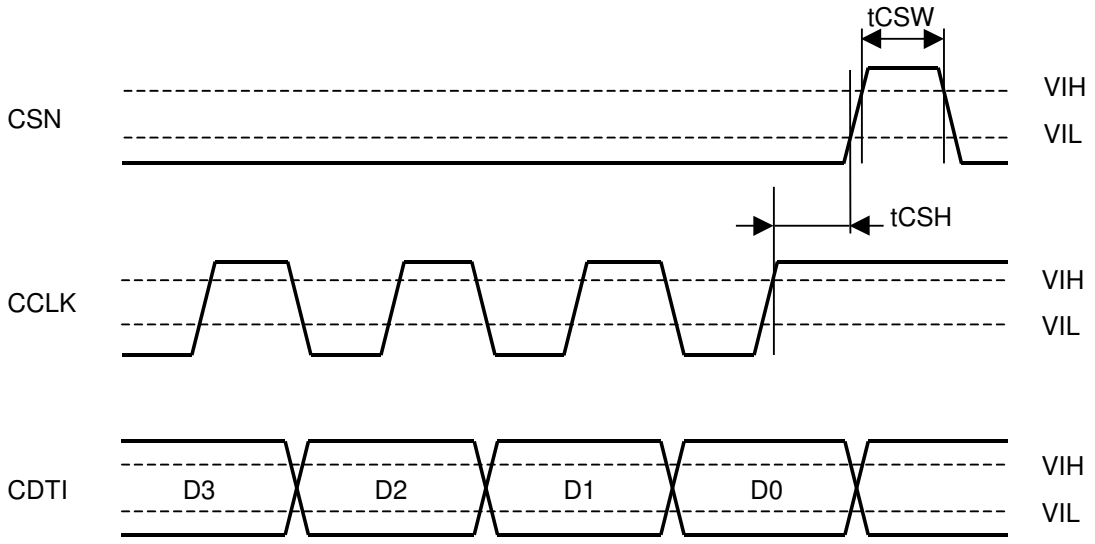
Audio Serial Interface Timing (DSD Normal Mode, DCKB bit = "0")



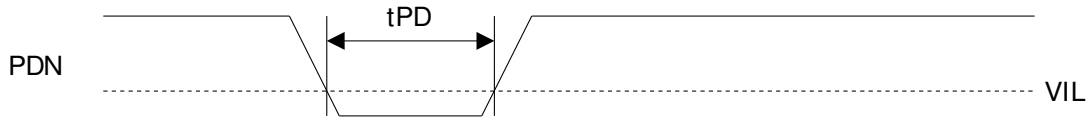
Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB bit = "0")



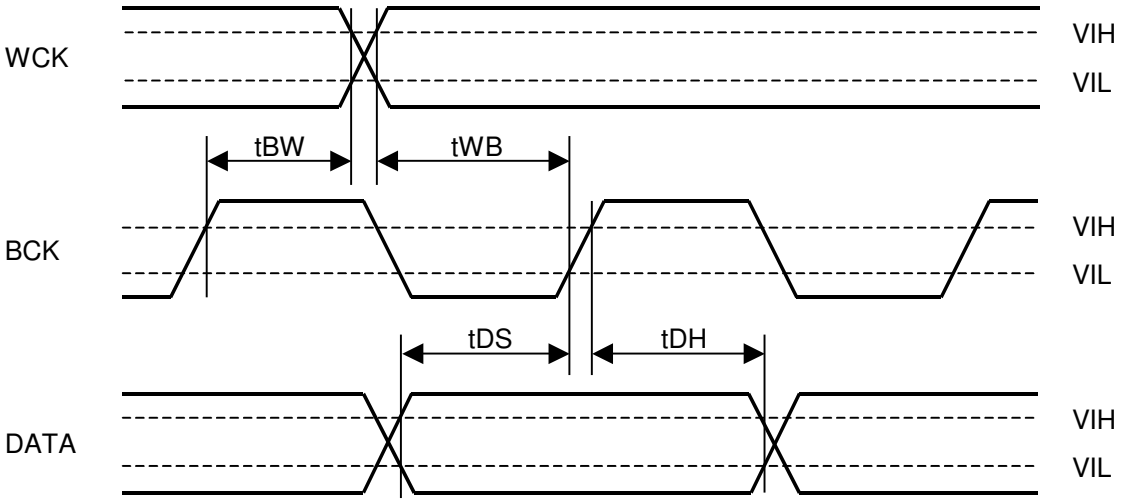
WRITE Command Input Timing



WRITE Data Input Timing



Power Down & Reset Timing



External Digital Filter I/F mode