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AK4497

Quality Oriented 32-Bit 2ch DAC

1. General Description

The AK4497 is a new generation Premium 32-bit 2ch DAC with VELVET SOUND™ technology, achieving industry's leading level low distortion characteristics and wide dynamic range. The AK4497 integrates a newly developed switched capacitor filter "OSR Doubler", making it capable of supporting wide range signals and achieving low out-of-band noise while realizing low power consumption. Moreover, the AK4497 has six types of 32-bit digital filters, realizing simple and flexible sound tuning in wide range of applications. The AK4497 accepts up to 768kHz PCM data and 22.4MHz DSD data, ideal for a high-resolution audio source playback that are becoming widespread in network audios, USB-DACs and Car Audio Systems.

Application: AV Receivers, CD/SACD player, Network Audios, USB DACs, USB Headphones, Sound Plates/Bars, Measurement Equipment, Control Systems, Public Audios (PA), IC-Recorders, Bluetooth Headphones, HD Audio/Voice Conference Systems

2. Features

- **THD+N: -116dB**
- **DR, S/N: 131dB (2.6 Vrms Output)**
  128dB (2 Vrms Output)
- **256 Times Over Sampling**
- **Sampling Rate: 8kHz ~ 768kHz**
- **32-bit 8x Digital Filter**
  - **Short Delay Sharp Roll-off, GD=6.0/fs,**
    Ripple: ±0.005dB, Attenuation: 100dB
  - **Short Delay Slow Roll-off, GD=5.0/fs**
  - **Sharp Roll-off**
  - **Slow Roll-off**
  - **Low-dispersion Short Delay Filter**
  - **Super Slow Roll-off**
- **2.8MHz, 5.6MHz, 11.2MHz, 22.4MHz DSD Input Support**
  - **Filter1 (fc=39kHz, 2.8MHz mode), Filter2 (fc=76kHz, 2.8MHz mode)**
- **Digital De-emphasis for 32, 44.1, 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (255 levels and 0.5dB step + mute)**
- **Mono Mode**
- **External Digital Filter Interface**
- **Audio I/F Format: 24/32 bit MSB justified, 16/20/24/32 bit LSB justified, I^2S, DSD, TDM**
- **Master Clock**
  8kHz ~ 32kHz: 256fs or 384fs or 512fs or 768fs or 1152fs
  8kHz ~ 54kHz: 256fs or 384fs or 512fs or 768fs
  8kHz ~ 108kHz: 256fs or 384fs
  108kHz ~ 216kHz: 128fs or 192fs
  ~ 384kHz: 32fs or 48fs or 64fs or 96fs
  ~ 768kHz: 16fs or 32fs or 48fs or 64fs
- **Power Supply:**
  TVDD=AVDD= 3.0 ~ 3.6V (by Internal LDO), VDDL/R= 4.75 ~ 5.25V
  TVDD=AVDD= 1.7 ~ 3.6V (by external supply), DVDD=1.7 ~ 1.98V,
  VDDL/R= 4.75 ~ 5.25V
- **Digital Input Level: CMOS**
- **Package: 64-pin TQFP**

Audio 4pro™

3. Table of Contents

4. Block Diagram

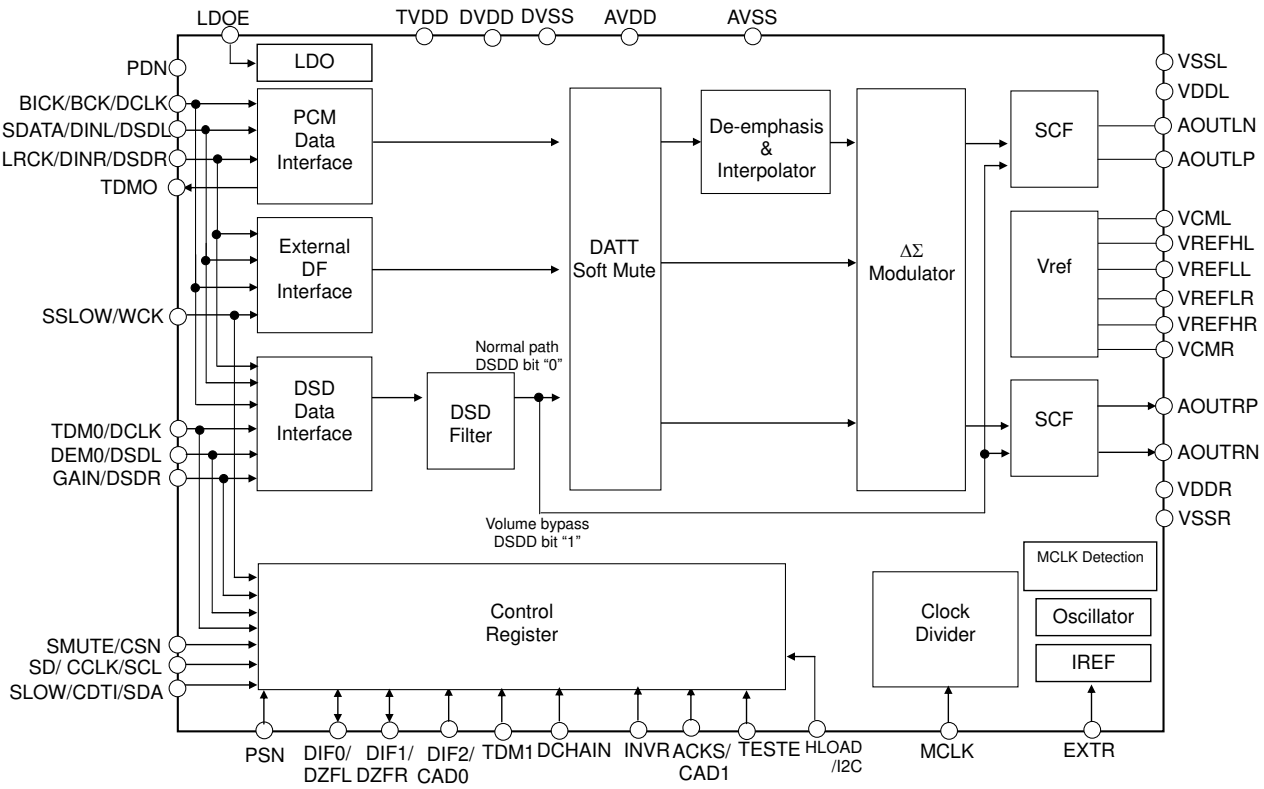

Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations

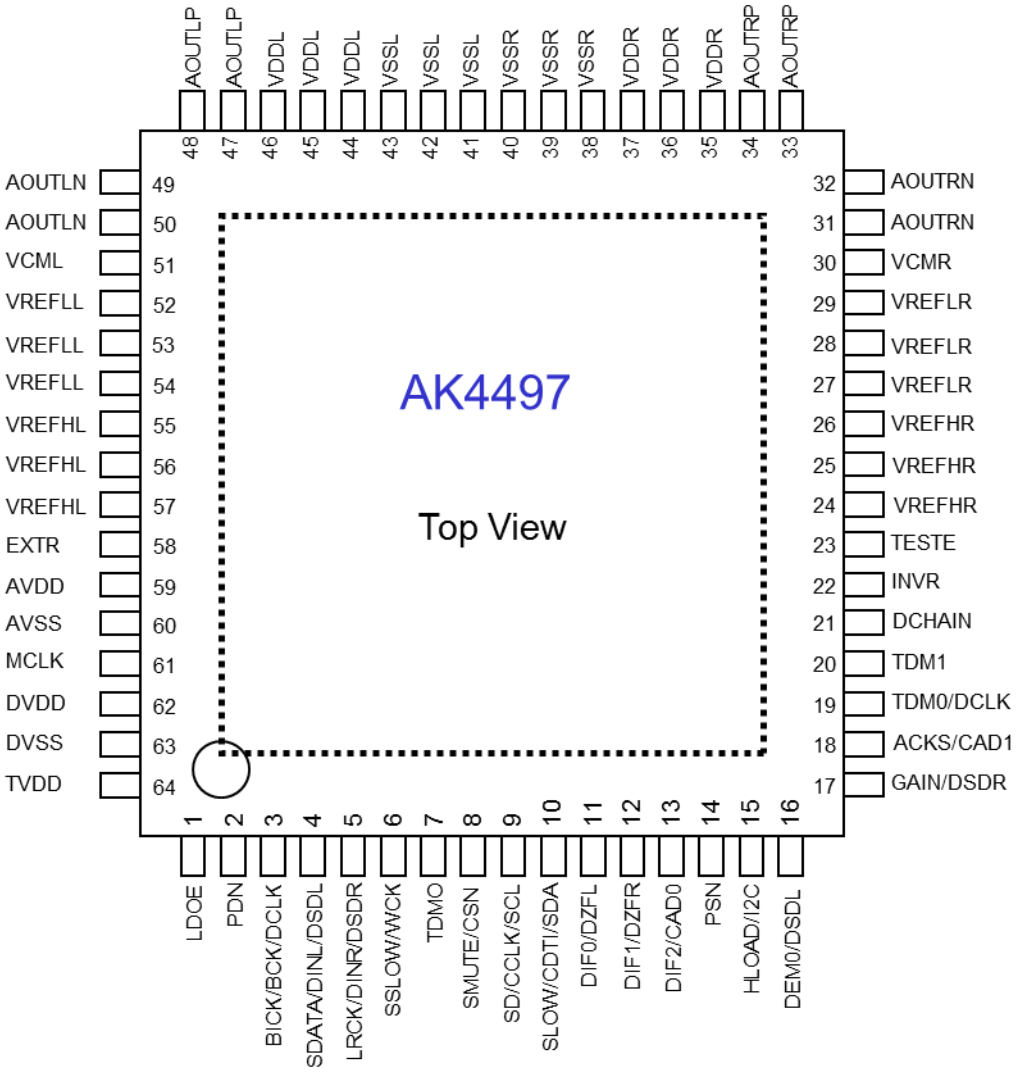

Figure 2. Pin Configurations

The exposed pad on the bottom surface of the package must be connected to AVSS.

■ Pin Functions

No.	Pin Name	I/O	Function
1	LDOE	I	Internal LDO Enable Pin. “L”: Disable, “H”: Enable
2	PDN	I	Power-Down Mode Pin When at “L”, the AK4497 is in power-down mode and is held in reset. The AK4497 must always be reset upon power-up.
3	BICK	I	Audio Serial Data Clock Pin in PCM Mode
	BCK	I	Audio Serial Data Clock Pin
	DCLK	I	DSD Clock Pin in DSD Mode (DSDPATH bit = “1”)
4	SDATA	I	Audio Serial Data Input Pin in PCM Mode
	DINL	I	Lch Audio Serial Data Input Pin
	DSDL	I	DSD Lch Data Input Pin in DSD Mode(DSDPATH bit = “1”)
5	LRCK	I	L/R Clock Pin in PCM Mode
	DINR	I	Rch Audio Serial Data Input Pin
	DSDR	I	DSD Rch Data Input Pin in DSD Mode(DSDPATH bit = “1”)
6	SSLOW	I	Digital Filter Select Pin in Pin Control Mode
	WCK	I	Word Clock input pin
7	TDMO	O	Audio Serial Data Output in Daisy Chain mode (Internal pull-down pin)
8	SMUTE	I	When this pin is changed to “H”, soft mute cycle is initiated. When returning “L”, the output mute releases.
	CSN	I	Chip Select Pin in Register Control Mode
9	SD	I	Digital Filter Select Pin in Pin Control Mode
	CCLK	I	Control Data Clock Pin in Register Control Mode
	SCL	I	I2C=”H”: Control Data Clock Input Pin
10	SLOW	I	Digital Filter Select Pin in Pin Control Mode
	CDTI	I	Control Data Input Pin in Register Control Mode
	SDA	I/O	I2C=”H”: Control Data Input Pin
11	DIF0	I	Digital Input Format 0 Pin in Pin Control Mode
	DZFL	O	Lch Zero Input Detect Pin in Register Control Mode (Internal pull-down pin)
12	DIF1	I	Digital Input Format 1 Pin in Pin Control Mode
	DZFR	O	Rch Zero Input Detect Pin in Register Control Mode (Internal pull-down pin)
13	DIF2	I	Digital Input Format 2 Pin in Pin Control Mode
	CAD0	I	Chip Address 0 Pin in Register Control Mode
14	PSN	I	Pin Control Mode or Register Control Mode select Pin (Internal pull-up pin) “L”: Register Control Mode, “H”: Pin Control Mode
15	HLOAD	I	Heavy Load Mode Enable Pin in Pin Control Mode.
	I2C		Resister Control Interface Pin in Register Control Mode.
16	DEM0	I	De-emphasis Enable 0 Pin in Pin Control Mode
	DSDL	I	DSD Lch Data Input Pin in DSD Mode (DSDPATH bit =”0”)
17	GAIN	I	Output Gain Control Pin in Pin control mode (+2.5dB)
	DSDR	I	DSD Rch Input Pin in DSD Mode (DSDPATH bit =”0”)
18	ACKS	I	Auto Setting Mode Select Pin in Pin control mode “L”: Manual Setting Mode, “H”: Auto Setting Mode
	CAD1	I	Chip Address 1 Pin in Register Control Mode

No.	Pin Name	I/O	Function
19	TDM0	I	TDM Mode Select Pin in Pin Control Mode.
	DCLK	I	DSD clock Pin in DSD Mode (DSDPATH bit = "0")
20	TDM1	I	TDM Mode select Pin in Pin Control Mode.
21	DCHAIN	I	Daisy Chain Mode Select Pin in Pin Control Mode.
22	INVR	I	Rch Output Data Invert Enable Pin in Pin Control Mode.
23	TESTE	I	Test Mode Enable Pin. (Internal pull-down pin)
24-26	VREFHR	I	Rch High Level Voltage Reference Input Pin
27-29	VREFLR	I	Rch Low Level Voltage Reference Input Pin
30	VCMR	I	Right Channel Common Voltage Pin, Normally connected to VREFLR with a 10uF electrolytic cap. This pin is prohibited to connect other devices.
31,32	AOUTRN	O	Rch Negative Analog Output Pin
33,34	AOUTRP	O	Rch Positive Analog Output Pin
35-37	VDDR	-	Rch Analog Power Supply Pin
38-40	VSSR	-	Analog Ground Pin
41-43	VSSL	-	Analog Ground Pin
44-46	VDDL	-	Lch Analog Power Supply Pin
47,48	AOUTLP	O	Lch Positive Analog Output Pin
49,50	AOUTLN	O	Lch Negative Analog Output Pin
51	VCML	-	Left channel Common Voltage Pin Normally connected to VREFLL with a 10uF electrolytic cap. This pin is prohibited to connect other devices.
52-54	VREFLL	I	Lch Low Level Voltage Reference Input Pin
55-57	VREFHL	I	Lch High Level Voltage Reference Input Pin
58	EXTR	I	External Resistor Connect Pin Rext=33kΩ(±0.1%) to AVSS
59	AVDD	-	(LDOE pin = "H") Analog Power Supply Pin, 3.0 ~ 3.6V
		-	(LDOE pin = "L") Analog Power Supply Pin, 1.7 ~ 3.6V
60	AVSS	-	Analog Ground Pin
61	MCLK	I	Master Clock Input Pin
62	DVDD	O	(LDOE pin = "H") LDO Output Pin, This pin should be connected to DVSS with 1.0µF. This pin is prohibited to connect other devices.
		-	(LDOE pin = "L") Digital Power Supply Pin, 1.7 ~ 1.98V
63	DVSS	-	Digital Ground Pin
64	TVDD	-	(LDOE pin = "H") Digital Power Supply Pin, 3.0 ~ 3.6V
		-	(LDOE pin = "L") Digital Power Supply Pin, 1.7 ~ 3.6V

Note 1. All input pins except internal pull-up/down pins must not be left floating.
Note 2. The AK4497 must be reset by PDN pin after changing Pin/Register control mode by the PSN pin.
Note 3. PCM mode, DSD mode and EXDF mode are controlled by register settings.

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

(1) Pin Control Mode (PCM mode only)

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
Digital	TESTE	Connect to DVSS or Open

(2) Resister Control Mode

1. PCM Mode

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
Digital	TESTE	Connect to DVSS or Open
	TDMO, DZFL, DZFR	Open

2. DSD Mode

DSDPATH bit = "0"

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
Digital	BICK, SDATA, LRCK, WCK, TDM1, DCHAIN, INVR, TESTE	Connect to DVSS
	TESTE	Connect to DVDD or Open
	TDMO, DZFL, DZFR	Open

DSDPATH bit = "1"

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
Digital	DEM0, GAIN, TDM0, WCK, TDM1, DCHAIN, INVR	Connect to DVSS
	TESTE	Connect to DVSS or Open
	TDMO, DZFL, DZFR	Open

3. EXDF Mode

Classification	Pin Name	Status
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
Digital	DEM0, GAIN, TDM0, TDM1, DCHAIN, INVR	Connect to DVSS
	TESTE	Connect to DVSS or Open
	TDMO, DZFL, DZFR	Open

4. I^2C-Bus Mode

Classification	Pin Name	Status
Digital	CSN	Connect to DVSS

Pull-up and Pull-down pins List

Classification	Pin Name	Status
pull-up pin (typ=100kΩ)	PSN	Connect to TVDD or Open
pull-down pin (typ=100kΩ)	TDMO, DZFL, DZFR, TESTE	Connect to DVSS or Open

6. Absolute Maximum Ratings

(AVSS=DVSS=VSSL=VSSR=VREFLL=VREFLR=0V; Note 4)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Digital I/O	TVDDam	−0.3	4.0	V
	Digital Core	DVDDam	−0.3	2.5	V
	Clock Interface	AVDDam	−0.3	4.0	V
	Analog	VDDL/Ram	−0.3	6.0	V
	|AVSS − DVSS| (Note 5)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	−0.3	TVDD+0.3	V
Ambient Temperature (Power supplied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 4. All voltages with respect to ground.

Note 5. AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane. Connect the exposed pad on the bottom surface of the package to AVSS.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS=VSSL=VSSR=VREFLL=VREFLR=0V; Note 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	■ LDOE pin= "L"					
	Digital I/O	TVDD	DVDD	1.8	3.6	V
	Clock Interface	AVDD	DVDD	1.8	3.6	V
	Digital Core	DVDD	1.7	1.8	1.98	V
	Analog	VDDL/R	4.75	5.0	5.25	V
	■ LDOE pin= "H"					
	Digital I/O	TVDD	3.0	3.3	3.6	V
	Clock Interface	AVDD	3.0	3.3	3.6	V
	Analog	VDDL/R	4.75	5.0	5.25	V
Voltage Reference (Note 7)	"H" voltage reference	VREFHL/R	VDDL/R-0.5	-	VDDL/R	V
	"L" voltage reference	VREFLL/R	-	VSSL/R	-	V

Note 4. All voltages with respect to ground.

Note 6. The analog output voltage scales with the voltage of (VREFHL/R − VREFLL/R).

Note 7. TVDD and AVDD must be connected to the same ground plane and powered up at the same time. When not using the LDO (LDOE pin = "L"), all power supplies (DVDD (1.8V), TVDD and AVDD (3.3V) and VDDL/R (5V)) should be powered up at the same time or sequentially in the order of 3.3V (TVDD, AVDD), 1.8V (DVDD) and 5V (VDDL/R).

Note 8. The internal LDO outputs DVDD (1.8V) when the LDOE pin = "H". 3.3V (TVDD and AVDD) power supplies must be powered up before or at the same time with 5V (VDDL/R) power supplies when the LDOE pin = "H".

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

■ Analog Characteristics

(Ta=25°C; LDOE pin = "L", AVDD=TVDD=3.3V, DVDD=1.8V, AVSS=DVSS=VSSL/R=0V; VREFHL/R=VDDL/R=5.0V, VREFLL/R= 0V; Input data = 24bit; BICK=64fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: Figure 77; SC[2:0] bit="000"; 2Vrms output mode (GC[2:0] bit="000" or GAIN pin="L"); Heavy load drive mode=off(HLOAD bit="0" or HLOAD pin="L"); unless otherwise specified.)

Parameter					Min.	Typ.	Max.	Unit
Resolution					-	-	32	Bits
Dynamic Characteristics (Note 9)								
THD+N	fs=44.1kHz	BW=20kHz	0dBFS	GC[2:0]= "000" or GAIN= "L"	-	–116	–108	dB
				GC[2:0]= "100" or GAIN= "H"	-	–113	-	
			–60dBFS		-	–65	-	dB
	fs=96kHz	BW=40kHz	0dBFS		-	–113	-	dB
			–60dBFS		-	–62	-	dB
	fs=192kHz	BW=40kHz	0dBFS		-	–110	-	dB
			–60dBFS		-	-62	-	dB
		BW=80kHz	–60dBFS		-	-59	-	dB
Dynamic Range (–60dBFS with A-weighted) (Note 10)					125	128	-	dB
S/N (A-weighted) (Note 11)	GC[2:0]= "000" or GAIN= "L"				125	128	-	dB
	GC[2:0]= "100" or GAIN= "H"			Stereo mode	-	131	-	dB
				Mono mode (Note 17)	-	133	-	
Interchannel Isolation (1kHz)					110	120	-	dB
DC Accuracy								
Interchannel Gain Mismatch					-	0.15	0.3	dB
Gain Drift (Note 12)					-	20	-	ppm/°C
Output Voltage	GC[2:0] bits="000" or GAIN pin="L" (Note 13)				±2.65	±2.8	±2.95	Vpp
	GC[2:0] bits="100" or GAIN pin="H" (Note 14)				±3.55	±3.75	±3.95	Vpp
Load Resistance (Note 15)	HLOAD bit="0" or HLOAD pin="L"				8	10	-	kΩ
	HLOAD bit="1" or HLOAD pin="H"				120	-	-	Ω
Load Capacitance (Note 15)					-	-	25	pF

Note 9. Measured by Audio Precision APx555. Averaging mode.
Note 10. 101dB at 16bit data and 118dB at 20bit data.
Note 11. S/N does not depend on the input data size.
Note 12. The voltage on (VREFH – VREFL) is held +5V externally.
Note 13. The analog output voltage with 0dBFS input signal when GC[2:0] bits = "000" or the GAIN pin = "L" is calculated by the following formula.
AOUTL/R (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFHL/R – VREFLL/R)/5.
Note 14. The analog output voltage with 0dBFS input signal when GC[2:0] bits = "100" or the GAIN pin = "H" is calculated by the following formula.
AOUTL/R (typ.@0dB) = (AOUT+) – (AOUT–) = ±3.75Vpp × (VREFHL/R – VREFLL/R)/5.
Note 15. Regarding Load Resistance, AC load is 8kΩ (min) with a DC cut capacitor when HLOAD bit = "0" or the HLOAD pin = "L". DC load is 120Ω (min) without a DC cut capacitor if the HLOAD pin = "H". The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore the capacitive load must be minimized.
Note 16. It is recommended to use a resistor with 0.1% absolute error for the output stage of the adding circuit.
Note 17. This mode is shown in Figure 78.

(Ta=25°C; AVDD=TVDD=3.3V, DVDD=1.8V(@LDOE pin= "L"), AVSS=DVSS=VSSL/R=0V; VREFHL/R=VDDL/R=5.0V, VREFLL/R= 0V; Input data = 24bit; BICK=64fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; SC[2:0] bits= "000"); 2Vrms output mode (GC[2:0] bits= "000" or GAIN pin = "L"); Heavy load drive mode=off (HLOAD bit= "0" or HLOAD pin= "L"); unless otherwise specified.)

Power Supplies						
Parameter			**Min.**	**Typ.**	**Max.**	**Unit**
Power Supply Current						
Normal operation (PDN pin = "H")						
VDDL/R(total)				64	96	mA
VREFHL/R				1	1.5	mA
AVDD			-	1	1.5	mA
TVDD						
	LDOE pin = "H"	fs= 44.1kHz		8	12	mA
		fs= 96kHz	-	13	20	mA
		fs = 192kHz	-	20	30	mA
	LDOE pin = "L"			1	1.5	mA
DVDD						
	LDOE pin = "L"	fs= 44.1kHz		8	12	mA
		fs= 96kHz		13	20	mA
		fs = 192kHz		20	30	mA
Total Idd per channel (HLOAD pin = "H") ・fs=44.1kHz				45	72	mA/ch
Power down (PDN pin = "L") (Note 18) TVDD+AVDD+VDDL/R+DVDD			-	10	100	μA

Note 18. In power down mode, the PSN pin = TVDD and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held to DVSS.

Note 19. The DVDD pin becomes an output pin when the LDOE pin = "H".

■ DSD Mode

(Ta=25°C; AVDD=TVDD=3.3V, DVDD=1.8V (@LDOE pin = "L"), AVSS=DVSS=VSSL/R=0V; VREFHL/R=VDDL/R=5.0V, VREFLL/R= 0V; Signal Frequency = 1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit; Example circuit 3 (Figure 77); SC[2:0] bit="000"; 2Vrms output mode (GC[2:0] bits="000" or GAIN pin="L"); Heavy load drive mode=off(HLOAD bit="0" or HLOAD pin= "L"); unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Dynamic Characteristics						
THD+N (Note 20)	DSD dataStream: 2.8224MHz	0dBFS	-	−116	-	dB
	DSD dataStream: 5.6448MHz	0dBFS	-	−116	-	dB
	DSD dataStream: 11.2896MHz	0dBFS	-	−116	-	dB
S/N (A-weighted, Normal path) (Note 20)	DSD dataStream: 2.8224MHz	Digital"0" (Note 23)	-	128	-	dB
	DSD dataStream: 5.6448MHz	Digital"0" (Note 23)	-	128	-	dB
	DSD dataStream: 11.2896MHz	Digital"0" (Note 23)	-	128	-	dB
DC Accuracy						
Output Voltage (Normal path)		(Note 13)	±2.65	±2.8	±2.95	Vpp
Output Voltage (Volume Bypass)		(Note 24)	±2.38	±2.5	±2.63	Vpp

Note 20. Analog characteristics are not guaranteed when the DSD dataStream is 22.5782MHz.

Note 21. The peak level of DSD signal should be in the range of 25% ~ 75% Duty according to the SACD format book (Scarlet Book).

Note 22. The output level is assumed as 0dB when a 1kHz 25% ~ 75% duty sine wave is input. Click noise may occur if the input signal exceeds 0dB.

Note 23. Digital "0" is a digital zero code pattern ("01101001") according to the SACD format book (Scarlet Book).

Note 24. When DSDD bit = "1", the analog output voltage with 25 ~ 75% input duty is given by following formula.

AOUTL/R (typ.@0dB) = (AOUTLP/RP) − (AOUTLN/RN) = ±2.5Vpp × (VREFHL/R − VREFLL/R)/5.0.

■ Sharp Roll-Off Filter Characteristics

Sharp Roll-Off Filter Characteristics (fs=44.1kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Normal Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L", SSLOQ bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 25)	±0.01dB −6.0dB	PB -	0 -	 22.05	20.0 -	kHz kHz
Passband	(Note 26)	PB	0		20.0	kHz
Stopband	(Note 26)	SB	24.1			kHz
Passband Ripple	(Note 27)	PR			±0.005	dB
Stopband Attenuation	(Note 25)	SA	100			dB
Group Delay	(Note 28)	GD	-	29.2	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 20.0kHz			−0.2	-	+0.1	dB

Sharp Roll-Off Filter Characteristics (fs=96kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Double Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L", SSLOW bit = "0" or SSLOW pin = "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 25)	±0.01dB −6.0dB	PB	0 -	 48.0	43.5 -	kHz kHz
Passband	(Note 26)	PB	0		43.5	kHz
Stopband	(Note 26)	SB	52.5			kHz
Passband Ripple	(Note 27)	PR			±0.005	dB
Stopband Attenuation	(Note 25)	SA	100			dB
Group Delay	(Note 28)	GD	-	29.2	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 40.0kHz			−0.6	-	+0.1	dB

Sharp Roll-Off Filter Characteristics (fs=192kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Quad Speed Mode; DEM=OFF; SD bit="0" or SD pin="L", SLOW bit="0" or SLOW pin="L", SSLOW bit="0" or SSLOW pin="L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 25)	±0.01dB −6.0dB	- -	0 -	 96.0	87.0 -	kHz kHz
Passband	(Note 26)	PB	0		87.0	kHz
Stopband	(Note 26)	SB	105			kHz
Passband Ripple	(Note 27)	PR			±0.005	dB
Stopband Attenuation	(Note 25)	SA	100			dB
Group Delay	(Note 28)	GD	-	29.2	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 80.0kHz			−2.0	-	+0.1	dB

Note 25. Frequency response refers to the output level (0dB) of a 1kHz, 0dB sine wave input.

Note 26. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

Note 27. The first stage of the Interpolator. This is a passband gain amplitude of the 4 times oversampling filter.

Note 28. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32 bit data of both channels to the output of analog signal.

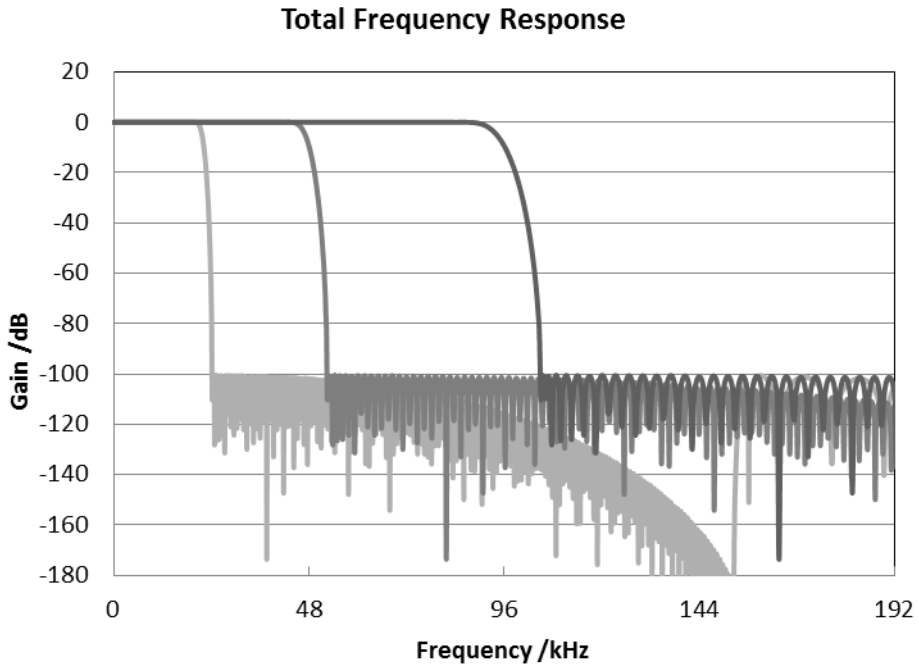

Figure 3. Sharp Roll-off Filter Frequency Response

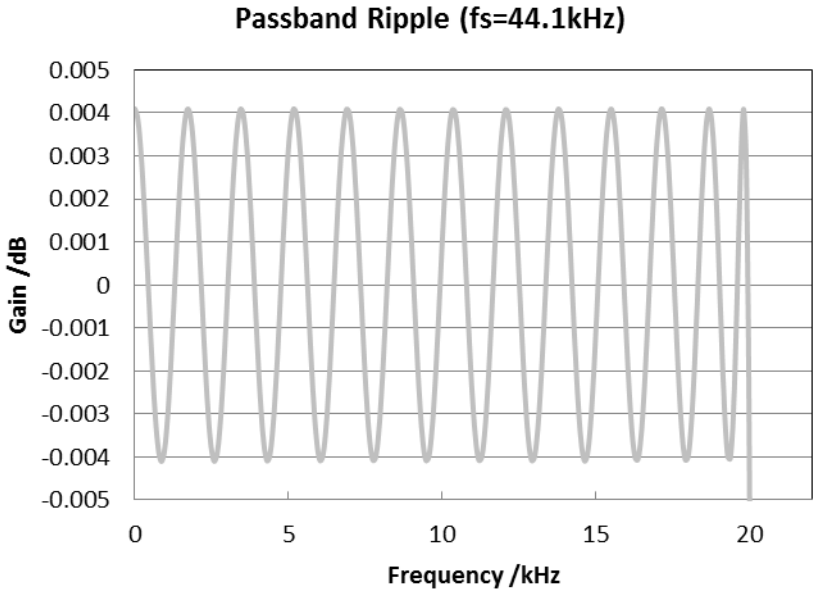

Figure 4. Sharp Roll-off Filter Passband Ripple

■ Slow Roll-Off Filter Characteristics

Slow Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Normal Speed Mode; DEM=OFF; SD bit="0" or SD pin="L", SLOW bit="1" or SLOW pin="H", SSLOW bit="0" or SSLOW pin="L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 25)	±0.01dB −6.0dB	PB -	0 -	- 21.0	8.0 -	kHz kHz
Passband	(Note 29)	PB	0	-	8.0	kHz
Stopband	(Note 29)	SB	39.2	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 25)	SA	92	-	-	dB
Group Delay	(Note 28)	GD	-	6.5	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 20.0kHz			−5.0	-	+0.1	dB

Slow Roll-Off Filter Characteristics (fs = 96kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Double Speed Mode; DEM=OFF; SD bit="0" or SD pin="L", SLOW bit="1" or SLOW pin="H", SSLOW bit="0" or SSLOW pin="L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 25)	±0.01dB −6.0dB	PB	0 -	- 45.6	17.6 -	kHz kHz
Passband	(Note 29)	PB	0	-	17.6	kHz
Stopband	(Note 29)	SB	85.4	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 25)	SA	92	-	-	dB
Group Delay	(Note 28)	GD	-	6.5	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 40.0kHz			−3.8	-	+0.1	dB

Slow Roll-Off Filter Characteristics (fs = 192kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Quad Speed Mode; DEM=OFF; SD bit="0" or SD pin="L", SLOW bit="1" or SLOW pin="H", SSLOW bit="0" or SSLOW pin="L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 25)	±0.01dB −6.0dB	- -	0 -	- 91.2	35.2 -	kHz kHz
Passband	(Note 29)	PB	0	-	35.2	kHz
Stopband	(Note 29)	SB	170.7	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 25)	SA	100	-	-	dB
Group Delay	(Note 28)	GD	-	6.5	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 80.0kHz			−5.0	-	+0.1	dB

Note 29. The passband and stopband frequencies scale with fs. For example, PB = 0.1836 × fs (@±0.01dB), SB = 0.8889 × fs.

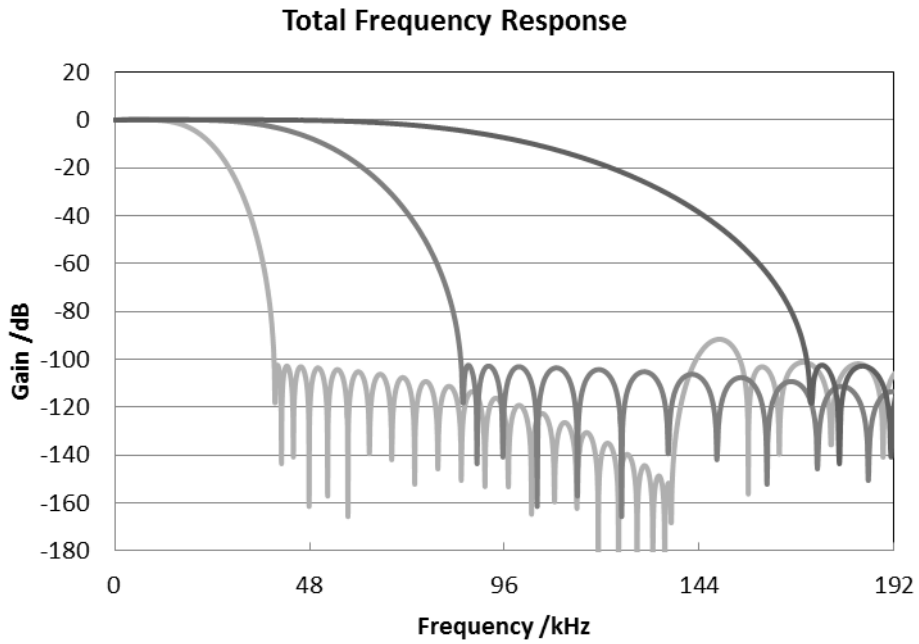

Figure 5. Slow Roll-off Filter Frequency Response

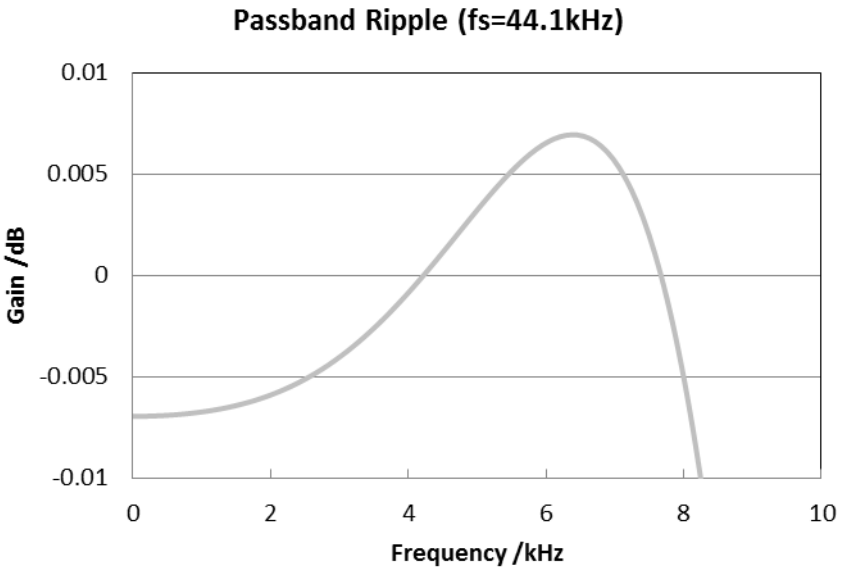

Figure 6. Slow Roll-off Filter Passband Ripple

■ Short Delay Sharp Roll-Off Filter Characteristics

Short Delay Sharp Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Normal Speed Mode; DEM=OFF; SD bit="1" or SD pin="H", SLOW bit="0" or SLOW bit="L", SSLOW bit="0" or SSLOW pin="L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.01dB	-	0	-	20.0	kHz
(Note 25)	−6.0dB	-	-	22.05	-	kHz
Passband	(Note 30)	PB	0	-	20.0	kHz
Stopband	(Note 30)	SB	24.1	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 25)	SA	100	-	-	dB
Group Delay	(Note 28)	GD	-	6.0	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 20.0kHz			−2.0	-	+0.1	dB

Short Delay Sharp Roll-Off Filter Characteristics (fs = 96kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Double Speed Mode; DEM=OFF; SD bit="1" or SD pin="H", SLOW bit="0" or SLOW bit="L", SSLOW bit="0" or SSLOW pin="L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.01dB	-	0	-	43.5	kHz
(Note 25)	−6.0dB	-	-	48.0	-	kHz
Passband	(Note 30)	PB	0	-	43.5	kHz
Stopband	(Note 30)	SB	52.5	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 25)	SA	100	-	-	dB
Group Delay	(Note 28)	GD	-	6.0	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 40.0kHz			−6.0	-	+0.1	dB

Short Delay Sharp Roll-Off Filter Characteristics (fs = 192kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Quad Speed Mode; DEM=OFF; SD bit="1" or SD pin="H", SLOW bit="0" or SLOW bit="L", SSLOW bit="0" or SSLOW pin="L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.01dB	-	0	-	87.0	kHz
(Note 25)	−6.0dB	-	-	96.0	-	kHz
Passband	(Note 30)	PB	0	-	87.0	kHz
Stopband	(Note 30)	SB	104.9	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 25)	SA	100	-	-	dB
Group Delay	(Note 28)	GD	-	6.0	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 80.0kHz			−2.0	-	+0.1	dB

Note 30. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

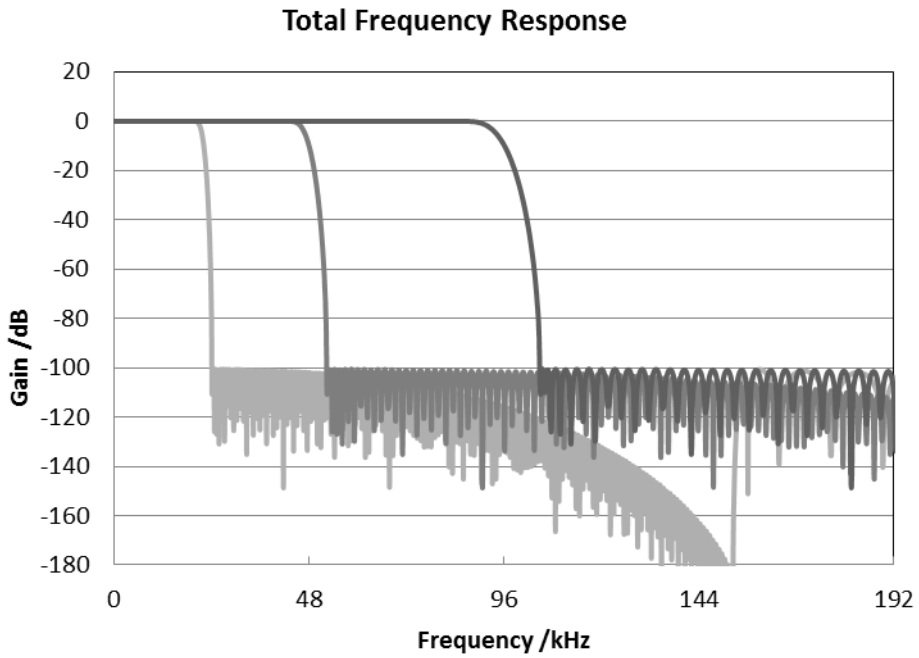

Figure 7. Short delay Sharp Roll-off Filter Frequency Response

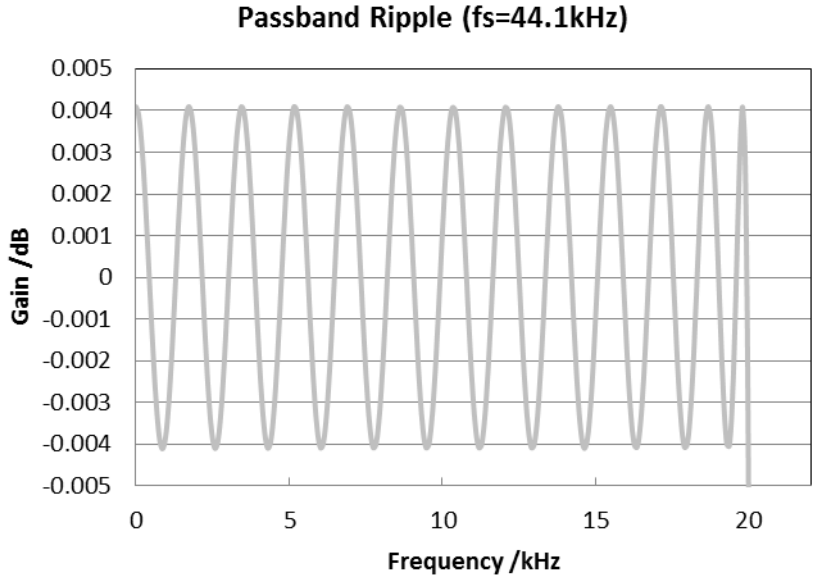

Figure 8. Short delay Sharp Roll-off Filter Passband Ripple

■ Short Delay Slow Roll-Off Filter Characteristics

Short Delay Slow Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Normal Speed Mode; DEM=OFF; SD bit="1" or SD pin="H", SLOW bit="1" or SLOW pin="H", SSLOW bit="0" or SSLOW pin="L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.01dB	-	0	-	8.0	kHz
(Note 25)	−6.0dB	-	-	21.0	-	kHz
Passband	(Note 30)	PB	0	-	8.0	kHz
Stopband	(Note 30)	SB	39.2	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 25)	SA	92		-	dB
Group Delay	(Note 28)	GD	-	5.0	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 20.0kHz			−5.0	-	+0.1	dB

Short Delay Slow Roll-Off Filter Characteristics (fs = 96kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Double Speed Mode; DEM=OFF; SD bit="1" or SD pin="H", SLOW bit="1" or SLOW pin="H", SSLOW bit="0" or SSLOW pin="L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.01dB	-	0	-	17.6	kHz
(Note 25)	−6.0dB	-	-	45.6	-	kHz
Passband	(Note 30)	PB	0	-	17.6	kHz
Stopband	(Note 30)	SB	85.4	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 25)	SA	100	-	-	dB
Group Delay	(Note 28)	GD	-	5.0	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 40.0kHz			−3.8	-	+0.1	dB

Short Delay Slow Roll-Off Filter Characteristics (fs = 192kHz)

(Ta=-40~85°C; VDDL/R=4.75 ~ 5.25V, AVDD= TVDD=1.7 ~3.6V, DVDD=1.7~1.98V; Quad Speed Mode; DEM=OFF; SD bit="1" or SD pin="H", SLOW bit="1" or SLOW pin="H", SSLOW bit="0" or SSLOW pin="L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.01dB	-	0	-	35.2	kHz
(Note 25)	−6.0dB	-	-	91.2	-	kHz
Passband	(Note 30)	PB	0	-	35.2	kHz
Stopband	(Note 30)	SB	170.7	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 25)	SA	100	-	-	dB
Group Delay	(Note 28)	GD	-	5.0	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 80.0kHz			−5.0	-	+0.1	dB

Note 31. The passband and stopband frequencies scale with fs. For example, PB = 0.1836 × fs (@±0.01dB), SB = 0.8866 × fs.

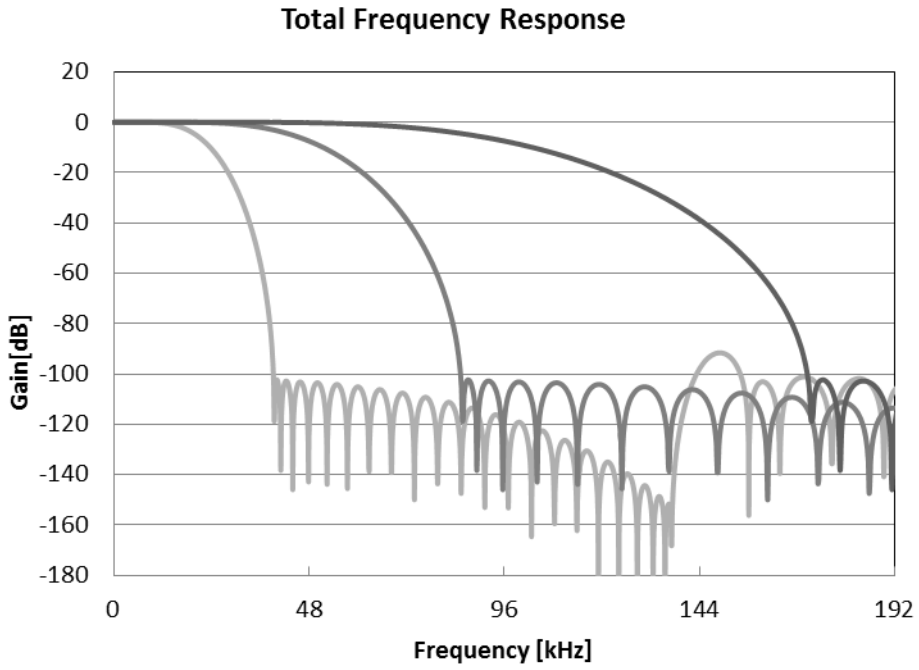

Figure 9. Short Delay Slow Roll-off Filter Frequency Response

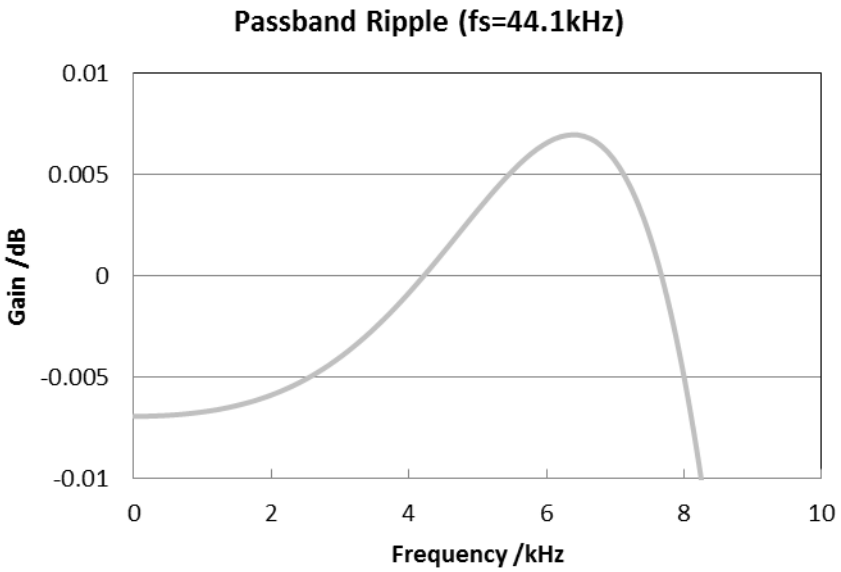

Figure 10. Short Delay Slow Roll-off Filter Passband Ripple

■ Low-dispersion Short Delay Filter Characteristics

Low-dispersion Short Delay Filter Characteristics (fs = 44.1kHz)

(Ta=-40~85°C; VDDL/R=4.75~5.25V, AVDD=TVDD=1.7~3.6V, DVDD=1.7~1.98V; Normal Speed Mode DEM=OFF; SD bit="1" or SD pin ="H", SLOW bit="0" or SLOW pin="L", SSLOW bit="1" or SSLOW pin="H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.05dB	PB	0	-	18.4	kHz
(Note 25)	−6.0dB	-	-	22.5	-	kHz
Passband	(Note 32)	PB	0	-	18.4	kHz
Stopband	(Note 32)	SB	25.7	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 25)	SA	80	-	-	dB
Group Delay	(Note 28)	GD	-	10.0	-	1/fs
Group Delay Distortion		ΔGD	-	±0.035	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 20.0kHz			−0.8	-	+0.1	dB

Low-dispersion Short Delay Filter Characteristics (fs = 96kHz)

(Ta=-40~85°C; VDDL/R=4.75~5.25V, AVDD=TVDD=1.7~3.6V, DVDD=1.7~1.98V; Double Speed Mode; DEM=OFF; SD bit="1" or SD pin ="H", SLOW bit="0" or SLOW pin="L", SSLOW bit="1" or SSLOW pin="H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.05dB	PB	0	-	40.1	kHz
(Note 25)	−6.0dB		-	48.0	-	kHz
Passband	(Note 32)	PB	0	-	40.1	kHz
Stopband	(Note 32)	SB	55.9	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 25)	SA	80	-	-	dB
Group Delay	(Note 28)	GD	-	10.0	-	1/fs
Group Delay Distortion		ΔGD		±0.035	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 40.0kHz			−0.6	-	+0.1	dB

Low-dispersion Short Delay Filter Characteristics (fs = 192kHz)

(Ta=-40~85°C; VDDL/R=4.75~5.25V, AVDD=TVDD=1.7~3.6V, DVDD=1.7~1.98V; Quad Speed Mode; DEM=OFF; SD bit="1" or SD pin ="H", SLOW bit="0" or SLOW pin="L", SSLOW bit="1" or SSLOW pin="H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response	±0.05dB	-	0	-	80.2	kHz
(Note 25)	−6.0dB	-	-	98.0	-	kHz
Passband	(Note 32)	PB	0	-	80.2	kHz
Stopband	(Note 32)	SB	111.8	-	-	kHz
Passband Ripple	(Note 27)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 25)	SA	80	-	-	dB
Group Delay	(Note 28)	GD	-	10.0	-	1/fs
Group Delay Distortion		ΔGD	-	±0.035	-	1/fs
Digital Filter + SCF	(Note 25)					
Frequency Response: 0 ~ 80.0kHz			−2.0	-	+0.1	dB

Note 32. The passband and stopband frequencies scale with fs. For example, PB = 0.418 × fs (@±0.05dB), SB = 0.582 × fs.

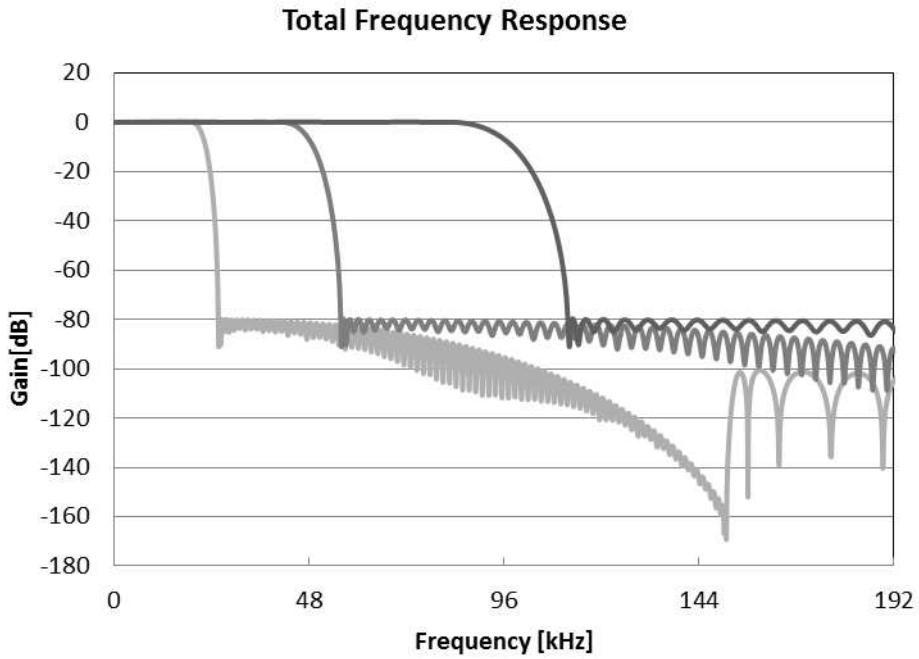

Figure 11. Low Dispersion Short Delay Filter Frequency Response

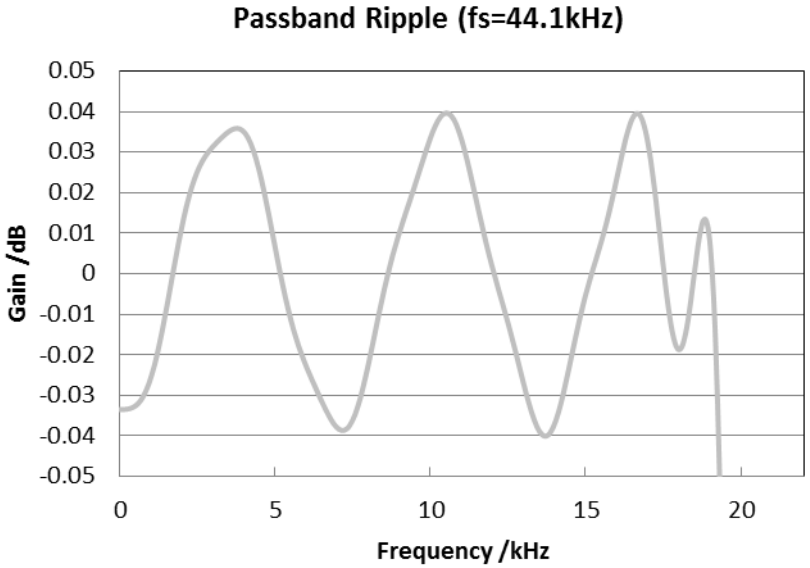

Figure 12. Low Dispersion Short Delay Filter Passband Ripple

■ DSD Filter Characteristics

(Ta=-40~85°C; VDDL/R=4.75~5.25V, AVDD=TVDD=1.7~3.6V, DVDD=1.7~1.98V; fs=44.1kHz; DP bit="1", DSDF bit = "0", DSDSEL[1:0] bits = "00")

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response (Note 34)					
Frequency Response (Note 35)	20kHz		-0.77		dB
	50kHz		-5.25		dB
	100kHz		-18.80		dB

(Ta=-40~85°C; VDDL/R=4.75~5.25V, AVDD=TVDD=1.7~3.6V, DVDD=1.7~1.98V; fs=44.1kHz; DP bit="1", DSDF bit="1", DSDSEL[1:0] bits= "00")

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response (Note 34)					
Frequency Response (Note 35)	20kHz		-0.19		dB
	100kHz		-5.29		dB
	150kHz		-15.57		dB

Note 33. The peak level of DSD signal should be in the range of 25% ~ 75% duty according to the SACD format book (Scarlet Book).

Note 34. The frequency response refers to the output level of 0dB when a 1kHz 25%~75% duty sine wave is input.

Note 35. The frequency (20k, 100k and 200kHz) will be doubled when the sampling speed is 128fs (DSDSEL[1:0] bits = "01") and it will be quadrupled when the sampling speed is 256fs (DSDSEL[1:0] bits = "10").

■ DC Characteristics

(Ta=-40~85°C; VDDL/R=4.75~5.25V, AVDD=TVDD=1.7~3.6V, DVDD=1.7~1.98V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
AVDD=TVDD= 1.7 ~ 3.0V					
High-Level Input Voltage	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	20%TVDD	V
AVDD=TVDD= 3.0V ~ 3.6V					
High-Level Input Voltage	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD	V
High-Level Output Voltage (TDMO, DZFL, DZFR pins: Iout=-100µA)	VOH	TVDD−0.5	-	-	V
Low-Level Output Voltage (except SDA pin: Iout= 100µA)	VOL	-	-	0.5	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout= 3mA)	VOL	-	-	0.4	V
(SDA pin, 1.7V ≤ TVDD ≤ 2.0V: Iout= 3mA)	VOL	-		20%TVDD	V
Input Leakage Current (Note 36)	Iin	-	-	±10	µA

Note 36. The TESTE, TDMO, DIF0 and DIF1 pins have internal pull-down and the PSN pin has internal pull-up devices. Therefore the TESTE, TDMO, DIF0, DIF1 and PSN pins are not included in this specification.

■ Switching Characteristics

(Ta=-40~85°C; VDDL/R=4.75~5.25V, AVDD=TVDD=1.7~3.6V, DVDD=1.7~1.98V, C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
Frequency	fCLK	2.048	-	49.152	MHz
Duty Cycle	dCLK	40	-	60	%
Minimum Pulse Width	tCLKH	9.155	-	-	nsec
	tCLKL	9.155	-	-	nsec
LRCK Clock Timing (Note 37)					
Normal Mode (TDM[1:0] bits = "00")					
Normal Speed Mode	fsn	8	-	54	kHz
Double Speed Mode	fsd	54	-	108	kHz
Quad Speed Mode	fsq	108	-	216	kHz
Oct speed mode	fso	-	384	-	kHz
Hex speed mode	fsh	-	768	-	kHz
Duty Cycle	Duty	45	-	55	%
TDM128 mode (TDM[1:0] bits = "01")					
Normal Speed Mode	fsn	8	-	54	kHz
Double Speed Mode	fsd	54	-	108	kHz
Quad Speed Mode	fsq	108	-	216	kHz
High time	tLRH	1/128fs	-	-	nsec
Low time	tLRL	1/128fs	-	-	nsec
TDM256 mode (TDM[1:0] bits = "10")					
Normal Speed Mode High time	fsn	8	-	54	kHz
Double Speed Mode	fsd	54	-	108	kHz
High time	tLRH	1/256fs	-	-	nsec
Low time	tLRL	1/256fs	-	-	nsec
TDM512 mode (TDM[1:0] bits = "11")					
Normal Speed Mode	fsn	8	-	54	kHz
High time	tLRH	1/512fs	-	-	nsec
Low time	tLRL	1/512fs	-	-	nsec

Note 37. The MCLK frequency must be changed while the AK4497 is in reset state by setting the PDN pin = "L" or RSTN bit = "0".