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AK4516A

3V 16bit ADC&DAC with built-in PGA

FEATURE

1 . Resolution: 16 bits
2 . Recording Function
- Analog Input PGA (Programmable Gain Amp)
- Peak-Meter Output
- Overflow Flag Output
- Auto Limitter Circuit
- Auto Recovery Circuit
- HPF(fc=3.4Hz) for offset cancel

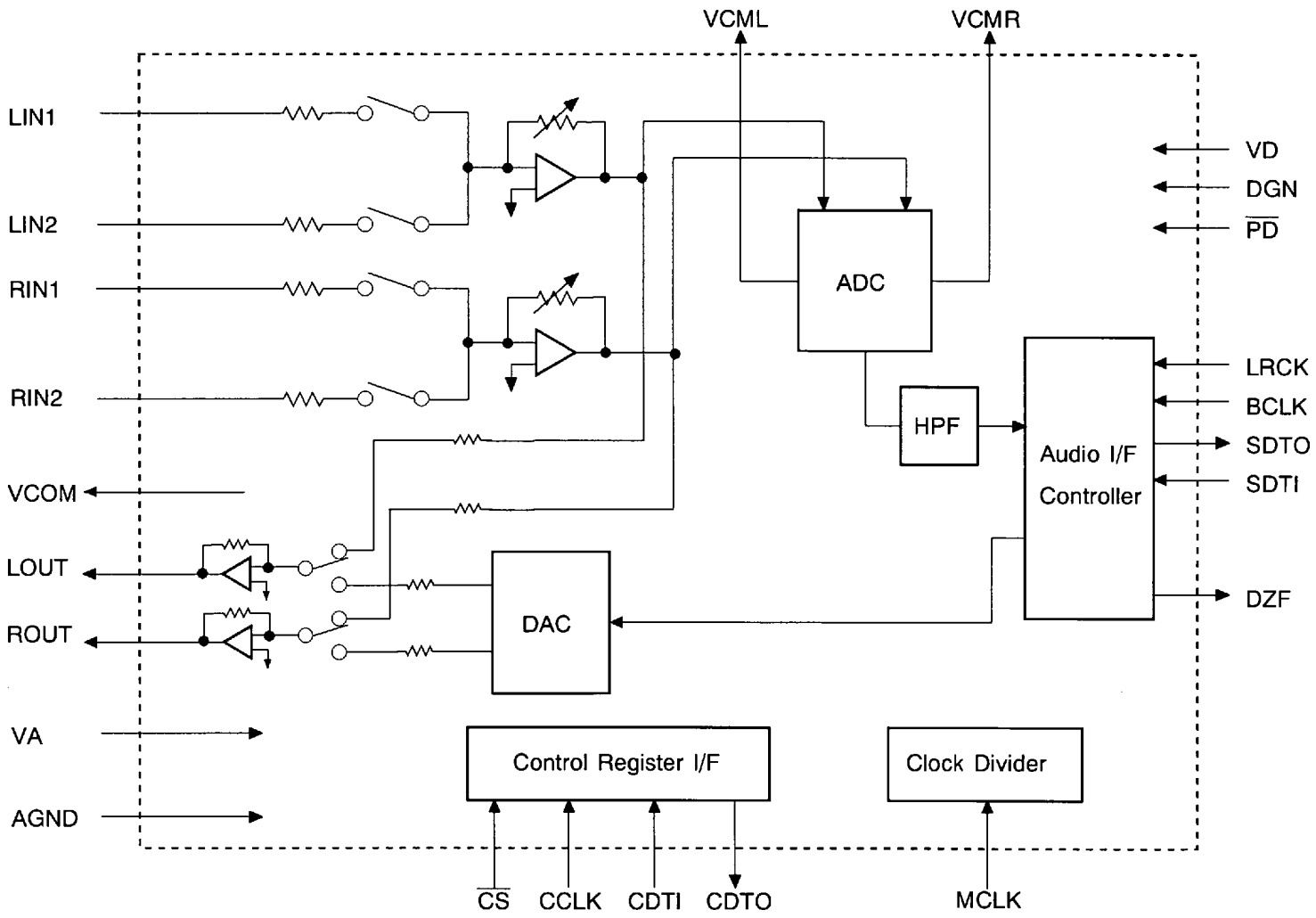
3 . Playback Function
- Digital De-emphasis Filter(tc=50/15us, fs=32kHz, 44.1kHz, 48kHz)

4 . Analog-Through Mode
5 . Power Management
6 . ADC Input (Including the PGA)
- Single-ended Input
- Input Level: 1.7Vpp (=0.57×VA, VA=3V)
- THD+N: -85dB
- DR,S/N: 90dB

7 . DAC Output
- Single-ended Output
- Output Level: 1.8Vpp (=0.6×VA, VA=3V, $R_L \geq 10k\Omega$)
- Frequency Response: ±0.5dB(~20kHz)
- THD+N: -86dB
- DR,S/N: 90dB

8 . Master Clock: 256fs/384fs
9 . Audio Data Format
- ADC: 16bit, MSB first,
  MSB justified, IIS, LSB justified(only BICK=64fs correspondent)
- DAC: 16bit, MSB first,
  MSB justified, IIS, MSB justified

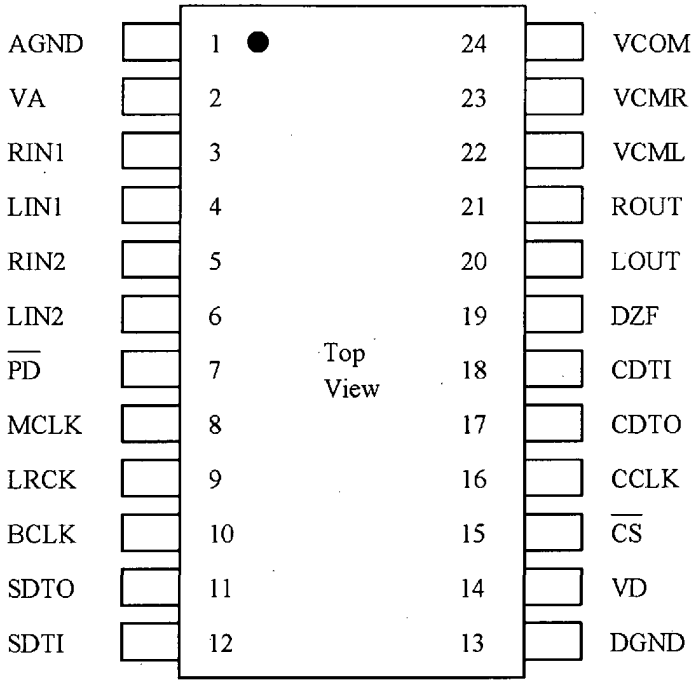
10 . Ta: -20~85°C
11 . Power Supply: 2.5~3.6V
12 . Power Dissipation: 18mA
13 . 24pinVSOP (0.65mm Pitch)


VCML
VCMR
LIN1
LIN2
RIN1
RIN2
VCOM
LOUT
ROUT
VA
AGND
ADC
HPF
DAC
Audio I/F
Controller
Control Register I/F
Clock Divider
VD
DGN
PD
LRCK
BCLK
SDTO
SDTI
DZF
CS
CCLK
CDTI
CDTO
MCLK

■ Ordering Guide

AK4516AVF	-20~+85°C	24pin VSOP(0.65mm Pitch)
AKD4516A	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	AGND	-	Analog Ground pin
2	VA	-	Analog Power Supply Pin, +3V
3	RIN1	I	Rch #1 input pin
4	LIN1	I	Lch #1 input pin
5	RIN2	I	Rch #2 input pin
6	LIN2	I	Lch #2 input pin
7	$\overline{PD}$	I	Reset & Power down Pin
8	MCLK	I	Master Clock Input Pin
9	LRCK	I	Input/Output Channel Clock Pin
10	BCLK	I	Audio Serial Data Clock Pin
11	SDTO	O	Audio Serial Data Output Pin
12	SDTI	I	Audio Serial Data Input Pin
13	DGND	-	Digital Ground Pin
14	VD	-	Digital Power Supply Pin, +3V
15	$\overline{CS}$	I	Chip Select Pin
16	CCLK	I	Control Clock Input Pin
17	CDTO	O	Control Data Output Pin
18	CDTI	I	Control Data Input Pin
19	DZF	O	Zero Detect Pin
20	LOUT	O	Lch analog output pin
21	ROUT	O	Rch analog output pin
22	VCML	O	Lch Common Voltage Output Pin, 0.5 x VA Don't be connected with external circuit.
23	VCMR	O	Rch Common Voltage Output Pin, 0.5 x VA Don't be connected with external circuit.
24	VCOM	O	Common Voltage Output Pin, 0.5 x VA Don't be connected with external circuit.

ABSOLUTE MAXIMUM RATING

(AGND,DGND=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog	VA	-0.3	6.0	V
Digital	VD	-0.3	6.0	V
VD-VA	ΔVDA	-	0.3	V
Input Current (Any pin except supplies.)	IIN	-	±10	mA
Analog Input Voltage LIN1,LIN2,RIN1,RIN2	VINA	-0.3	VA+0.3	V
Digital Input Voltage	VIND	-0.3	VA+0.3	V
Ambient Temperature	Ta	-20	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1 . All Voltage with respect to ground.

RECOMMENDED OPERATING CONDITIONS

(AGND,DGND=0V; Note1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	VA	2.5	3.0	3.6	V
	Digital	VD	2.5	3.0	VA	V

Note 1 . All Voltage with respect to ground

ANALOG CHARACTERISTICS

(Ta=25°C; VA,VD=3.0V; fs=44.1kHz; Signal Frequency=1kHz; Measurement Frequency=10Hz~20kHz ; S/(N+D), DR, S/N are specification toward full scale.signal; Unless otherwise specified)

Parameter			min	typ	max	units
Input PGA(IPGA) Characteristics:						
Input Voltage(LIN1,LIN2,RIN1,RIN2=0.57xVA)(Note2)			1.53	1.7	1.87	Vpp
Input Resistance			25	40	60	kΩ
Step Size	MIC	LINE				
	+28dB~-8dB	+8.0dB~-28dB	0.1	0.5		dB
	-8dB~-32dB	-28dB~-52dB	0.1	1		dB
	-32dB~-40dB	-52dB~-60dB	0.1	2		dB
	-40dB~-52dB	-60dB~-72dB	0.1	4		dB
ADC Analog Input Characteristics : (Note 3)						
Resolution					16	Bits
S/(N+D) (-2dB Input)			75	85		dB
DR (-60dB Input, A-Weighted)			84	90		dB
S/N (A-Weighted)			84	90		dB
Interchannel Isolation			80	90		dB
Interchannel Gain Mismatch				0.2	0.5	dB
DAC Analog Output Characteristics:(Note 4)						
Resolution					16	Bits
S/(N+D)			75	86		dB
DR (-60dB Output, A-Weighted)			84	90		dB
S/N (A-Weighted)			84	90		dB
Interchannel Isolation			90	100		dB
Interchannel Gain Mismatch				0.1	0.3	dB
Output Voltage (AOUT=0.6 x VA) (Note 2)			1.62	1.8	1.98	Vpp
Load Resistance			10			kΩ
Power Supply						
Power supply: VA+VD						
Normal Operation ($\overline{PD}$="H")						
AD+DA (PM0=1,PM1=1,PM2=1,PM3=0)				18	27	mA
AD (PM0=1,PM1=1,PM2=0,PM3=0)				11	17	mA
DA (PM0=0,PM1=0,PM2=1,PM3=0)				9	14	mA
Power-down-mode($\overline{PD}$="L") (Note 5)				10	100	uA

Note 2 . Analog Input and Output voltage (Full-Scale voltage:0dB) scale with VA.
IPGA: 0.57 x VA(typ.), DAC : 0.6 x VA(typ).

3 . ADC is input from LIN1/RIN1 or LIN2/RIN2 and it measures included in IPGL/IPGR. The value of IPGL/IPGR is set 0dB.
Internal HPF removes offset in the ADC, IPGL/IPGR.

4 . Measured by AD725C(SHIBASOKU), RMS mode.

5 . In case of the power-down mode, all digital input pins including clock(MCLK, BCLK, LRCK) pins are held VD or DGND.

FILTER CHARACTERISTICS

(Ta=25°C; VA,VD=2.5~3.6V; fs=44.1kHz; DEM bit="0")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (LPF):						
Passband (Note 6)	±0.1dB	PB	0		16.5	kHz
	-0.55dB			19.0		kHz
	-1.2dB			20.0		kHz
Stopband		SB	26.0			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	68			dB
Group Delay (Note 7)		GD		16.1		1/fs
Group Delay Distortion		ΔGD		0		us
ADC Digital Filter (HPF):						
Frequency Response (Note 6)	-3.0dB	FR		3.4		Hz
	-0.5dB			10		Hz
	-0.1dB			22		Hz
DAC Digital Filter:						
Passband (Note 6)	±0.1dB	PB	0		20.0	kHz
	-6.0dB			22.05		kHz
Stopband		SB	24.1			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 7)		GD		14.7		1/fs
DAC Digital Filter + Analog Filter						
Frequency Response 0~20.0kHz		FR		±0.5		dB

Note 6 .The passband and stopband frequencies scale with fs (system sampling rate).
For example, ADC is PB=0.431*fs(@-0.55dB), DAC is PB=0.454*fs(@-0.1dB).

7 .The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 16 bit data of both channels to the output register for ADC.
For DAC, this time is from setting the 16 bit data of both channels on input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=25°C; VA,VD=2.5~3.6V)

Parameter	Symbol	min	typ	max	units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage (Iout=-400uA)	VOH	VD-0.4	-	-	V
Low-Level Output Voltage (Iout=400uA)	VOL	-		0.4	V
Input Leakage Current	Iin	-	-	±10	uA

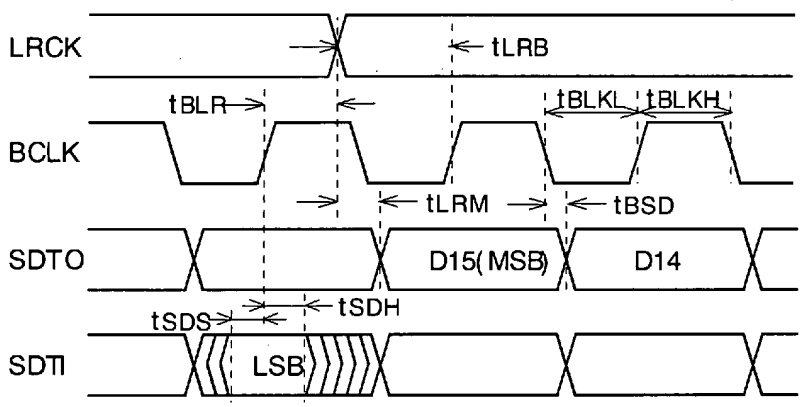
SWITCHING CHARACTERISTICS

(Ta=25°C; VA,VD=2.5~3.6V; C_L=20pF)

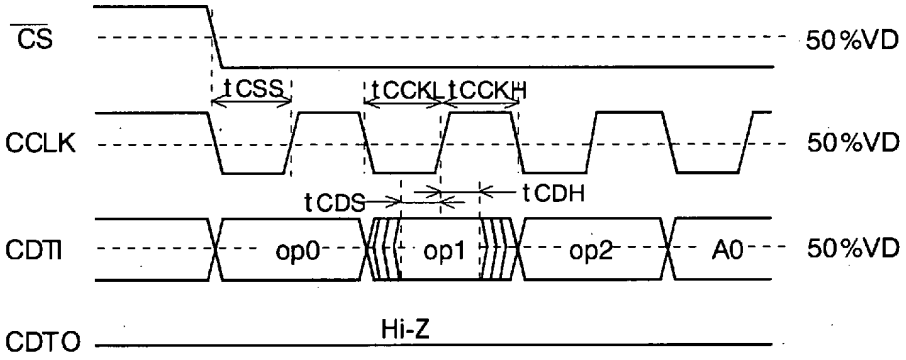
Parameter	Symbol	min	typ	max	Units
Control Clock Frequency					
Master Clock (MCLK) 256fs:	fCLK	7.68	11.2896	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs:	fCLK	11.52	16.9344	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
Channel Select Clock(LRCK) Frequency	fs	30	44.1	50	kHz
Duty		45	50	55	%
Audio Interface Timing					
BCLK period	tBLK	312.5			ns
BCLK Pulse Width Low	tBLKL	130			ns
Pulse Width High	tBLKH	130			ns
LRCK Edge to BCLK "↑"	tLRB	50			ns
BCLK "↑" to LRCK Edge	tBLR	50			ns
LRCK to SDTO(MSB) Delay Time	tLRM			80	ns
BCLK "↓" to SDTO Delay Time	tBSD			80	ns
SDTI Latch Hold Time	tSDH	50			ns
SDTI Latch Set up Time	tSDS	50			ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDATA Latch Set Up Time	tCDS	50			ns
CDATA Latch Hold Time	tCDH	50			ns
$\overline{CS}$ High Level Time	tCSW	150			ns
$\overline{CS}$ "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to $\overline{CS}$ "↑"	tCSH	50			ns
CDTO Output Delay Time	tDCD			70	ns
$\overline{CS}$ "↑"to CDTO(Hi-Z)Time (Note 8)	tCCZ			70	ns
Reset Timing					
$\overline{PD}$ Pulse Width	tPDW	150			ns
$\overline{PD}$ "↑" to SDTO Delay Time	tPDV		8224		1/fs

Note 8 .RL=1kΩ/10% Change (Pull-up operates for VD)

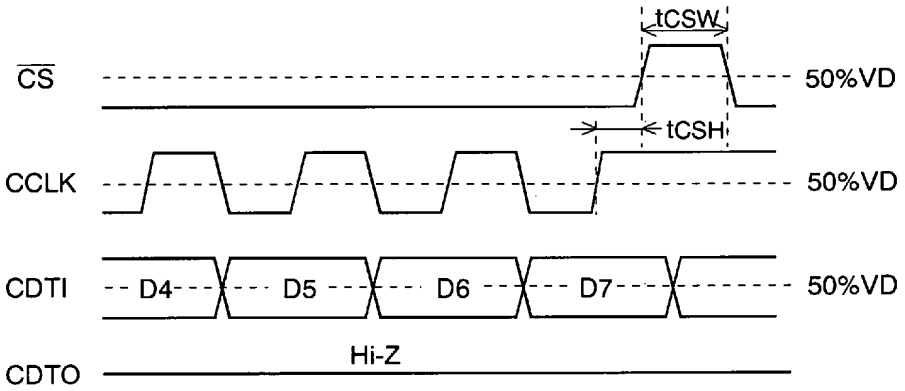
■ **Timing Diagram**



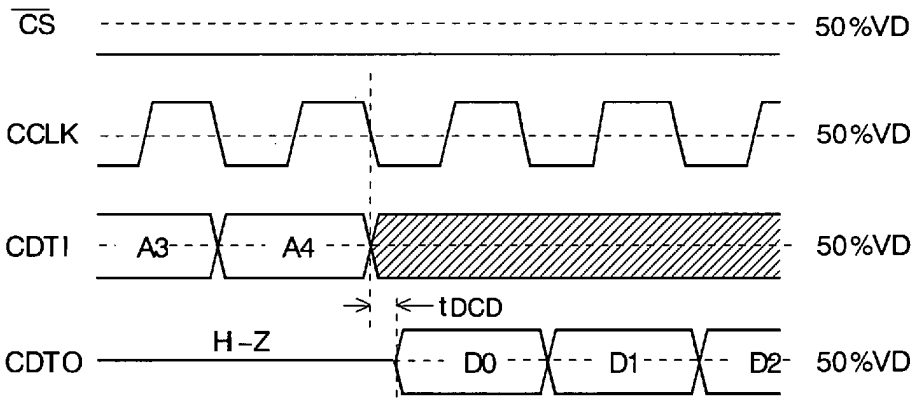
Audio Data Input/Output Timing



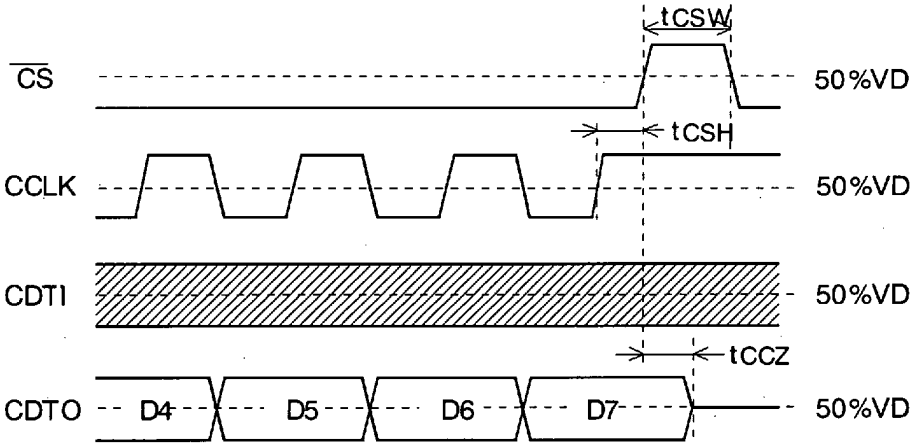
Command Input Timing in WRITE/READ



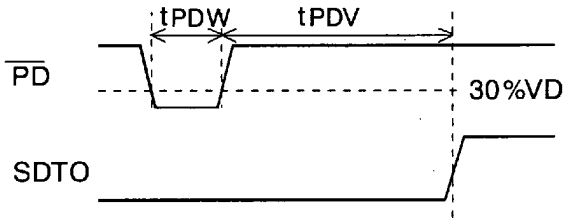
Data Input Timing in WRITE



Data Output Timing 1 in READ



Data Output timing 2 in READ



Reset Timing

OPERATION OVERVIEW

■ System Clock

The clocks which are required to operate are MCLK(256fs/384fs), LRCK(fs), BCLK(32fs~). The master clock (MCLK) should be synchronized with LRCK but the phase is free of care.
The MCLK can be input 256fs or 384fs. When 384fs is input, the internal master clock is divided into 2/3 automatically. *fs is sampling frequency.

All external clocks (MCLK, BCLK, LRCK) should always be present whenever IPGA or ADC or DAC is in operation. If these clocks are not provided, the AK4516A may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4516A should be in the power-down mode. (Please refer to the "Mode Control 1" section.)

■ System Reset

AK4516A should be reset once by bringing $\overline{PD}$ pin "L" upon power-up. The internal timing starts clocking by LRCK "↑" after exiting reset by MCLK. After the system reset operation, the all internal AK4516A registers are initial value.

■ Zero detection

When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes to "L", if the input data are not zero. When the DAC is power-down, DZF becomes to "L".

■ Digital High Pass Filter(HPF)

The ADC has HPF for the DC offset cancel. The cut-off frequency of HPF is 3.4Hz(@fs=44.1kHz) and it is -0.1dB at 22Hz. It also scales with the sampling frequency(fs).

■ Audio Serial Interface Format

Data is shifted in/out the SDTI/SDTO pins using BCLK and LRCK inputs. Four serial data are selected by the DIF0 and DIF1 pins as shown in Table 1 . In all modes, the serial data is MSB-first, 2's compliment format and it is latched by "↑" of BCLK.

When DIF1="0" and DIF0="1", only BCLK=64fs is acceptable.

No.	DIF1	DIF0	SDTO(ADC)	SDTI(DAC)	BCLK	Figure	
0	0	0	MSB justified	LSB justified	≥32fs	Figure 1	RESET
1	0	1	LSB justified	LSB justified	= 64fs	Figure 2	
2	1	0	MSB justified	MSB justified	≥32fs	Figure 3	
3	1	1	I^2S compatible	I^2S compatible	≥32fs	Figure 4	

Table 1 . Audio Data Format

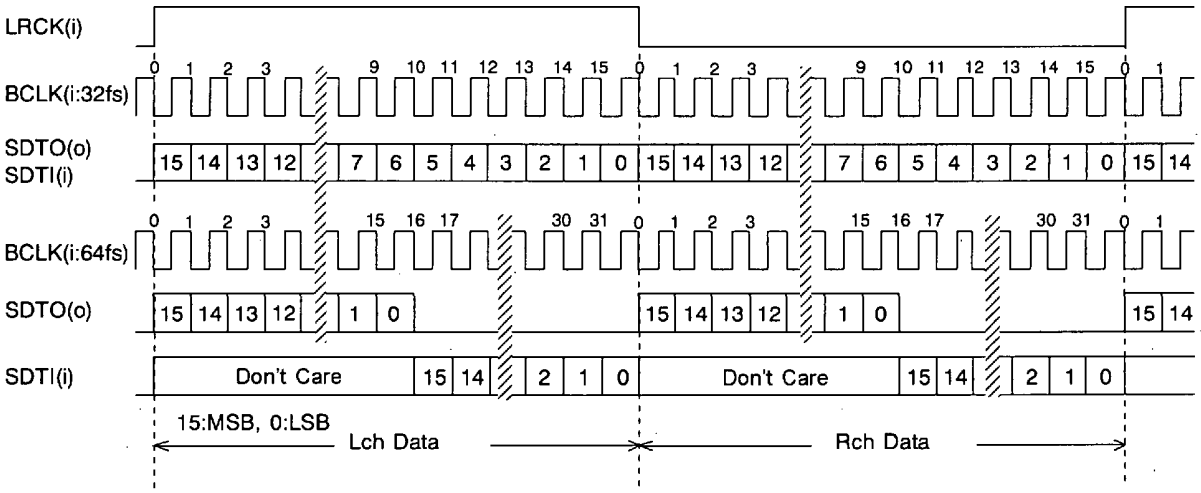


Figure 1. Audio Data Timing (No.0)

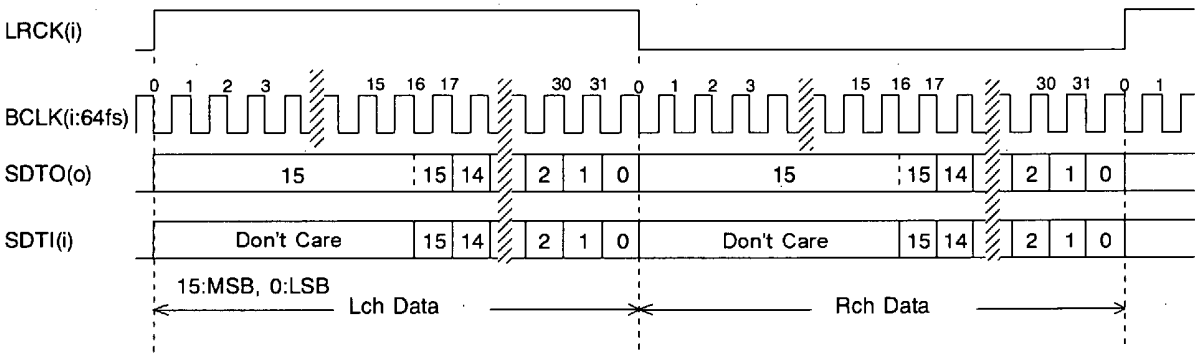


Figure 2. Audio Data Timing (No.1)

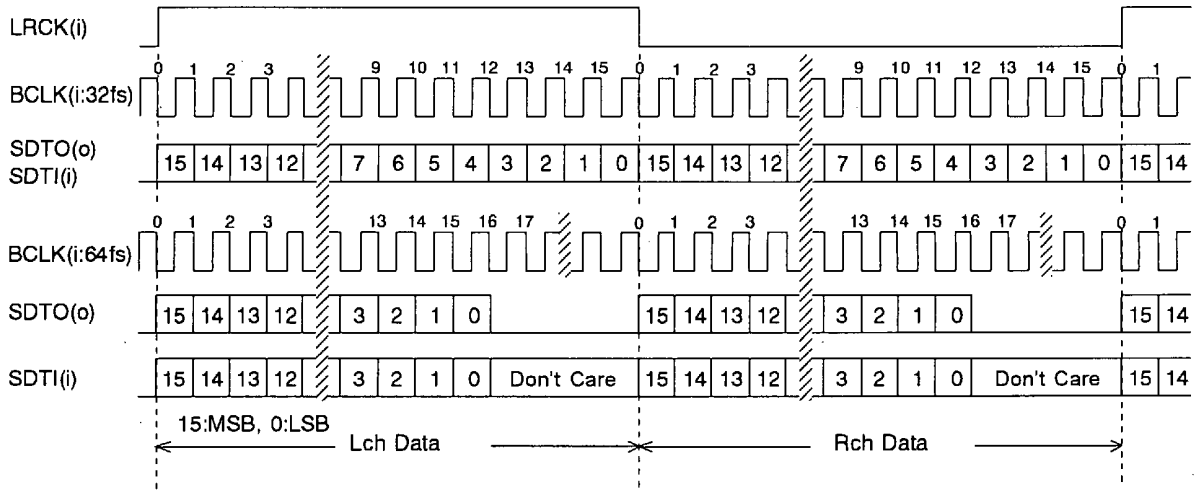


Figure 3. Audio Data Timing (No.2)

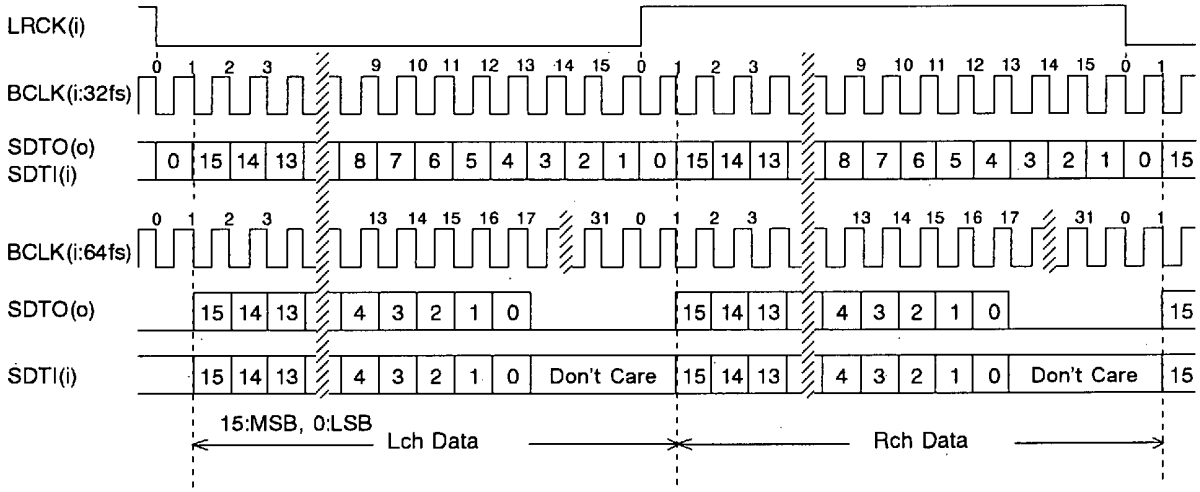
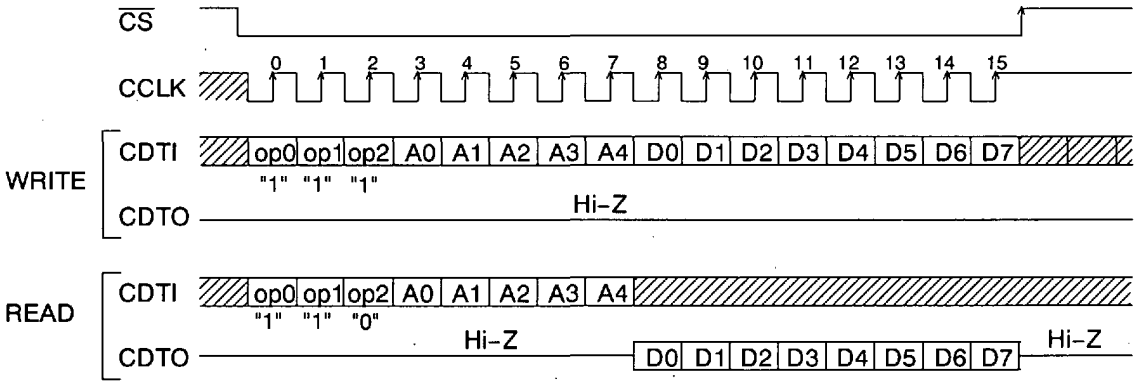


Figure 4. Audio Data Timing (No.3)

■ **Control Register R/W Timing**

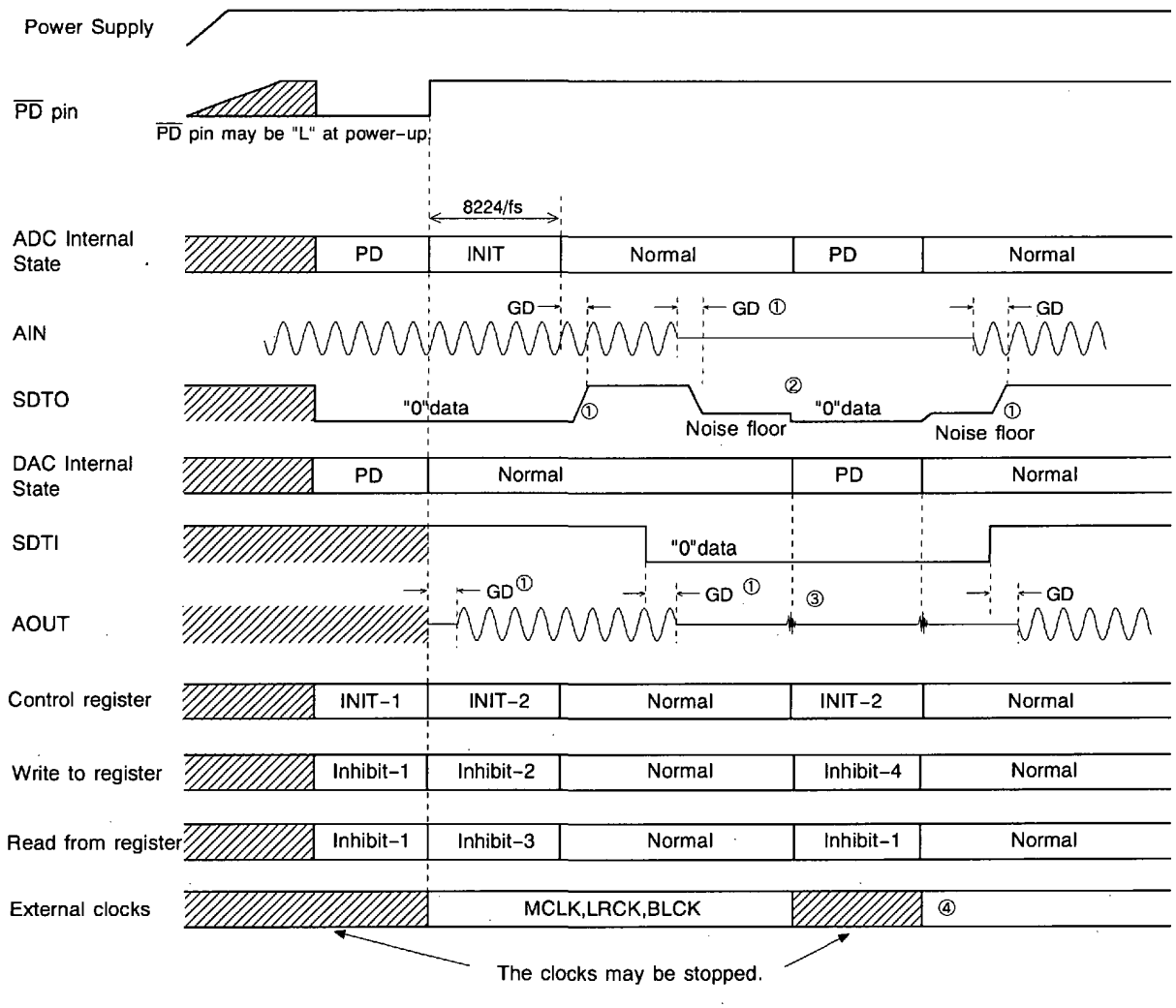
The data on the 4 wires serial interface consists of op-code(3bit), address(LSB-first, 5bit) and control data (LSB-first, 8bit). The transmitting data is output to each bit by "↓" of CCLK, the receiving data is latched by "↑" of CCLK. Writing data becomes effective by "↑" of $\overline{CS}$. Reading data becomes Hi-Z(floating) by "↑" of $\overline{CS}$. $\overline{CS}$ should be held to "H" at no access. In case of connecting between CDTI and CDTO, the I/F can be also controlled by 3-wires.

CCLK always needs 16 edges of "↑" during $\overline{CS}$="L". Reading/Writing of the address except 00H~0DH are inhibited.
Reading/Writing of the control registers by except op0=op1="1" are invalid.



op0- op2: Op- code (111:WRITE, 110:READ)
A0- A4: Address
D0- D7: Control Data

Figure 5 . Control Data Timing



- INIT: Initializing. At this time, ZFIPL and ZFIPR are "0". When these flags becomes "1", INIT process has completed.
- PD: Power-down state. ADC is output "0", analog output of DAC goes floating.
- INIT-1: Initializing all registers.
- INIT-2: Initializing read only registers in control registers.
- Inhibit-1: Inhibits writing and reading to all control registers.
- Inhibit-2: Enable writing to control registers except "Mode Control 1 (01H)" register.
- Inhibit-3: Enable reading from control registers.
- Inhibit-4: Enable writing to only "Mode Control 1 (01H)" register of the control registers.

Note: Please refer to "explanation of register" about the condition of each register.

① Digital output corresponding to analog input and analog output corresponding to digital input have the group delay(GD).

② If the analog signal does not be input, the digital outputs have the offset to the op-amp of input and some offset error of the internal ADC.

③ A few noise occurs at the "↓↑" of $\overline{PD}$ signal.
Please mute the analog output externally if the noise influences the system application.

④ When the external clocks are stopped, the AK4516A should be in the power-down mode.

Figure 6 .Power-up/Power-down Timing Example

■ **Operation mode explanation**

The AK4516A can perform the limitter operation and the recovery operation automatically. There are three operation modes.

1. Manual Mode

The manual mode is used when the AK4516A mode is changed (for example, when the input pin or the De-emphasis etc setting is changed) or the recording level is adjusted from uP writing operation by manual. In case of the semi-auto or the full-auto modes, it is impossible to set up a part of the register.
(Refer to "Semi-auto mode", "Full-auto mode" section).

2. Semi-auto Mode

The semi-auto mode is the mode that uses the AK4516A auto limitter function, and the recovery operation is processed by uP or DSP etc.
During the semi-auto mode, writing to the following registers from uP is inhibited.

- LRGA, LTM1-0, ZELM, LMTH1-0, LMAT2-0

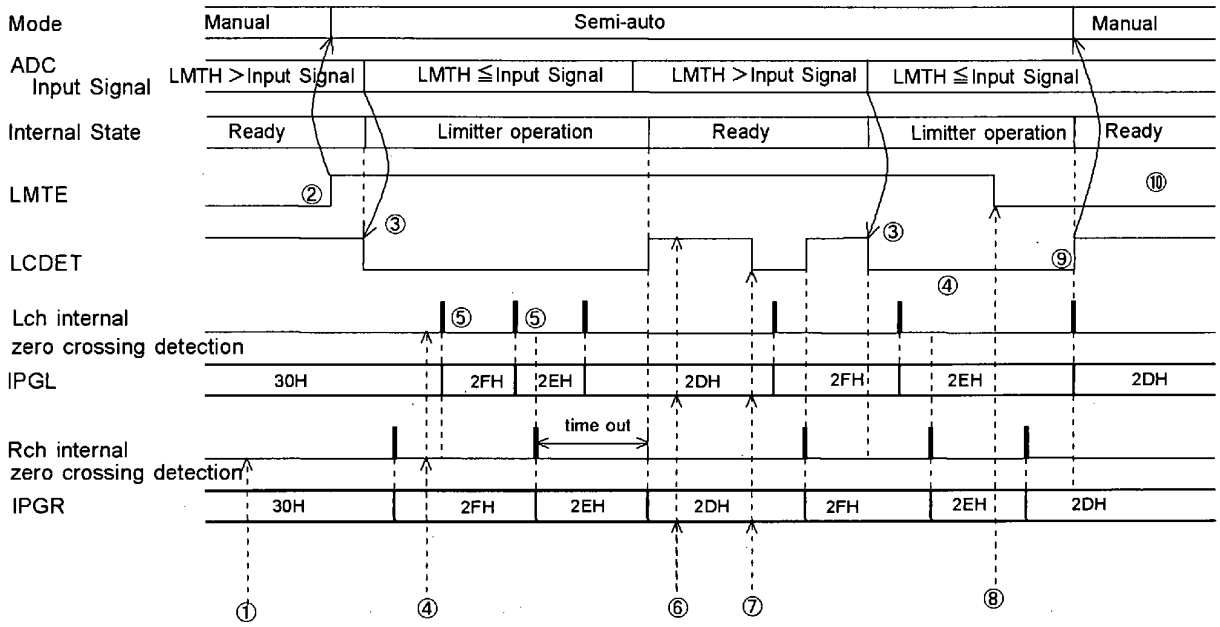


Figure 7 . Control example of semi-auto mode operation(LMAT = 1 step, ZENM=ZELM="1")

① Setting up the registers for the semi-auto mode operation.
(LTM1-0, ZELM, LMTH1-0, LMAT2-0, IPGL, IPGR, LRGA="1", GSEL)

② WR(LMTE="1", RCVE="0"): After the registers concerned in the auto limitter operation is set up and confirming the zero crossing flags(ZFIPL,ZFIPR)="1", LMTE is set "1".

③ As the input signal of ADC exceeds LMTH, the auto limitter operation starts.

④ WR(IPGA="31H"):As the auto limitter is in operation, writing by uP is ignored.

⑤ After the zero crossing operation of both Lch and Rch is completed, the next operation starts.

⑥ RD(LCDET&IPGA):Confirm to complete auto limitter operation and reads the IPGA present value.

⑦ WR(IPGA="2FH"):Update IPGA value.

⑧ WR(LMTE="0")

⑨ In Figure 7 , since "0" is written to LMTE during ATT operation, the operation changes to manual mode after completing ATT operation. After confirming LCDET="1", it is possible to change the each register set-up. If LMTE is set "0" during the auto limitter operation or the update of the IPGA value by uP, LCDET becomes "1" after the max "1" ATT/GAIN operation is completed by internal state.

⑩ In this case, the input signal of ADC exceeds LMTH, the auto limitter does not operate because of LMTE="0".

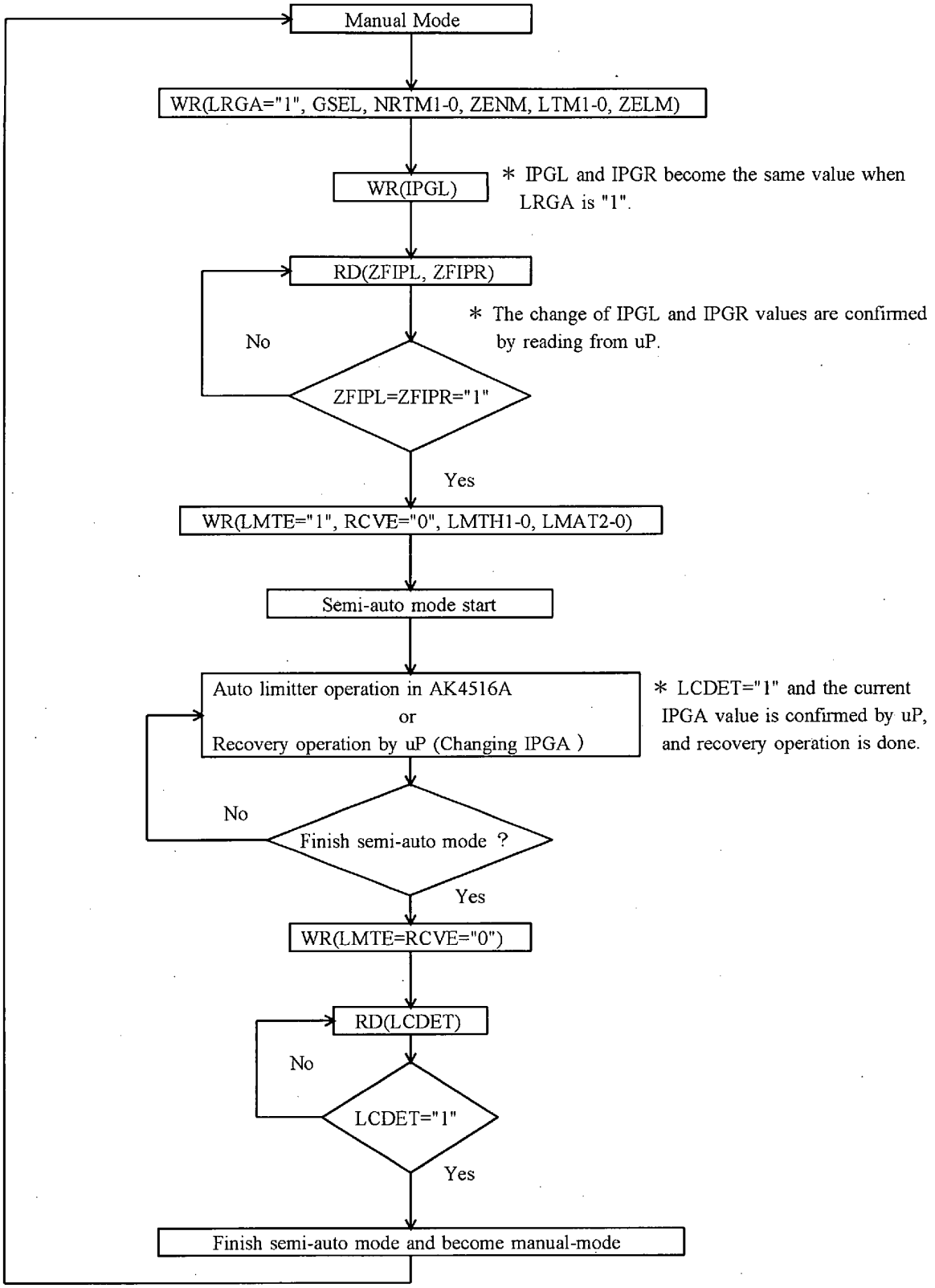


Figure 8 Register set-up sequence at Semi-auto mode

3. Full-auto Mode

The full-auto mode is done automatically by the auto limitter and the auto recovery function of the AK4516A. However, writing to the register is needed to enable these functions.
During the full-auto mode, writing to the following registers from uP is inhibited.

- LRGA, LTM1-0, ZELM, LMTH1-0, LMAT2-0, WTM1-0, NRTM1-0, RATT1-0, ZENM, REF6-0, IPGL, IPGR

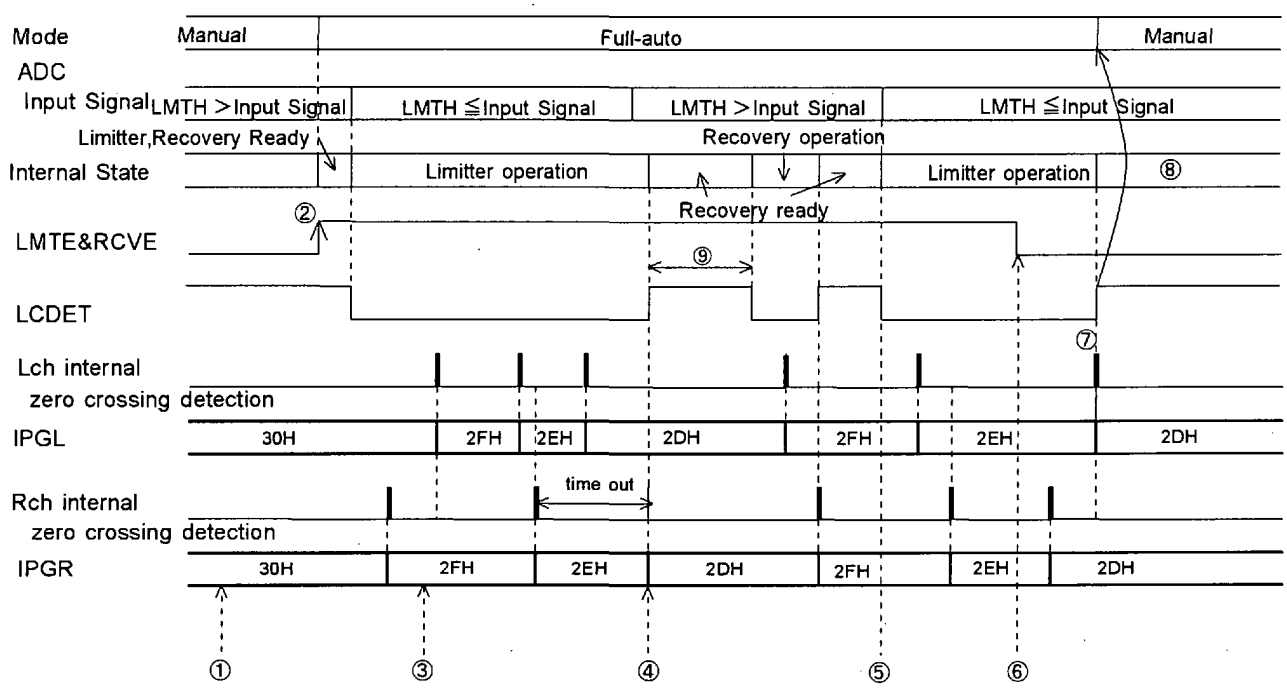


Figure 9 . Control example of full-auto mode operation (LMAT=RATT: 1 step, ZENM=ZELM="1")

① Set-up the registers of full-auto mode
(LTM1-0, ZELM, LMTH1-0, LMAT2-0, WTM1-0, RATT1-0, NRTM1-0, ZENM, REF6-0, GSEL, IPGL, IPGR, LRGA="1")

② WR(LMTE=RCVE="1"): After the registers concerned in the auto limitter operation is set up and confirming the zero crossing flags(ZFIPL, ZFIPR)="1", LMTH and RCVE are set "1".

③ WR(IPGA="31H"):As the operation is full-auto mode, writing by uP is ignored.

④ The ready of recovery starts.

⑤ As the input signal of ADC exceeds LMTH, the recovery operation (in the figure, recovery ready) is discontinued and the limitter operation starts.

⑥ WR(LMTE=RCVE="0"):The full-auto mode operation is completed.

⑦ In Figure 9 , since "0" is written to LMTE& RCVE during the ATT operation, the operation changes to the manual mode after completing ATT operation. After confirming LCDET="1", it is possible to change the each register set-up. If LMTE&RCVE are set "0" during the full-auto mode operation, LCDET becomes "1" after the max "1" ATT/GAIN operation is completed by internal state.

⑧ In this case, the input signal of ADC exceeds LMTH, the auto limitter does not operate because of LMTE=RCVE="0".

⑨ After the limitter operation is completed, the AK4516A waits for the time set by WTM1-0. If the input signal does not exceed (LMTH - 2dB), the recovery operation is executed. After the waiting time finishes the next waiting time starts immediately. In recovery ready, the waiting timer is reset under the condition of (LMTH - 2dB) ≤Input Signal<LMTH. And the timer starts under the condition of (LMTH - 2dB)>Input Signal.

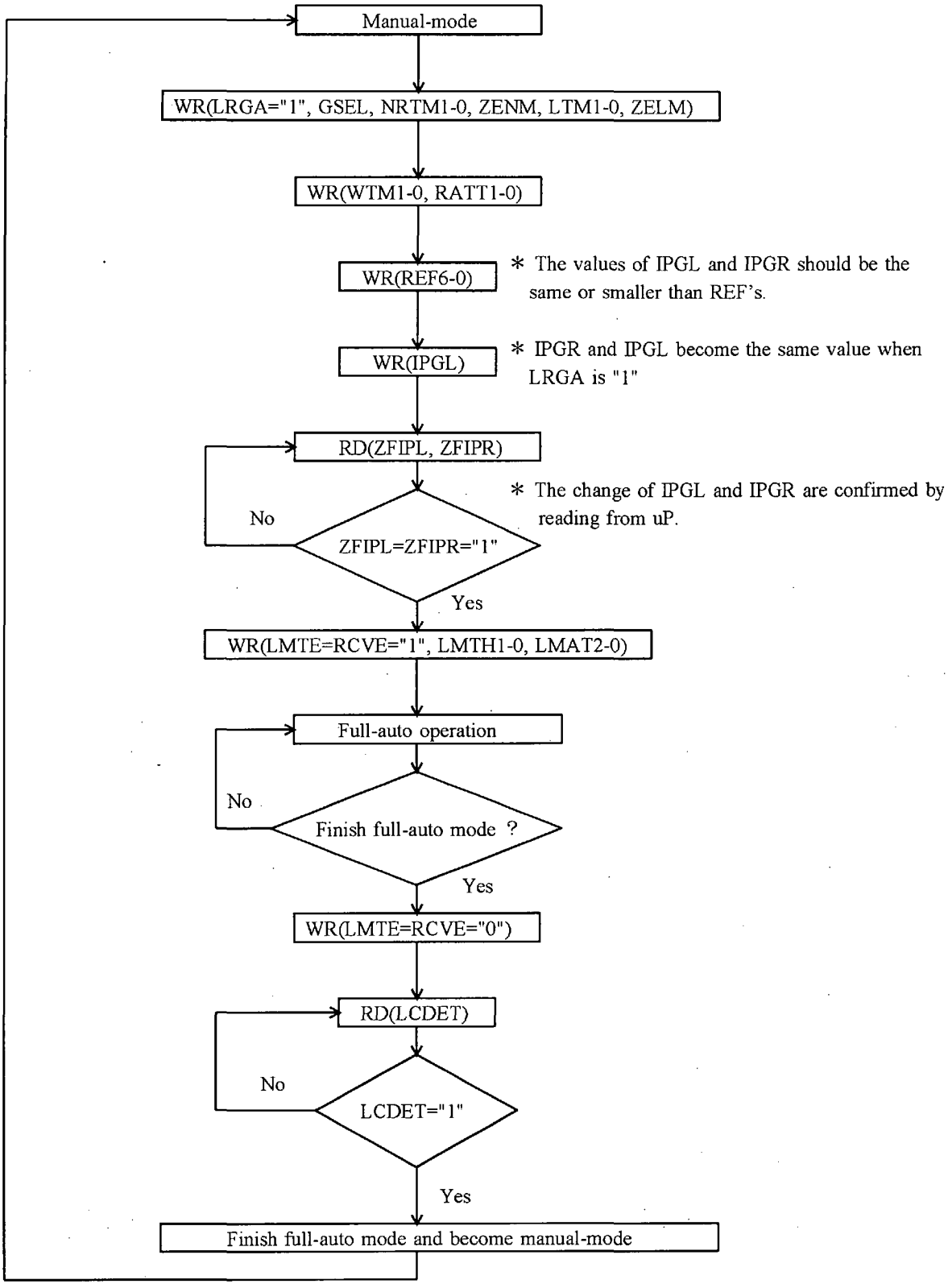


Figure 10 . Registers set-up sequence at Full-auto mode

Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Select	0	0	0	0	RIN2	RIN1	LIN2	LIN1
01H	Mode Control 1	0	0	0	0	PM3	PM2	PM1	PM0
02H	Mode Control 2	MONO1	MONO0	DIF1	DIF0	FS1	FS0	DEM	0
03H	Zero Cross & Timer Control	LRGA	GSEL	NRTM1	NRTM0	ZENM	LTM1	LTM0	ZELM
04H	Peak Hold Low Byte Lch	PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0
05H	Peak Hold High Byte Lch	PUL7	PUL6	PUL5	PUL4	PUL3	PUL2	PUL1	PUL0
06H	Peak Hold Low Byte Rch	PLR7	PLR6	PLR5	PLR4	PLR3	PLR2	PLR1	PLR0
07H	Peak Hold High Byte Rch	PUR7	PUR6	PUR5	PUR4	PUR3	UR2	PUR1	PUR0
08H	Overflow Status	ZFIPR	ZFIPL	ROF2	ROF1	ROF0	LOF2	LOF1	LOF0
09H	Auto LMT&RCV Control	LMTE	RCVE	0	LMTH1	LMTH0	LMAT2	LMAT1	LMAT0
0AH	Input PGA Control Lch	LCDET	IPGL6	IPGL5	IPGL4	IPGL3	IPGL2	IPGL1	IPGL0
0BH	Input PGA Control Rch	LCDET	IPGR6	IPGR5	IPGR4	IPGR3	IPGR2	IPGR1	IPGR0
0CH	Auto Recovery Control 1	0	0	0	0	WTM1	WTM0	RATT1	RATT0
0DH	Auto Recovery Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0

Table 2 . AK4516A Register Map

Input Select

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Select	0	0	0	0	RIN2	RIN1	LIN2	LIN1
R/W		R/W							
RESET		0	0	0	0	0	1	0	1

LIN2-1 : Select ON/OFF of Lch input (0:OFF, 1:ON). These bits can select to ON/OFF at the same time.
RIN2-1 : Select ON/OFF of Rch input (0:OFF, 1:ON). These bits can select to ON/OFF at the same time.

This register is reset at $\overline{PD}$ pin="L", then inhibits writing to this register.

Mode Control 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Mode Control 1	0	0	0	0	PM3	PM2	PM1	PM0
R/W		R/W							
RESET		0	0	0	0	0	1	1	1

PM3-0: Power Management (0: Power Down, 1:Power Up)

PM0: Mixer, PGA input, Auto Limitter and Auto Recovery power control.

PM1: Power control of ADC

PM2: Power control of DAC

PM3: Used both as power control of analog loopback circuit and as selection of MUX.
(0: DAC, 1:Analog loopback)

PM0-3 can be partially powered-down by ON/OFF of PM0-3. When $\overline{PD}$ pin goes "L", all the circuit in AK4516A can be powered-down regardless of PM0-3.
When PM0-3 go all "0", all the circuits in AK4516A can be also powered-down.
When PM3 goes "1", input for output-AMP is selected to analog loopback circuit from DAC output.
Output MUX and AMP are powered-down when $\overline{PD}$="L" or PM2=PM3="0". Refer to Figure 11 .

The loopback output and the MUX selecting DAC output is a MIXER with the switch in practice. Therefore, when both PM2 and PM3 select ON, the analog loopback signal and DAC output are mixed by Gain 1.

Except the case of PM0=PM1=PM2=PM3="0" or $\overline{PD}$ pin="L", MCLK, BCLK, LRCK should not be stopped.

When the input PGA and MUX are powered-down by PM0-3 or $\overline{PD}$ pin, the output of AMP becomes Hi-Z(floating).

This register is reset by the $\overline{PD}$ pin="L", then inhibits writing to this register.

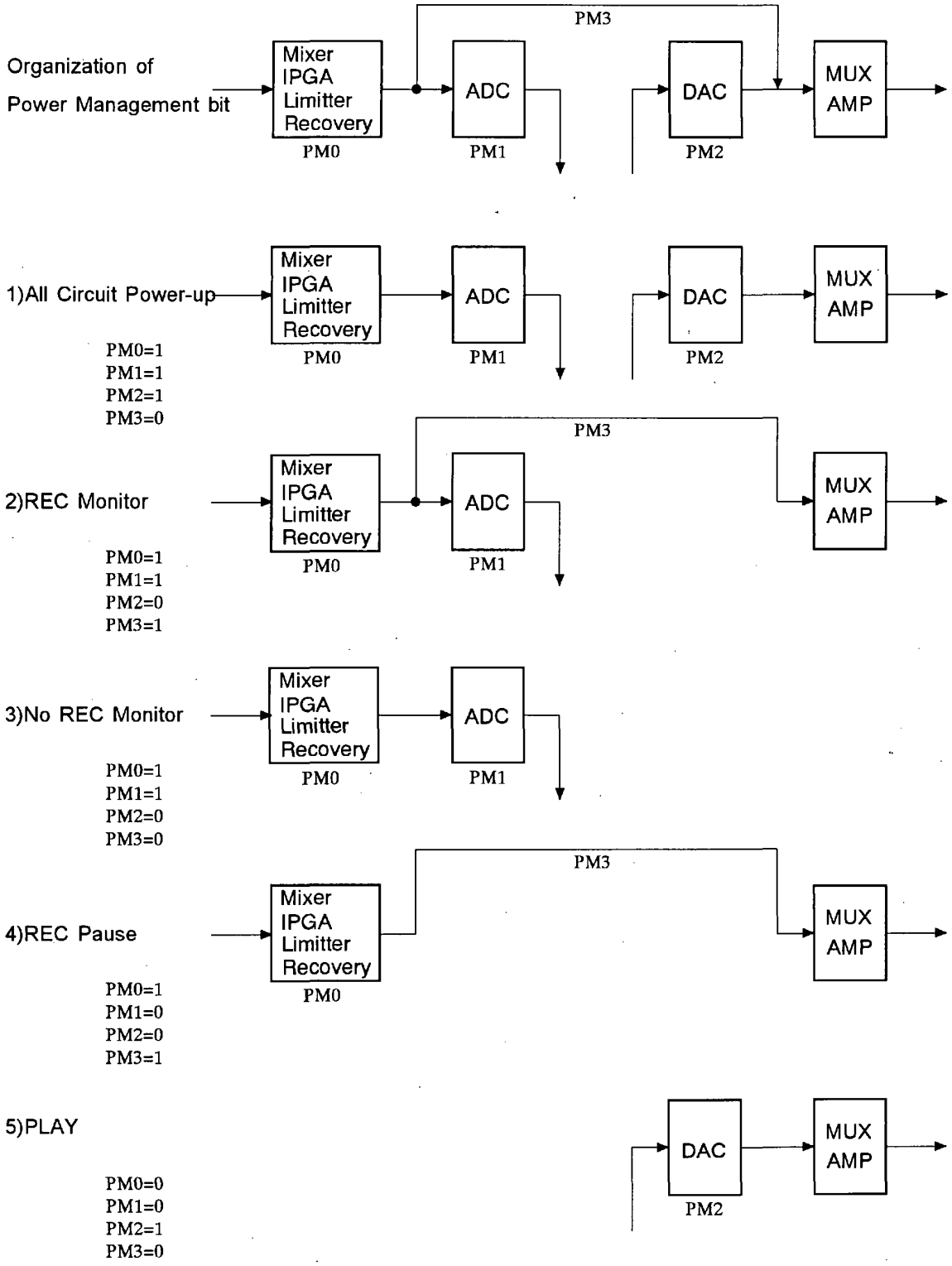


Figure 11 . Power Management

Mode Control 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Mode Control 2	MONO1	MONO0	DIF1	DIF0	FS1	FS0	DEM	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	RD
RESET		0	0	0	0	0	0	0	0

MONO1-0:Monaural Mixing

00: Stereo (RESET)
01: (L+R)/2
10: LL
11: RR

DIF1-0: Select Audio Serial Interface Format

The data is all 2's complement, MSB first.

No.	DIF1	DIF0	SDTO(ADC)	SDTI(DAC)	BCLK	Figure	
0	0	0	MSB justified	LSB justified	≥32fs	Figure 1	RESET
1	0	1	LSB justified	LSB justifed	= 64fs	Figure 2	
2	1	0	MSB justified	MSB justified	≥32fs	Figure 3	
3	1	1	I^2S compatible	I^2S compatible	≥32fs	Figure 4	

Table 3 . Audio Serial Interface Format

FS1-0:Select De-emphasis frequency

The AK4516A includes the digital de-emphasis filter(tc=50/15us) by IIR filter. The filter corresponds to three sampling frequency (32kHz, 44.1kHz, 48kHz). The de-emphasis filter selected by FS0 and FS1 registers are enabled for input audio data.

FS1	FS0	Mode	
0	0	44.1kHz	RESET
0	1	OFF	
1	0	48kHz	
1	1	32kHz	

Table 4 . De-empahsis frequency

DEM: Control of De-emphasis (0: Disable, 1: Enable)

FS0 and FS1 registers of the de-emphasis are enabled by setting DEM=1. FS0 and FS1 are ignored at DEM=0.

This register is reset by the $\overline{PD}$ pin="L", then inhibits writing to this register.

Zero Cross & Timer Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Zero Cross & Timer Control	LRGA	GSEL	NRTM1	NRTM0	ZENM	LTM1	LTM0	ZELM
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET		1	1	1	0	0	1	0	0

LRGA: Selects the method of writing to IPGA

0: Independent data can be written to IPGA and IPGR.

1: Common data can be written to IPGL and IPGR.

In this case, when a data is written to IPGL, the same data is also written to IPGR. When a data is written to IPGR, a data is only written to IPGR. When IPGL value differs from IPGR value, IPGL and IPGR values can be set by a common data after writing IPGL value at LRGA="1". (RESET)

GSEL:Selects input gain (set a common Lch and Rch)

0: LINE

1: MIC (RESET)

Even if LINE and MIC are the same data value, both gain values are different.

NRTM1-0: Zero crossing timeout at writing operation by uP and auto recovery operation.

Set-up zero crossing timeout at writing operation by uP and the auto recovery operation. The writing operation by uP and the auto recovery operation set up in common. In case of the auto limitter operation, zero crossing operation is set by different bits(LTM1-0).

NRTM1	NRTM0	Zero crossing timeout(ZENM="1")				
			48kHz	44.1kHz	32kHz	
0	0	513/fs	10.7ms	11.6ms	16.0ms	
0	1	1025/fs	21.4ms	23.2ms	32.0ms	
1	0	2049/fs	42.7ms	46.5ms	64.0ms	RESET
1	1	4097/fs	85.4ms	92.9ms	128.0ms	

Table 5 . Zero crossing timeout at uP writing operation and auto recovery operation.
(NRTM1="1", NRTM0="0" at RESET)

ZENM: Enables zero crossing detection at uP WRITE operation or auto recovery operation
(0: Disable, 1: Enable)

1: When IPGA of each L/R channels do zero crossing or timeout independently, the IPGA value is changed by uP WRITE operation or auto recovery operation.

0: IPGA is changed immediately.