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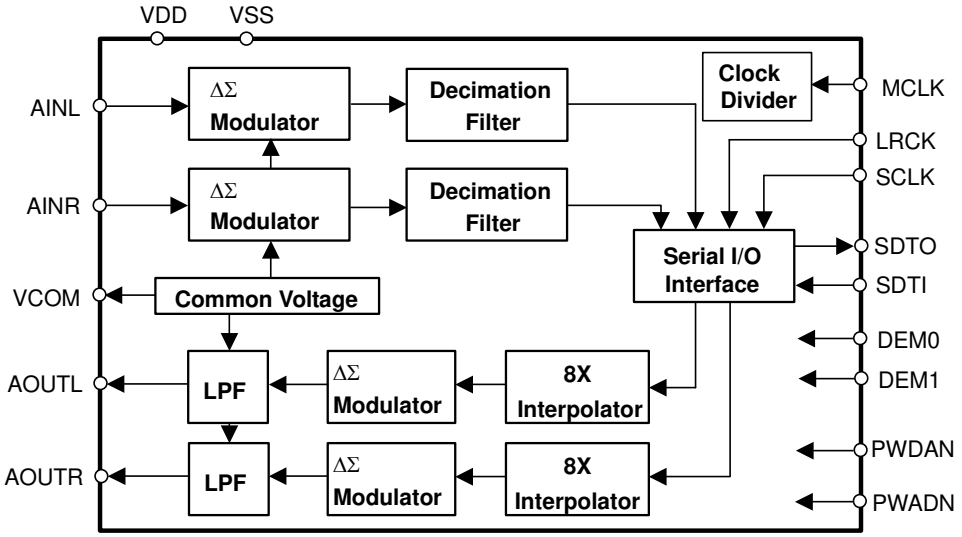
AK4555
Low Power & Small Package 20bit ΔΣ CODEC

GENERAL DESCRIPTION

The AK4555 is a low voltage 20bit A/D & D/A converter for portable digital audio system. In the AK4555, the loss of accuracy form clock jitter is also improved by using SCF techniques for on-chip post filter. Analog signal input/output of the AK4555 are single-ended, therefore, any external filters are not required. The AK4555 is suitable for portable digital audio system, as the AK4555 is low power dissipation and a small package.

FEATURES

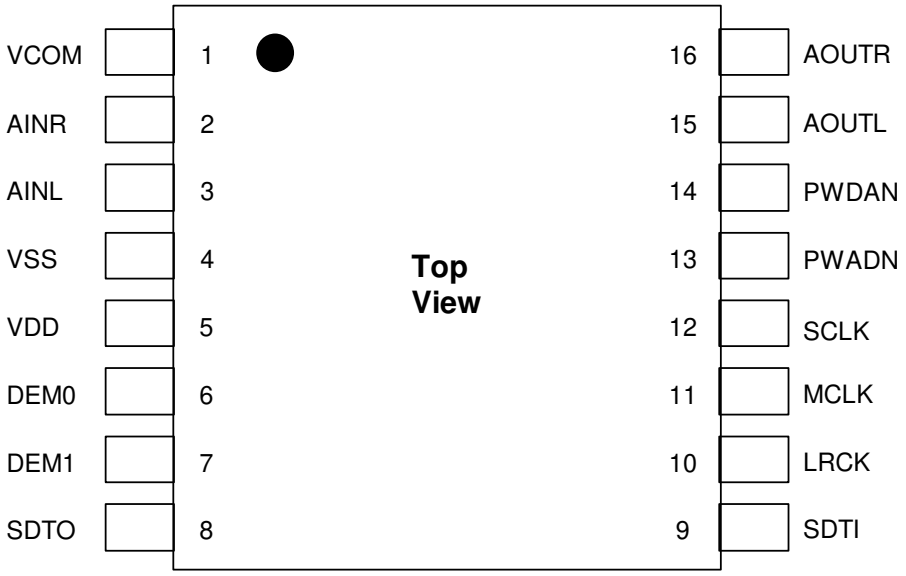
- ☐ **HPF for DC-offset cancel (fc=3.4Hz)**
- ☐ **Single-ended ADC**
  - **S/(N+D): 80dB@VDD=2.5V**
  - **Dynamic Range, S/N: 89dB@VDD=2.5V**
- ☐ **Single-ended DAC**
  - **Digital de-emphasis for 32kHz, 44.1kHz, 48kHz sampling**
  - **S/(N+D): 85dB@VDD=2.5V**
  - **Dynamic Range, S/N: 92dB@VDD=2.5V**
- ☐ **Audio I/F format: MSB First, 2's Compliment**
  - **ADC, DAC: I^2S**
- ☐ **Input/Output Voltage: 0.6 x VDD (=1.5Vpp@VDD=2.5V)**
- ☐ **High Jitter Tolerance**
- ☐ **Sampling Rate: 8kHz to 50kHz**
- ☐ **Master Clock: 256fs/384fs/512fs/768fs (fs=8kHz to 50kHz)**
  1024fs (fs=8kHz to 25kHz)
- ☐ **Power Supply: 1.6 to 3.6V**
- ☐ **Low Power Supply Current: 8.6mA**
- ☐ **Ta = –40 to 85°C**
- ☐ **Very Small Package: 16pin TSSOP**



■ Ordering Guide

AK4555VT	–40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4555	Evaluation Board for AK4555	

■ Pin Layout



■ Comparison with AK4550 and AK4554

Item	AK4550	AK4554	AK4555
Power Supply Voltage	2.3 ~ 3.6V	1.6 ~ 3.6V	←
Audio I/F Format	ADC: 16bit MSB justified DAC: 16bit LSB justified	ADC: 16bit MSB justified DAC: 16bit LSB justified	I^2S
VCOM pin	0.45 x VDD	0.5 x VDD	←
ADC S/(N+D) (typ)	82dB	80dB	←
ADC Input Resistance (typ)	100kΩ	70kΩ	←
Power Supply Current (typ)			
AD+DA	10mA	8mA	←
AD	5.6mA	4mA	←
DA	5.6mA	4.4mA	←
DAC Digital Filter			
Stopband Attenuation (min)	43dB	54dB	←
Passband Ripple (max)	±0.06dB	±0.02dB	←
Group Delay	14.8/fs	19.0/fs	←
MCLK	256fs/384fs/512fs	256fs/384fs/512fs/768fs (fs=8~50kHz) 1024fs (fs=8~25kHz)	←
External Circuit			
VCOM pin	4.7μF + 0.1μF	0.1μF	←
AINL, AINR pins	RC filter is needed.	RC filter is on-chip.	←

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCOM	O	Common Voltage Output Pin, 0.5 x VDD
2	AINR	I	Rch Analog Input Pin
3	AINL	I	Lch Analog Input Pin
4	VSS	-	Ground Pin
5	VDD	-	Power Supply Pin
6	DEM0	I	De-emphasis Control Pin
7	DEM1	I	De-emphasis Control Pin
8	SDTO	O	Audio Serial Data Output Pin
9	SDTI	I	Audio Serial Data Input Pin
10	LRCK	I	Input/Output Channel Clock Pin
11	MCLK	I	Master Clock Input Pin
12	SCLK	I	Audio Serial Data Clock Pin
13	PWADN	I	ADC Power-Down & Reset Mode Pin "L": Power down. ADC should always be reset upon power-up.
14	PWDAN	I	DAC Power-Down & Reset Mode Pin "L": Power down. DAC should always be reset upon power-up.
15	AOUTL	O	Lch Analog Output Pin
16	AOUTR	O	Rch Analog Output Pin

Note: All input pins except analog input pins (AINR and AINL) should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	AINR, AINL, AOUTL, AOUTR	These pins should be open.
Digital	SDTO	This pin should be open.
	SDTI	This pin should be connected to VSS.

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VDD	–0.3	4.6	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage	VIN	–0.3	VDD+0.3	V
Ambient Temperature (power applied)	Ta	–40	85	°C
Storage Temperature	Tstg	–65	150	°C

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	1.6	2.5	3.6	V

Note 1. All voltages with respect to ground.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VDD=2.5V; fs=44.1kHz; Signal Frequency=1kHz; SCLK=64fs; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
ADC Analog Input Characteristics: (Note 2)					
Resolution		-	-	20	Bits
S/(N+D)	(–0.5dB Input)	70	80	-	dB
D-Range	(–60dB Input, A-weighted)	82	89	-	dB
S/N	(A-weighted)	82	89	-	dB
Interchannel Isolation		80	95	-	dB
Interchannel Gain Mismatch		-	0.2	0.5	dB
Input Voltage	(Note 3)	1.35	1.50	1.65	Vpp
Input Resistance		40	70	-	kΩ
Power Supply Rejection	(Note 4)	-	45	-	dB
DAC Analog Output Characteristics:					
Resolution		-	-	20	Bits
S/(N+D)		75	85	-	dB
D-Range	(–60dB Output, A-weighted)	86	92	-	dB
S/N	(A-weighted)	86	92	-	dB
Interchannel Isolation		80	95	-	dB
Interchannel Gain Mismatch		-	0.2	0.5	dB
Output Voltage	(Note 3)	1.35	1.5	1.65	Vpp
Load Resistance		10	-	-	kΩ
Load Capacitance		-	-	30	pF
Power Supply Rejection	(Note 4)	-	50	-	dB
Power Supplies					
Power Supply Current					
AD+DA	PWADN= “H”, PWDAN= “H”	-	8	13	mA
AD	PWADN= “H”, PWDAN= “L”	-	4	-	mA
DA	PWADN= “L”, PWDAN= “H”	-	4.4	-	mA
Power down (Note 5)	PWADN= “L”, PWDAN= “L”	-	10	50	μA
Power Consumption					
AD+DA	PWADN= “H”, PWDAN= “H”	-	20	32.5	mW
AD	PWADN= “H”, PWDAN= “L”	-	10	-	mW
DA	PWADN= “L”, PWDAN= “H”	-	11	-	mW
Power down (Note 5)	PWADN= “L”, PWDAN= “L”	-	25	125	μW

Note 2. The offset of ADC is removed by internal HPF.
Note 3. Input/Output of ADC and DAC scales with VDD voltage. 0.6 x VDD(typ).
Note 4. PSR is applied to VDD with 1kHz, 50mV. No signal is input to AINL/R pins and “0” data is input to SDTI pin.
Note 5. In case of power-down mode, all digital input including clocks pins (MCLK, SCLK and LRCK) are held to VDD or VSS. PWADN and PWDAN pins are held to VSS.

FILTER CHARACTERISTICS

(Ta=25°C; VDD=1.6 ~ 3.6V; fs=44.1kHz; DEM1 pin = "L", DEM0 pin = "H")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 6)	±0.1dB	PB	0	-	17.4	kHz
	–1.0dB		-	20.0	-	kHz
	–3.0dB		-	21.1	-	kHz
Stopband		SB	25.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	65	-	-	dB
Group Delay (Note 7)		GD	-	17.0	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response (Note 6)	–3dB	FR	-	3.4	-	Hz
	–0.5dB		-	10	-	Hz
	–0.1dB		-	22	-	Hz
DAC Digital Filter:						
Passband (Note 6)	±0.05dB	PB	0	-	20.0	kHz
	–6.0dB		-	22.05	-	kHz
Stopband		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.02	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 7)		GD	-	19.0	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response	0 ~ 20.0kHz	FR	-	±0.5	-	dB

Note 6. The passband and stopband frequencies scale with fs (sampling frequency). For examples, PB=20.0kHz(@ADC: –1.0dB, DAC: –0.1dB) are 0.454 x fs.

Note 7. This is the calculated delay time caused by digital filtering. This time is measured from the input of analog signal to setting the 20 bit data of both channels on input register to the output register of ADC. This time also includes group delay of HPF. For DAC, this time is from setting the 20 bit data of both channels on input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=25°C; VDD=1.6 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	2.2V≤VDD≤3.6V	VIH	70%VDD	-	-	V
	1.6V≤VDD<2.2V	VIH	80%VDD	-	-	V
Low-Level Input Voltage	2.2V≤VDD≤3.6V	VIL	-	-	30%VDD	V
	1.6V≤VDD<2.2V	VIL	-	-	20%VDD	V
High-Level Output Voltage	(Iout= –20μA)	VOH	VDD–0.1	-	-	V
Low-Level Output Voltage	(Iout= 20μA)	VOL	-	-	0.1	V
Input Leakage Current		Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; VDD=1.6 ~ 3.6V; C_L=20pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency	256fs/384fs/512fs/768fs	fCLK	2.048	-	38.4	MHz
	1024fs	fCLK	2.048	-	25.6	MHz
Duty Cycle		dCLK	40	-	60	%
LRCK Timing						
Frequency		fs	8	44.1	50	kHz
Duty Cycle		Duty	45	-	55	%
Serial Interface Timing						
SCLK Period	(8kHz ≤ fs ≤ 33kHz)	tSCK	1/(96fs)	-	-	ns
	(33kHz < fs ≤ 50kHz)	tSCK	312.5	-	-	ns
SCLK Pulse Width Low		tSCKL	130	-	-	ns
Pulse Width High		tSCKH	130	-	-	ns
LRCK Edge to SCLK "↑"	(Note 8)	tLRS	50	-	-	ns
SCLK "↑" to LRCK Edge	(Note 8)	tSLR	50	-	-	ns
SCLK "↓" to SDTO		tDSS	-	-	80	ns
SDTI Hold Time		tSDH	50	-	-	ns
SDTI Setup Time		tSDS	50	-	-	ns
Reset Timing						
PWADN or PWDAN Pulse Width		tPW	150	-	-	ns
PWADN "↑" to SDTO Valid	(Note 9)	tPWV	-	2081	-	1/fs

Note 8. SCLK rising edge must not occur at the same time as LRCK edge.
Note 9. These cycles are the number of LRCK rising from PWADN rising.

■ Timing Diagram

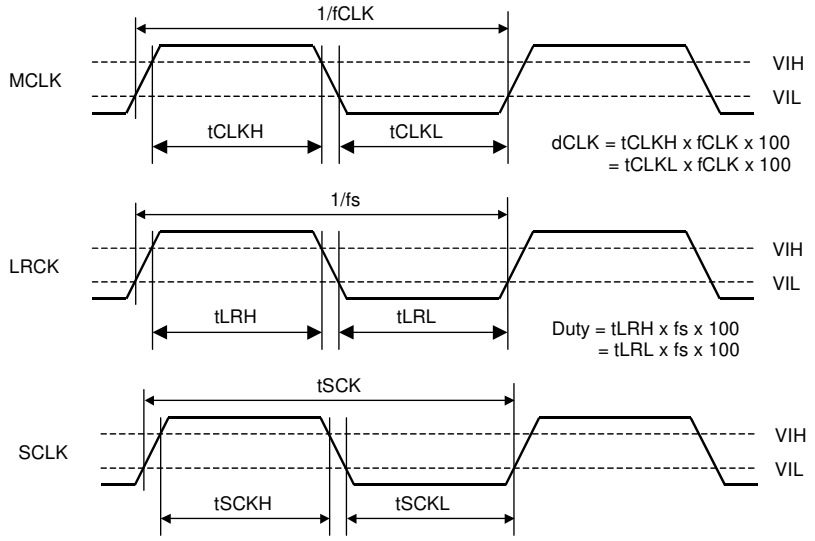


Figure 1. Clock Timing

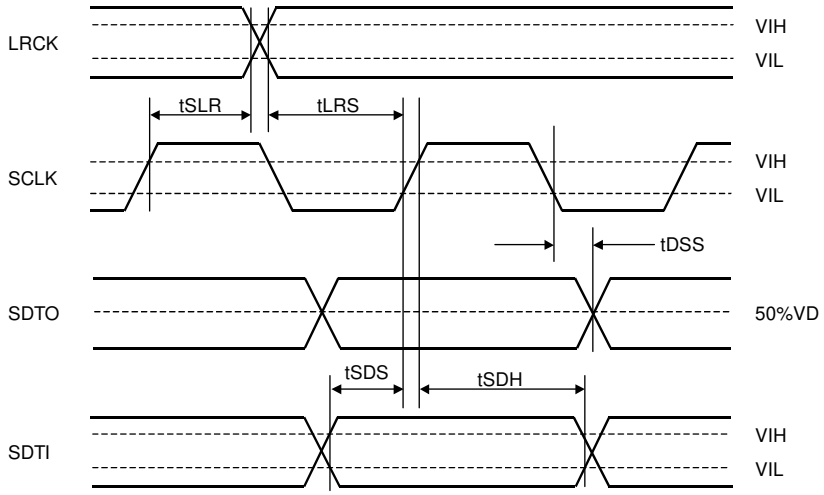


Figure 2. Serial Interface Timing

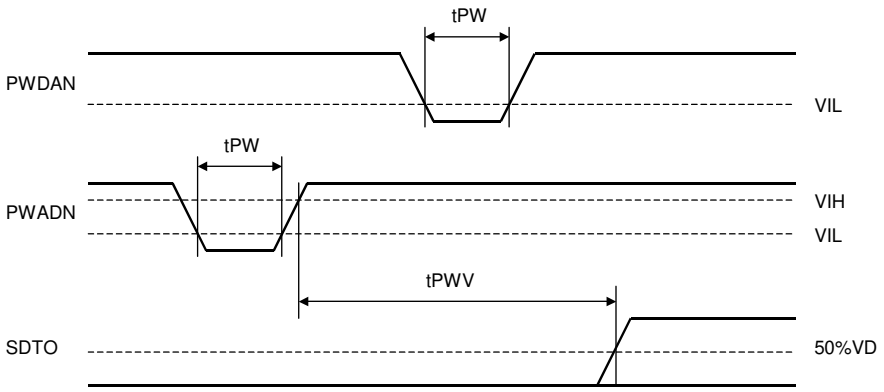


Figure 3. Reset & Initialize Timing

OPERATION OVERVIEW

■ System Clock Input

The AK4555 can be input MCLK=256fs, 384fs, 512fs, 768fs or 1024fs (fs is equal to or lower than 25kHz when MCLK is 1024fs). The input clock applied to the MCLK pin as internal master clock is divided into 256fs automatically. When MCLK is 1024fs, oversampling rate of D/A converter is automatically changed from 128fs to 256fs. The relationship between the external clock applied to the MCLK input and the desired sample rate is defined in Table 1. The LRCK clock input should be synchronized with MCLK. The phase between these clocks does not matter. *fs is sampling frequency.

When the synchronization is out of phase by changing the clock frequencies during normal operation, the AK4555 may occur click noise. In case of DAC, click noise is avoided by setting the inputs to "0".

All external clocks(MCLK, SCLK and LRCK) must be present unless PWADN=PWDAN= "L". If these clocks are not provided, the AK4555 may draw excess current and may not possibly operate properly because the device utilizes dynamic refreshed logic internally.

fs	MCLK					SCLK	
	256fs	384fs	512fs	768fs	1024fs	32fs	64fs
8.0kHz	2.0480MHz	3.0720MHz	4.0960MHz	6.1440MHz	8.1920MHz	0.2560MHz	0.512MHz
16.0kHz	4.0960MHz	6.1440MHz	8.1920MHz	12.2880MHz	16.3840MHz	0.5120MHz	1.024MHz
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	N/A	1.0240MHz	2.048MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	N/A	1.4112MHz	2.822MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	N/A	1.5360MHz	3.072MHz

Table 1. System Clock Example

For low sampling rates, outband noise causes S/N of DAC to degrade. S/N is improved by setting MCLK to 1024fs. Table 2 shows S/N of DAC output.

fs	MCLK	S/N(fs=8kHz, A-weighted)
8kHz ~ 50kHz	256fs/384fs/512fs/768fs	84dB
8kHz ~ 25kHz	1024fs	90dB

Table 2. Relationship among fs, MCLK frequency and S/N of DAC

■ Audio Serial Interface Format

Data is shifted in/out the SDTI/SDTO pins using SCLK and LRCK inputs. The data is MSB first, 2's compliment. The following formats are also valid when SCLK is 64fs: 16-bit data followed by four zeros and 18-bit data followed by two zeros.

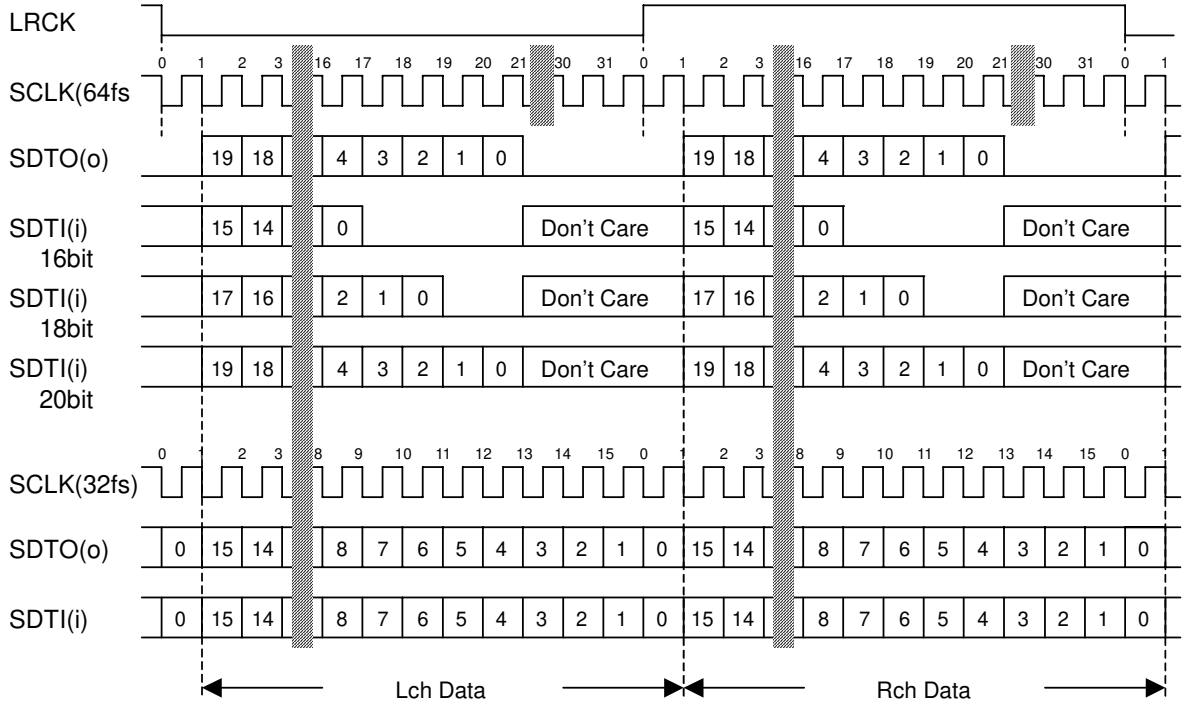


Figure 4. Audio Interface Timing

■ De-emphasis filter

The DAC of AK4555 includes the digital de-emphasis filter (tc=50/15μs) by IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter selected by DEM0 and DEM1 pins is enabled for input audio data. The de-emphasis is also disabled at DEM1 pin = "L" and DEM0 pin = "H".

DEM1 pin	DEM0 pin	Mode
L	L	44.1kHz
L	H	OFF
H	L	48kHz
H	H	32kHz

Table 3. De-emphasis filter control

■ Digital High Pass Filter

The AK4555 has a Digital High Pass Filter (HPF) for DC-offset cancel. The cut-off frequency of the HPF is 3.4Hz at fs=44.1kHz and the frequency response at 20Hz is –0.12dB. It also scales with the sampling frequency (fs).

■ Power-down & Reset

The ADC and DAC of AK4555 are placed in the power-down mode by bringing each power down pin, PWADN, PWDAN = "L" independently and each digital filter is also reset at the same time. These resets should always be done after power-up. In case of the ADC, an anlog initialization cycle starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 2081 cycles of LRCK clock. This initialization cycle does not affect the DAC operation. Figure 5 shows the power-up sequence when the ADC is powered up before the DAC power-up.

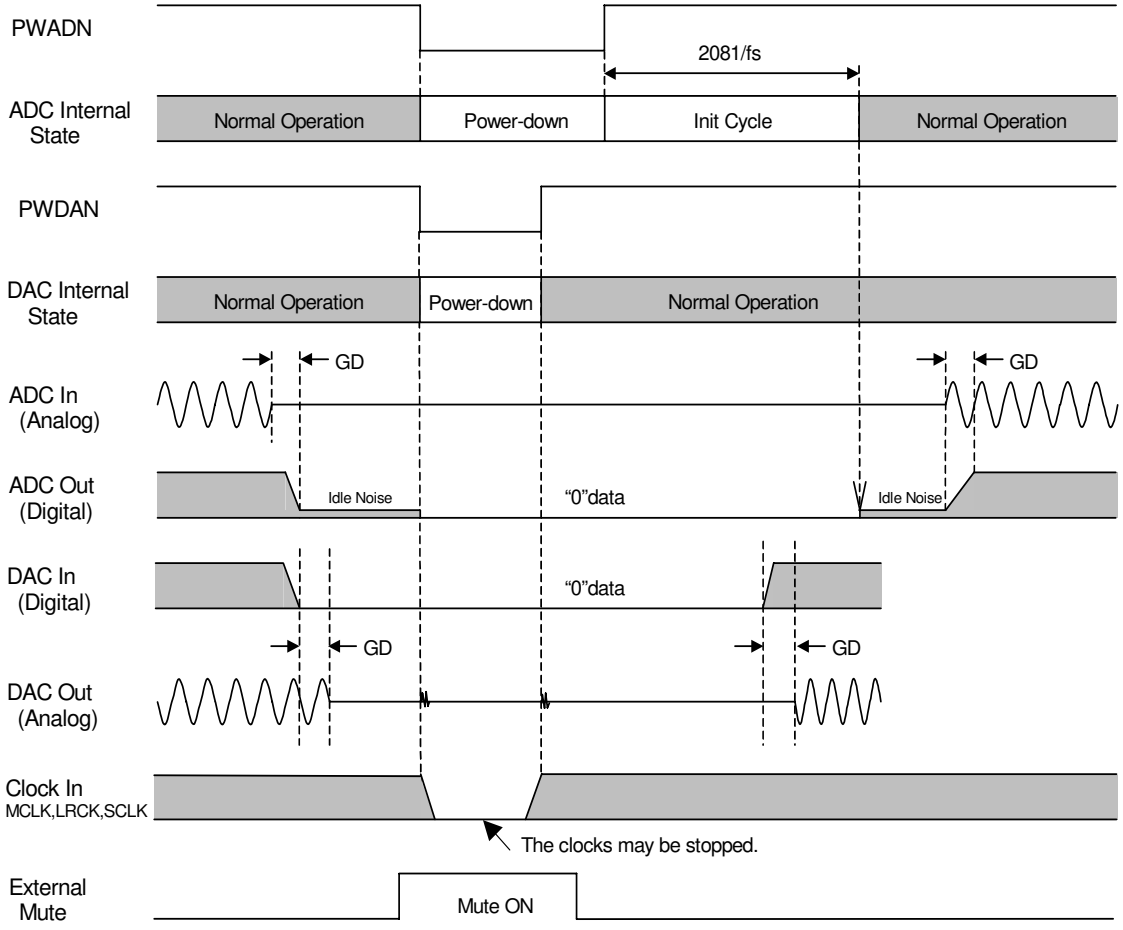


Figure 5. Power-up Sequence

SYSTEM DESIGN

Figure 6 shows the system connection diagram. An evaluation board[AKD4555] is available which demonstrates application circuit, optimum layout, power supply arrangements and measurement results.

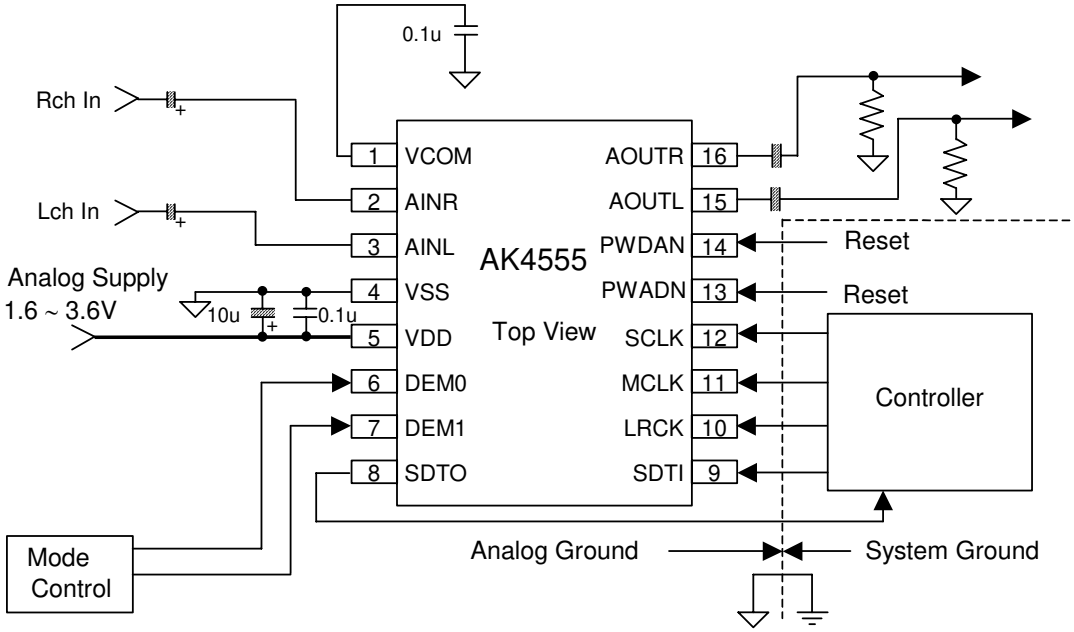


Figure 6. System Connection Diagram Example

Notes:

- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.

1. Grounding and Power Supply Decoupling

VDD and VSS are supplied from analog supply and should be separated from system digital supply. Decoupling capacitors should be as near to the AK4555 as possible, with the small value ceramic capacitor being nearest.

2. Voltage Reference

The input to VDD voltage sets the analog input/output range. A 0.1μF ceramic capacitor is connected to VDD and VSS pins, normally. VCOM is a signal ground of this chip. A 0.1μF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clock, should be kept away from the VDD and VCOM pins in order to avoid unwanted coupling into the AK4555.

3. Analog Inputs

ADC inputs are single-ended and internally biased to VCOM. The input signal range scales with the supply voltage and nominally 0.6xVDD Vpp(typ). The ADC output data format is 2's compliment.

The AK4555 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK4555 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range scales with the supply voltage and nominally 0.6xVDD Vpp(typ). The DAC input data format is 2's compliment. The output voltage is a positive full scale for 7FFFFH(@20bit) and a negative full scale for 80000H(@20bit). The ideal output is VCOM voltage for 00000H(@20bit). If the noise generated by the delta-sigma modulator beyond the audio band would be the problem, the attenuation by external filter is required.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

■ Layout Pattern Example

AK4555 requires careful attention to power supply and grounding arrangements to optimize performance.
(Please refer to AKD4555 Evaluation Board layout pattern.)

1. VDD pin should be supplied from analog power supply on system, and VSS pin should be connected to analog ground on system. The AK4555 is placed on the analog ground plane, and near the analog ground and digital ground split. And analog and digital ground planes should be only connected at one point. The connection point should be near to the AK4555.

2. VDD pin should be distributed from the point with low impedance of regulator etc.

3. The series resistors are prevent on the clock lines to reduce overshoot and undershoot. To avoid digital noise coupling to analog circuit in the AK4555, a 10pF ceramic capacitor on MCLK pin is connected with digital ground.

4. 0.1μF ceramic capacitors of VDD-VSS pins and VCOM-VSS pins should be located as close to the AK4555 as possible. And these lines should be the shortest connection to pins.

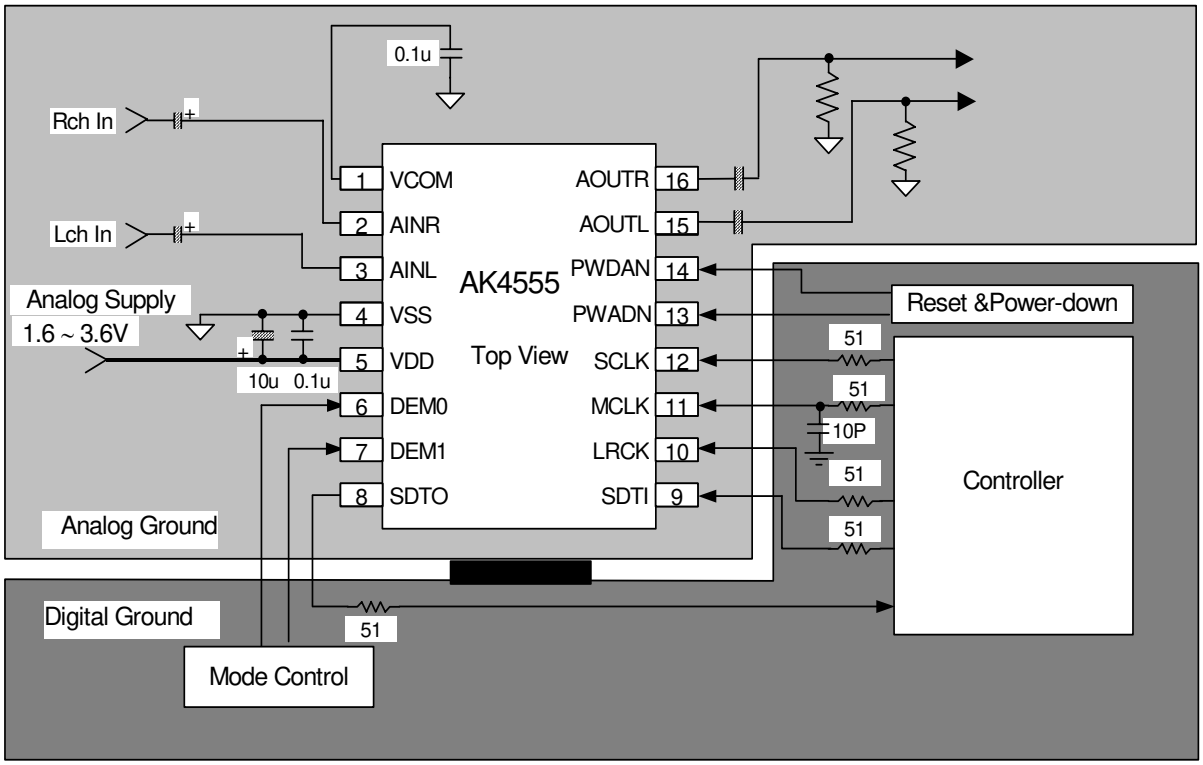
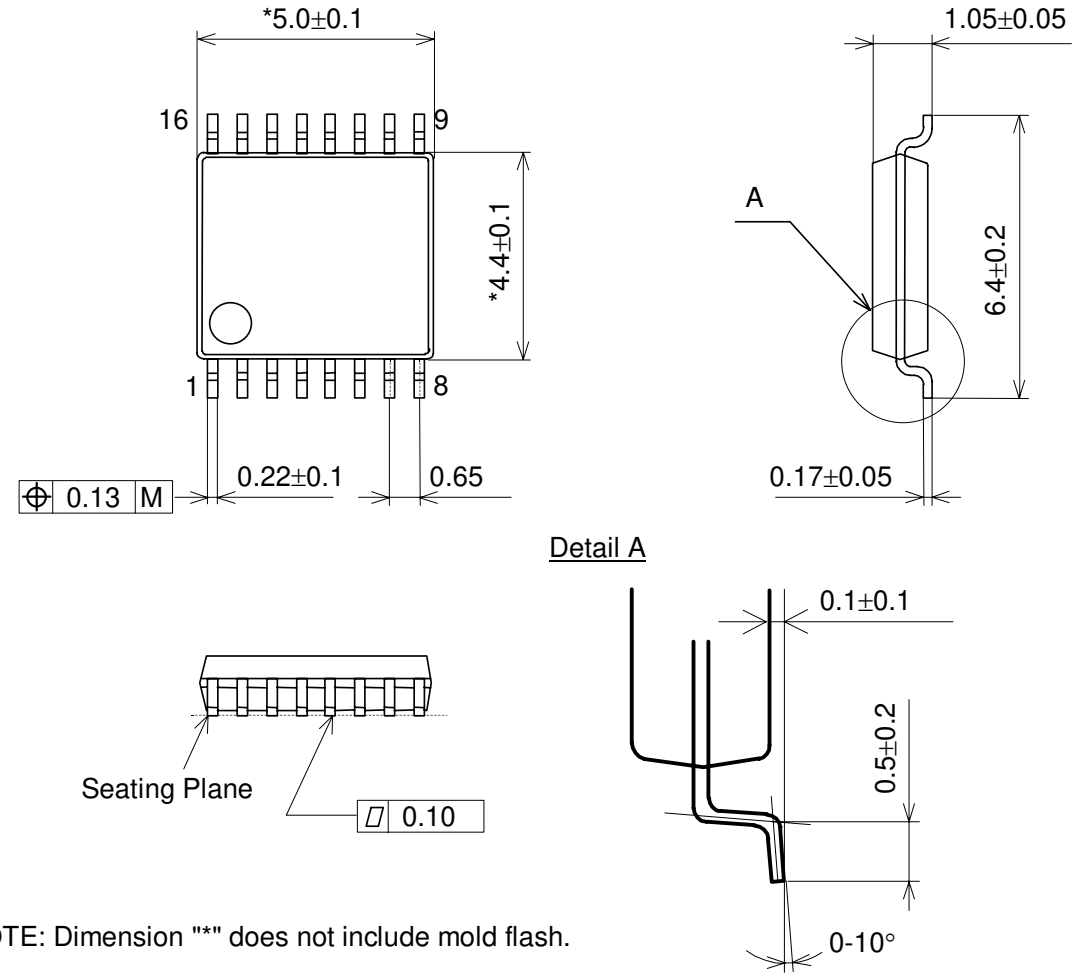


Figure 7. Layout Pattern Example

PACKAGE

16pin TSSOP (Unit: mm)

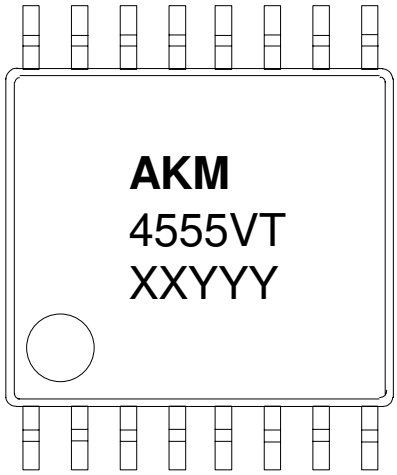


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: Lot#
   YYY: Date Code
3) Marketing Code : 4555VT
4) Asahi Kasei Logo

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
04/11/24	00	First Edition		
05/08/08	01	Spec Change	7	Switching Characteristics tSCK(min): 312.5ns → 1/(96fs) or 312.5ns

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