Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AK4558

108dB 216kHz 32Bit ΔΣ CODEC with PLL

1. General Description

The AK4558 is a low voltage 32bit 216kHz CODEC for high performance battery powered digital audio subsystems. An internal circuit includes newly developed 32-bit Digital Filter achieving short group delay and high quality sound. In addition, "OSR-Doubler" technology is newly adopted, making the AK4558 capable of supporting wide range signals and achieving low out-of-band noise while realizing low power consumption. The AK4558 is ideal for a wide range of applications that demands high sound quality including Electronic musical instruments and Audio Interfaces. The analog inputs and outputs are single-ended to minimize pin count and external filtering requirements. The AK4558 is housed in a very small 28-pin QFN. It is ideal for space-sensitive applications.

2. Features

- **Single-ended ADC**
  - **Dynamic Range, S/N: 108dB@AVDD=3.3V**
  - **S/(N+D): 92dB@AVDD=3.3V**
  - **Selectable HPF for DC-offset cancel (fc = 1Hz @ fs=48kHz)**
  - **4-types Digital Filter for High Sound Quality**
- **Single-ended DAC**
  - **Dynamic Range, S/N: 108dB@AVDD=3.3V**
  - **S/(N+D): 100dB@AVDD=3.3V**
  - **Digital de-emphasis for 32kHz, 44.1kHz and 48kHz sampling**
  - **5-types Digital Filter for High Sound Quality**
  - **Channel Independent Digital Attenuator (256 levels, 0.5dB steps)**
- **Audio I/F format: MSB First, 2's Complement**
  - **ADC: 24/32bit MSB justified , 24/32bit I^2S compatible or TDM**
  - **DAC: 24/32bit MSB justified, 16/20/24/32bit LSB justified, 24/32bit I^2S compatible or TDM**
- **Input/Output Voltage: ADC = 2.64Vpp @ AVDD=3.3V**
  DAC = 2.51Vpp @ AVDD=3.3V
- **Master/Slave mode**
- **μP I/F: I^2C Bus**
- **Sampling Rate:**

(1) PLL Mode

- **PLL Slave Mode (LRCK pin): fs = 8kHz ~ 216kHz**
- **PLL Slave Mode (BICK pin): fs = 8kHz ~ 216kHz**
- **PLL Master Mode: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 54kHz, 88.2kHz, 96kHz, 128kHz, 176.4kHz, 192kHz**

(2) External Clock Mode

- **Normal Speed: 8kHz to 54kHz (256fs or 512fs)**
  8kHz to 48kHz (384fs or 768fs)
- **Double Speed: 54kHz to 108kHz (256fs)**
  48kHz to 96kHz (384fs)
- **Quad Speed: 108kHz to 216kHz (128fs)**
  96kHz to 192kHz (192fs)

☐ Master Clock:
(1) PLL Mode
• MCKI pin: 27MHz, 26MHz, 24MHz, 19.2MHz, 13.5MHz, 13MHz, 12.288MHz, 12MHz, 11.2896MHz
• LRCK pin: 1fs
• BICK pin: 32fs, 64fs, 128fs(TDM), 256fs(TDM)
(2) External Clock Mode (MCKI pin)
• Slave mode: 256fs, 384fs, 512fs or 768fs (Normal Speed)
256fs or 384fs (Double Speed)
128fs or 192fs (Quad Speed)
• Master mode: 256fs or 512fs (Normal Speed)
256fs (Double Speed)
128fs (Quad Speed)
☐ Power Supply:
• AVDD = 2.4 to 3.6V (typ. 3.3V)
• TVDD = 1.7 to 3.6V (typ. 1.8V)
☐ Power Supply Current: 18mA(fs=48kHz)
☐ Ta = -40 to 105°C
☐ Package: 28-pin QFN (0.5mm pitch)

3. Table of Contents

4. Block Diagram and Functions

■ Block Diagram

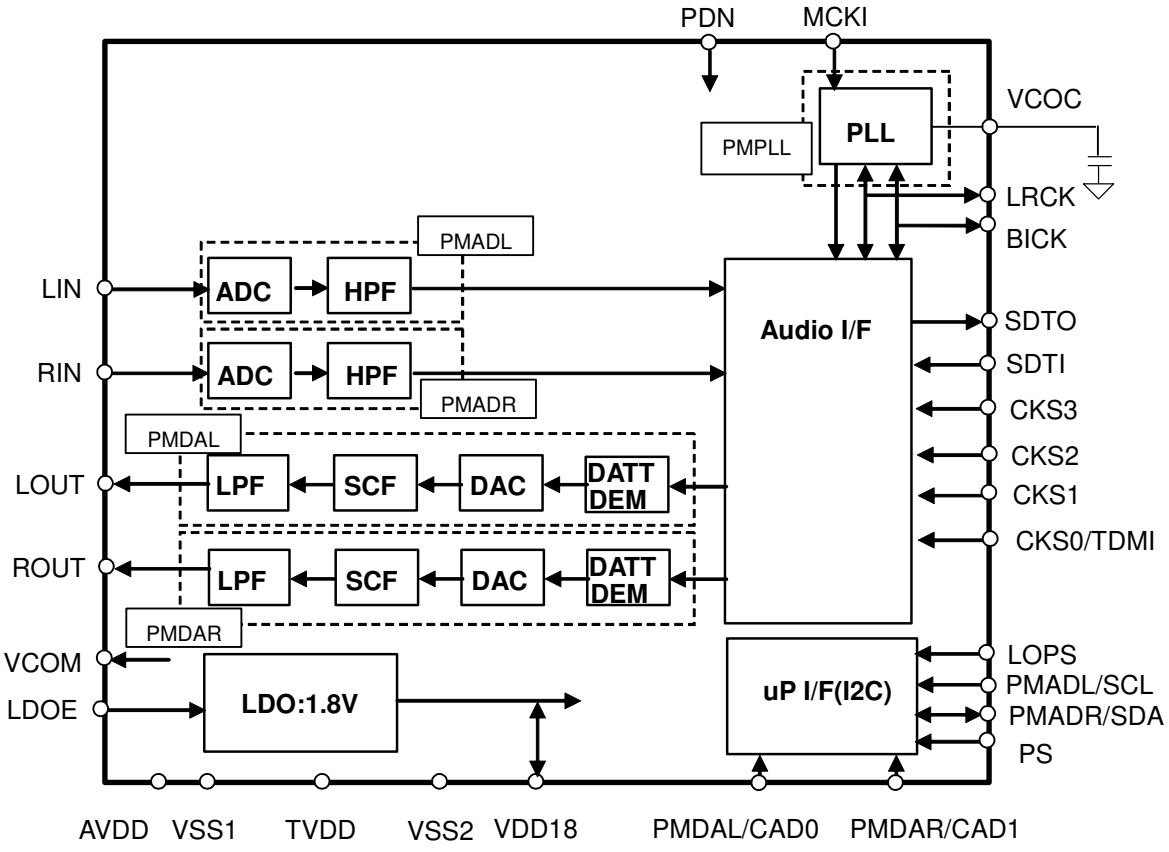


Figure 1. Block Diagram

■ Compatibility with the AK4556

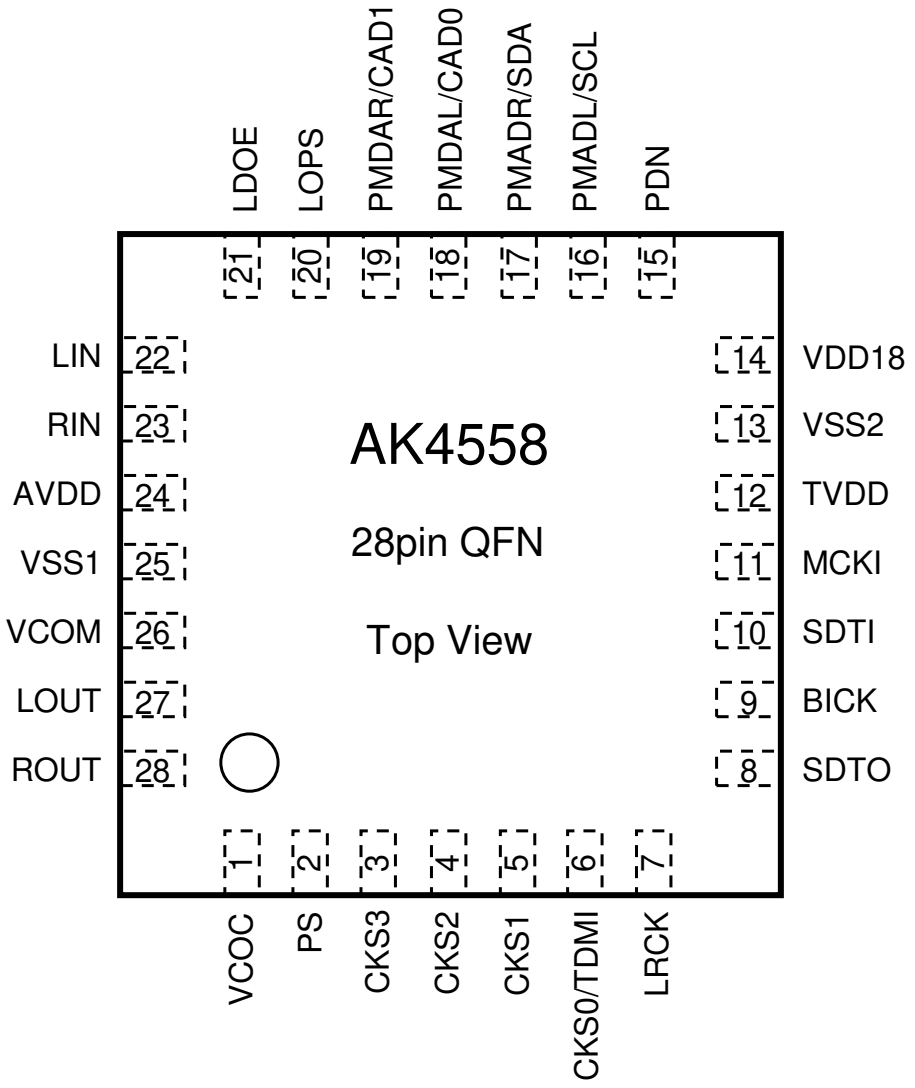
Function		AK4556	AK4558
fs (max)		216kHz	216kHz
HFP Cut-off		1Hz @ fs = 48kHz	1Hz @ fs = 48kHz
HPF Disable		Yes	Yes
ADC			
Input Level		0.7 x VA	0.8 x AVDD
Input Resistance		8kΩ@ fs = 48kHz, 96kHz, 192kHz	8kΩ@ fs = 48kHz, 96kHz, 192kHz
Init Cycle		4134/fs @ Normal Speed, Slave mode	5200/fs @ Normal Speed, Slave mode
S/(N+D)		91dB	92dB
DR, S/N		103dB	108dB
DF	SA	68dB	85dB
	SB	28kHz	27.8kHz
	GD	18/fs	5/fs
DAC			
Output Level		0.7 x VA	0.76 x AVDD
Load Resistance		5kΩ	5kΩ
S/(N+D)		90dB	100dB
DR, S/N		106dB	108dB
DF	SA	54dB	80dB
	GD	21/fs	6.8/fs
MCKI (Slave)		256/384/512/768fs @ Normal Speed	256/384/512/768fs @ Normal Speed
		256/384fs @ Double Speed	256/384fs @ Double Speed
		128/192fs @ Quad Speed	128/192fs @ Quad Speed
Audio I/F	ADC	24bit MSB justified / I^2S	24/32bit MSB justified 24/32bit I^2S/TDM
	DAC	24bit MSB justified /24bit LSB justified / I^2S	24/32bit MSB justified 16/20/24/32bit LSB justified 24/32bit I^2S/TDM
Volume		No	0.5dB/step
Digital Filter Option		No	Yes
PLL		No	Yes
M/S mode		Master / Slave	Master / Slave
Parallel/Serial mode		No	Yes
Pop Guard		No	Yes
Idd		27.5mA (Vdd = 3V)	18.0mA (AVDD = 3.3V,TVDD=1.8V)
AVDD		2.4V to 3.6V	2.4V to 3.6V
VDD18		2.4V to 3.6V (Normal/Double Speed) 2.7V to 3.6V (Quad Speed)	1.7V to 1.98V
TVDD		-	1.7V to 3.6V
Package		20TSSOP (6.5mm x 6.4mm, 0.65mm Pitch)	28QFN (5.0mm x 5.0mm, 0.5mm Pitch)

5. Pin Configurations and Functions

■ Ordering Guide

AK4558EN	-40 ~ +105°C	28-pin QFN (0.5mm pitch)
AKD4558	Evaluation Board for the AK4558	

■ Pin Layout



Note 1. The exposed pad on the bottom surface of the package must be connected to VSS.

■ Pin Functions

No.	Pin Name	I/O	PD State	Function
1	VCOC	O	Hi-z	(PS pin = "H") This pin should be connected to VSS. (PS pin = "L") Output Pin for Loop Filter of PLL Circuit This pin should be connected to VSS, unless PLL Mode 15 used.
2	PS	I	Hi-z	Parallel/Serial Mode Select Pin "L": Serial Mode, "H": Parallel Mode Do not change this pin during PDN pin = "H".
3	CKS3	I	Hi-z	Mode Setting Pin #3
4	CKS2	I	Hi-z	Mode Setting Pin #2
5	CKS1	I	Hi-z	Mode Setting Pin #1
6	CKS0	I	Hi-z	(PS pin = "H") Mode Setting Pin #0
	TDMI	I	Hi-z	(PS pin = "L") TDM Data Input Pin
7	LRCK	I/O	Hi-Z /L	Input/Output Channel Clock Pin When PDN pin is "L", LRCK pin outputs "L" in master mode. LRCK pin outputs "Hi-Z" in slave mode.
8	SDTO	O	L	Audio Serial Data Output Pin When PDN pin is "L", SDTO pin outputs "L".
9	BICK	I/O	Hi-Z /L	Audio Serial Data Clock Pin When PDN pin is "L", BICK pin outputs "L" in master mode. BICK pin outputs "Hi-Z" in slave mode.
10	SDTI	I	Hi-z	Audio Serial Data Input Pin
11	MCKI	I	Hi-z	External Master Clock Input Pin
12	TVDD	-	-	LDO Power Supply/Digital I/F Power Supply Pin
13	VSS2	-	-	Digital Ground Pin
14	VDD18	O	Pulldown (500ohm)	(LDOE pin = "H") LDO Output Pin This pin must be connected to VSS2 pin with 1μF ± 50% capacitor in series.
		I	Hi-z	(LDOE pin = "L") 1.8V Power Input Pin
15	PDN	I	Hi-z	Power-Down & Reset Mode Pin "L": Power-down and Reset, "H": Normal operation The AK4558 should be reset once by bringing PDN pin = "L".
16	PMADL	I	Hi-z	(PS pin = "H") ADC Lch Power Management Pin
	SCL	I	Hi-z	(PS pin = "L") Control Data Clock Pin
17	PMADR	I	Hi-z	(PS pin = "H") ADC Rch Power Management Pin
	SDA	I/O	Hi-z	(PS pin = "L") Control Data Input/Output Pin
18	PMDAL	I	Hi-z	(PS pin = "H") DAC Lch Power Management Pin
	CAD0	I	Hi-z	(PS pin = "L") Chip Address 0 Pin
19	PMDAR	I	Hi-z	(PS pin = "H") DAC Rch Power Management Pin
	CAD1	I	Hi-z	(PS pin = "L") Chip Address 1 Pin
20	LOPS	I	Hi-z	(PS pin = "H") DAC Output Power Save Mode Control Pin (PS pin = "L") This pin must be connected to VSS2.
21	LDOE	I	Hi-z	LDO Enable Pin "L": LDO Disable, "H": LDO Enable
22	LIN	I	Hi-z	Lch Analog Input Pin
23	RIN	I	Hi-z	Rch Analog Input Pin
24	AVDD	-	-	Analog Power Supply Pin

25	VSS1	-	-	Analog Ground Pin
26	VCOM	O	Pulldown (400ohm)	Common Voltage Output Pin, 0.5 x AVDD This pin must be connected to VSS1 pin with 1μF±50% capacitor in series.
27	LOUT	O	Pulldown (100kohm)	Lch Analog Output Pin
28	ROUT	O	Pulldown (100kohm)	Rch Analog Output Pin

Note 2. All input pins except analog input pins (LIN and RIN) must not be allowed to float.

■ Handling of Unused Pins

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	LOUT, ROUT, LIN, RIN	Open
Digital	MCKI, SDTI, CKS0/TDMI, CKS1, LOPS	Connect to VSS2
	SDTO	Open

6. Absolute Maximum Ratings

(VSS1=VSS2=0V; Note 3)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital core	VDD18	-0.3	2.5	V
	Digital I/O	TVDD	-0.3	6.0	V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
Analog Input Voltage (LIN, RIN pin)		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage (Note 4)		VIND	-0.3	TVDD+0.3	V
Ambient Temperature (power applied) (Note 5)		Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 3. All voltages with respect to ground. VSS1 and VSS2 must be connected to analog ground.

Note 4. PMDAL/CAD0, PMDAR/CAD1, LOPS, CKS0/TDMI, CKS3, CKS2, CKS1, PMADL/SCL, PMADR/SDA, SDTI, LRCK, BICK, MCKI, SDA, PS, LDOE and PDN pins. The external pull-up resistors at the SDA and SCL pins should be connected to (TVDD+0.3) voltage or less.

Note 5. In case that PCB drawing density is more than 100%. The exposed pad on the bottom surface of the package must be connected to VSS.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1=VSS2=0V; Note 3)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 6)	Analog	AVDD	2.4	3.3	3.6	V
	Digital (LDOE pin="L")	TVDD	VDD18	1.8	3.6	V
	Digital Core(LDOE pin="L")	VDD18	1.7	1.8	1.98	V
	Digital (LDOE pin="H")	TVDD	2.4	3.3	3.6	

Note 3. All voltages with respect to ground. VSS1 and VSS2 must be connected to analog ground.

Note 6. When the LDOE pin = "L" VDD18 must be powered up either at the same time or after TVDD is powered up. Internal LDO generates 1.8V, when the LDOE pin ="H". The power-up sequence with AVDD and TVDD is not critical. The PDN pin should be held "L" prior to when power is applied. The PDN pin is allowed to be "H" after all power supplies are applied and settled. All power pins of the AK4558 must be supplied. Do not turn any power supply off independently (neither grounded nor floating). When using the AK4558 with I²C bus, the power supply of the AK4558 must not be turned off unless the power supplies of the surrounding device are turned off.

*AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Analog Characteristics

(Ta=25°C; AVDD= TVDD=3.3V; VSS1=VSS2=0V; EXT Slave Mode; fs=48kHz, 96kHz, 192kHz; Signal Frequency=1kHz; BICK=64fs; Data=32bit, Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 20Hz ~ 40kHz at fs=96kHz, 20Hz ~ 40kHz at fs=192kHz; unless otherwise specified)

Parameter			Min.	Typ.	Max.	Unit
ADC Analog Input Characteristics:						
Resolution			-	-	32	bit
Input Voltage		(Note 7)	2.38	2.64	2.90	Vpp
S/(N+D)	fs=48kHz	−1dBFS	82	92	-	dB
	BW=20kHz	−60dBFS	-	43	-	dB
	fs=96kHz	−1dBFS	81	91	-	dB
	BW=40kHz	−60dBFS	-	40	-	dB
	fs=192kHz	−1dBFS	-	91	-	dB
	BW=40kHz	−60dBFS	-	40	-	dB
DR	(−60dBFS with A-weighted)		100	108	-	dB
S/N	(A-weighted)		100	108	-	dB
Input Resistance			7	10	-	kΩ
Interchannel Isolation			90	110	-	dB
Interchannel Gain Mismatch			-	0	0.5	dB
Gain Drift			-	100	-	ppm/°C
Power Supply Rejection		(Note 11)	-	50	-	dB
DAC Analog Output Characteristics:						
Resolution			-	-	32	bit
Output Voltage		(Note 8)	2.26	2.51	2.76	Vpp
S/(N+D)	fs=48kHz	0dBFS	90	100	-	dB
	BW=20kHz	−60dBFS	-	45	-	dB
	fs=96kHz	0dBFS	88	98	-	dB
	BW=40kHz	−60dBFS	-	42	-	dB
	fs=192kHz	0dBFS	-	98	-	dB
	BW=40kHz	−60dBFS	-	42	-	dB
DR	(−60dBFS with A-weighted)		100	108	-	dB
S/N	(A-weighted)		100	108	-	dB
Load Capacitance		(Note 9)	-	-	30	pF
Load Resistance		(Note 10)	5	-	-	kΩ
Interchannel Isolation			90	107	-	dB
Interchannel Gain Mismatch			-	0	0.5	dB
Gain Drift			-	100	-	ppm/°C
Power Supply Rejection		(Note 11)	-	50	-	dB

Note 7. This value is the full scale (0dB) of the input voltage. Input voltage is proportional to AVDD voltage. Vin = 0.8 x AVDD (Vpp).

Note 8. This value is the full scale (0dB) of the output voltage. Output voltage is proportional to AVDD voltage. Vout = 0.76 x AVDD (Vpp).

Note 9. When LOUT/ROUT drives some capacitive load, a 220Ω resistor should be added in series between LOUT/ROUT and capacitive load. In this case, LOUT/ROUT pins can drive a capacitor of 400pF.

Note 10. For AC-load

Note 11. VCOM pin is connected to VSS1 pin with 1μF±50% capacitor in series.
When LDOE pin = "L", PSR is applied to AVDD, VDD18 and TVDD with 1kHz, 50mVpp.
When LDOE pin = "H", PSR is applied to AVDD and TVDD with 1kHz, 50mVpp.

Ta=25℃; AVDD=3.3V, TVDD=VDD18=1.8V;
Slave Mode, MCKI=24.576MHz, ADC Single Input / DAC Single Output (LDOE pin= “L”)
Register Setting: TDM1-0 bits = “00”, DIF2-0 bits = “111”, CKS1-0 bits = “10”, DFS1-0 bits = “00”
Output Pin Load: DAC Single-end＝4.7kohm, 33pF, LRCK=BICK=SDTO pins=22pF

Parameter		Min.	Typ.	Max.	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = “H”)					
AVDD	fs=48kHz, 96kHz, 192kHz		12.0	16.0	mA
TVDD+VDD18	fs=48kHz		6.0	9.0	mA
	fs=96kHz		10.0	15.0	mA
	fs=192kHz		10.0	15.0	mA
Power-down mode					
(PDN pin = “L”) (Note 12)			1	100	μA
AVDD+ TVDD+VDD18					

Note 12. Powered-down. All digital input pins are held VSS2.

9. ADC Filter Characteristics (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.7~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF): SHARP ROLL-OFF (SLAD bit="0" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.06dB –6.0dB	PB	0 -	- 24.4	22.1 -	kHz kHz
Stopband (Note 13)		SB	27.8	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	19	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (SLAD bit="0" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.06dB –6.0dB	PB	0 -	- 24.4	22.1 -	kHz kHz
Stopband (Note 13)		SB	27.8		-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	2.6	1/fs
Group Delay (Note 14)		GD	-	5.0	-	1/fs
ADC Digital Filter (Decimation LPF): SLOW ROLL-OFF (SLAD bit="1" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.074dB –6.0dB	PB	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 13)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	7.0	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (SLAD bit="1" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.074dB –6.0dB	PB -	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 13)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 14)		GD	-	5.0	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response	–3.0dB –0.5dB	FR	- -	1.0 2.5	- -	Hz Hz
(Note 13)	–0.1dB		-	6.5	-	Hz

Note 13. The passband and stopband frequencies scales with fs (sampling frequency).
For example, PB(0dB/-0.06dB) = 0.46 x fs (@fs=48kHz) for ADC block(SHARP ROLL-OFF).
For example, PB(0dB/-0.074dB) = 0.26 x fs (@fs=48kHz) for ADC block(SLOW ROLL-OFF).

Note 14. The calculated delay time by digital filtering. This is the time from the input of an analog signal to the output of MSB for L channel of SDTO. The error of the delay at audio interface is within +1[1/fs].

10. ADC Filter Characteristics (fs=96kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.7~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF): SHARP ROLL-OFF (SLAD bit="0" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.06dB –6.0dB	PB	0	- 48.7	44.2	kHz kHz
Stopband (Note 13)		SB	55.6	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	19	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (SLAD bit="0" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.06dB –6.0dB	PB	0 -	- 48.7	44.2 -	kHz kHz
Stopband (Note 13)		SB	55.6		-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	2.6	1/fs
Group Delay (Note 14)		GD	-	5.0	-	1/fs
ADC Digital Filter (Decimation LPF): SLOW ROLL-OFF (SLAD bit="1" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.074dB –6.0dB	PB	0 -	- 43.7	25	kHz kHz
Stopband (Note 13)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	7.0	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF FILTER (SLAD bit="1" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.074dB –6.0dB	PB	0 -	- 43.7	25 -	kHz kHz
Stopband (Note 13)		SB	73	-	-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 14)		GD	-	5.0	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response	–3.0dB	FR	- -	2.0 5.0	- -	Hz Hz
(Note 13)	–0.1dB		-	13	-	Hz

Note 13. The passband and stopband frequencies scales with fs (sampling frequency).
For example, PB(0dB/-0.06dB) = 0.46 x fs (@fs=96kHz) for ADC block(SHARP ROLL-OFF).
For example, PB(0dB/-0.074dB) = 0.26 x fs (@fs=96kHz) for ADC block(SLOW ROLL-OFF).

Note 14. The calculated delay time by digital filtering. This is the time from the input of an analog signal to the output of MSB for L channel of SDTO. The error of the delay at audio interface is within +1[1/fs].

11. ADC Filter Characteristics (fs=192kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.6~ 1.98V, 2.4~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF): SHARP ROLL-OFF (SLAD bit="0" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.04dB –6.0dB	PB	0	- 100.1	83.7	kHz kHz
Stopband (Note 13)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	15	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (SLAD bit="0" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.04dB –6.0dB	PB	0 -	- 100.1	83.7 -	kHz kHz
Stopband (Note 13)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	0.3	1/fs
Group Delay (Note 14)		GD	-	6.0	-	1/fs
ADC Digital Filter (Decimation LPF): SLOW ROLL-OFF (SLAD bit="1" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.1dB –6.0dB	PB	0 -	- 75.2	31.1 -	kHz kHz
Stopband (Note 13)		SB	145.9	-		kHz
Stopband Attenuation		SA	85	-		dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	8.0	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF FILTER (SLAD bit="1" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.1dB –6.0dB	PB	0 -	- 75.2	31.1 -	kHz kHz
Stopband (Note 13)		SB	145.9	-		kHz
Stopband Attenuation		SA	85	-		dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	0.6	1/fs
Group Delay (Note 14)		GD	-	6.0	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response	–3.0dB	FR	- -	4.0 10.0	- -	Hz Hz
(Note 13)	–0.1dB		-	26.0	-	Hz

Note 13. The passband and stopband frequencies scales with fs (sampling frequency).
For example, PB(0dB/-0.04dB) = 0.436 x fs (@fs=192kHz) for ADC block(SHARP ROLL-OFF).
For example, PB(0dB/-0.1dB) = 0.16 x fs (@fs=192kHz) for ADC block(SLOW ROLL-OFF).

Note 14. The calculated delay time by digital filtering. This is the time from the input of an analog signal to the output of MSB for L channel of SDTO. The error of the delay at audio interface is within +1[1/fs].

12. DAC Filter Characteristics (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.7~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode(DEM=OFF; SLDA bit="0"; SDDA bit="0")						
Passband (Note 15)	±0.05dB −6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple		PR	-0.0032		0.0032	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	27.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 18)		FR	-0.3	-	0.2	dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SLDA bit="0" ; SDDA bit="1")						
Passband (Note 15)	±0.05dB −6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple		PR	-0.0031		0.0031	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	6.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 18)		FR	-0.4		0.3	dB
DAC Digital Filter (LPF): Slow roll-off mode(DEM=OFF; SLDA bit="1" ; SDDA bit="0")						
Passband (Note 16)	±0.07dB −3.0dB	PB	0 -	 19.7	8.8 -	kHz kHz
Stopband		SB	42.6			kHz
Passband Ripple		PR	-0.043		0.043	dB
Stopband Attenuation		SA	73			dB
Group Delay (Note 17)		GD	-	7.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 18)		FR	-5	-	0.1	dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode(DEM=OFF; SLDA bit="1" ; SDDA bit="1")						
Passband (Note 16)	±0.07dB −3.0dB	PB	0 -	- 24.3	12.1 -	kHz kHz
Stopband		SB	41.5	-	-	kHz
Passband Ripple		PR	-0.05		0.05	dB
Stopband Attenuation		SA	82	-	-	dB
Group Delay (Note 17)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 18)		FR	-5		0.1	dB

Note 15. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.454 x fs (@ fs=48kHz).

Note 16. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.204 x fs (@ fs=48kHz).

Note 17. The calculated delay time is resulting from digital filtering. For the DAC, this is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1[1/fs].

Note 18. The reference frequency is 1kHz.

13. DAC Filter Characteristics (fs=96kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.7~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode(DEM=OFF; SLDA bit="0" ; SDDA bit="0")						
Passband (Note 15)	±0.05dB	PB	0	-	43.5	kHz
	–6.0dB		-	48.0	-	kHz
Stopband		SB	52.5	-	-	kHz
Passband Ripple		PR	-0.0032		+0.0032	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	27.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 18)		FR	-0.4	-	0.3	dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SLDA bit="0" ; SDDA bit="1")						
Passband (Note 15)	±0.05dB	PB	0	-	43.5	kHz
	–6.0dB		-	48.0	-	kHz
Stopband		SB	52.5	-	-	kHz
Passband Ripple		PR	-0.0031		+0.0031	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	6.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 18)		FR	-0.4	-	0.3	dB
DAC Digital Filter (LPF): Slow roll-off mode (DEM=OFF; SLDA bit="1" ; SDDA bit="0")						
Passband (Note 16)	±0.07dB	PB	0		17.7	kHz
	–3.0dB		-	39.6	-	kHz
Stopband		SB	85.3			kHz
Passband Ripple		PR	-0.043		+0.043	dB
Stopband Attenuation		SA	73			dB
Group Delay (Note 17)		GD	-	7.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 18)		FR	-4	-	0.1	dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode(DEM=OFF; SLDA bit="1" ; SDDA bit="1")						
Passband (Note 16)	±0.07dB	PB	0	-	24.2	kHz
	–3.0dB		-	44.6	-	kHz
Stopband		SB	83.0	-	-	kHz
Passband Ripple		PR	-0.05		+0.05	dB
Stopband Attenuation		SA	82	-	-	dB
Group Delay (Note 17)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 18)		FR	-5	-	0.1	dB

Note 15. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.454 x fs (@ fs=96kHz).

Note 16. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.204 x fs (@ fs=96kHz).

Note 17. The calculated delay time is resulting from digital filtering. For the DAC, this is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1[1/fs].

Note 18. The reference frequency is 1kHz.

14. DAC Filter Characteristics (fs=192kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.7~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode(DEM=OFF; SLDA bit="0" ; SDDA bit="0")						
Passband (Note 15)	±0.05dB	PB	0	-	87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband		SB	105	-	-	kHz
Passband Ripple		PR	-0.0032		+0.0032	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	27.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 18)		FR	-1.0	-	1.0	dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SLDA bit="0" ; SDDA bit="1")						
Passband (Note 15)	±0.05dB	PB	0	-	87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband		SB	105	-	-	kHz
Passband Ripple		PR	-0.0031		+0.0031	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	6.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 18)		FR	-1.0	-	1.0	dB
DAC Digital Filter (LPF): Slow roll-off mode (DEM=OFF; SLDA bit="1" ; SDDA bit="0")						
Passband (Note 16)	±0.07dB	PB	0		35.5	kHz
	−3.0dB		-	79.1	-	kHz
Stopband		SB	171			kHz
Passband Ripple		PR	-0.043		+0.043	dB
Stopband Attenuation		SA	73			dB
Group Delay (Note 17)		GD	-	7.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 18)		FR	-5.0	-	0.1	dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode (DEM=OFF; SLDA bit="1" ; SDDA bit="1")						
Passband (Note 16)	±0.07dB	PB	0	-	48.4	kHz
	−3.0dB		-	89.2	-	kHz
Stopband		SB	165.9	-	-	kHz
Passband Ripple		PR	-0.05		+0.05	dB
Stopband Attenuation		SA	82	-	-	dB
Group Delay (Note 17)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 18)		FR	-5.0	-	0.1	dB

Note 15. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.454 x fs (@ fs=192kHz).

Note 16. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.204 x fs (@ fs=192kHz).

Note 17. The calculated delay time is resulting from digital filtering. For the DAC, this is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1[1/fs].

Note 18. The reference frequency is 1kHz.

15. DC Characteristics

(Ta= -40 ~ +105°C; AVDD=2.4~3.6V, TVDD=1.7~ 3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
TVDD ≤ 3.0V					
High-Level Input Voltage (CKS3, CKS2, CKS1, CKS0/TDMI, SDTI, LRCK, BICK, MCKI, PMADL/SCL, PMADR/SDA, PMDAL/CAD0, PMDAR/CAD1, PS, LDOE and PDN pins)	VIH	80%TVDD	-	-	V
Low-Level Input Voltage (CKS3, CKS2, CKS1, CKS0/TDMI, SDTI, LRCK, BICK, MCKI, PMADL/SCL, PMADR/SDA, PMDAL/CAD0, PMDAR/CAD1, PS, LDOE and PDN pins)	VIL	-	-	20%TVDD	V
TVDD > 3.0V					
High-Level Input Voltage (CKS3, CKS2, CKS1, CKS0/TDMI, SDTI, LRCK, BICK, MCKI, PMADL/SCL, PMADR/SDA, PMDAL/CAD0, PMDAR/CAD1, PS, LDOE and PDN pins)	VIH	70%TVDD	-	-	V
Low-Level Input Voltage (CKS3, CKS2, CKS1, CKS0/TDMI, SDTI, LRCK, BICK, MCKI, PMADL/SCL, PMADR/SDA, PMDAL/CAD0, PMDAR/CAD1, PS, LDOE and PDN pins)	VIL	-	-	30%TVDD	V
High-Level Output Voltage (SDTO,LRCK,BICK pins: Iout=-100μA)	VOH	TVDD-0.5	-	-	V
Low-Level Output Voltage (SDTO, LRCK, BICK pins: Iout= 100μA)	VOL	-	-	0.5	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V Iout= 3mA)	VOL	-	-	0.4	V
(SDA pin, 1.7V ≤ TVDD < 2.0V Iout= 3mA)	VOL	-	-	20%TVDD	V
Input Leakage Current	Iin	-	-	±10	μA

16. Switching Characteristics

(Ta= -40 ~ +105°C; AVDD= 2.4 ~ 3.6V; TVDD=1.7 ~ 3.6V; C_L=20pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing						
Frequency		fsn, fsd, fsq	-	Table 19	-	kHz
Stereo Mode: Duty Cycle		Duty	-	50	-	%
TDM128 Mode: (Note 19)						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(8fsn) 1/(8fsd)	-	s
MSB or LSB justified: Pulse Width High		tLRCKH	-	1/(8fsn) 1/(8fsd)	-	s
TDM256 Mode: (Note 19)						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(4fsq)	-	s
MSB or LSB justified: Pulse Width High		tLRCKH	-	1/(4fsq)	-	s
BICK Output Timing (Table 21)						
Period	BCKO1-0 bits = "00"	tBCK	-	1/(32fs)	-	s
	BCKO1-0 bits = "01"	tBCK	-	1/(64fs)	-	s
	BCKO1-0 bits = "10"	tBCK	-	1/(128fsn) 1/(128fsd)	-	s
	BCKO1-0 bits = "11"	tBCK	-	1/(256fsn)	-	s
	TDM Mode (Note 19)	tBCK	-	1/(256fsn) 1/(256fsd) 1/(128fsq)	-	s
Duty Cycle		dBCK	-	50	-	%

Note 19. In TDM modes, TVDD=3.0V~3.6V. The AK4558 does not support variable pitch mode.

Parameter		Symbol	Min.	Typ.	Max.	Unit
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency						
Normal Speed Mode: 256fs, 512fs		fsn	8	-	54	kHz
384fs, 768fs			8	-	48	kHz
Double Speed Mode: 256fs		fsd	54	-	108	kHz
384fs			48	-	96	kHz
Quad Speed Mode: 128fs		fsq	108	-	216	kHz
192fs			96	-	192	kHz
Stereo mode duty cycle		Duty	45		55	%
TDM128Mode: (Note 19)						s
I^2S compatible: Pulse Width Low		tLRCKL	1/(128fsq)	-	127/(128fsq)	s
MSB or LSB justified: Pulse Width High		tLRCKH	1/(128fsq)	-	127/(128fsq)	s
TDM256 Mode: (Note 19)						
I^2S compatible: Pulse Width Low		tLRCKL	1/(256fsn) 1/(256fsd)	-	255/(256fsn) 255/(256fsd)	s
MSB or LSB justified: Pulse Width High		tLRCKH	1/(256fsn) 1/(256fsd)	-	255/(256fsn) 255/(256fsd)	s
BICK Input Timing						
Period	Stereo Mode					
	PLL3-0 bits = “0011”	tBCK	-	1/(32fs)	-	s
	PLL3-0 bits = “0010”	tBCK	-	1/(64fs)	-	s
	PLL3-0 bits = “0001”	tBCK		1/(128fsn) 1/(128fsd)		s
	PLL3-0 bits = “0000”	tBCK	-	1/(256fsn)	-	s
	TDM128 Mode PLL3-0 bits = “0001”	tBCK	-	1/(128fsq)	-	s
	TDM256 Mode PLL3-0 bits = “0000”	tBCK	-	1/(256fsn) 1/(256fsd)	-	s
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	s
Pulse Width High		tBCKH	0.4 x tBCK	-	-	s

PLL Slave Mode (PLL Reference Clock = LRCK pin)						
LRCK Input Timing						
Frequency						
Normal Speed Mode:	256fs, 512fs	fsn	8	-	54	kHz
	384fs, 768fs		8	-	48	kHz
Double Speed Mode:	256fs	fsd	54	-	108	kHz
	384fs		48	-	96	kHz
Quad Speed Mode:	128fs	fsq	108	-	216	kHz
	192fs		96	-	192	kHz
Stereo Mode: Duty Cycle		Duty	45	-	55	%
TDM128Mode:						s
I^2S compatible: Pulse Width Low		tLRCKL	1/(128fsq)	-	127/(128fsq)	s
MSB or LSB justified: Pulse Width High		tLRCKH	1/(128fsq)	-	127/(128fsq)	s
TDM256 Mode:						
I^2S compatible: Pulse Width Low		tLRCKL	1/(256fsn) 1/(256fsd)	-	255/(256fsn) 255/(256fsd)	s
MSB or LSB justified: Pulse Width High		tLRCKH	1/(256fsn) 1/(256fsd)	-	255/(256fsn) 255/(256fsd)	s
BICK Input Timing						
Period	Stereo Mode	tBCK	1/(64fs) 1/(128fsd) 1/(256fsn)	-	1/(32fsn)	s
	TDM128 Mode (Note 19)	tBCK	-	1/(128fsq)	-	s
	TDM256 Mode (Note 19)	tBCK	-	1/(256fsn) 1/(256fsd)	-	s
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	s
Pulse Width High		tBCKH	0.4 x tBCK	-	-	s

Parameter	Symbol	Min.	Typ.	Max.	Unit
External Slave Mode					
MCKI Input Timing					
External Clock					
256fsn:	fCLK	2.048	-	13.824	MHz
Pulse Width Low	tCLKL	29	-	-	ns
Pulse Width High	tCLKH	29	-	-	ns
384fsn:	fCLK	3.072	-	18.432	MHz
Pulse Width Low	tCLKL	22	-	-	ns
Pulse Width High	tCLKH	22	-	-	ns
512fsn, 256fsd, 128fsq:	fCLK	4.096	-	27.648	MHz
Pulse Width Low	tCLKL	15	-	-	ns
Pulse Width High	tCLKH	15	-	-	ns
768fsn, 384fsd, 192fsq:	fCLK	6.144	-	36.864	MHz
Pulse Width Low	tCLKL	11	-	-	ns
Pulse Width High	tCLKH	11	-	-	ns
Pulse Width Low	tCLKL	0.4/fCLK	-	-	s
Pulse Width High	tCLKH	0.4/fCLK	-	-	s
LRCK Input Timing					
Stereo mode					
(TDM1-0 bits = "00")					
Normal Speed Mode: 256fs, 512fs	fsn	8	-	54	kHz
384fs, 768fs		8	-	48	kHz
Double Speed Mode: 256fs	fsd	54	-	108	kHz
384fs		48	-	96	kHz
Quad Speed Mode: 128fs	fsq	108	-	216	kHz
192fs		96	-	192	kHz
Duty Cycle	Duty	45	-	55	%
TDM256 mode (Note 19) (Note 20)					
(TDM1-0 bits = "01")					
LRCK frequency	fsn	8	-	48	kHz
"H" time	tLRH	1/256fsn	-	-	ns
"L" time	tLRL	1/256fsn	-	-	ns
TDM256 mode (Note 19) (Note 21)					
(TDM1-0 bits = "01")					
LRCK frequency	fsd	48	-	96	kHz
"H" time	tLRH	1/256fsd	-	-	ns
"L" time	tLRL	1/256fsd	-	-	ns
TDM128 mode (Note 19) (Note 22)					
(TDM1-0 bits = "10")					
LRCK frequency	fsq	96	-	192	kHz
"H" time	tLRH	1/128fsq	-	-	ns
"L" time	tLRL	1/128fsq	-	-	ns

Note 20. The AK4558 should be in Normal Speed mode.
Note 21. The AK4558 should be in Double Speed mode.
Note 22. The AK4558 should be in Quad Speed mode.

Parameter		Symbol	Min.	Typ.	Max.	Unit
External Master Mode						
MCKI Input Timing						
External Clock						
256fsn:		fCLK	2.048	-	13.824	MHz
384fsn:		fCLK	3.072	-	18.432	MHz
512fsn, 256fsd, 128fsq:		fCLK	4.096	-	27.648	MHz
768fsn, 384fsd, 192fsq:		fCLK	6.144	-	36.864	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing						
Stereo mode						
(TDM1-0 bits = "00")						
Normal Speed Mode: 256fs, 512fs		fsn	8	-	54	kHz
384fs, 768fs			8		48	
Double Speed Mode: 256fs		fsd	54		108	
384fs			48		96	
Quad Speed Mode: 128fs		fsq	108		216	
192fs			96		192	
Stereo Mode: Duty Cycle		Duty	-	50	-	%
TDM256 mode (Note 23)						
(TDM1-0 bits = "1X")		fsn	8	-	48	kHz
LRCK frequency						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(8fsn)	-	s
MSB justified: Pulse Width High		tLRCKH	-	1/(8fsn)	-	s
TDM256 mode (Note 24)						
(TDM1-0 bits = "1X")		fsd	48	-	96	kHz
LRCK frequency						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(8fsd)	-	s
MSB justified: Pulse Width High		tLRCKH	-	1/(8fsd)	-	s
TDM128 mode (Note 25)						
(TDM1-0 bits = "01")		fsq	96	-	192	kHz
LRCK frequency						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(4fsq)	-	s
MSB justified: Pulse Width High		tLRCKH	-	1/(4fsq)	-	s
BICK Output Timing (Table 15)						
Period	BCKO1-0 bits = "00"	tBCK	-	1/(32fs)	-	s
	BCKO1-0 bits = "01"	tBCK	-	1/(64fs)	-	s
	BCKO1-0 bits = "10"	tBCK	-	1/(128fs)	-	s
	BCKO1-0 bits = "11"	tBCK	-	1/(256fsn)	-	s
	TDM Mode	tBCK	-	1/(256fsn) 1/(256fsd) 1/(128fsq)	-	s
Duty Cycle (Note 26)		dBCK	-	50	-	%

Note 23. The AK4558 should be in Normal Speed mode.
Note 24. The AK4558 should be in Double Speed mode.
Note 25. The AK4558 should be in Quad Speed mode.
Note 26. When MCKI = 256fsn or 256fsd and BICK output frequency is 256fs, or when MCKI = 128fsq and BICK output frequency is 128fs, the Duty of BICK is MCKI pulse width.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Slave mode)					
Stereo mode (TDM1-0 bits = "00")					
Normal, Double, Quad Speed Mode (TVDD= 1.7V~3.6V)					
BICK Period	tBCK	1/128fsn	-	-	ns
		1/64fsd	-	-	ns
		1/32fsq	-	-	ns
BICK Pulse Width Low	tBCKL	58	-	-	ns
Pulse Width High	tBCKH	58	-	-	ns
LRCK Edge to BICK "↑" (Note 27)	tLRB	58	-	-	ns
BICK "↑" to LRCK Edge (Note 27)	tBLR	58	-	-	ns
LRCK to SDTO(MSB) (Except I^{2}S mode)	tLRS	-	-	48	ns
BICK "↓" to SDTO	tBSD	-	-	48	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
Normal, Double, Quad Speed Mode (TVDD= 2.7V~3.6V)					
BICK Period	tBCK	1/256fsn	-	-	ns
		1/128fsd	-	-	ns
		1/64fsq	-	-	ns
BICK Pulse Width Low	tBCKL	33	-	-	ns
Pulse Width High	tBCKH	33	-	-	ns
LRCK Edge to BICK "↑" (Note 27)	tLRB	33	-	-	ns
BICK "↑" to LRCK Edge (Note 27)	tBLR	33	-	-	ns
LRCK to SDTO(MSB) (Except I^{2}S mode)	tLRS	-	-	28	ns
BICK "↓" to SDTO	tBSD	-	-	28	ns
SDTI Hold Time	tSDH	5	-	-	ns
SDTI Setup Time	tSDS	5	-	-	ns