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AK4564
16bit CODEC with built-in ALC and MIC/HP/SPK-Amp

GENERAL DESCRIPTION

The AK4564 is a 16bit stereo CODEC with a built-in Microphone-Amp, Headphone-Amp and Speaker-Amp. AK4564 has new recording features, a digital equalizer for microphone inputs and a digital ALC (Automatic Level Control). The playback features also include LINEOUT-Amp, digital volume, Headphone-Amp and Speaker-Amp. The AK4564 suits a portable application with a built-in LCD and etc. The AK4564 is housed in a space-saving 48pin LQFP package.

FEATURE

1. **Resolution: 16bits**
2. **Recording Function:**
   - **4-Input Selector (Internal MIC, External MIC, LINE x 2)**
   - **Pre-Amp**
   - **Digital EQ/HPF/LPF**
   - **Digital ALC (Automatic Level Control) circuit**
   - **FADEIN / FADEOUT**
   - **Digital HPF for offset cancellation (fc=3.7Hz@fs=48kHz)**
   - **Enable mixing of BEEP signal**
3. **Playback Function**
   - **Digital De-emphasis Filter (tc = 50/15μs, fs = 32kHz, 44.1kHz and 48kHz)**
   - **LINEOUT-Amp**
   - **Digital Volume: 0dB ~ - 65.25dB, Mute**
   - **Headphone-Amp**
     - **Po: 5.3mW @ 16 Ω (AVDD = 2.8V)**
   - **Speaker-Amp with built-in ALC**
     - **BTL Output**
     - **Po: 80mW @ 8 Ω**
   - **Enable mixing of BEEP signal**
4. **Power Management**
5. **ADC characteristics (LIN → ADC)**
   - **S/(N+D): 87dB, DR=S/N: 90dB**
6. **DAC characteristics (DAC → LINEOUT-Amp)**
   - **S/(N+D): 82dB, DR=S/N: 88dB**
7. **Master Clock: 256fs/384fs**
8. **Sampling Rate: 8kHz ~50kHz**
9. **Audio Data Interface Format: MSB-First, 2's compliment**
   - **ADC, DAC: 16bit MSB justified, 16bit LSB justified, I^2S**
10. **Ta = -20 ~ 85 °C**
11. **Power Supply Voltage**
    - **CODEC, Speaker-Amp: 2.6 ~ 3.6V**
    - **MIC/Headphone/LINEOUT-Amp: 2.6 ~ 5.5V**
12. **Power Supply Current**
    - **All Power On: 30.5mA**
13. **Package: 48pin LQFP, 0.5mm Pitch**

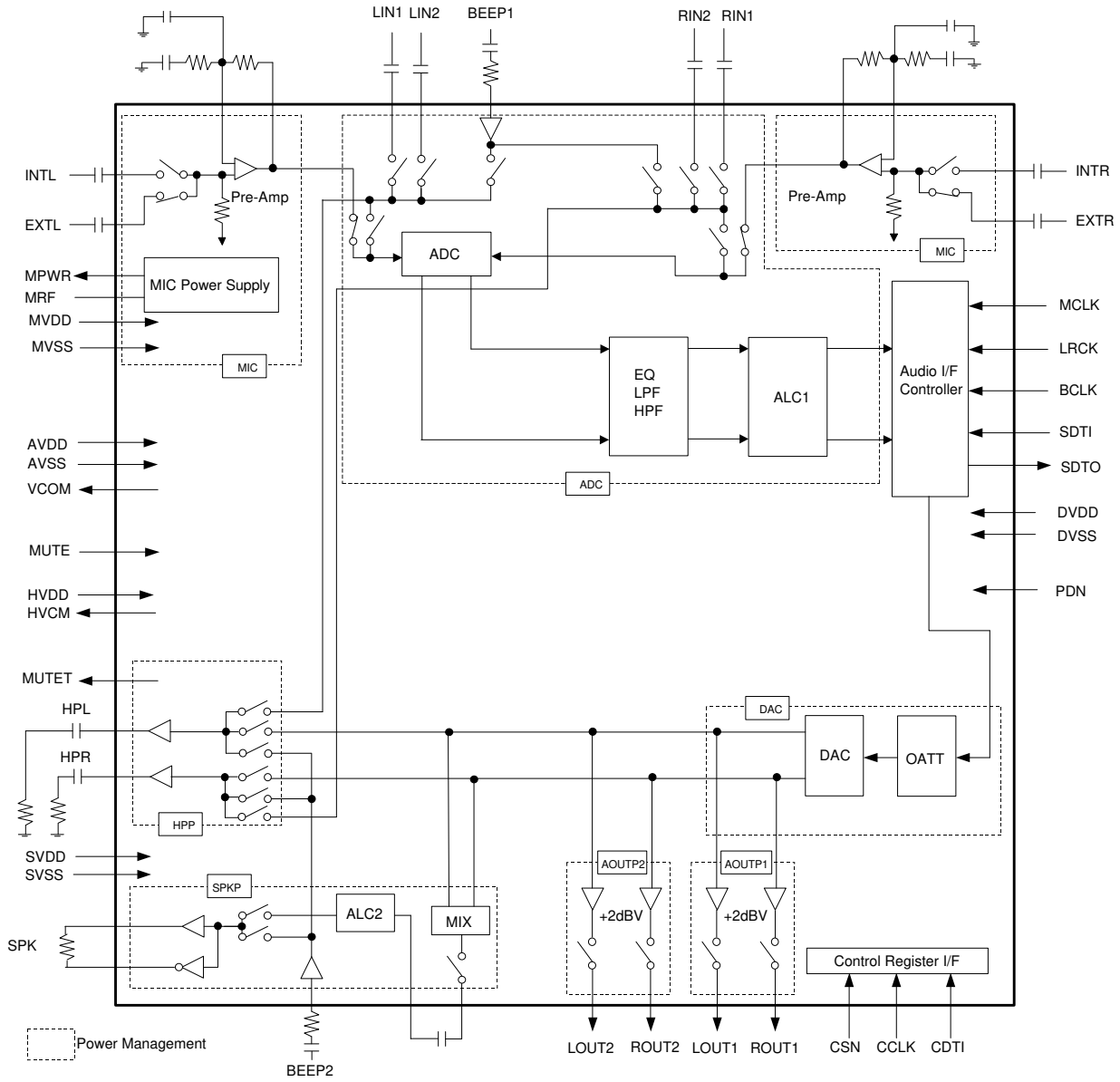


Figure 1. AK4564 block diagram

PIN/FUNCTION

No.	Pin Name	I/O	FUNCTION
Power Supply			
5	SVDD	-	Speaker Amp Power Supply Pin, +3.0V
6	SVSS	-	Speaker Amp Ground Pin
15	DVDD	-	Digital Power Supply Pin, +2.8V
16	DVSS	-	Digital Ground Pin
28	HVDD	-	Headphone-Amp, LINEOUT Power Supply Pin, +4.5V
30	HVCM	O	Headphone-Amp, LINEOUT Common Voltage Output Pin, 0.5 x HVDD
31	AVSS	-	Analog Ground Pin
32	AVDD	-	Analog Power Supply Pin, +2.8V
33	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD
41	MVSS	-	MIC Amp Ground Pin
42	MVDD	-	MIC Amp Power Supply Pin, +2.8V
43	MPWR	O	MIC Power Supply Pin, 1.6V@MVDD=2.8V, Idd=3mA(max)
44	MRF	O	MIC Power Supply Ripple Filter Pin
Operation Clock			
7	BCLK	I	Audio Serial Data Clock Pin
8	MCLK	I	Master Clock Input Pin
9	LRCK	I	Input/Output Channel Clock Pin
13	SDTI	I	Audio Serial Data Input Pin
14	SDTO	O	Audio Serial Data Output Pin
MIC Block			
37	PREOR	O	Rch Pre-Amp Output Pin
38	PRENR	I	Rch Pre-Amp Negative Input Pin
39	EXTR	I	Lch External MIC Input Pin
40	INTR	I	Rch Internal MIC Input Pin
45	INTL	I	Lch Internal MIC Input Pin
46	EXTL	I	Rch External MIC Input Pin
47	PRENL	I	Lch Pre-Amp Negative Input Pin
48	PREOL	O	Lch Pre-Amp Output Pin
Control Data Interface			
10	CDTI	I	Control Data Input Pin
11	CSN	I	Chip Select Pin
12	CCLK	I	Control Clock Input Pin
ADC Block			
17	LIN1	I	Lch Line #1 Input Pin
19	RIN1	I	Rch Line #1 Input Pin
21	LIN2	I	Lch Line #2 Input Pin
23	RIN2	I	Rch Line #2 Input Pin
DAC Block			
18	LOUT1	O	Lch Line #1 Output Pin
20	ROUT1	O	Rch Line #1 Output Pin
22	LOUT2	O	Lch Line #2 Output Pin
24	ROUT2	O	Rch Line #2 Output Pin

NOTE: All digital input pins must not be left floating.

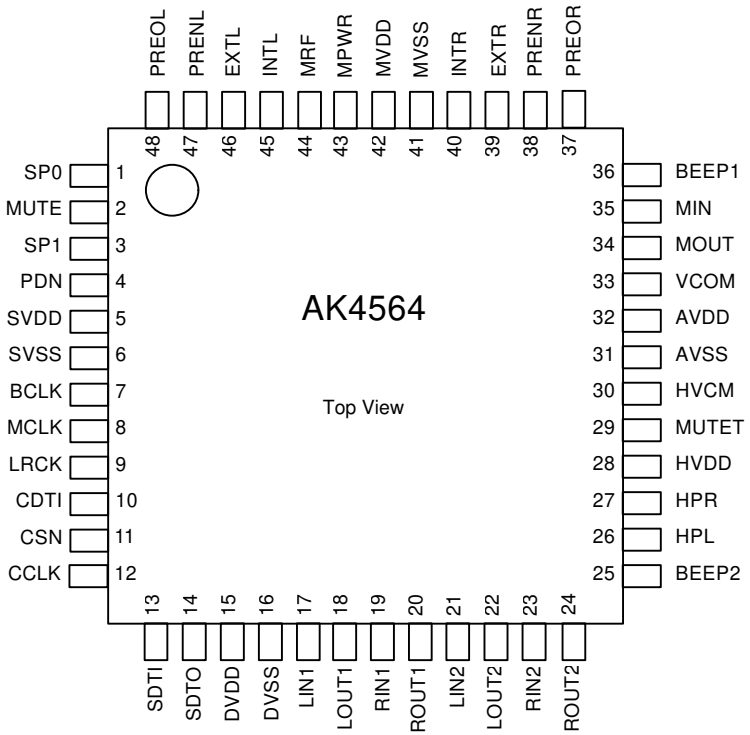
No.	Pin Name	I/O	FUNCTION
Headphone Amp			
26	HPL	O	Lch Headphone Amp Output Pin
27	HPR	O	Rch Headphone Amp Output Pin
29	MUTET	O	Headphone Amp MUTE Capacitor Pin
Speaker Amp Block			
1	SP0	O	Speaker Amp positive Output Pin
3	SP1	O	Speaker Amp negative Output Pin
34	MOUT	O	Analog Mixing Output Pin
35	MIN	I	ALC2 Input Pin
Other Functions			
2	MUTE	I	Mute Pin "L": Normal Operation, "H" MUTE
4	PDN	I	Reset & Power-down Pin "L": Reset & Power-down, "H": Normal Operation
25	BEEP2	I	Beep Signal #2 Input Pin
36	BEEP1	I	Beep Signal #1 Input Pin

NOTE: All digital input pins must not be left floating.

■ Ordering Guide

AK4564VQ	-20 ~ +85°C	48pin LQFP (0.5mm pitch)
AKD4564	Evaluation board for AK4564	

■ Pin layout



ABSOLUTE MAXIMUM RATING

(AVSS, DVSS, MVSS, SVSS=0V;Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog 1	AVDD	-0.3	6.0	V
	Analog 2	HVDD	-0.3	6.0	V
	MIC	MVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	Speaker	SVDD	-0.3	6.0	V
	| DVSS – AVSS | (Note 2)	ΔGND1	-	0.3	V
	| MVSS – AVSS | (Note 2)	ΔGND2	-	0.3	V
	| SVSS – AVSS | (Note 2)	ΔGND3	-	0.3	V
Input Current (Any pins except supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA1	-0.3	AVDD+0.3	V
(Note 4)		VINA2	-0.3	MVDD+0.3	V
Digital Input Voltage (Note 5)		VIND	-0.3	DVDD+0.3	V
Ambient Temperature		Ta	-20	85	°C
Storage Temperature		Tstg	-65	150	°C
Maximum Power Dissipation	Ta=85°C (Note 7)	Pd1	-	500	mW
(Note 6)	Ta=70°C (Note 8)	Pd2	-	700	mW

Note 1. All voltage with respect to ground.
Note 2. AVSS, DVSS, MVSS and SVSS must be connected to the same analog ground plane.
Note 3. LIN1, RIN1, LIN2, RIN2, BEEP1, BEEP2 and MIN pins
Note 4. EXTL, EXTR, INTL, INTR, PRENL and PRENR pins
Note 5. MCLK, LRCK, BICK, SDTI, PDN, CSN, CCLK, CDTI and MUTE pins
Note 6. Wiring density is 50% or more.
Note 7. **Headphone-Amp and Speaker-Amp shouldn't be powered up at the same time. The maximum power supply voltage of SVDD is 3.3V.**
Note 8. **Headphone-Amp and Speaker-Amp can be powered up at the same time.**

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(AVSS, DVSS, MVSS, SVSS=0V;Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog 1	AVDD	2.6	2.8	3.6	V
	Analog 2	HVDD	2.6	4.5	5.5	V
	MIC (Note 9)	MVDD	2.6 or "AVDD – 0.1"	2.8	5.5	V
	Digital	DVDD	2.6	2.8	AVDD	V
	Speaker (Note 10)	SVDD	2.6	3.0	3.3 or 3.6	V

Note 1. All voltage with respect to ground.
Note 9. Minimum value is higher value between 2.6V and "AVDD – 0.1"V.
Note 10. When Ta (max) is 85°C, SVDD (max) is 3.3V. Then Headphone-Amp and Speaker-Amp shouldn't be powered up at the same time.
When Ta (max) is 70°C, SVDD (max) is 3.6V. Then Headphone-Amp and Speaker-Amp can be powered-up at the same time.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, MVDD=2.8V, SVDD=3.0V, HVDD=4.5V; AVSS, DVSS, MVSS, SVSS=0V; fs=48kHz; Input Frequency =1kHz; Measurement width=20Hz ~ 20kHz, unless otherwise specified)

Parameter	min	typ	Max	Units
Pre-Amp Characteristics:				
Input Resistance (INTL, INTR, EXTL, EXTR pins)	70	100	130	kΩ
Maximum Output Voltage (Note 11)			-4.5	dBV
Gain	+18	+24	+30	dB
Load Resistance (Note 12)	3		30	kΩ
Load Capacitance (Note 13)			10	pF
MIC Power Supply Voltage Characteristics: MPWR pin				
Output Voltage (Output current = 0mA) (Note 14)	1.4	1.6	1.8	V
Maximum Output Current			3	mA
ADC Analog Input Characteristics: ALC1 = OFF				
Resolution			16	bits
Input Resistance (LIN1, RIN1, LIN2, RIN2 pins)	70	100	130	kΩ
Input Voltage (Note 15) (Note 16)	-5.1	-4.3	-3.5	dBV
(Note 15) (Note 17)	-58.5	-57.7	-56.9	dBV
S/(N+D) (-0.5dBFS) (Note 16)	78	88		dB
(Note 18)	75	85		dB
DR (-60dBFS, A-Weighted) (Note 16)	84	90		dB
(Note 17)	57	61		dB
S/N (A-Weighted) (Note 16)	84	90		dB
(Note 17)	57	61		dB
Interchannel Isolation (Note 16)	80	100		dB
(Note 17)	50	70		dB
Interchannel Gain Mismatch (Note 16)			0.5	dB
(Note 17)			0.5	dB

Note 11. Maximum output voltage is (0.6 x AVDD) Vpp.
Note 12. Load resistance is the value of "Rf + Ri". (Refer to Figure 12)
Note 13. When the output pin drives some capacitive load, some resistor should be added in series between output pin and capacitive load.
Note 14. When the output current is 0mA, the output voltage of MPWR pin is typically (MVDD – 1.2) V at MVDD=2.8V and typically (MVDD-1.4) V at MVDD=4.5V.
When the output current is 3mA, the output voltage of MPWR pin is typically (MVDD – 1.5) V at MVDD=2.8V and typically (MVDD-1.7) V at MVDD=4.5V.
Note 15. Input voltages are proportional to AVDD voltage.
LIN1, RIN1, LIN2, RIN2 = (0.62 x AVDD) Vpp
INTL, INTR, EXTL, EXTR = (0.0013 x AVDD) Vpp
Note 16. Input from LIN1, RIN1, LIN2 or RIN2 pins. IVOL=0dB.
Note 17. Input from INTL, INTR, EXTL or EXTR pins. Pre-Amp Gain = + 23.9dB, PRE = "1", IVOL = +29.625dB
External resistor of Pre-Amp is "Rf = 10kΩ, Ri = 680Ω". (Refer to Figure 12)
Note 18. Input from INTL, INTR, EXTL or EXTR pins. Pre-Amp Gain = + 23.9dB, PRE = "1", IVOL = +0dB
External resistor of Pre-Amp is "Rf = 10kΩ, Ri = 680Ω". (Refer to Figure 12)

*** 0dBV = 1Vrms = 2.83Vpp**

(Continue)

Parameter	min	typ	max	Units
DAC Analog Output characteristics: Measured via LOUT1/ROUT1, LOUT2/ROUT2, VOL=+6.5dB				
Resolution			16	bits
S/(N+D) (0dBFS)	76	82		dB
DR (-60dBFS, A-Weighted)	82	88		dB
S/N (A-Weighted)	82	88		dB
Output Voltage (Note 19)	+1.2	+2	+2.8	dBV
Interchannel Isolation	80	100		dB
Interchannel Gain Mismatch			0.5	dB
Load Resistance	10			kΩ
Load Capacitance (Note 13)			30	pF
Headphone-Amp Characteristics: DAC → HPL/HPR pin				
Output Voltage (Note 20) HVDD = 3V	-5.5	-4.7	-3.9	dBV
(Note 21) HVDD = 4.5V	-1.1	-0.3	+0.5	dBV
S/(N+D) (Note 20) HVDD = 3V	50	70		dB
(Note 21) HVDD = 4.5V	50	66		dB
Output Noise Voltage (A-Weighted);				
HPG="0", HVDD=3V, R_L=32Ω		-92	-86	dBV
HPG="1", HVDD=4.5V, R_L=100Ω		-77	-71	dBV
Interchannel Isolation; HPG="0", HVDD=3V, R_L=32Ω	60	80		dB
HPG="1", HVDD=4.5V, R_L=100Ω	60	80		dB
Interchannel Gain Mismatch; HPG="0", HVDD=3V, R_L=32Ω			0.5	dB
HPG="1", HVDD=4.5V, R_L=100Ω			0.5	dB
Load Resistance; HVDD=2.6~3.6V, HPG = "0"	22			Ω
HVDD=4.0~5.5V, HPG = "1"	100			Ω
Load Capacitance (C1 in Figure 2)			30	pF
(C2 in Figure 2)			6.8	nF
Speaker-Amp Characteristics: R_L = 8Ω, BTL, MIN → SP0/SP1, ALC2 = OFF				
Output Voltage (-6.5dBV Input)	-4	-2	0	dBV
S/(N+D) (-2dBV Output)	30	60		dB
S/N (A-Weighted)	81	89		dB
Load Resistance	8			Ω
Load Capacitance			10	pF

Note 19. Output voltages are proportional to AVDD voltage.
LOUT1, ROUT1, LOUT2, ROUT2 = (1.27 x AVDD) Vpp @VOL = +6.5dB

Note 20. When DAC = 0dBFS Output, OATT = 0dB, HPG = "0", R_L = 32Ω, the output voltage is (0.59 x AVDD) Vpp.

Note 21. When DAC = -12dBFS Output, OATT = 0dB, HPG = "1", R_L = 100Ω, the output voltage is (0.98 x AVDD) Vpp.

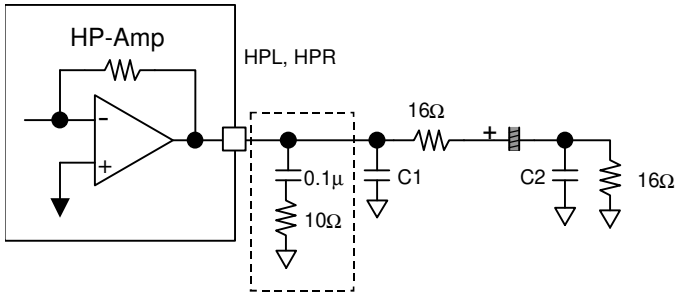


Figure 2. Headphone-Amp Output Circuit

*** 0dBV = 1Vrms = 2.83Vpp**

(Continue)

Parameter	min	typ	max	Units
Monaural Input: (MIN pin)				
Maximum Input Voltage (Note 22)			-4.5	dBV
Input Resistance	14	23	33	kΩ
Monaural Output: DAC → MIX → MOUT pin				
Output Voltage (Note 23)	-5.3	-4.5	-3.7	dBV
Load Resistance	10			kΩ
Load Capacitance (Note 13)			30	pF
BEEP1 Input: BEEP1 pin				
Maximum Output Voltage of Internal Amplifier (Note 24)			-4.5	dBV
Feed-back Resistance	14	20	26	kΩ
BEEP2 Input: BEEP2 pin				
Maximum Output Voltage of Internal Amplifier (Note 24)			-4.5	dBV
Feed-back Resistance	14	20	26	kΩ
Power Supply Current				
Power Up (PDN = "H")				
All Circuit Power-Up: (MIC=ADC=DAC=VCOM=HPP=SPKP=AOUTP1=AOUTP2= "1")				
AVDD+DVDD		13	19.5	mA
MVDD (Note 25)		4.5	6.8	mA
HVDD: HP-Amp Normal operation (AOUTP2,1 = "1", HP-Amp No output)		6.5	9.8	mA
SVDD: SPK-Amp Normal operation (SPPS= "1", SPK-Amp No output)		6.5	9.8	mA
ADC: (ADC=VCOM= "1") (Note 26)				
AVDD+DVDD		7.5	-	mA
DAC+LINEOUT: (DAC=AOUTP1=AOUTP2=VCOM= "1")				
AVDD+DVDD		5.5	-	mA
HVDD: LINEOUT Normal operation, HP-Amp Power OFF (AOUT1,2= "1", HPP = "0")		2.5	-	mA
Power Down (PDN= "L")				
AVDD+DVDD+HVDD+MVDD+SVDD (Note 27)			200	μA

Note 22. Maximum input voltage is proportional to AVDD voltage. (0.6 x AVDD) Vpp
Note 23. DAC 0dBFS Output (Both L/R channels and the same phase) and OATT = 0dB.
Note 24. Maximum output voltage is proportional to AVDD voltage. (0.6 x AVDD) Vpp
Note 25. MPWR pin supplies 0mA.
Note 26. As VCOM bit = "1", power supply current of HVDD is 0.8mA (typ.).
Note 27. In power-down, all digital input pins including clock (MCLK, BCLK and LRCK) pins are held at "DVDD" or "DVSS". PDN pin is held at "DVSS".

*** 0dBV = 1Vrms = 2.83Vpp**

FILTER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, SVDD=2.6 ~ 3.6V, MVDD, HVDD=2.6~ 5.5V; fs=48kHz; De-emphasis = OFF, Digital EQ/HPF/LPF = OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (LPF):						
Passband (Note 28)	±0.1dB	PB	0		18.9	kHz
	-1.0dB		-	21.8	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband (Note 28)		SB	29.4			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note 29)		GD	-	19.0	-	1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 28)	-3.0dB	FR	-	3.7	-	Hz
	-0.56dB		-	10	-	Hz
	-0.15dB		-	20	-	Hz
DAC Digital Filter:						
Passband (Note 28)	±0.1dB	PB	0		21.7	kHz
	-6.0dB		-	24.0	-	kHz
Stopband (Note 28)		SB	26.2			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 29)		GD	-	15.8	-	1/fs
DAC Digital Filter + Analog Filter: (Note 30)						
Frequency Response	0 ~ 20.0kHz	FR		±0.5		dB

Note 28. The passband and stopband frequencies scale with fs (system sampling rate).
For example, ADC is PB=0.454*fs (@-1.0dB), DAC is PB=0.454*fs (@-0.1dB).

Note 29. The calculated delay time caused by digital filtering. This time is from the input of an analog signal to setting the 16bit data of both channels to the output register of the ADC and includes the group delay of the HPF.
For DAC, this time is from setting the 16bit data of both channels on input register to the output of analog signal.

Note 30. DAC → LOUT1/ROUT1, LOUT2/ROUT2

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, SVDD=2.6 ~ 3.6V, MVDD, HVDD=2.6~ 5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	1.5	-	-	V
Low-Level Input Voltage	VIL	-	-	0.6	V
High-Level Output Voltage Iout=-200μA	VOH	DVDD-0.2	-	-	V
Low-Level Output Voltage Iout=200μA	VOL	-	-	0.2	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHRACTERISTICS

(Ta=25°C; AVDD, DVDD, SVDD=2.6 ~ 3.6V, MVDD, HVDD=2.6~ 5.5V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing (MCLK)					
256fs: Frequency	fCLK	2.048	12.288	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs: Frequency	fCLK	3.072	18.432	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
LRCK Timing					
Frequency	fs	8	48	50	kHz
Duty Cycle	Duty	45	50	55	%
Audio Interface Timing					
BCLK Period	tBLK	312.5			ns
BCLK Pulse Width Low	tBLKL	130			ns
Pulse Width High	tBLKH	130			ns
LRCK Edge to BCLK "↑" (Note 31)	tLRB	50			ns
BCLK "↑" to LRCK Edge (Note 31)	tBLR	50			ns
LRCK to SDTO (MSB) Delay Time	tLRM			80	ns
BCLK "↓" to SDTO Delay Time	tBSD			80	ns
SDTI Latch Hold Time	tSDH	50			ns
SDTI Latch Set up Time	tSDS	50			ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Latch Set up Time	tCDS	50			ns
CDTI Latch Hold Time	tCDH	50			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Reset Timing					
PDN Pulse Width	tPDW	150			ns
PDN "↑" to SDTO Delay Time	tPDV		4128		1/fs

Note 31. BCLK rising edge must not occur at the same time as LRCK edge.

■ **Timing Diagram**

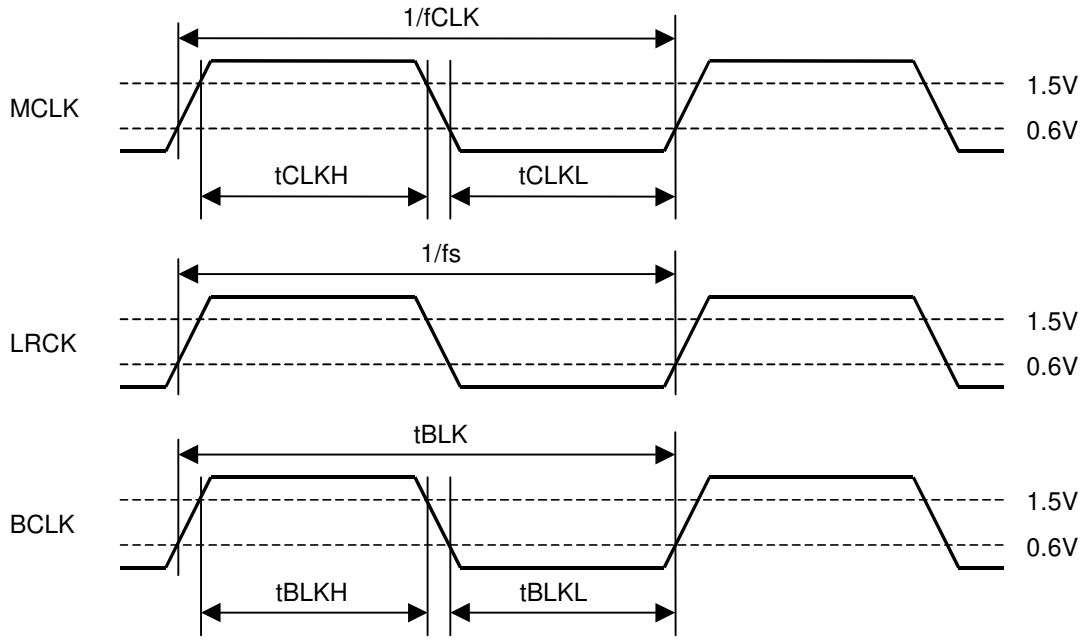


Figure 3. Clock Timing

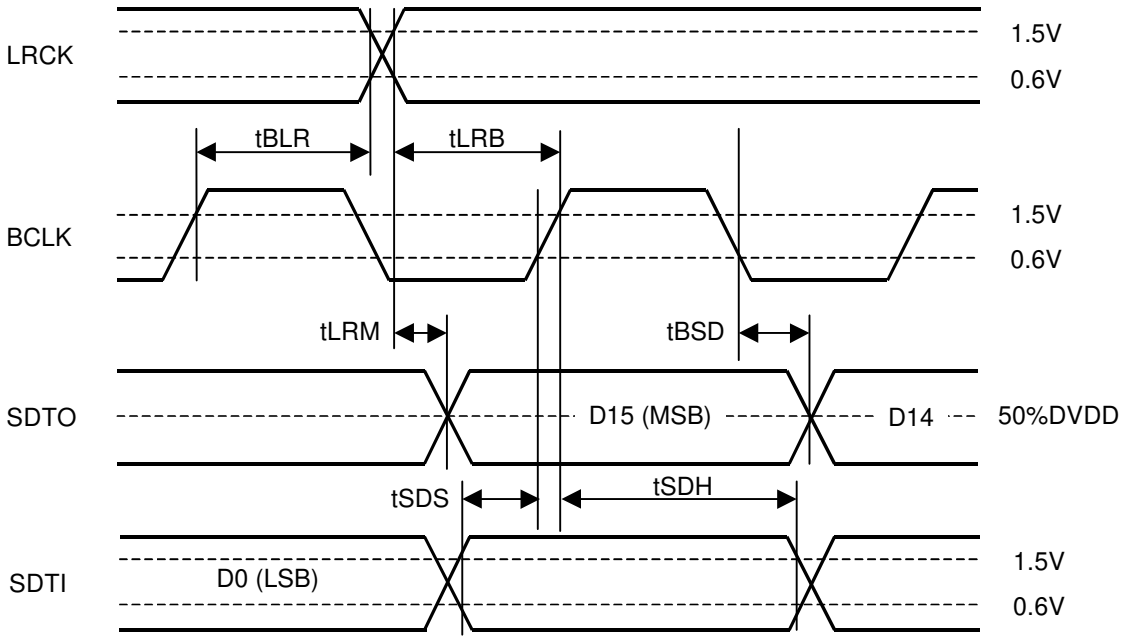


Figure 4. Audio Data Input/Output Timing (Audio I/F format: No. 0)

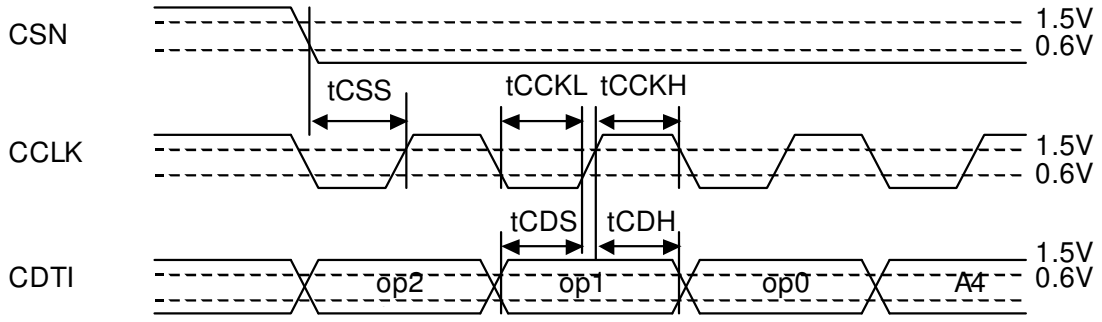


Figure 5. WRITE Command Input Timing

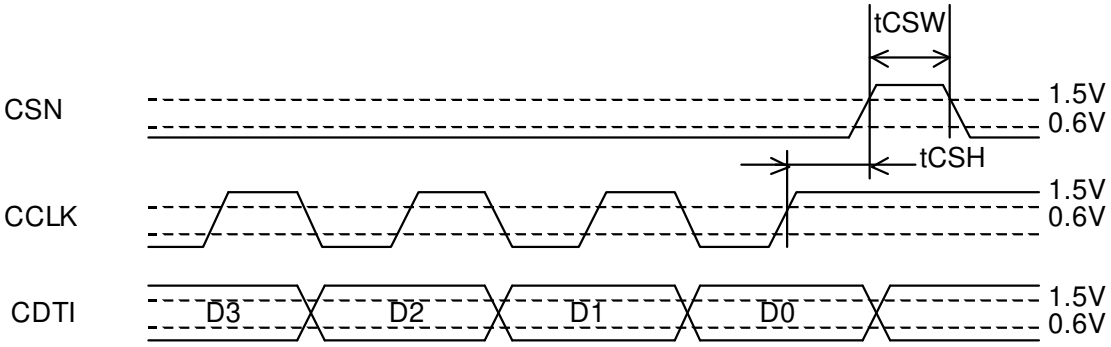


Figure 6. WRITE Data Input Timing

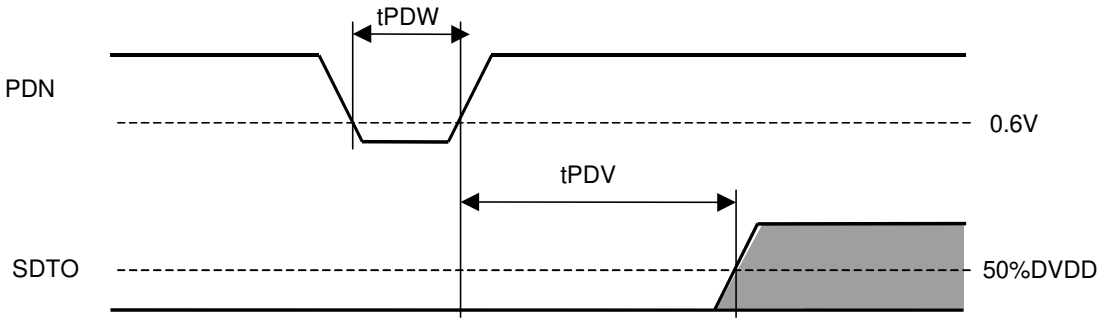


Figure 7. Reset Timing

OPERATION OVERVIEW

■ System Clock

The clocks required to operate are MCLK (256fs/384fs), LRCK (fs) and BCLK (32fs~). The master clock (MCLK) should be synchronized with LRCK. The phase between these clocks does not matter. The frequency of MCLK can be input as 256fs or 384fs. When the 384fs is input, the internal master clock is divided into 2/3 automatically.
*fs is sampling frequency.

When the synchronization is out of phase by changing the clock frequencies during normal operation, the AK4564 may occur click noise. DAC input data should be "0" to avoid click noise.

All external clocks (MCLK, BCLK and LRCK) should always be present except MIC = ADC = DAC = VCOM = HPP = SPKP = AOUT1P = AOUT2P = "0" or PDN = "L". If these clocks are not provided, the AK4564 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the AK4564 should be placed in MIC = ADC = DAC = VCOM = HPP = SPKP = AOUT1P = AOUT2P = "0" or PDN = "L". However, ADC, DAC and ALC2 are in power-down mode until MCLK, BCLK and LRCK is input, even if they release a power-down mode by PDN pin or control register. (Refer to the "Power Management Mode".)

■ System Reset

AK4564 should be reset once by bringing PDN pin "L" upon power-up. After the system reset operation, the all internal registers become initial value.

Initializing cycle is 4128/fs=86ms@fs=48kHz. During initializing cycle, the ADC digital data outputs of both channels are forced to a 2's compliment, "0". Output data of ADC settles data equivalent for analog input signal after initializing cycle. This cycle is not for DAC.

■ Digital High Pass Filter

The AK4564 has a Digital High Pass Filter (HPF) to cancel DC-offset in ADC. The cut-off frequency of the HPF is 3.7Hz at fs=48kHz and it is attenuated to –0.15dB at 20Hz. This cut-off frequency scales with the sampling frequency (fs).

■ Audio Serial Interface Format

The SDTI, SDTO, BCLK and LRCK pins are connected to an external controller. The audio data format has four modes, MSB-first and 2's compliment. The data format is set by the DIF1-0 bits. SDTI is latched by "↑" of BCLK. SDTO is latched by "↓".

When DIF1= "0" and DIF0="1", only BCLK=64fs is acceptable.

No.	DIF1 bit	DIF0 bit	SDTO(ADC)	SDTI(DAC)	BCLK	Figure
0	0	0	MSB justified	LSB justified	≥ 32fs	Figure 8
1	0	1	LSB justified	LSB justified	= 64fs	Figure 9
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 10
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 11

RESET

Table 1. Audio Data Format

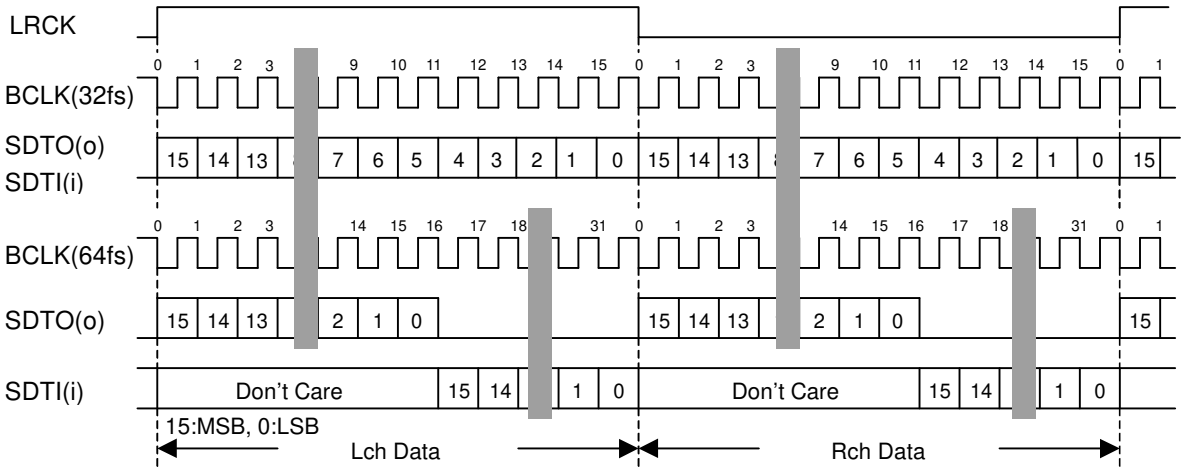


Figure 8. Audio Data Timing (No.0)

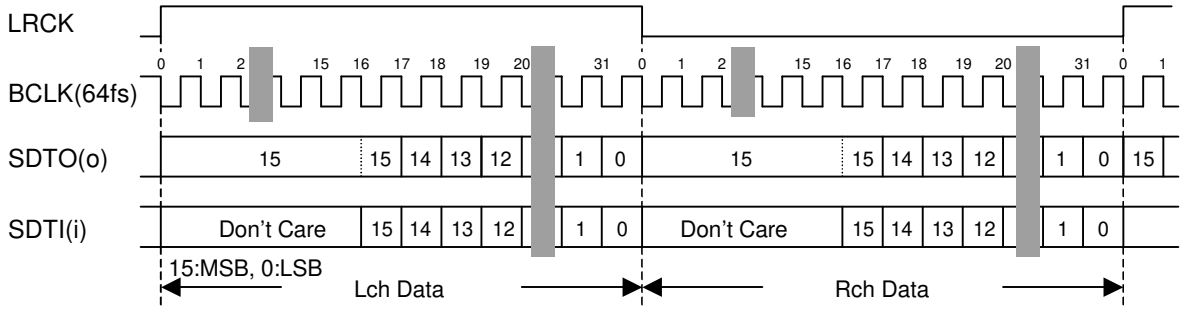


Figure 9. Audio Data Timing (No.1)

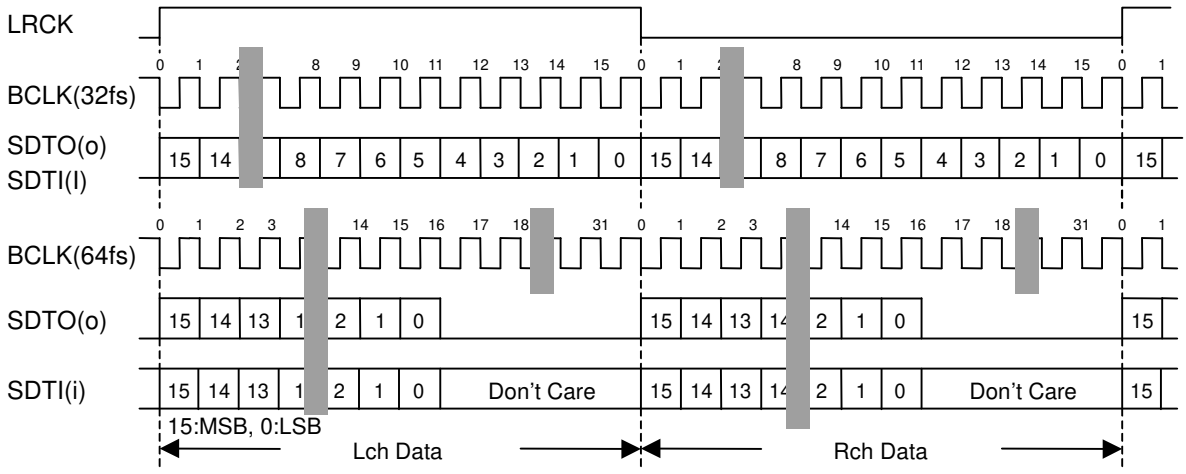


Figure 10. Audio Data Timing (No.2)

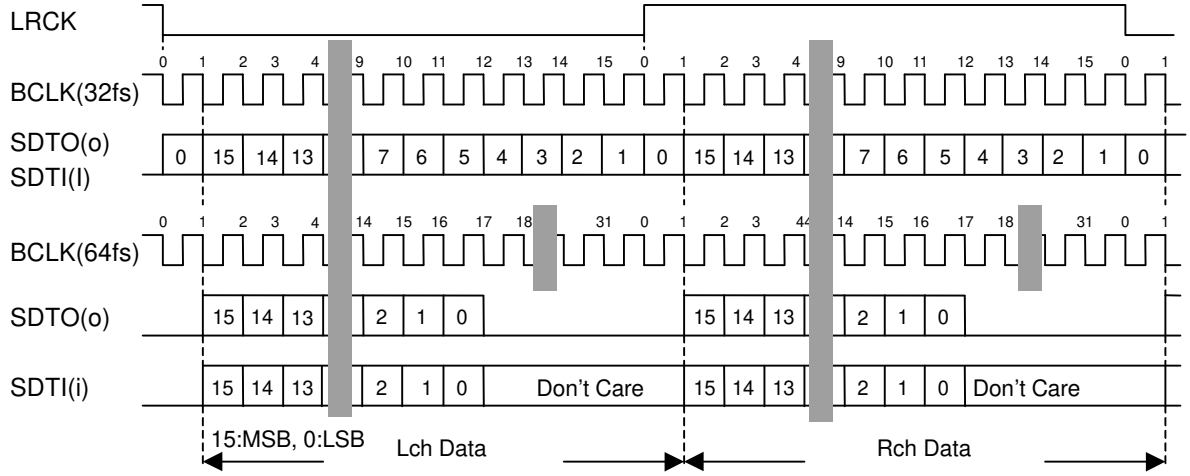


Figure 11. Audio Data Timing (No.3)

■ MIC BLOCK

1. Pre- Amp

Pre-Amp includes selector, Internal MIC or External MIC Mode can be selected by INT/EXT bit. The Pre-Amp is non-inverting amplifier and internally biased to VCOM voltage with 100kΩ (typ.). Gain (1+Rf/Ri) of the Pre-Amp is adjusted by external resistors and should be a range of +18 ~ +30dB.

An external capacitor is needed to cancel DC gain. The Cut-off frequency is determined by an external resistor (Ri) and a capacitor (C1).

A capacitor of 100pF (C2) should be connected to prevent oscillation of Pre-Amp.

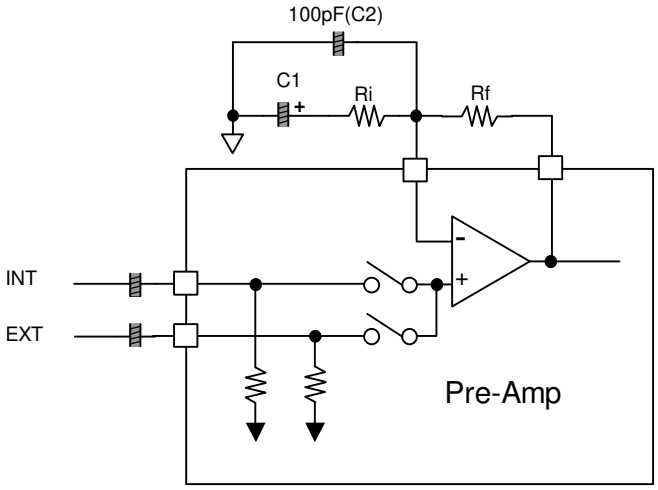


Figure 12. Pre-Amp

2. Power Supply for MIC

The Power Supply for microphone device is supplied from MPWR pin. MPWR pin can supply the current up to 3mA. When the output current is 0mA, the output voltage is typically (MVDD – 1.2) V at MVDD=2.8V and typically (MVDD – 1.4) V at MVDD=4.5V. When the output current is 3mA, the output voltage is typically (MVDD – 1.5) V at MVDD=2.8V and typically (MVDD – 1.7) V at MVDD=4.5V. When MIC bit is “0”, the output current is not supplied.

■ Analog Mixing Circuit for Recording Block

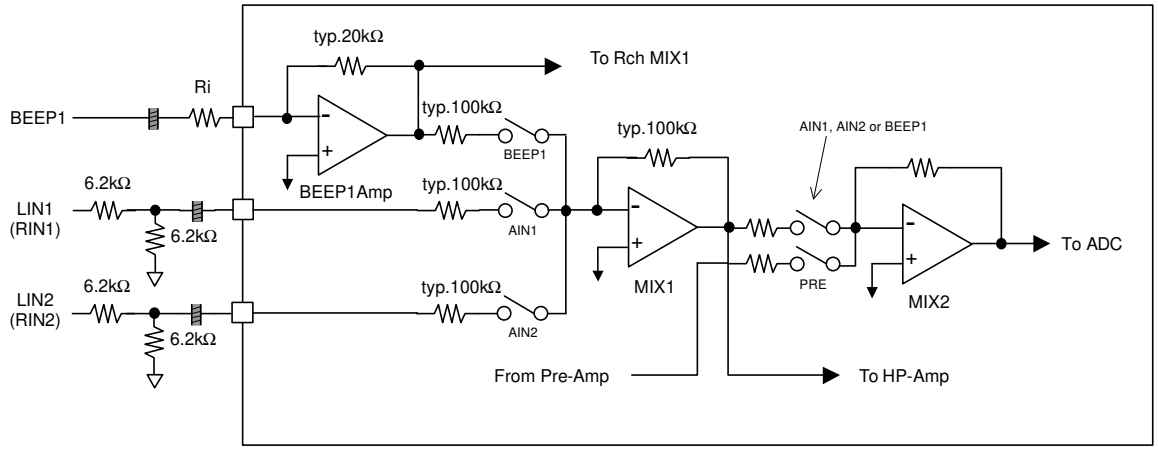


Figure 13. Analog Mixing Circuit for Recording Block

1. BEEP1 Input

When BEEP1 bit is "1", the input signal via BEEP1 pin can be applied to ADC. This signal level can be adjusted by an external resistor (Ri). Feed-back resistor of BEEP1-Amp is 20k ± 30% Ω. (Refer to Figure 13)

2. LINE Input

Input resistance of LIN1, RIN1, LIN2 and RIN2 are typically 100kΩ and centered around the VCOM voltage. When the input voltage exceeds +2dBV, the input signals should be attenuated down to –4.3dBV at VA=2.8V by external resistor divider.

When AIN1 bit is "1", LIN1 and RIN1 pins are selected. When AIN2 bit is "1", LIN2 and RIN2 pins are selected. If AIN1 and AIN2 bits are selected at the both input signals are mixed by the ratio of "1:1"

3. MIX1-Amp

MIX1-Amp is powered-up when ADC bit = "1" or MIX1P bit = "0".

4. MIX2-Amp

MIX2-Amp mixes Pre-Amp output and MIX1-Amp output at the ratio of "1:1".

5. Polarity

Input signals from INTL/INTR, EXTL/EXTR and BEEP1 pins are inverted and are output from ADC. Input signals from LIN1/RIN1 and LIN2/RIN2 pins are non-inverted and output from ADC.

Signal Path	Polarity
INTL/INTR → ADC	Inverted
EXTL/EXTR → ADC	Inverted
BEEP1 → ADC	Inverted
LIN1/RIN1 → ADC	Non-inverted
LIN2/RIN2 → ADC	Non-inverted

Table 2. Polarity of Recording Block

6. MONO Mode

When MONO bit is "1", the recording blocks in the AK4564 becomes MONO mode. The Pre-Amp, MIX1-Amp, MIX2-Amp and ADC analog block of the right channel are powered-down. And the right channel data of ADC is the same as the left channel data of ADC. When changing MONO mode, the ADC should be powered-up by changing ADC bit = "1" after MONO bit is changed to "1". Because click noise may occur when MONO bit is changed during ADC normal operation.

■ BEEP2 Input

When BEEP2H bit is "1", the input signal from BEEP2 pin is output to Headphone-Amp. When BEEP2S bit is "1", the input signal from BEEP2 pin is output to Speaker-Amp.

This signal level can be adjusted by an external resistor (Ri). An internal resistor value (Rf) is 20k ± 30% Ω. In Speaker-Amp, the signal level is gained to +4.6dB internally.

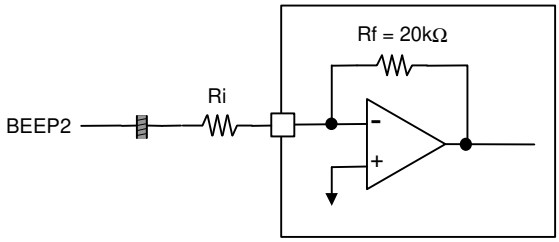


Figure 14. Block diagram of BEEP2 inputs

■ MUTE Function

When MUTE pin is "H", the output signals of LINEOUT, Headphone and Speaker-Amp are muted, and become VCOM or HVCM voltage. The switches of AOUT1, AOUT2, HPDAC, HPMIX, BEEP2H, ALCS and BEEP2S become "OFF" at the same time.

■ Output Digital Volume (OATT)

Attenuation range of the output digital volume is 0dB to -65.25dB with MUTE, and the step width is 0.75dB. When ZEC bit is "1", the attenuation level is changed by zero crossing detection or zero crossing timeout operation. Zero crossing timeout period is set by TM1-0 bits and FSTM bit. When ZCE is "0", it is changed immediately without zero crossing detection.

Channel independent zero crossing detection is used. If new value is written to the OATT register before OATT changes by zero crossing or timeout, the previous value becomes invalid. When the OATT register is written continually, it should take an interval of zero crossing timeout and over.

■ LINEOUT

LINEOUT signals are output from LOUT1/ROUT1 and LOUT2/ROUT2 pins. The output gain is set by VOL1 and VOL2 bits. The common voltage of these outputs is HVCM voltage and load resistance is min. 10kΩ. The Power supply voltage for LINEOUT-Amp is supplied from HVDD pin. The output level of LINEOUT is constant regardless of HVDD voltage. When the voltage of HVDD pin is low, the distortion of LINEOUT degrades.

When LINEOUTs are muted by AOUT1 or AOUT2 bit, the outputs become HVCM voltage and the amps go to Power-Save-Mode. When AOUTP1 (AOUTP2) bit is "0", LINEOUT-Amps become Power-Down-Mode and the output signal goes to Hi-Z.

When PDN pin changes from "L" to "H" after power-up, LINEOUT-Amps become Power-Save-Mode. In Power-Save-Mode, LOUT1/ROUT1 (LOUT2/ROUT2) pins gradually become HVCM voltage via an internal resistor (typ.200kΩ) from Hi-Z to decrease a pop noise. When Power OFF, the pop noise can be decreased by using Power-Save-Mode.

■ Headphone-Amps

The Power supply voltage for Headphone-Amp is supplied from HVDD pin and centered around HVCM voltage. The load resistance and output voltage are specified by HVDD voltage. The output voltage can be changed by supplying AVDD voltage and HPG bit. (Refer to Table 3)

HVDD	2.6 ~ 3.6V	4.0 ~ 5.5V
HPG bit	0	1
Output Voltage	(0.59 x AVDD) Vpp	(0.98 x AVDD) Vpp
Load Resistance (min)	22Ω	100Ω

Table 3. Load resistance and output voltage of Headphone-Amp

When HPG bit is "0", the signals from MIX1, DAC and BEEP2 are output from Headphone-Amps with 0dB gain. When HPG is "1", the signals from MIX1, DAC and BEEP2 output from Headphone-Amps with +16.5dB gain. (Refer to Figure 15)

When HPDAC, HPMIX and BEEP2H bits are "0", the input signals to Headphone-Amp are disabled and HPL/HPR pins output HVCM voltage.

HPMIX, HPDAC and BEEP2H bits control ON/OFF of each input signal. When these bits are "1" at the same time, all input signals are mixed by the ration of "1:1". (Refer to Figure 13 and Figure 16)

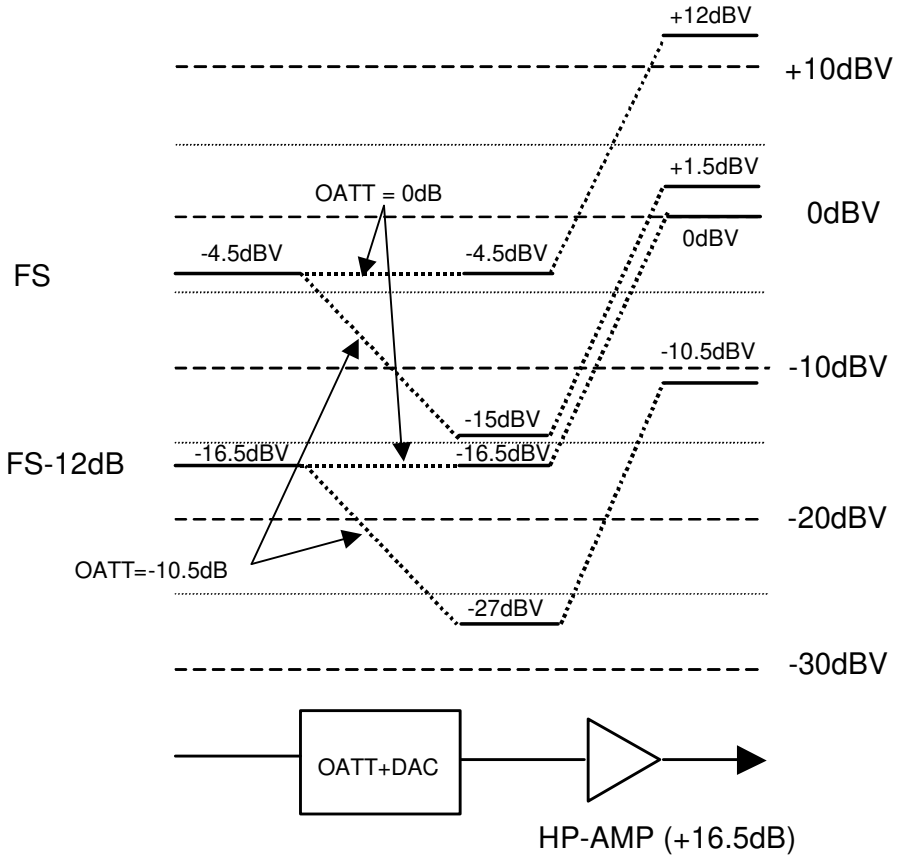


Figure 15. Headphone-Amp Level Diagram (AVDD=2.8V, HVDD=4.5V, HPG = "1", OATT = 0dB& -10.5dB)
* FS = Full Scale

Headphone-Amps are powered-up/down by HPP bit. When HPP bit is "0", Headphone-Amps are powered-down and HPL and HPR pins are fixed to "L" (AVSS). At power-up/down, the common voltage of HPL/HPR pin is settled by a constant which determined by the internal resistor and the external capacitors. The internal resistor is 50kΩ(typ) at power-up, and 1kΩ(typ) at power-down. (Refer to Figure 16)

Rising Time of Headphone-Amp: τ1 = 50kΩ x C1
Falling Time of Headphone-Amp: τ2= 1kΩ x (C1 + 2 x C2)

For example; C1 = 4.7μF, C2 = 100μF

τ1 = 235ms
τ2 = 205ms

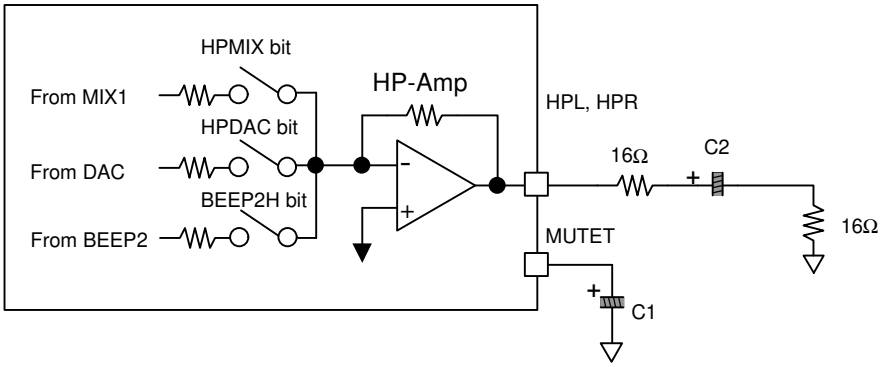


Figure 16. Headphone-Amp internal equivalent circuit

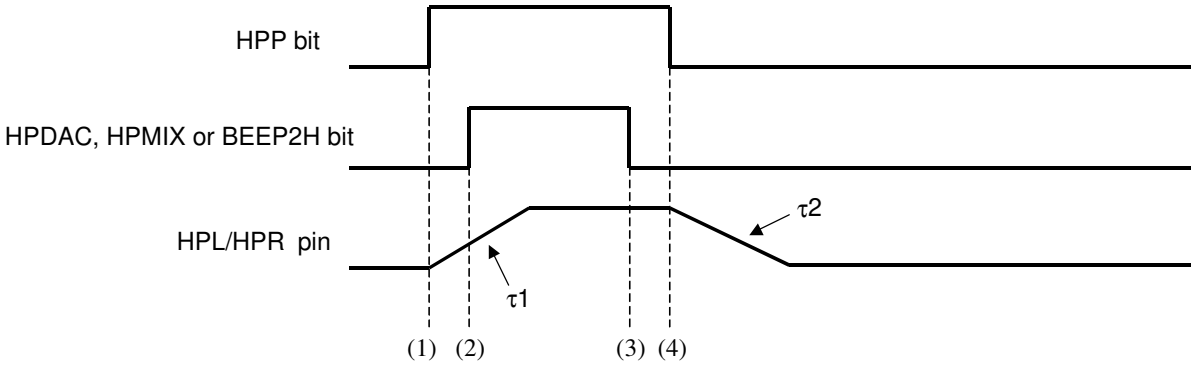


Figure 17. Headphone-Amp Power-Up/Down Timing

(1) Power-up Headphone-Amps: WR (HPP= "1")
The common voltage of HPL/HPR pins rises by the time constant. (τ1)
(2) Enable Headphone-Amp inputs: WR (HPDAC, HPMIX or BEEP2H ="1")
The input signals from MIX1, DAC and BEEP2 are output. Headphone-Amps can output the signals while the common voltage is rising.
(3) Disable Headphone-Amp inputs: WR (HPDAC=HPMIX=BEEP2H="0")
The input signal from MIX1, DAC and BEEP2 are muted. Headphone-Amps output HVCM voltage during muting.
(4) Power-down Headphone-Amps: WR (HPP="0")
The common voltage of HPL/HPR pins falls by the time constant. (τ2)

Headphone-Amps of the AK4564 has a possibility of oscillation depending on headphone characteristics. Therefore, Headphone-amp oscillation prevention circuit may be needed. Headphone-Amps oscillation prevention circuit example is shown in Figure 18.

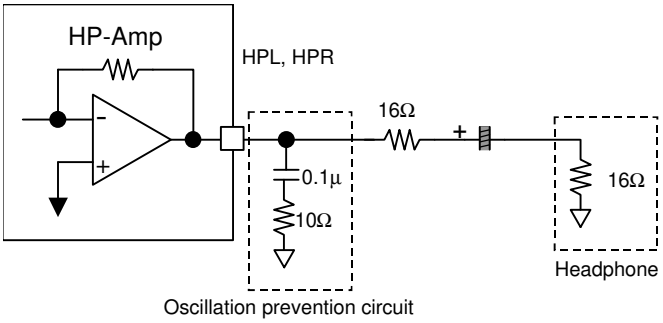


Figure 18. Headphone-Amp oscillation prevention circuit example

*** When Headphone-Amp and Speaker-Amp are powered-up at the same time, refer to the condition of "Note 7", "Note 8" and "Note 10".**

■ SPEAKER BLOCK

The output signal from DAC is converted into a mono signal, [(L+R)/2], and is supplied to Speaker-Amp via ALC2 circuit. This Speaker-Amp has a monaural output by BTL, which can be output up to 80mW at 8Ω. Speaker Blocks (MOUT, ALC2 and Speaker-Amp) can be powered-up/down by SPKP bit. When SPKP bit is "0", MOUT, SP0 and SP1 pins go Hi-Z. When SPPS bit is "0" and SPKP bit is "1", Speaker-Amp becomes Power-Save-Mode. Then SP0 pin goes Hi-Z and SP1 pin is output to SVDD/2 via 100k Ω (typ.).

When PDN pin changes from "L" to "H" after power-up, Speaker-Amp goes to Power-Save-Mode. In Power-Save-Mode, SP1 pin gradually become HVCM voltage via an internal resistor (typ.200kΩ) from Hi-Z to decrease a pop noise. When Power-down (SPKP = "0"), the pop noise can be decreased by controlling via Power-Save-Mode.

*** When Headphone-Amp and Speaker-Amp are powered-up at the same time, refer to the condition of "Note 7", "Note 8" and "Note 10".**

1. Mono Output

MOUT pin outputs analog mixed signal, [(L+R)/2] of DAC output. When MOUT bit is "0", this output is disabled and MOUT pin goes to VCOM voltage. The load impedance is 10kΩ (min.). When SPKP bit is "0", MOUT pin becomes Power-Down-Mode and outputs Hi-Z.

2. ALC2

The input resistance of ALC2 is 23kΩ (typ.) and centered around VCOM voltage. The level diagram of ALC2 operation is shown in Figure 19

ALC2 limiter detection level is –6.5dBV regardless of power supply voltage. When the input signal level exceeds –6.5dBV (=FS-2dB@AVDD=2.8V), the output level of ALC2 is limited.

When the signal over –6.5dBV and is input continuously to the ALC2 circuit, the changing period of ALC2 limiter operation is 2/fs=42μs@fs=48kHz and the output level is attenuated by 0.5dB/step. The ALC2 recovery operation is done by zero crossing detection and the output is gained by 1dB/step. The ALC2 recovery operation is done until the output level of Speaker-Amp goes to –8.5dBV(=FS-4dB@AVDD=2.8V). The ALC2 recovery operation period is fixed to 2048/fs=42.7mS@fs=48kHz. When inputting signal between –6.5dBV and –8.5dBV, both the limiter and recovery operations of ALC2 are not done.

When PDN pin changes from "L" to "H" or SPKP bit changes from "0" to "1", the initilizing cycle (2048/fs = 42.7ms @fs=48kHz) starts. ALC2 is disabled during initilizing cycle, ALC2 starts after finishing the initilizing cycle.

Parameter		ALC2 Limiter operation	ALC2 Recovery operation
Operation Start Level		-6.5dBV	-8.5dBV
Period	fs=48kHz	2/fs = 42μs	2048/fs = 42.7ms
	fs=32kHz	2/fs = 63μs	2048/fs = 64ms
Zero Crossing Detection		No	Yes(Timeout = 2048/fs)
ATT/GAIN		0.5dB step	1dB step

Table 4. Content of ALC2

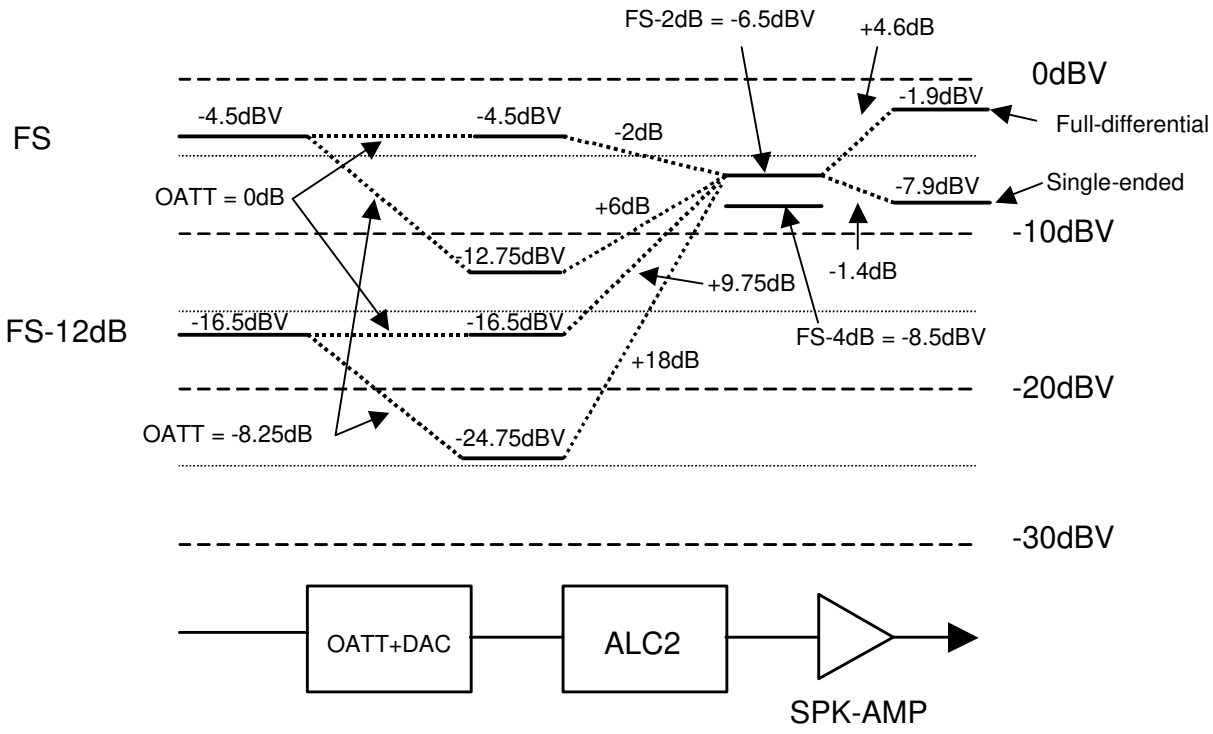


Figure 19. Speaker-Amp Output Level Diagram (AVDD=2.8V, OATT= -8.25dB & 0dB)
*FS = Full Scale

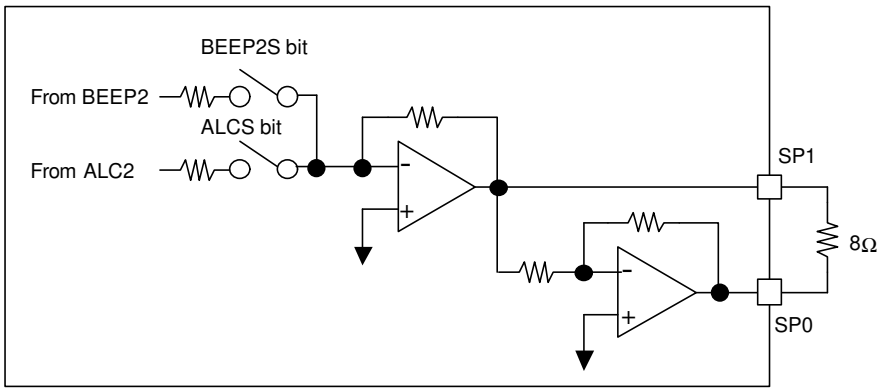


Figure 20. Speaker-Amp Internal equivalent circuit