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AK4571 USB Interface Audio CODEC

Features:

■ USB Audio Controller
- 12 Mbps bit rate
- USB Serial Interface Engine (SIE)
- Audio Class Processing Block
- 4 Endpoints
- USB transceiver

■ 16bit CODEC
- Single-channel A/D Converter
  - Microphone Pre-Amp (Fixed Gain: 20dB)
  - Mute/Volume Control
  - Programmable Gain Control
    - +24dB to –31dB (1dB step)
- D/A Converter
  - 2 channels
- Mixer
  - Mute/Attenuation Control
    - +0dB to –47dB (1dB step)
  - Analog Bass Boost

■ HID Support
- remote control of playback volume/mute
- recording mute/status function

■ Power Management
- control of external headphone amplifier
- low power at suspend mode (< 1uA)

■ EEPROM Interface (Microwire Interface)
- can read Device/String Descriptor from EEPROM
- 1K/2K/4K bit EEPROM

■ On-chip PLL
- 7 sampling frequencies:
  - 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz, 48kHz

■ Single Power Supply, Low Power
- +3.3Volts±0.3V

■ Package
- 48pin LQFP

General Description:

The AK4571 is a USB Interface audio CODEC. The AK4571 incorporates a 16-bit CODEC, PLLs, USB transceiver, SIE (serial interface engine), audio class processing unit, FIFO and other required signals into a single chip. The AK4571 can simultaneously transmit and receive audio stream data through USB bus. In addition to this, the single-channel ADC and 2-channel DAC can operate at different sampling rates.

The AK4571 has a programmable gain amplifier for analog input (IPGA). The gain range is from –31dB to +24dB with 1dB steps. In addition to the IPGA, the AK4571 also has a fixed +20dB pre-amplifier. Analog input signals can be mixed directly with the D/A signal and sent to the LINEOUT pins of the chip.

The analog outputs of the AK4571 can be attenuated up to –47dB in 1dB steps. The AK4571 also has an analog bass boost circuit. Bass Boost response can be modified by changing the values of external resistors and capacitors.

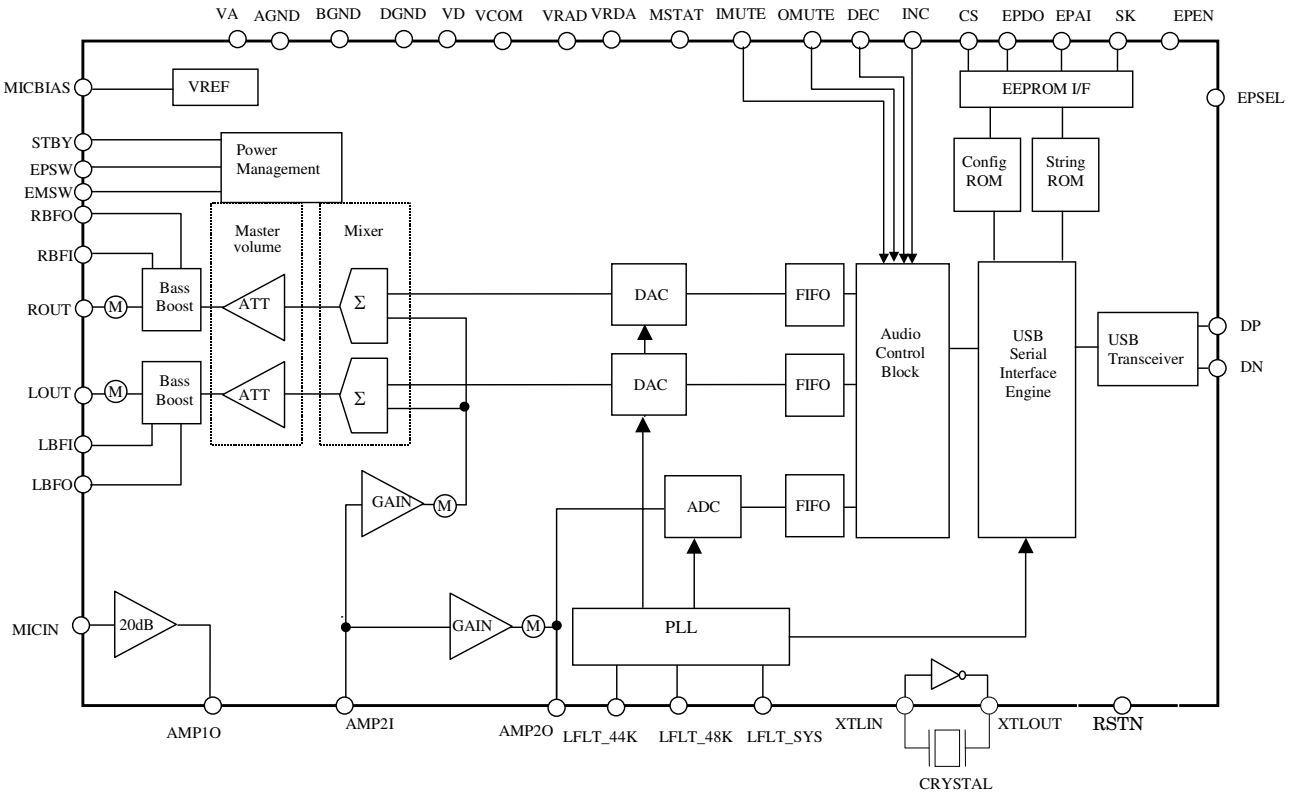
The AK4571 has a Human Interface Device function that allows a user to control the playback volume at the device side. The playback volume on mixer applet moves up or down automatically by the operation of HID buttons. The AK4571 also can mute analog input signal locally in addition to mixer applet control.

The AK4571 has advanced power management capabilities. Suspend current is less than 1uA. The AK4571 can also control the power of an external headphone amplifier to conform to the USB suspend current requirement of 500uA maximum.

The AK4571 has a Microwire interface for an external EEPROM, allowing customization of Vendor ID and product ID.

The high integration of the AK4571 reduces both the number of external components required and the PCB area required to build USB devices, including small format products such as USB headsets.

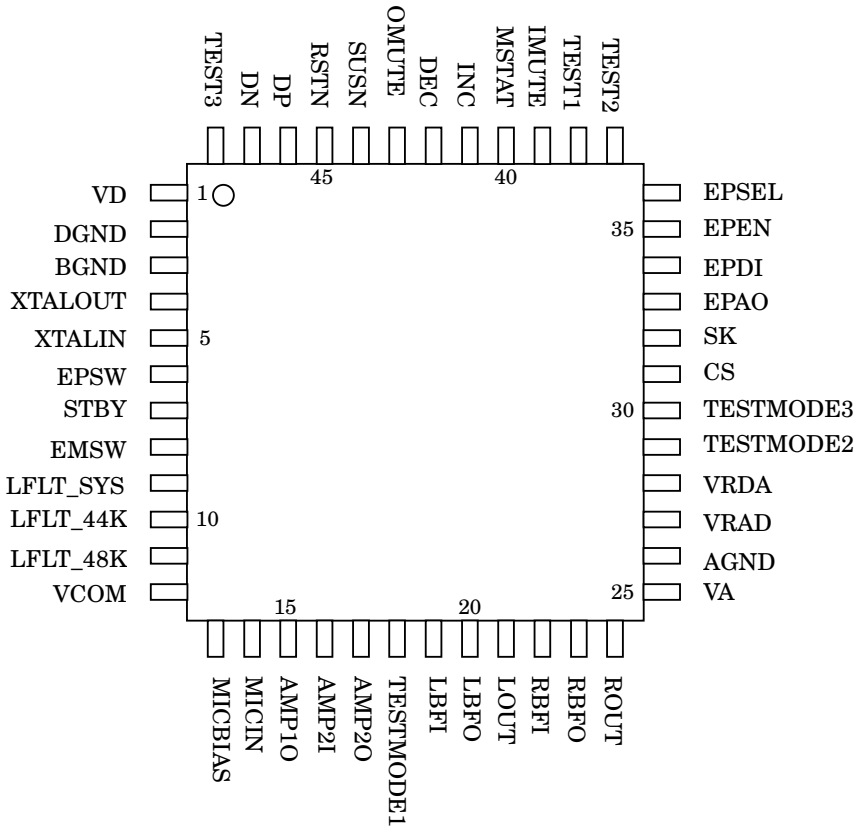
Block Diagram



Ordering Guide

AK4571VQ	0 ~ +70°C	48pinLQFP(0.5mm pitch)
AKD4571	Evaluation Board for AK4571	

Pin Layout



Pin/Function

No.	Signal Name	I/O	Ana / Dig	Description
USB Interface				
46	DP	I/O	D	USB bus Non-Inverting pin. Since the AK4571 is a full-speed device, a 1.5kΩ resistor must be connected between D+ node to VD.
47	DN	I/O	D	USB bus Inverting Pin.
Reset, Crystal, PLL				
45	RSTN	I	D	Reset Pin. Low input resets the chip. Schmitt Trigger input.
44	SUSN	O	D	Suspend Pin "L": Suspend Mode "H": Normal Mode
4	XTALOUT	O	A	Crystal Oscillator Output, Connect Crystal Resonator. Connect capacitor
5	XTALIN	I	A	Crystal Oscillator Input, Connect Crystal Resonator. Connect capacitor
9	LFLT_SYS	O	A	System PLL loop filter Pin. Connect 2.7kΩ resistor and 22nF capacitor in series externally.
10	LFLT_44K	O	A	Codec PLL loop filter Pin. Connect 120kΩ resistor and 6.8nF capacitor in series externally.
11	LFLT_48K	O	A	Codec PLL loop filter Pin. Connect 120kΩ resistor and 6.8nF capacitor in series externally.
Analog Input/Output				
12	VCOM	O	A	Analog Common Voltage Reference Pin
27	VRAD	O	A	ADC Common Voltage Reference Pin.
28	VRDA	O	A	ADC Common Voltage Reference Pin.
14	MICIN	I	A	Mono Channel Microphone Input
15	AMP1O	O	A	Mono Channel 1st Amplifier Output Pin
16	AMP2I	I	A	Mono Channel 2nd Amplifier Input Pin
17	AMP2O	O	A	Mono Channel 2nd Amplifier Output Pin Please Connect 1nF capacitor.
21	LOUT	O	A	Left Channel D/A Out
24	ROUT	O	A	Right Channel D/A Out
19	LBFI	I	A	Left Channel Bass Boost Filter Input Pin
20	LBFO	O	A	Left Channel Bass Boost Filter Output Pin
22	RBFI	I	A	Right Channel Bass Boost Filter Input Pin
23	RBFO	O	A	Right Channel Bass Boost Filter Input Pin
13	MICBIAS	O	A	Voltage Reference Output for the Microphone's bias voltage When the chip goes into Suspend mode, this pin goes to Hi-Z.
External Headphone Amplifier Control				
6	EPSW	O	External Headphone Amplifier Power Switch Control Pin 1 "H": Normal Operation "L": Suspend Mode	
7	STBY	O	External Headphone Amplifier Power Switch Control Pin 2 "L": Normal Operation "H": Suspend Mode	
8	EMSW	O	External Headphone Amplifier Mute Control Pin "H": MUTE ON "L": MUTE OFF	

No.	Signal Name	I/O	Ana / Dig	Description
EEPROM I/F				
31	CS	O	D	EEPROM I/F Chip Select Pin
32	SK	O	D	Read Clock Pin
34	EPDI	I	D	EEPROM Data Input Pin
33	EPAO	O	D	EEPROM Address Output Pin
35	EPEN	I	D	EEPROM Enable Pin "H": Read Device/String Descriptor from external EEPROM "L": Read Device/String Descriptor from internal ROM. CS,SK,EPDI,EPAO are Hi-Z
36	EPSEL	I	D	EEPROM Select "L": 1Kbit Type EEPROM is connected. "H": 2Kbit/4Kbit EEPROM is connected
HID Interface				
39	IMUTE	I	D	A/D Mute Toggles mute status at the rising edge. If this pin is not used, please connect this pin to DGND.
43	OMUTE	I	D	D/A Mute Sets "1" to internal register at the rising edge, and reset to "0" at the falling edge. If this pin is not used, please connect this pin to DGND.
41	INC	I	D	D/A Volume Up Pin Sets "1" to internal register at the rising edge, and reset to "0" at the falling edge. If this pin is not used, please connect this pin to DGND.
42	DEC	I	D	D/A Volume Down Pin Sets "1" to internal register at the rising edge, and reset to "0" at the falling edge. If this pin is not used, please connect this pin to DGND.
40	MSTAT	O	D	Recording Mute Status Pin. "H": Mute ON "L": Mute OFF In suspend mode, this pin is "L".
Power Supply				
25	VA	P	A	Analog Power Supply, 3.3V
26	AGND	P	A	Analog Ground
1	VD	P	D	Digital Power Supply, 3.3V
2	DGND	P	D	Digital Ground
3	BGND	P	D	Bulk Ground, 0V
Test Mode				
18	TESTMODE1	I		Please tie down to AGND for normal operation.
29	TESTMODE2	I		Please tie down to AGND for normal operation.
30	TESTMODE3	I		Please tie down to AGND for normal operation.
38	TEST1	I		Please tie down to DGND for normal operation.
37	TEST2	O		Please open state
48	TEST3	I		Please tie down to DGND for normal operation.

Absolute Maximum Rating

AGND, DGND=0V

Parameter	Symbol	min	Max	Units
Power Supplies				
Analog	VA	-0.3	4.5	V
Digital	VD	-0.3	4.5	V
|DGND-AGND|	ΔGND		0.3	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Analog Input Voltage	VINA	-0.3	VA+0.3	V
Digital Input Voltage	VIND	-0.3	VD+0.3	V
Ambient Temperature	Ta	0	70	°C
Storage Temperature	Tstg	-40	125	°C

Note 1. All voltages with respect to ground

Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Condition

AGND, DGND=0V

Parameter	Symbol	min	typ	Max	Units
Power Supplies					
Analog	VA	3.0	3.3	3.6	V
Digital	VD	3.0	3.3	3.6	V

All voltages with respect to ground.

* AKM assumes no responsibility for usage beyond the conditions set forth in this datasheet.

Analog Characteristics

Ta=25°C,VA=VD=3.3V, Signal Frequency=1kHz, Sampling Frequency Fs=44.1kHz BW=20Hz – 20kHz, TEST mode; unless otherwise specified

Parameter	Min	typ	Max	Units
Mono ADC (1 channel)				
Resolution			16	bits
S/N (A weight) @44.1kHz (PGA is set to 0dB) AMP2I input : USB Normal mode		83		dBA
S/(N+D) (-1.0dB analog input) USB Normal mode		73		dB
Full scale input Voltage	0.53	0.6	0.67	Vrms
MIC amplifier				
S/N (A weight) MICIN input AMP1O output	76	84		dBA
Gain 20dB Selected	+17	+20	+23	dB
Input Impedance	10	20		kΩ
Stereo DAC (2 channel)				
Resolution			16	bits
S/N (A weight) @44.1kHz (DAC volume &master volume is set to 0dB) USB Normal mode		84		dBA
S/(N+D) (-1.0dB digital input) USB Normal mode		75		dB
Full scale output Voltage	0.53	0.6	0.67	Vrms
PGA				
Step size	0	1.0	2.0	dB
Attenuation control range	-31		+24	dB
Input Impedance AMP2I input	10	20		kΩ
Master volume:				
step size	0	1.0	2.0	dB
Attenuation control range	-47		0	dB
Output Load Resistance	10			kΩ
Output Load Capacitance			5	pF
Bass Boost				
Internal Resistance		40		kΩ
External Resistance		360	400	kΩ
External Capacitance			5	pF
MIC Bias (Buffer Amp)				
Output Voltage	1.94	2.2	2.46	Vdc
Output Current			2	mA
Power Supplies				
Analog		35	52	mA
Digital		15	23	mA
Total		50	75	mA
Power Down(Suspend)		0	150	uA

Filter Characteristics

Ta=25°C, VA=VD=3.3V, fs=44.1kHz

Parameter	min	typ	max	Units
ADC Digital Filter (Decimation LPF)				
Pass band (±0.2dB)	0		17.64	kHz
Stop band	26.5			kHz
Stop band Attenuation	70			dB
Group Delay		0.363		ms
ADC Digital Filter (HPF)				
Frequency Response: -3dB -0.5dB -0.1dB		6.89 19.3 44.9		Hz
DAC Digital Filter				
Pass band (±0.2dB)	0		17.64	kHz
Stop band	26.5			kHz
Stop band Attenuation	70			dB
Group Delay		0.312		ms
DAC Analog Post filter				
Pass band Frequency Response	-	±0.1	-	dB

Digital DC Characteristics

Ta=0 - 70°C; VD=3.0 - 3.6V; DGND=0V Measurement under static state
All digital pins except DP, DN. Schmitt hysteresis level of RSTN pin and levels of all test pins will not be tested.

Parameter	Symbol	Min	Typ	Max	Units
EPDI,EPEN, EPSEL, pin "H" level input voltage	VIH	70%VD			V
EPDI, EPEN, EPSEL pin "L" level input voltage	VIL			30%VD	V
RSTN pin "H" level voltage	VIHR	2.4			V
RSTN pin "L" level voltage	VILR			0.8	V
IMUTE, OMUTE, INC, DEC pin "H" level voltage	VIHR	2.4			V
IMUTE, OMUTE, INC, DEC pin "L" level voltage	VILR			0.8	V
SUSN, EPSW, STBY, EMSW, MSTAT pin "H" level output voltage IOH= 2mA	VOH	2.4			V
SUSN, EPSW, STBY, EMSW, MSTAT pin "L" level output voltage IOL= -2mA	VOL			0.6	V
CS, SK, EPAO pin "H" level output voltage IOH= 2mA	VOH	2.4			V
CS, SK, EPAO pin "L" level output voltage IOL= -2mA	VOL			0.6	V
DP, DN Single Ended Receiver Threshold for "H" level	VIHR	2.0			V
DP, DN Single Ended Receiver Threshold for pin "L" level	VILR			0.8	V
Input Leakage Current	Iin			±10	μA
Pull down Resistance (only EPDI pin)@3.3V Ta=25°C	Rpd		100		kΩ

Switching Characteristics

Ta=25°C, VA=VD=3.3V

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency	MCLK	-	12.000	-	MHz
Reset input width @RSTN pin(low active)	Wrst	1.0			us
Time Width for USB Reset Signal Recognition DP<VseL & DN< VseL to USB Reset mode	Trst_rec	3.0			μs
Device Ready Time from USB Reset After releasing from USB Reset to Device Ready (Transaction can start)	Tdrr			10	ms
Time Width for Suspend Recognition Idle state (DP > VseL & DN < VseL) to Suspend mode	Tsus_rec	4.36			ms
Resume Time from Suspend First flip of DP/DN from Idle state To Device Ready*)	Tresm			30	ms
Imute input width with @IMUTE pin(High active)	Wimute	10.005			ms
Omute,Dec,Inc input width with @OMUTE,DEC,INC pin (High active)	Wodi	2.001			ms

Device Ready: VREF, X'tal oscillator and PLL are stable and standard bus transactions can proceed

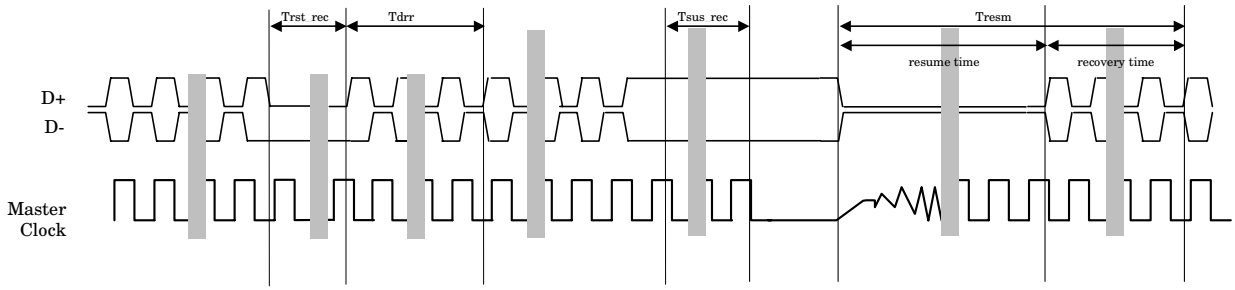


Figure 1. Mode Change with respect to Bus States

Transmitter/Receiver Characteristics

Ta=25°C; VD=3.3V; DGND=0V; CL=50pF

Parameter	Symbol	Pins	Conditions	Min	Typ	Max	Units
Transmitter							
Data Rate	DR	DP,DN		11.97	12	12.03	MHz
Output Impedance (Hi)	Roh	DP, DN	DP, DN="H" at Iout = -10mA		36		Ω
Output Impedance (Lo)	Rol	DP, DP	DP, DN="L" at Iout = 10mA		36		Ω
"H" level Output Voltage	Vohd	DP, DN	at Iout =-200uA	2.8			V
"L" level Output Voltage	Vold	DP, DN	at Iout =2.2mA			0.3	V
Tri-state Leakage Current	Iolk	DP, DN	0 < DP, DN< 3.3V	-10		10	μA
Rise/Fall Time	Trf/Tff	DP, DN		4	10	20	ns
Rise/Fall Time Matching	Trfm	DP, DN			100		%
Crossover Point	Vcrs	DP, DN			1.65		V
Receiver							
Input Common Mode range	CMR	DP, DN		0.8		2.5	V
Differential Input Level	Vdiff	DP, DN	| DP – DN |	0.2			V

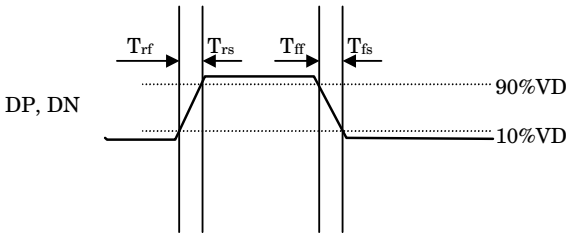


Figure 2. Rise/Fall Time

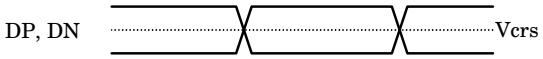


Figure 3. Crossover Point

1 Device Overview

1.1 PLL and Sampling Rates

The AK4571 has three PLLs in addition to a crystal oscillation circuit. The first PLL generates a system clock at 48MHz, the second PLL generates the clock for 44.1kHz sample rates (including derivatives of this sample rate) and third PLL generates the clock for 48kHz sample rates (including derivatives).

The CODEC clocks are generated from the USB SOF, so they are synchronized with USB SOF. The ADC and DAC operate at one of seven sampling rates, 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz, and 48kHz. The ADC and DAC can operate at different sampling rates.

1.2 A/D Converter & D/A Converter

The AK4571 has a 16-bit single-channel A/D converter, and a 16-bit two-channel D/A converter. The AK4571 has a programmable gain amplifier for the analog input (IPGA) with a range from –31dB to + 24dB in 1dB steps. In addition to the IPGA, the AK4571 has a fixed 20dB gain pre-amplifier. Therefore the total gain of the analog input is +44dB maximum. Analog output can be attenuated from 0dB to 47dB in 1dB steps. Analog input and the D/A signal can be mixed in the chip and sent to the Line outputs. The Lineout volume, the microphone playback volume, and the microphone recording volume can be controlled directly from the PC

1.3 Bass Boost Control

The AK4571 has an analog bass boost circuit, and can boost the bass frequencies of the lineout signal by up to 20dB. Frequency response and DC gain are adjusted by external resistors and capacitors. The Bass boost effect is controlled via the HID application.

1.4 Serial Interface Engine (SIE) & Audio Class Processing Block

The AK4571 has a Serial Interface Engine that processes lower-level protocols like CRC checking, bit stuffing, NRZI encoding/decoding, in addition to higher-level protocol like USB standard requests. SIE also notifies the backend that it has received an Audio Class Request, and passes the request to the backend. The backend decodes and processes Audio Class Request like mute requests, volume requests and sampling frequency control requests. Therefore, the AK4571 does not require a micro-controller for this processing.

1.5 HID (Human Interface Device)

Since the AK4571 supports HID function, mute and volume can be controlled remotely. The host knows whether the playback volume/mute button has been pressed or not by issuing an Interrupt Request periodically, and notifies the application that the status has changed. The software application issues the volume/mute request in order to synchronize the software with the AK4571. Input/ Recording signals can be also muted independently of the software application.

1.6 EEPROM I/F

The AK4571 has all of its descriptors in its internal ROM, so it does not require external an EEPROM. However vendor ID, vendor name, product ID, and product name can be also customized by using an external Microwire interface EEPROM. A Microwire™ type, 1K, 2K, or 4K EEPROM can be used.

1.7 Power Management

The AK4571 starts its transition to suspend mode when the idle state of USB bus continues more than 3ms. The AK4571 suppresses the power-supply current (typ.1uA) while in suspend mode because all blocks, including PLLs, pare placed in power-down mode. Under normal operation the AK4571 supplies a bias voltage via the output buffer to the microphone. In suspend mode, the MICBIAS pin goes to a Hi-Z state, and the AK4571 does not supplying this current to the microphone.

The AK4571 also has 3 pins for control of an external headphone amplifier. These pins are used to suppress the power-supply current during suspend mode in addition to suppressing “pop noise” during the transition of suspend/resume. The AK4571 has two pins for power-control because there are “active high” types and “active low” types of external headphone amplifiers. Third pin is for the mute control to suppress transitional pop noise.

The USB bus consumes 200uA current even in suspend mode. A regulator also consumes current in standby mode. Even with these devices consuming power the system can still conform to the 500uA USB specification because of the AK4571 low-power consumption and its control of the microphone and headphone power circuits.

TheAK4571 is ready for operation 30ms after transitioning from suspend mode to normal operating mode.

1.8 USB Transceiver

The AK4571 includes a USB transceiver.

2 Functional Description

2.1 Synchronization of the host and the AK4571

The ADC and DAC in the AK4571 operate synchronously with the SOF (Start of frame) of the USB bus. USB's Isochronous transfer guarantees that audio stream data is transferred once per frame. However, USB does not specify the start point of the transfer in a frame. The worst-case period between two transfers is about 2ms.therefore the AK4571 has a FIFO that stores 2ms audio stream data.

If the CODEC operates at 44.1kHz sampling frequency, the AK4571 expects that 45 samples are transferred once per10 frames. (Please see Figure 4)
The average sampling frequency in Figure 4 is 44.1kHz.

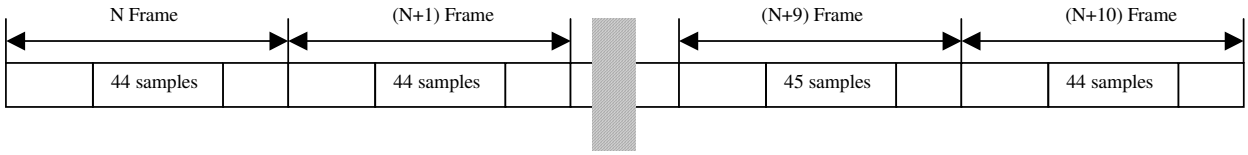


Figure 4 Synchronization Scheme

The AK4571 transmits all A/D data stored to FIFO in the previous frame while updating the A/D data to FIFO in the current frame. The sample count of 48kHz series D/A data per frame is fixed in all frames. For 44.1kHz, the appearance of 45 samples should be just one time per 10 frames. If the D/A clock and SOF clock operated asynchronously, the FIFO would overrun or underrun, and an audible pop noise would occur periodically. Therefore, CODEC clocks are synchronized with SOF clock. In order to achieve this synchronization, the AK4571 has built-in two PLLs for CODEC clocks and generates clocks for both of 48kHz sample rate series and 44.1 sample rate series.

2.2 Power Management

USB devices fall into one of three power categories: 1) Low-power Bus-powered Devices (<100mA) 2) High-power Bus-powered Devices(>100mA, <500mA) 3) Self-powered Devices.

As the AK4571 is a low-power consumption device, it can be defined as a Low-power Bus-powered Device and can be connected to a bus-powered Hub. (High-power Bus-powered Devices can't be connected to a Bus-powered Hub)

USB specifications require a maximum of 500uA in suspend mode. This includes the current drawn between Vbus and ground through the 1.5 k ohm resistor tied to D+ line and Vbus. This current is about 200uA.

Two points should be considered in order to observe the USB suspend mode specification.

a) Suppression of the AK4571 current
   All blocks including ADC, DAC, PLL go to power-down mode when the idle state continues for more than 3ms. Values like volume and mute status are preserved in suspend mode.
b) Control of External Circuits
   The USB specification does not permit more than 500μA of current in suspend mode. Therefore, the AK4571 must control the power dissipation of the external headphone amplifier and microphone. Since the MICBIAS pin is in a Hi-Z state in suspend mode, the AK4571 does not supply current to the microphone.

Headphone Amplifiers commonly have power-down pin and can be controlled externally. There are two types of power-control logic; active-low and active-high. Some headphone amplifiers have a mute pin for suppressing pop noise. The AK4571 supports all of these headphone amplifiers.

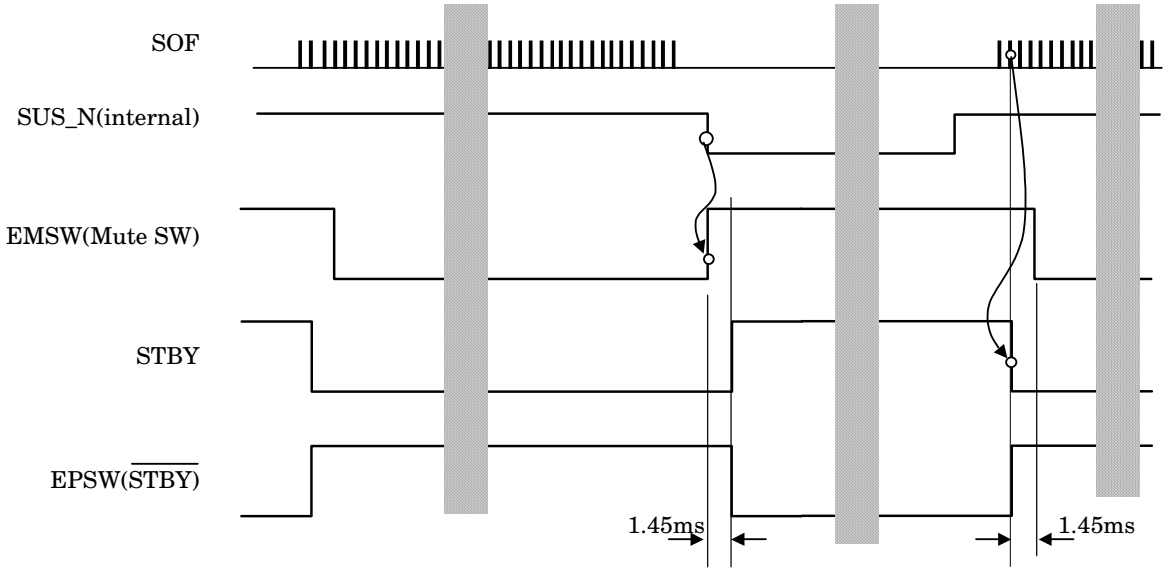


Figure 5 Suspend and Resume Sequence

2.3 Bias Circuit for Microphone

The AK4571 supplies a bias voltage to the microphone through the MICBIAS pin. The output voltage is about 2.2 volts and output current is 2mA maximum. Since the microphone's output signal level is very low, the noise level of the bias voltage should also be low. USB bus transactions typically cause variation of the regulator's output. However, the AK4571 has a built-in voltage reference for mic bias, and suppresses the bias noise caused by the regulator.

Coupling capacitors should be connected in parallel between the two resistors (i.e. Ra=300Ω, and Rb=4.7kΩ/2.2kΩ) in order to make the bias circuit stable. The appropriate value, Rb, depends on the microphone ‘s characteristics.

The output is placed in a Hi-Z state in suspend mode.

2.4 EEPROM Interface

The AK4571 has all descriptors, including String Descriptors, in its internal ROM so it does not require an external EEPROM. The AK4571 also has an EEPROM interface so that an external EEPROM can be attached for customizing Vendor ID, Product ID, vendor name and product name.

The EPEN pin should be “L” if the EEPROM is not used. CS, SK, EPAO pins are at a Hi-Z state in this configuration.
Please see “Descriptors in Detail” section for internal ROM information.

The EPEN pin should be “H” if an external EEPROM is used. The AK4571 reads the Device Descriptor from the EEPROM after a USB Reset. The AK4571 starts to read String Descriptor just after receiving “GET Descriptor (String)” request.

With the AK4571 you can customize the following fields:
1) Device Descriptor (18 bytes)
2) String Descriptor (Language ID, Manufacturer Name, Product Name)

Microwire type (4 wire) , 1K/2K/4K bit EEPROM can be used (for example, AK93C45A/55A/65A)

If a 1Kbit EEPROM is selected, the length of Manufacturer name or Product name should be just 50 bytes. As each String Descriptor requires 2-bytes of length information, the total length of each String Descriptor is 52 bytes.
If a 2K/4K bit EEPROM is selected, the length of Manufacturer name or Product name should be just 100 bytes. As each String Descriptor requires 2-bytes of length information, the total length of each String Descriptor is 102 bytes.
If a 1K bit EEPROM is used, EPSEL pin should be “L” while EPSEL pin should be “H” for a 2K/4K EEPROM.

The length in both cases should be exactly 52 bytes or 102 bytes, no longer, no shorter.

Table 1 shows the relationship between EEPROM address and Descriptor.

	1K bit EEPROM (AK93C45A)	2K/4K bit EEPROM (AK93C55A/65A)
Device Descriptor (18 bytes)	00h -08h	00h-08h
String Descriptor Lang ID (4 bytes index = 0)	09h –0Ah	09h-0Ah
String Descriptor iManufacturer (52 or 102 bytes: index =1)	0Bh-24h-	0Bh-3Dh
String Descriptor iProduct (52 or 102 bytes: index = 2)	25h-3Eh	3Eh-71h

Table 1 Relationship between EEPROM Address and Descriptor

Since the AK4571 cannot write data to the EEPROM, the EEPROM should be mounted on the PCB after it has been programmed with the necessary data. Please refer to the AKM EEPROM datasheet for the write sequence. If EEPROM is not used (EPEN =”L"), an EEPROM should not be mounted on the PCB because the CS, CK and EPAO outputs are Hi-Z when EPEN = “L”.

2.5 Bass Boost

The AK4571 has an analog bass boost that is activated by mounting a resistor and a capacitor between LBFO-LBFI, and RBFO-RBFI respectively as Figure 6 shows. Bass frequencies can be amplified up to 20dB by selecting an appropriate resistor. Cut-off frequency shifts as the capacitor value varies.

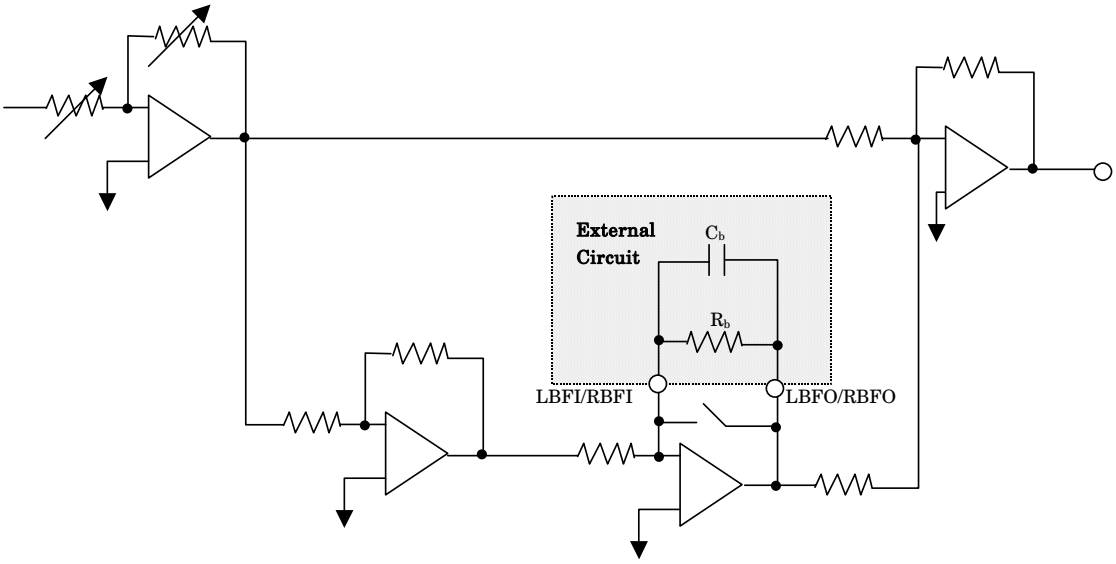


Figure 6 Analog Bass Boost Circuit

Bass Boost

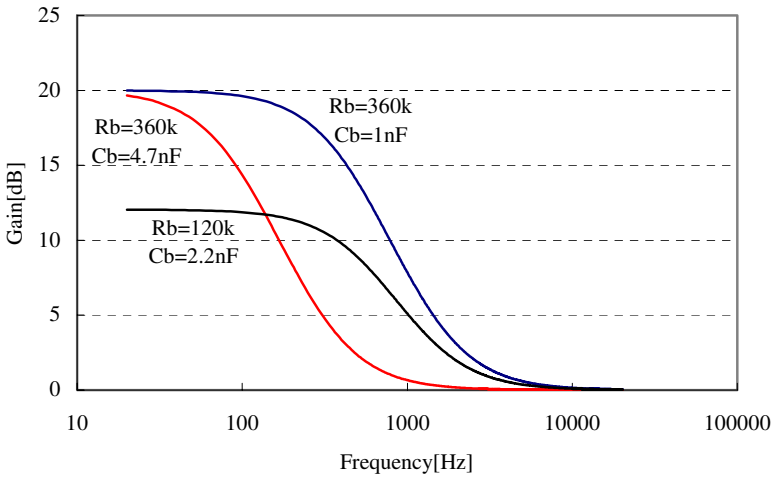


Figure 7 Bass Boost Characteristics

2.6 HID (Human Interface Device)

2.6.1 HID Overview

The AK4571 has two pins for incrementing or decrementing the lineout volume (INC pin and DEC pin), and has a pin for the control of mute (OMUTE pin). For example, the lineout volume slider in a Windows application automatically moves up at the rising edge of INC pin. This means that the value in the Windows program is synchronized with the device's hardware value.

If a button is pressed, the internal bit assigned to it is set to "1". Based on the USB spec for HID, the host knows whether the INC button and/or DEC button and/or OMUTE buttons are pressed or not by periodically issuing an Interrupt transfer request. The AK4571 notifies the host of the status change, but does not change the value itself. The application program changes the value by issuing a SET FEATURE REQUEST.

2.6.2 HID Details

The AK4571 has Interface (#3) and Interrupt Endpoint (#4: 1 byte) commands for HID.
Figure 8 shows hierarchy of HID Interface.

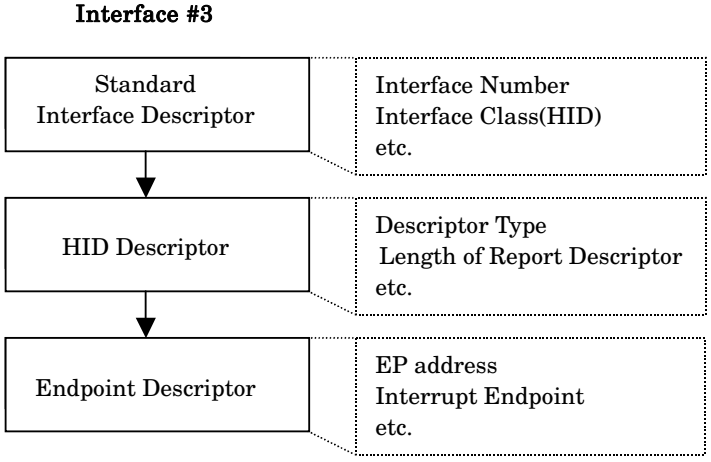


Figure 8 Hierarchy of HID Interface

Interrupt Endpoint is 1 byte, and lower 3 bits are valid.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	"0"	OMUTE	DEC	INC

Internal bits[2:0] are set to "1" at the rising edge of OMUTE, INC or DEC pins, and are cleared to "0" at the falling edge of these respective pins. The AK4571 transmits 1 byte of data through the Interrupt Pipe. If none of the buttons are pressed or if a button is continually pressed, the AK4571 sends NAK to the host.

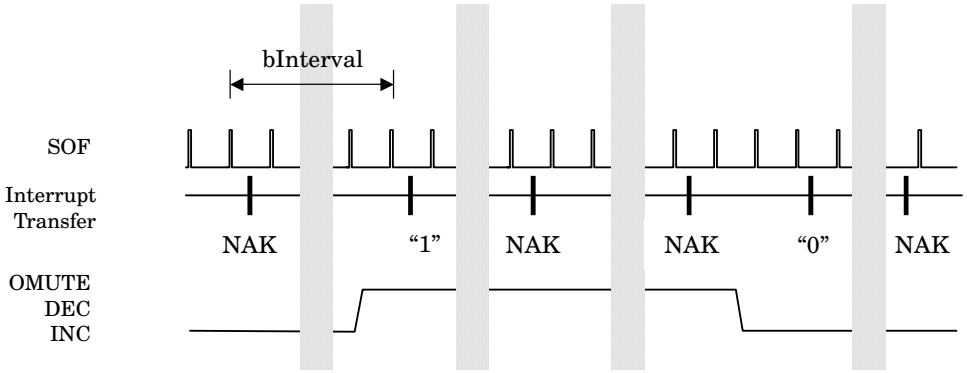


Figure 9 Interrupt Transfer Timing

illustrates a switch de-bounce circuit (highly recommended)

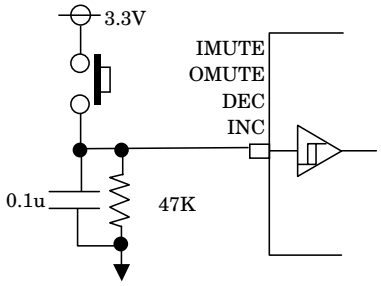


Figure 10 Switch De-Bounce Circuit

Figure 10 illustrates a switch de-bounce circuit (highly recommended)

If HID function is not used, please connect OMUTE pin, DEC pin, INC pin, to DGND.

2.6.3 IMUTE pin and MSTAT pin

The AK4571 has an IMUTE pin for mute control of the recording path. Mute status toggles on the rising edge of the IMUTE pin. Note that pressing a physical button connected to IMUTE changes the internal state. This may cause an inconsistent mute state between the device and the Windows application. MSTAT pin reflects the actual mute status of the device. This limitation comes from the fact that the Windows OS does not support HID audio for recording. The MSTAT pin is forced to "L" in suspend mode regardless of previous state.

MSTAT = (Internal IMUTE status) & SUS_N;
Normal Operation: "H" -> Mute ON
"L" -> Mute OFF
Suspend State: "L"

Figure 10 illustrates a switch de-bounce circuit (highly recommended)

If IMUTE pin is not used, please connect it to DGND.

2.7 Audio Format

The AK4571 supports only the 16-bit, 2's compliment audio format, and outputs LSB first.

1) 16bit mono data format on the USB (A/D data)

Sample #	#1		#2		#3		…
	mono		mono		mono		…
	Lower 8 bit	Upper 8 bit	Lower 8bit	Upper 8 bit	Lower 8 bit	Upper 8 bit	…
bit position	0-7	8-15	0-7	8-15	8-15	8-15	…

2) 16bit stereo data format on the USB (D/A data)

Sample #	#1				#2				…
	Left channel data		Right channel data		Left channel data		Right channel data		…
	Lower 8 bit	Upper 8 bit	Lower 8 bit	Upper 8 bit	Lower 8 bit	Upper 8 bit	Lower 8bit	Upper 8 bit	…
bit position	0-7	8-15	0-7	8-15	0-7	8-15	0-7	8-15	…

2.8 Device topology and function

USB audio devices must report their capabilities to the host and must report the topology that describes the connections between blocks. Figure 11 shows the topology of the AK4571.

The host obtains the capabilities and connection diagram from the device by reading the Audio Control (AC) Interface Descriptor. The volume, mute, and sampling rate are controlled via Audio Class Specific Requests.

1) IN Endpoint#1 for A/D data is related to the MIC signal that is described as [OT1]. The MIC signal is amplified via FU1 and is digitized by the A/D converter and transmitted to the host.

2) OUT Endpoint#2 for D/A data is related to the Lineout. The D/A analog signal is mixed with the MIC analog signal that is amplified through FU2. The mixed analog signal can be attenuated/boosted by FU3, and is output via Lineout.

3) Endpoint#3 for HID is related to playback mute and volume up/down.

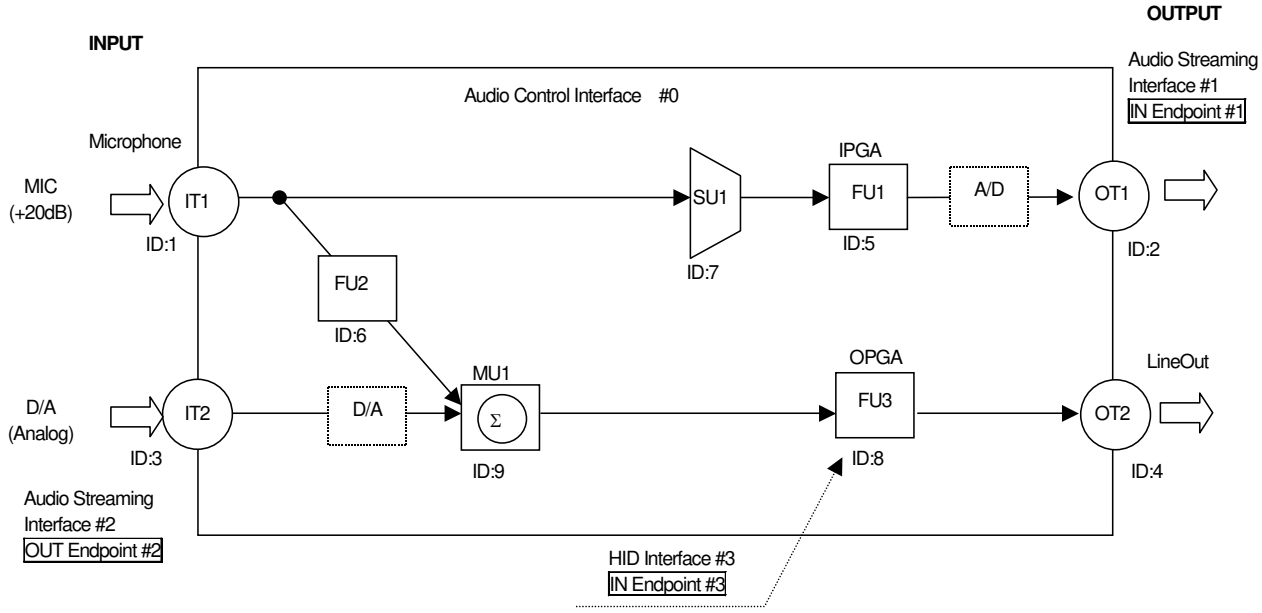


Figure 11 AK4571 Topology

2.8.1 Terminal/Units

a) Input Terminal (IT)
IT is abbreviation of Input Terminal: IT1 (Microphone Input ID:1), IT2 (D/A Input ID:3)

b) Output Terminal (OT)
OT is abbreviation of Output Terminal: OT1(A/D Output ID:2), OT2 (Lineout ID:4)

c) FU (Feature Unit)
The FU (Feature Unit) describes that the AK4571 has volume/mute/bass-boost functions by setting the **bmaControls(0), bmaControls(1) , bmaControls(2)** to "1". The bit position assigned to the bass-boost function is D8, the length of **bcontrolSize** for FU3 is 0x02, and others are 0x01.
bmaControl(0) means master channel. The AK4571 controls DAC mute or bass-boost via the master channel, and controls DAC volume via channel 1 and channel 2 controls. Since the AK4571 input is a single-channel, it controls both ADC mute and volume via the master channel.

e) MU (Mixer Unit)
The MU (Mixer Unit) describes mixing and volume control functions. Each input channel is connected to all output channels per the USB Audio Class specification shown in Figure 12. Only mixing function is available in the AK4571 because the volume is controlled via Feature Unit. Therefore, bitmap of **bmControl** in Mixer Unit Descriptor is all "0".

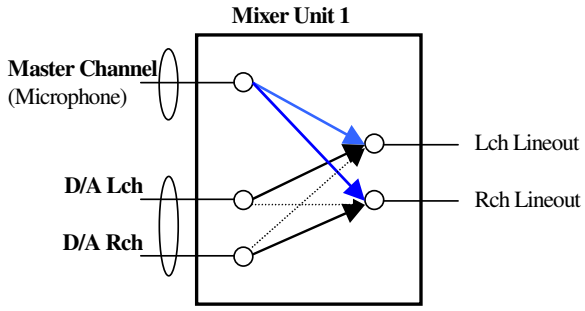


Figure 12 Channel Connection

f) SU (Selector Unit)
Selector Unit is unnecessary for the AK4571's topology. Windows application does not display playback MIC volume slider if the AK4571 does not define Selector Unit.

2.8.2 Descriptor Overview

When the AK4571 is connected to the USB bus, the host assigns unique address to the device first, and starts reading of the device's information via a default pipe. Descriptors consist of (1) Device Descriptor, (2) Configuration Descriptor, (3) Interface Descriptor, (4) Endpoint Descriptor.

The AK4571 is defined as a device with one configuration and four interfaces.
It has one Endpoint (EP) for Interface#0, one EP for Interface#1 (ADC), one for Interface#2 (DAC), and one for Interface#3 (HID)

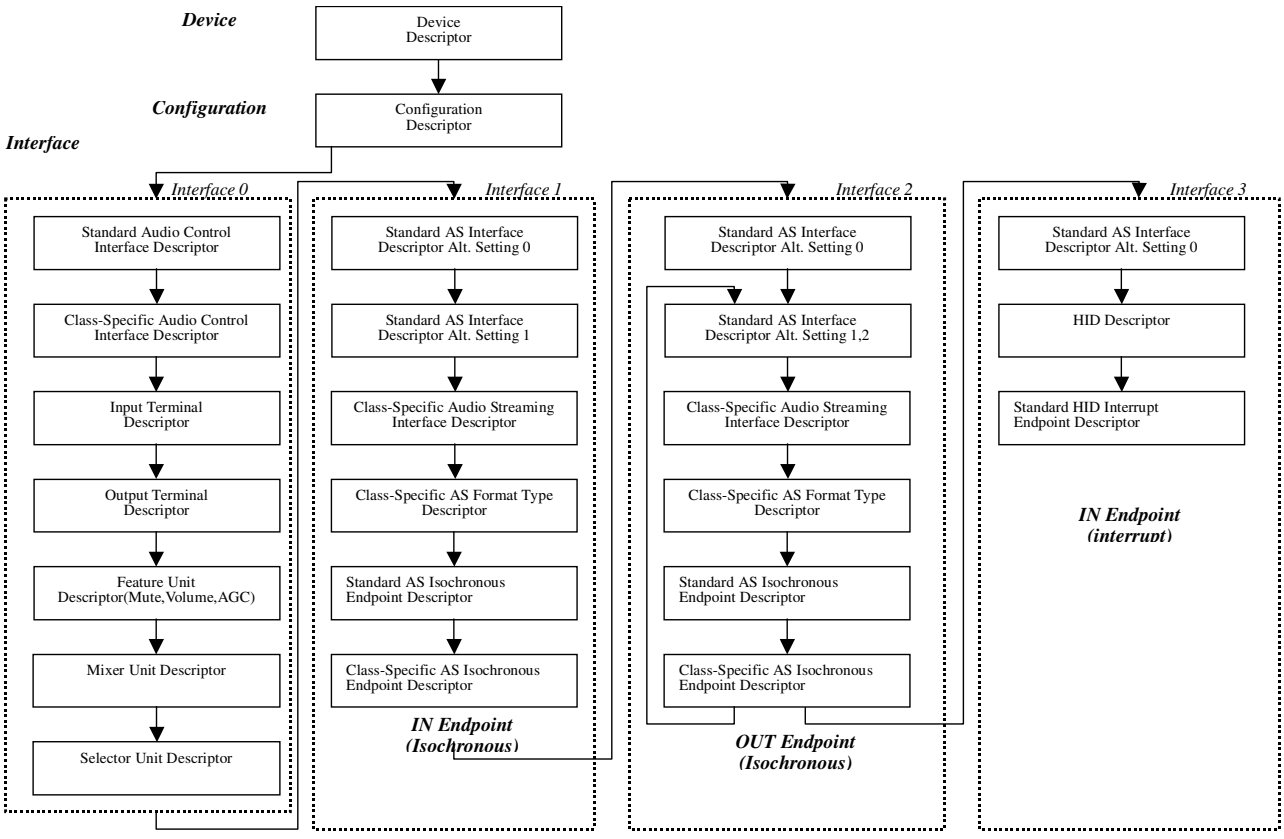


Figure 13 Descriptor Hierarchy

■ **Device Descriptor**
Device Descriptor includes product name, manufacturer name, product revision, etc. And it also includes the number of configurations (The AK4571 is a one configuration device).

■ **Configuration Descriptor**
Configuration Descriptor includes the device type, which is described as bus-powered device or self-powered device, power consumption, number of interfaces, etc. The AK4571 is defined as a low-power bus-powered device with four interfaces.

■ **Interface Descriptor**
The AK4571 has four interfaces as follows.
a) Audio Control (AC) Interface
b) Audio Streaming (AS) Interface1 for A/D converter
c) Audio Streaming (AS) Interface2 for D/A converter
d) HID Interface for Mute & Volume Control

AC Interface includes topology information, Input/Output Terminal information, and Function information in addition to the standard Class Interface Descriptor.

AS Interface also includes audio format and sampling frequencies.

The AK4571 has two alternates for Interface#1 (ADC), and Interface#2 (DAC). The default state is Alt0, and Alt 0 does not occupy USB bandwidth.

Alt 1 is used as the interface for audio streaming data. The bandwidth occupied by A/D data and D/A data are 100 bytes and 200 bytes respectively, and each value is described in the **wMaxPacketSize** field in the Standard Endpoint Descriptor in each interface.

■ **Endpoint Descriptor**
Endpoint 0 (EP0: default pipe) is used for AC Interface. The EP for the AS interface includes IN/OUT, synchronization type, maximum packet length, etc.

The AK4571 also has one Interrupt Endpoint for the HID Interface. The AK4571 returns one byte of information at the Interrupt transfer just after the playback volume or mute buttons are pressed. If no buttons are pressed, the AK4571 returns NAK.

3 Descriptors in Detail

3.1 Device Descriptor

Offset	Field	Size	Value	Description
0	bLength	1	0x12	Size of this descriptor in bytes
1	bDescriptorType	1	0x01	DEVICE descriptor
2	BcdUSB	2	0x0110	1.10 - current revision of USB spec.
4	bDeviceClass	1	0x00	Device defined at Interface level
5	bDeviceSubClass	1	0x00	Unused
6	bDeviceProtocol	1	0x00	Unused
7	bMaxPacketSize0	1	0x08	8 bytes
8	IdVendor	2	0x0556	AKM's Vendor ID
10	IdProduct	2	0x0004	Upper 00 means Audio Product Lower 03 means AKM product ID
12	bcdDevice	2	0x0100	Device release code
14	IManufacturer	1	0x01	" AKM "
15	Iproduct	1	0x02	" AK4571"
16	ISerialNumber	1	0x00	Unused
17	bNumConfigurations	1	0x01	One configuration

Table Device Descriptor

3.2 Configuration Descriptor

Offset	Field	Size	Value	Description
0	Blength	1	0x09	Size of this descriptor
1	bDescriptorType	1	0x02	CONFIGURATION descriptor
2	WTotalLength	2	0x011C	length of entire configuration block total 284 bytes including this interface descriptor.
4	BnumInterfaces	1	0x04	Four interfaces
5	bConfigurationValue	1	0x01	index of this configuration
6	IConfiguration	1	0x00	null string
7	BmAttributes	1	0x80	supports Bus Powered Device
8	MaxPower	1	0x31	98mA