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AK4584

24Bit 96kHz Audio CODEC with DIT/DIR

GENERAL DESCRIPTION

AK4584 is a high-performance 24-bit CODEC for 96kHz consumer audio and digital recording applications. The on-board analog-to-digital converter has an impressive dynamic range, thanks in part to AKM's Enhanced Dual-Bit architecture. The DAC features the newly developed Advanced Multi-Bit architecture and achieves low out-of-band noise and high jitter tolerance through the use of Switched Capacitor Filter (SCF) technology. The AK4584 also has a S/PDIF-AES/EBU digital audio transmitter (DIT) and a digital audio receiver (DIR) that are compatible with 24-bit, 192kHz formats. The AK4584 can automatically detect NON-PCM bit streams like AC-3, MPEG and DTS. Either the ADC or the digital audio input can be routed directly to the digital audio output. The AK4584 has an input Programmable Gain Amplifier and is well suited for computer DAWs, MiniDisc, DVD-R, hard disk and CD-R recording/playback systems.

*AC-3 is a trademark of Dolby Laboratories. DTS is a trademark of Digital Theater Systems, Inc.

FEATURES

1. 24bit 2ch ADC
- **fs: max 96kHz**
- **Single-end Input**
- **S/(N+D): 90dB**
- **Dynamic Range, S/N: 100dB**
- **Digital HPF for offset cancellation**
- **Input PGA with +18dB gain & 0.5dB step**
- **Input DATT with –72dB ATT**
- **I/F format: MSB justified or I^2S**

2. 24bit 2ch DAC
- **fs: max 192kHz**
- **24bit 8 times Digital Filter**
  - **Ripple: ±0.005dB, Attenuation: 75dB**
- **Single-end Output**
- **S/(N+D): 94dB**
- **Dynamic Range, S/N: 104dB**
- **De-emphasis for 32kHz, 44.1kHz, 48kHz sampling**
- **Digital Attenuator with soft-transition**
- **Soft Mute**
- **Zero Detect Function**
- **I/F format: MSB justified, LSB justified or I^2S**

3. 3 Outputs 24 bit 192kHz DIT
- **3-Channel Transmission Outputs (2 Through outputs & DIT Output)**
- **40 bits Channel Status Buffer**

4. 4 Inputs 24bit 192kHz DIR
- **Supports AES3, IEC60958, S/PDIF, EIAJ CP1201**
- **Low Jitter Analog PLL**
- **PLL Lock Range: 32k ~ 192kHz**
- **Clock Source: PLL or X'tal**
- **4 Digital Receive Channel inputs**
- **Detect Function**
  - **Non-PCM Bit Stream Detection**
  - **DTS-CD Bit Stream Detection**
  - **Validity Flag Detection**
  - **Sampling Frequency Detection**
  - **Unlock & Parity Error Detection**
- **40 bits Channel Status Buffer**
- **Burst Preamble bit Pc, Pd Buffer for Non-PCM bit Stream**

5. Support External Audio Clock Input
- **Master Clock Input**
  - **256fs, 384fs, 512fs, 768fs (fs = 44.1kHz ~ 48kHz)**
  - **256fs, 384fs (fs = 88.2kHz ~ 96kHz)**
  - **128fs, 192fs (fs = 176.4kHz ~ 192kHz)**

6. Support Master & Slave Mode

7. Serial μP I/F: 4-wire serial

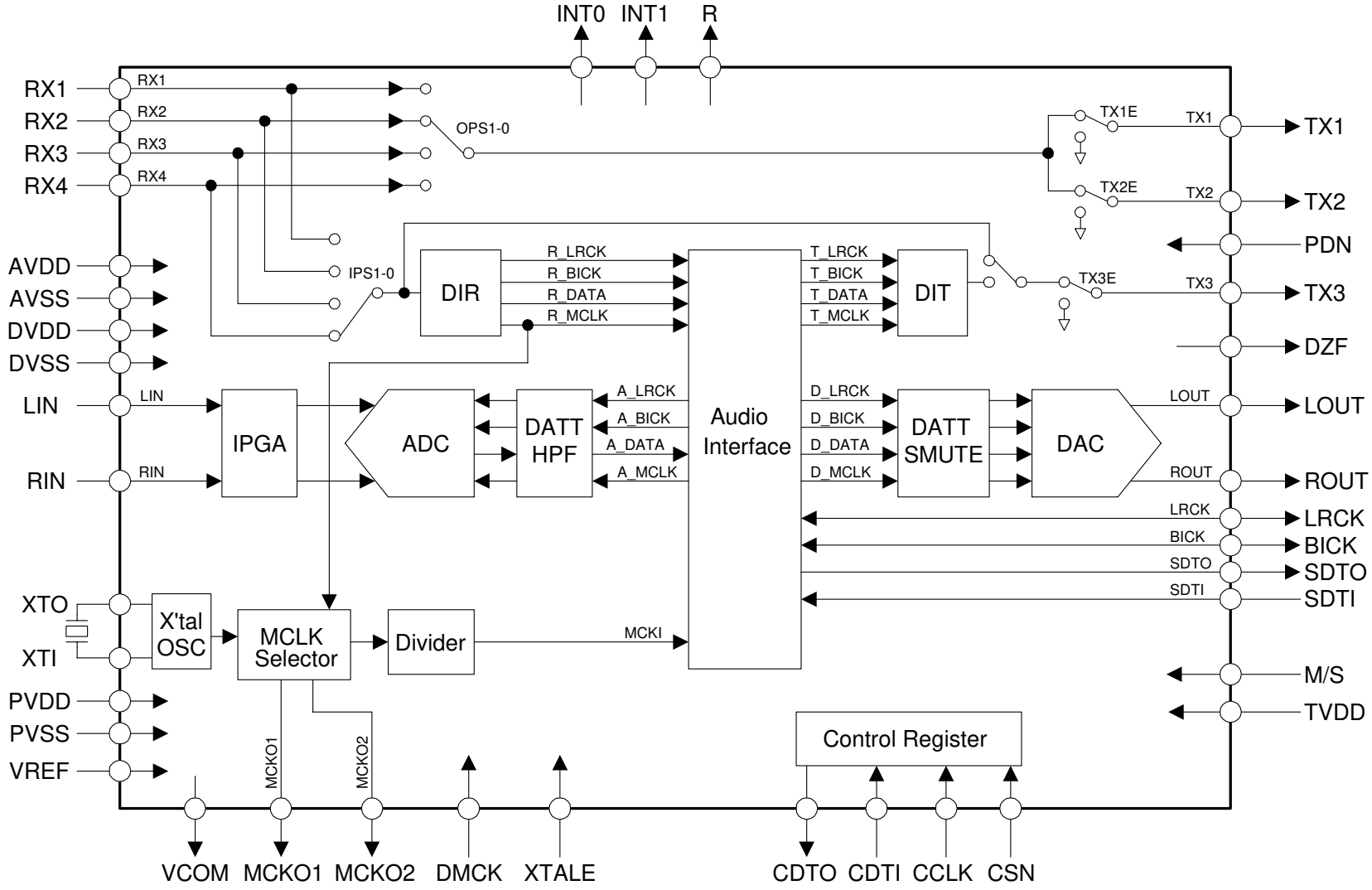
8. 5V operation

9. 3V Power Supply Pin for 3V I/F

10. 44pin LQFP Package

11. Ta: –10 to 70°C

■ Block Diagram

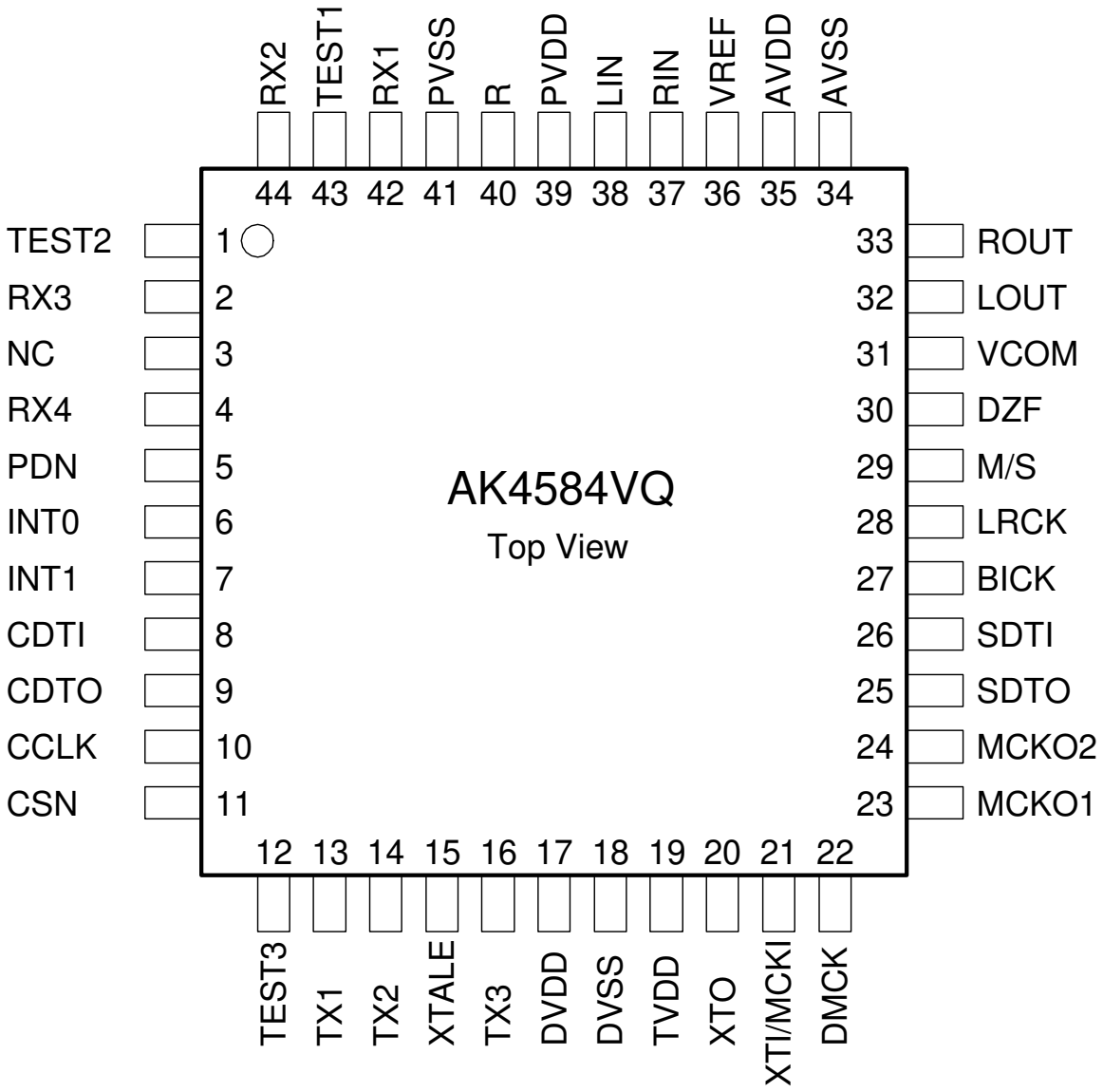


Block Diagram

■ Ordering Guide

AK4584VQ	−10 ~ +70°C	44pin LQFP (0.8mm pitch)
AKD4584	Evaluation Board for AK4584	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	TEST2	I	Test 2 Pin (Internal pull-down pin)
2	RX3	I	Receiver Input 3 with Amp for 0.2Vpp
3	NC	I	NC Pin (No Internal bonding pin, Fixed to "AVSS")
4	RX4	I	Receiver Input 4 with Amp for 0.2Vpp
5	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initialize the control registers.
6	INT0	O	Interrupt 0 Pin
7	INT1	O	Interrupt 1 Pin
8	CDTI	I	Control Data Input Pin
9	CDTO	O	Control Data Output Pin
10	CCLK	I	Control Data Clock Pin
11	CSN	I	Chip Select Pin
12	TEST3	I	Test 3 Pin (Fixed to AVSS)
13	TX1	O	Transmitter 1 Output Pin
14	TX2	O	Transmitter 2 Output Pin
15	XTALE	I	X'tal Osc Enable Pin "H" : Enable, "L" : Disable
16	TX3	O	Transmitter 3 Output Pin
17	DVDD	-	Digital Power Supply Pin, 4.75 ~ 5.25V
18	DVSS	-	Digital Ground Pin
19	TVDD	-	Output Buffer Power Supply Pin, 2.7 ~ 5.25V
20	XTO	O	X'tal Output Pin
21	XTI	I	X'tal Input Pin
	MCKI	I	External Master Clock Input Pin
22	DMCK	I	MCKO1 Disable Pin "H" : MCKO1 "L" output, "L" : MCKO1 output

23	MCKO1	O	Master Clock Output 1 Pin
24	MCKO2	O	Master Clock Output 2 Pin
25	SDTO	O	Audio Serial Data Output Pin
26	SDTI	I	Audio Serial Data Input Pin
27	BICK	I/O	Audio Serial Data Clock Pin
28	LRCK	I/O	Input / Output Channel Clock Pin
29	M/S	I	Master / Slave Mode Pin "H" : Master Mode, "L" : Slave Mode
30	DZF	O	Zero Input Detect Pin
31	VCOM	O	Common Voltage Output Pin, AVDD/2 Bias voltage of ADC inputs and DAC outputs.
32	LOUT	O	Lch Analog Output Pin
33	ROUT	O	Rch Analog Output Pin
34	AVSS	-	Analog Ground Pin
35	AVDD	-	Analog Power Supply Pin, 4.75 ~ 5.25V
36	VREF	I	Voltage Reference Input Pin, AVDD Used as a voltage reference by ADC & DAC. VREF is connected externally to filtered AVDD.
37	RIN	I	Rch Analog Input Pin
38	LIN	I	Lch Analog Input Pin
39	PVDD	-	PLL Power Supply Pin, 4.75 ~ 5.25V
40	R	-	External Resistor Pin for PLL **13kΩ ± 1% resistor to PVSS externally.**
41	PVSS	-	PLL Ground Pin
42	RX1	I	Receiver Input 1 with Amp for 0.2Vpp
43	TEST1	I	Test 1 Pin (Internal pull-down pin)
44	RX2	I	Receiver Input 2 with Amp for 0.2Vpp

Note: All input pins except pull-down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS=DVSS, PVSS=0V; Note 1)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	6.0	V
	PLL	PVDD	–0.3	6.0	V
	Output Buffer	TVDD	–0.3	6.0	V
	|AVSS – DVSS| (Note 2)	ΔGND1	-	0.3	V
	|AVSS – PVSS| (Note 2)	ΔGND2	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (VREF, LIN, RIN pins)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage 1 (Except RX1-4, BICK, LRCK pins)		VIND1	–0.3	DVDD+0.3	V
Digital Input Voltage 2 (RX1-4 pins)		VIND2	–0.3	PVDD+0.3	V
Digital Input Voltage 3 (BICK, LRCK pins)		VIND3	–0.3	TVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–10	70	°C
Storage Temperature		Tstg	–65	150	°C

Note: 1. All voltages with respect to ground.
Note: 2. AVSS, DVSS and PVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS=DVSS, PVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 3)	Analog	AVDD	4.75	5.0	5.25	V
	Digital	DVDD	4.75	5.0	AVDD	V
	PLL	PVDD	4.75	5.0	AVDD	V
	Output Buffer	TVDD	2.7	3.0	DVDD	V
Voltage Reference (Note 4)		VREF	3.0	-	AVDD	V

Note: 1. All voltages with respect to ground.
Note: 3. The power up sequence between AVDD, DVDD, PVDD and TVDD is not critical.
Note: 4. Normally, VREF voltage is the same as AVDD voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=PVDD=TVDD=5.0V; AVSS=DVSS=PVSS=0V; VREF=AVDD; fs=44.1kHz, 96kHz, 192kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=10Hz ~ 20kHz at fs=44.1kHz, 10Hz ~ 40kHz at fs=96kHz; 10Hz ~ 80kHz at fs=192kHz; unless otherwise specified)

Parameter		min	typ	max	Unit
Input PGA Characteristics:					
Input Voltage (Note 5)	fs=44.1kHz, AIN=0.6 x AVDD	2.8	3.0	3.2	Vpp
	fs=96kHz, AIN=0.62 x AVDD	2.9	3.1	3.3	Vpp
Input Resistance		5	10	15	kΩ
Step Size		0.2	0.5	0.8	dB
Gain Control Range		0		18	dB
ADC Analog Input Characteristics: IPGA=0dB					
Resolution				24	Bits
S/(N+D) (-0.5dBFS)	fs=44.1kHz	84	90		dB
	fs=96kHz	80	88		dB
DR (-60dBFS)	fs=44.1kHz, A-weighted	94	100		dB
	fs=96kHz	88	96		dB
S/N	fs=44.1kHz, A-weighted	94	100		dB
	fs=96kHz	88	96		dB
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20	-	ppm/°C
Power Supply Rejection (Note 6)			50	-	dB
DAC Analog Output Characteristics:					
Resolution				24	Bits
S/(N+D) (0dBFS)	fs=44.1kHz	88	94		dB
	fs=96kHz	86	92		dB
	fs=192kHz	-	84		dB
DR (-60dBFS)	fs=44.1kHz, A-weighted	98	104		dB
	fs=96kHz	90	98		dB
	fs=192kHz	-	85		dB
S/N	fs=44.1kHz, A-weighted	98	104		dB
	fs=96kHz	90	98		dB
	fs=192kHz	-	85		dB
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20	-	ppm/°C
Output Voltage (Note 7)		2.8	3.0	3.2	Vpp
Load Resistance		5			kΩ
Load Capacitance				25	pF
Power Supply Rejection (Note 6)			50	-	dB

Note: 5. Full scale (0dB) of the input voltage at IPGA = 0dB.
Note: 6. PSR is applied to AVDD, DVDD, PVDD and TVDD with 1kHz, 50mVpp.VREF pin is held a constant voltage.
Note: 7. This voltage is proportional to VREF. Vout = 0.6 x VREF.

Parameter		min	typ	max	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN = "H")					
AVDD			23	35	mA
PVDD	(fs=44.1kHz)		12	18	mA
DVDD+TVDD	(fs=44.1kHz)		24	36	mA
	(fs=96kHz)		36	54	mA
Power-down mode (PDN = "L")	(Note 8)				
AVDD			10	100	μA
PVDD			10	100	μA
DVDD+TVDD			10	100	μA

Note: 8. All digital input pins are held DVDD or DVSS.

S/PDIF RECEIVER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=PVDD=4.75 ~ 5.25V; TVDD=2.7 ~ 5.25V)

Parameter	Symbol	min	typ	Max	Unit
Input Resistance	Zin		10		kΩ
Input Voltage	VTH	200			mVpp
Input Hysteresis	VHY	-	50		mV
Input Sample Frequency	fs	32	-	192	kHz

FILTER CHARACTERISTICS

(Ta=−10 ~ 70°C; AVDD=DVDD=PVDD=4.75 ~ 5.25V; TVDD=2.7 ~ 5.25V; fs=44.1kHz; DEM=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 9)	±0.005dB	PB	0		19.76	kHz
	-0.02dB		-	20.02	-	kHz
	-0.06dB		-	20.20	-	kHz
	-6.0dB		-	22.05	-	kHz
Stopband		SB	24.34			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 10)		GD		31		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 9)	-3dB	FR		0.9		Hz
	-0.5dB			2.7		Hz
	-0.1dB			6.0		Hz
DAC Digital Filter:						
Passband (Note 9)	±0.01dB	PB	0		20.0	kHz
	-6.0dB		-	22.05	-	kHz
Stopband		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	75			dB
Group Delay (Note 10)		GD		30		1/fs
DAC Digital Filter + SCF + SMF:						
Frequency Response:		FR				
0 ~ 20.0kHz				−0.1		dB
~ 40kHz (Note 11)				−0.2		dB
~ 80kHz (Note 12)				−1.0		dB

Note: 9. The passband and stopband frequencies scale with fs. For example, 20.02kHz at −0.02dB is 0.454 x fs.

Note: 10. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.
For DAC, this time is from setting the 24bit data of both channels on DAC input register to the output of an analog signal.

Note: 11. fs = 96kHz.

Note: 12. fs = 192kHz.

DC CHARACTERISTICS

(Ta=−10 ~ 70°C; AVDD=DVDD=PVDD=4.75 ~ 5.25V; TVDD=2.7 ~ 5.25V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage					
(Except XTI pin)	VIH	2.2	-	-	V
(XTI pin)	VIH	70%DVDD	-	-	V
Low-Level Input Voltage					
(Except XTI pin)	VIL	-	-	0.8	V
(XTI pin)	VIL	-	-	30%DVDD	V
Input Voltage at AC Coupling (XTI pin, Note 13)	VAC	40%DVDD	-	-	Vpp
High-Level Output Voltage					
(Except TX1-3, DZF pins : Iout=−400μA)	VOH	TVDD-0.5	-	-	V
(TX1-3 pin : Iout=−400μA)	VOH	DVDD-0.5	-	-	V
(DZF pin : Iout=−400μA)	VOH	AVDD-0.5	-	-	V
Low-Level Output Voltage (Iout=400μA)	VOL	-	-	0.5	V
TX Output Voltage Level (Note 14)	VOH	0.4	0.5	0.6	V
Input Leakage Current	Iin	-	-	±10	μA

Note: 13. In case of connecting capacitance to XTI pin. (Refer to Figure 3)
Note: 14. Refer to Figure 7.

SWITCHING CHARACTERISTICS

(Ta=−10 ~ 70°C; AVDD=DVDD=PVDD=4.75 ~ 5.25V, TVDD=2.7 ~ 5.25V; C_L=20pF)

Parameter			Symbol	min	typ	max	Unit
Master Clock Timing							
	Crystal Resonator	Frequency		11.2896		24.576	MHz
	External Clock	Frequency	fCLK	11.2896		36.864	MHz
		Pulse Width Low	tCLKL	0.4/fCLK			ns
		Pulse Width High	tCLKH	0.4/fCLK			ns
MCKO1 Output		Frequency	fMCK	11.2896		24.576	MHz
		Duty Cycle (Note 15)	dMCK	40	50	60	%
MCKO2 Output		Frequency	fMCK	5.6448		18.432	MHz
		Duty Cycle	dMCK	40	50	60	%
PLL Clock Recover Frequency			fPLL	32		192	kHz
LRCK Frequency							
Normal Speed Mode (DFS0="0", DFS1="0")			fsn	32		48	kHz
Double Speed Mode (DFS0="1", DFS1="0")			fsd	88.2		96	kHz
Quad Speed Mode (DFS0="0", DFS1="1")			fsq	176.4		192	kHz
	Duty Cycle	Slave mode		45		55	%
		Master mode			50		%
Audio Interface Timing							
	Slave mode						
	BICK Period		tBCK	81			ns
	BICK Pulse Width Low		tBCKL	33			ns
	Pulse Width High		tBCKH	33			ns
	LRCK Edge to BICK "↑" (Note 16)		tLRB	20			ns
	BICK "↑" to LRCK Edge (Note 16)		tBLR	20			ns
	LRCK to SDTO (MSB) (Except I^2S mode)		tLRS			20	ns
	BICK "↓" to SDTO		tBSD			20	ns
	SDTI Hold Time		tSDH	20			ns
	SDTI Setup Time		tSDS	20			ns
	Master mode						
	BICK Frequency		fBCK		64fs		Hz
	BICK Duty		dBCK		50		%
	BICK "↓" to LRCK		tMBLR	−20		20	ns
	BICK "↓" to SDTO		tBSD	−20		20	ns
	SDTI Hold Time		tSDH	20			ns
	SDTI Setup Time		tSDS	20			ns

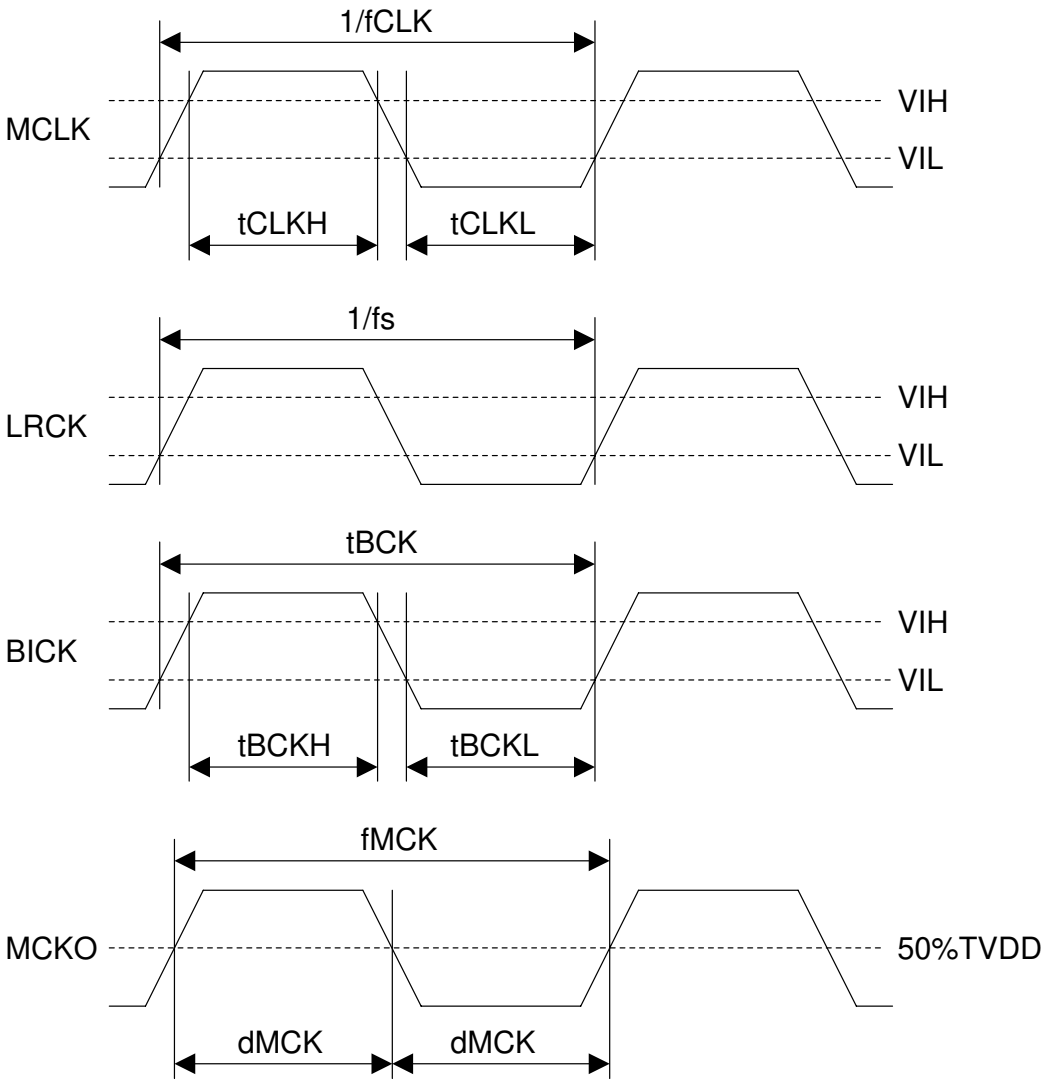
Note: 15. Duty cycle is not guaranteed when using the external clock input.

Note: 16. BICK rising edge must not occur at the same time as LRCK edge.

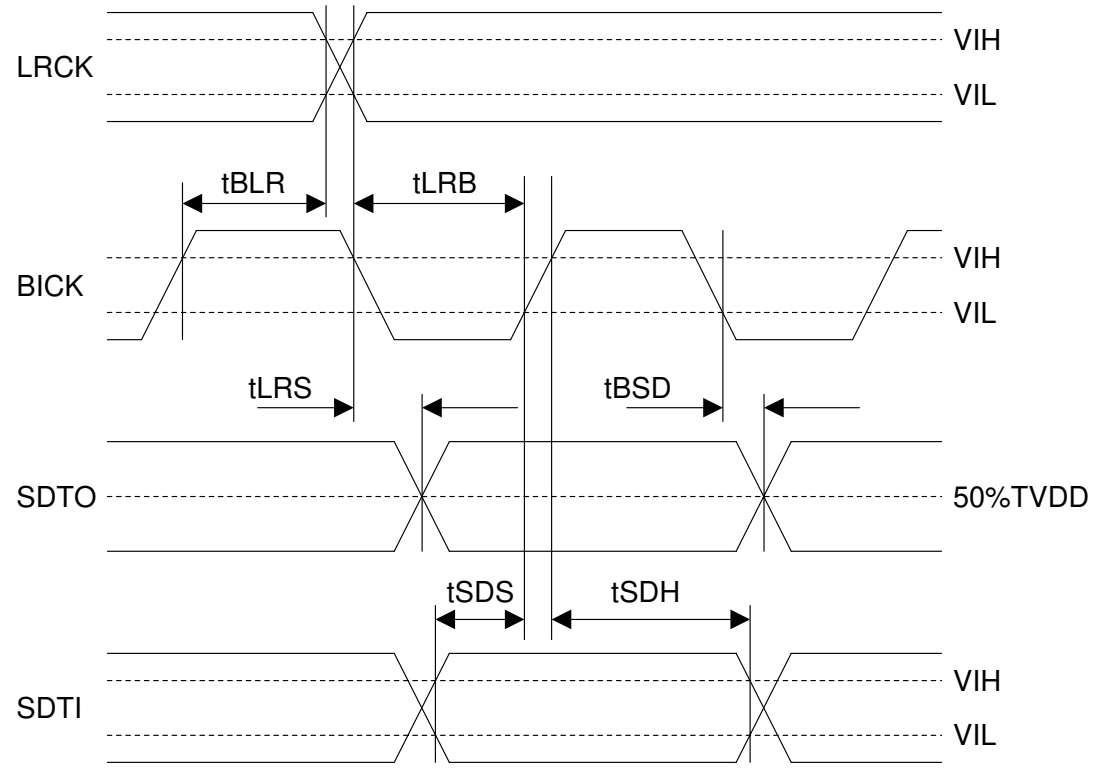
Parameter	Symbol	min	typ	max	Unit
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
CDTO Delay	tDCD			45	ns
CSN "↑" to CDTO Hi-Z	tCCZ			70	ns
Reset Timing					
PDN Pulse Width (Note 17)	tPD	150			ns
RSTADN "↑" to SDTO valid (Note 18)	tPDV		516		1/fs

Note: 17. The AK4584 can be reset by bringing PDN pin = "L".
Note: 18. This cycle is the number of LRCK rising edges from the RSTADN bit.

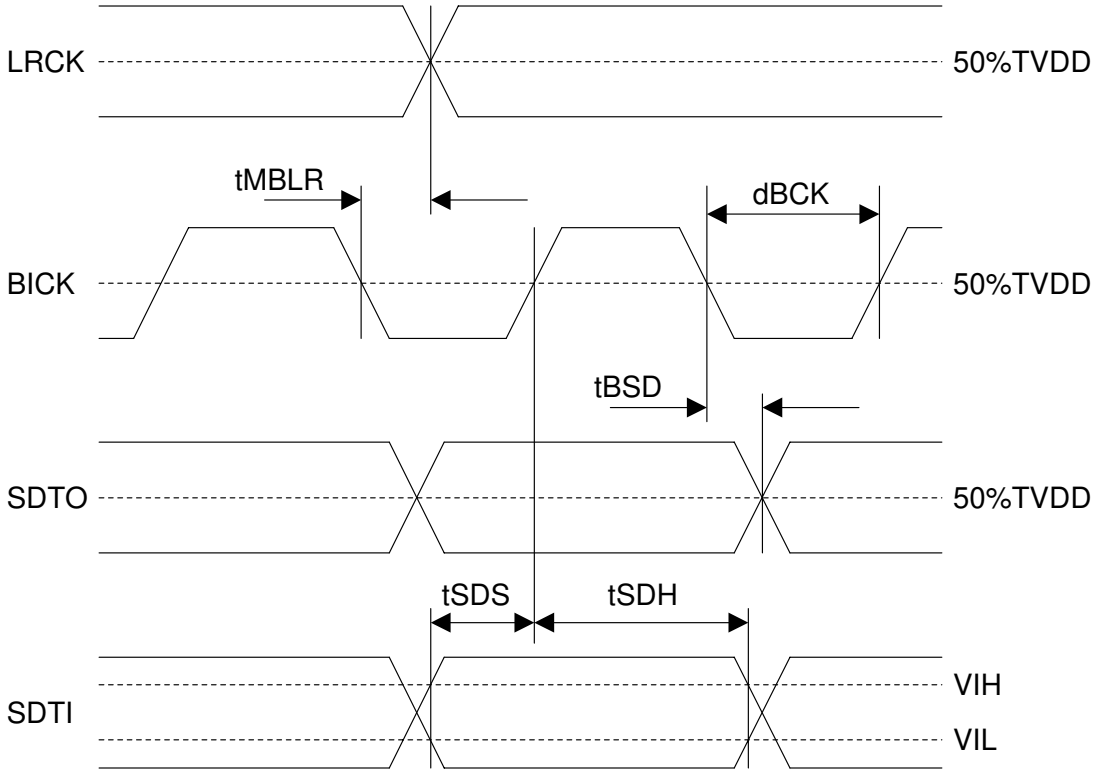
■ **Timing Diagram**



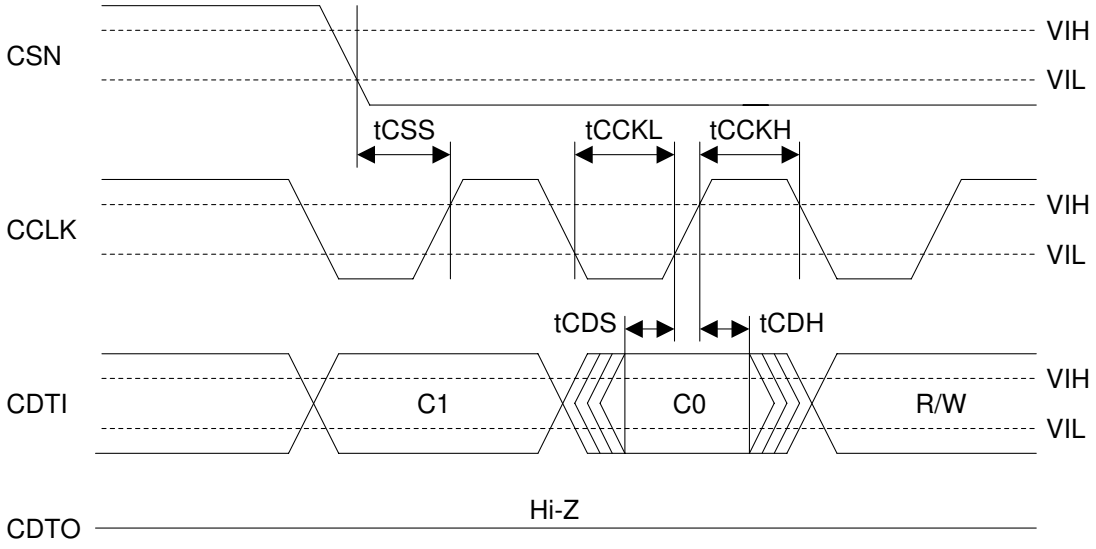
Clock Timing



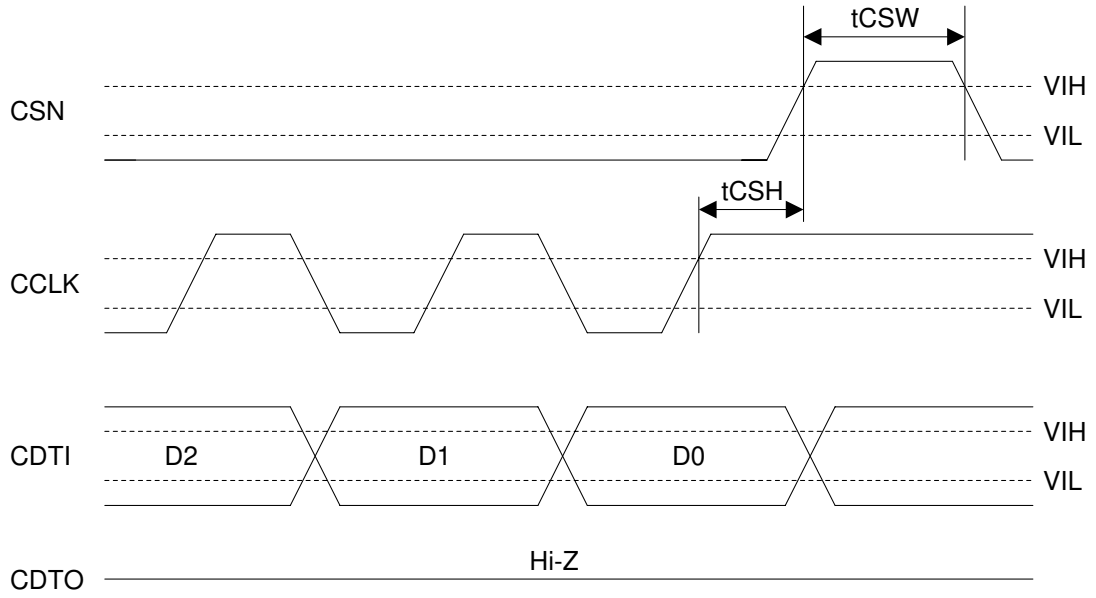
Audio Interface Timing (Slave mode)



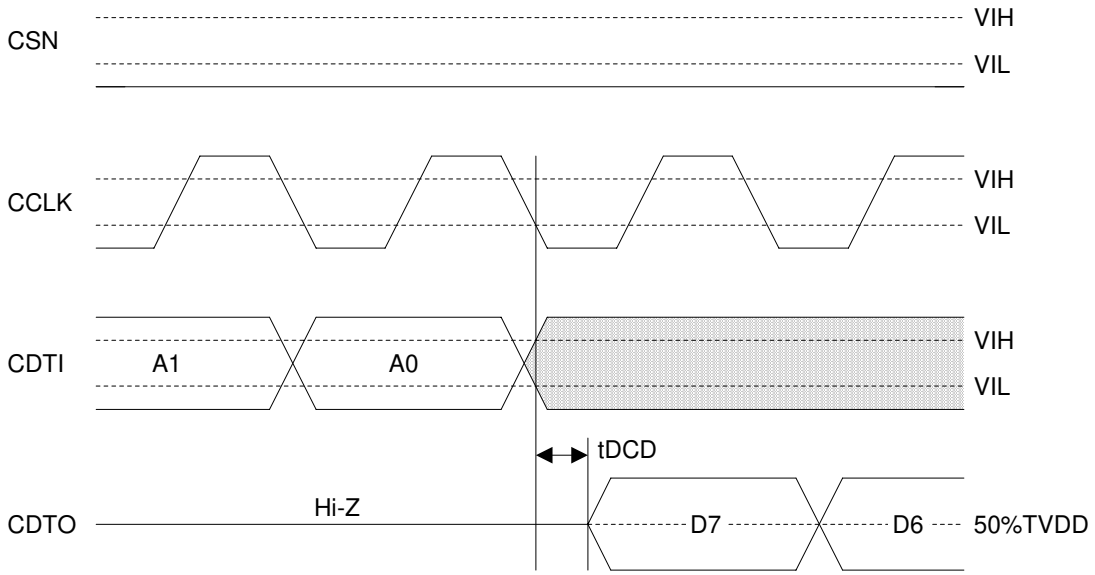
Audio Interface Timing (Master mode)



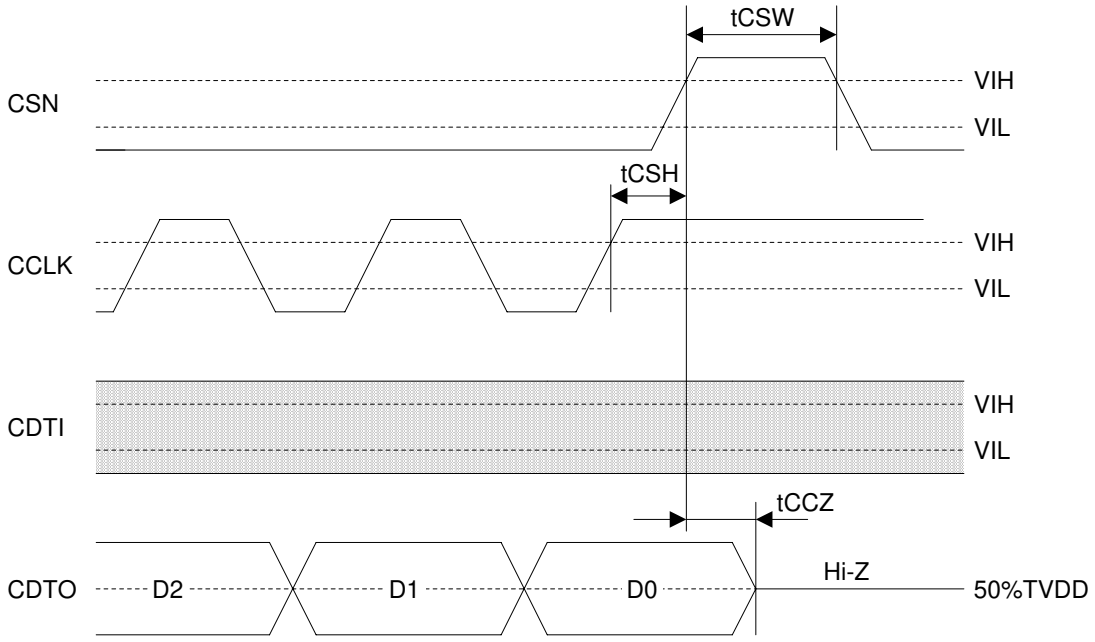
WRITE/READ Command Input Timing



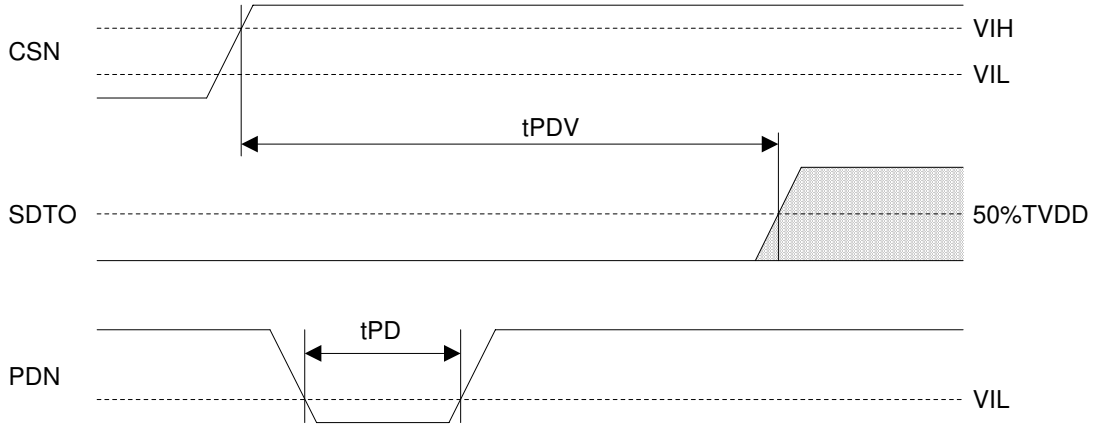
WRITE Data Input Timing



READ Data Output Timing 1



READ Data Output Timing 2



Power Down & Reset Timing

OPERATION OVERVIEW

■ Internal Signal Path

The input source of the DAC and SDTO can be switched between the outputs of the ADC, SDTI or the DIR. The input source of the DIT can be switched between the outputs of ADC or SDTI. There is also a through/bypass path from the DIR to the DIT that can be also selected. The Switch Names (DAC1-0 etc) in Figure 1 correspond to the register bits that control the switch function. Refer to "Register Definitions" (Address 08H).

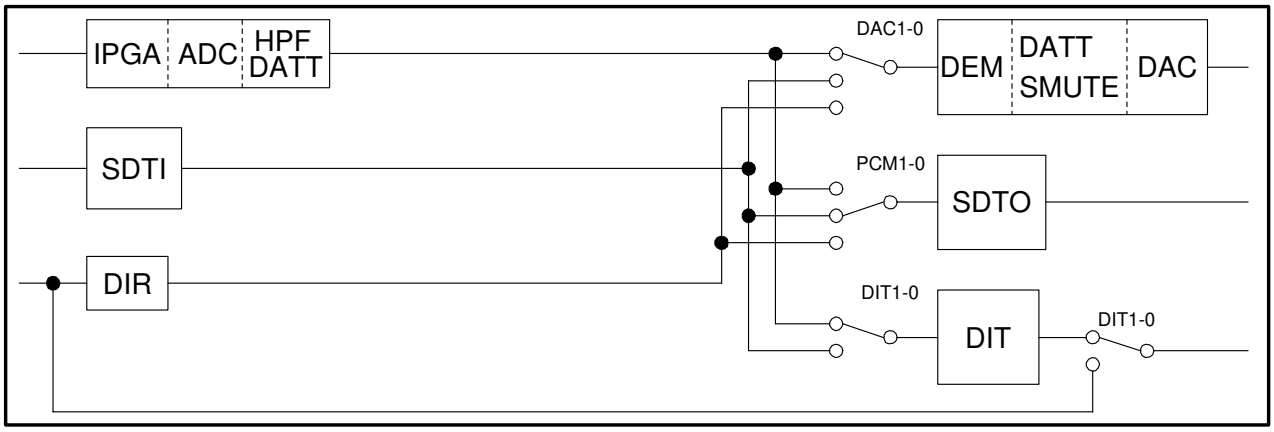


Figure 1. Connection between Input Sources & Output Sources

■ Clock Operation Mode

The CM1-0 bits determine the clock source of the AK4584; either PLL or X'tal (including external clock source, Table 1). In mode 2, the clock source is switched automatically from PLL to X'tal when the PLL loses lock. In mode 3, the clock source is fixed to the external X'tal input, however the PLL is also operating enabling the monitoring of recovered data such as C bits. For mode 2 and mode 3, the frequency of the X'tal should be different from that of the recovered frequency from PLL. When XTL1-0 bits are "11", the X'tal oscillator is stopped in mode 0. The default values are "01" for CM1-0 bits.

Since the signal path is not changed automatically when changing the CM1-0 bits, the output source should be selected by changing register 08H.

Mode	CM1	CM0	UNLOCK	PLL	X'tal	Clock Source	
0	0	0	-	ON	*	PLL	
1	0	1	-	OFF	ON	X'tal	Default
2	1	0	0	ON	ON	PLL	
			1	ON	ON	X'tal	
3	1	1	-	ON	ON	X'tal	

ON: Oscillation (Power-up), OFF: STOP (Power-down)
* : OFF at XTALE pin = "L" and XTL1-0 bits = "11", ON at others
Table 1. Clock Operation Mode Select

■ Master Clock Output

The AK4584 has two clock outputs, MCKO1 and MCKO2. These clocks are derived from either the recovered clock or the X'tal oscillator. In PLL mode, the master clock output frequencies (MCKO1, MCKO2) are set by OCKS1-0 bits as shown in Table 2. In the X'tal mode or external clock mode, the frequency of MCKO1 is the same as the X'tal or external clock. MCKO2 outputs a half frequency of MCKO1 (Table 3). MCKO1 output can be disabled by the DMCK pin. MCKO1 output is "L" (Disable) when the DMCK pin = "H", MCKO1 output is normal output when the DMCK pin = "L". In PLL mode, mode 0 does not support 96kHz. The default values of OCKS1-0 bits are "01"

Mode	OCKS1	OCKS0	MCKO1	MCKO2	fs	
0	0	0	512fs	256fs	~ 48kHz	
1	0	1	256fs	128fs	~ 96kHz	Default
2	1	0	128fs	64fs	~ 192kHz	
3	1	1	64fs	32fs	~ 192kHz	

Table 2. Master Clock Output Frequency Select (PLL Mode)

X'tal	MCKO1	MCKO2
11.2896MHz	11.2896MHz	5.6448MHz
12.288MHz	12.288MHz	6.144MHz
24.576MHZ	24.576MHz	12.288MHz

Table 3. Master Clock Output Frequency Select (X'tal Mode)

Table 4 is a connection example when using AK5394 and AK4394 in slave mode.

	AK5394	AK4394
Clock Output	MCKO2	MCKO1
Normal Speed	256fs	512fs
Double Speed	128fs	256fs
Quad Speed	64fs	128fs

Table 4. Clock Select for AK5394 & AK4394

■ System Clock

The master clock (MCLK) is derived from either a X'tal oscillator or the recovered clock from the AK4584's PLL. MCLK frequency is set by ICKS1-0 bits (Table 5) for X'tal mode and external clock mode. The sampling speed (normal, double or quad speed modes) is selected by DFS1-0 bits (Table 6). The ADC is powered down during quad speed mode.

When using a X'tal oscillator, external loading capacitors between XTI/XTO pins and DVSS are required. An external clock can be input to the XTI pin with the XTO pin left floating. The input can accept both CMOS and AC coupled clock sources with 40%DVDD.

In slave mode, the LRCK clock input must be synchronized with MCLK, however the phase is not critical. All external clocks (MCLK, BICK and LRCK) must be present unless PDN pin = "L" or all parts are powered down by control register, otherwise excessive current may be produced by the internal dynamic logic. In master mode, the master clock (MCLK) must be provided by a X'tal oscillator, external clock or internal PLL unless PDN pin = "L".

			MCLK			
Mode	ICKS1	ICKS0	Normal (DFS1-0 = "00")	Double (DFS1-0 = "01")	Quad (DFS1-0 = "10")	
0	0	0	256fs	N/A	N/A	Default
1	0	1	384s	N/A	N/A	
2	1	0	512fs	256fs	128fs	
3	1	1	768fs	384fs	192fs	

Table 5. Master Clock Input Frequency Select (X'tal Mode)

DFS1	DFS0	Sampling Rate	
0	0	Normal Speed	Default
0	1	Double Speed	
1	0	Quad Speed	
1	1	N/A	

Table 6. Sampling Speed

MCLK Normal		MCLK Double		MCLK Quad	
	fs=44.1kHz		fs=88.2kHz		fs=176.4kHz
256fs	11.2896MHz	128fs	N/A	64fs	N/A
384fs	16.9344MHz	192fs	N/A	96fs	N/A
512fs	22.5792MHz	256fs	22.5792MHz	128fs	22.5792MHz
768fs	33.8688MHz	384fs	33.8688MHz	192fs	33.8688MHz

MCLK Normal		MCLK Double		MCLK Quad	
	fs=48kHz		fs=96kHz		fs=192kHz
256fs	12.288MHz	128fs	N/A	64fs	N/A
384fs	18.432MHz	192fs	N/A	96fs	N/A
512fs	24.576MHz	256fs	24.576MHz	128fs	24.576MHz
768fs	36.864MHz	384fs	36.864MHz	192fs	36.864MHz

Table 7. Master Clock Frequencies example

* X'tal mode supports from 11.2896MHz to 24.576MHz.
* Frequencies over 24.576MHz are supported in external clock mode only.

■ Clock Source

(1) Using X'tal

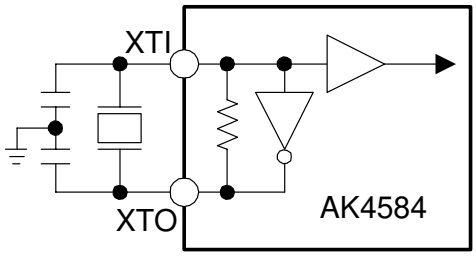


Figure 2. X'tal mode
- Note: External capacitance depends on the crystal oscillator (Typ. 10-40pF)

(2) Using external clock

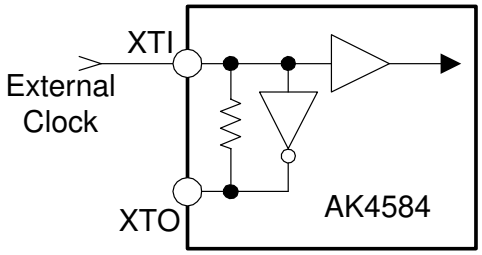


Figure 3. (a) External Clock mode
(Input : CMOS Level)

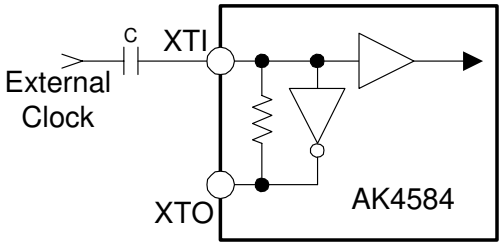


Figure 3. (b) External Clock Mode
(Input : ≥ 40%DVDD)

- Note: Input clock must not exceed DVDD.

(3) Clock Operation Mode 0

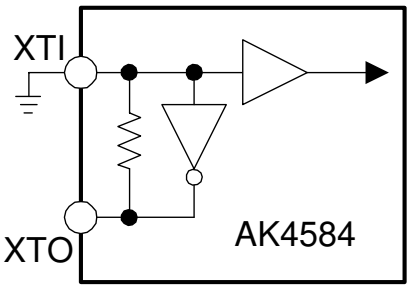


Figure 4. Off mode

■ 192kHz Clock Recovery

The on chip low jitter PLL has a wide lock range from 32kHz to 192kHz and a lock time of less than 20ms. The AK4584 also has a sampling frequency detect function that works by performing either a clock comparison against the X'tal oscillator or by using the channel status. The AK4584 detects the following sampling frequencies : 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz. The PLL loses lock when the incoming sync interval is incorrect.

■ Biphase Input

Four receiver inputs (RX1-4 pins) are available. Each input includes an unbalanced input amplifier and can accept input signals of 200mV or more.

IPS1	IPS0	Input Data	
0	0	RX1	Default
0	1	RX2	
1	0	RX3	
1	1	RX4	

Table 8. Recovery Data Select

■ Biphase Output

The AK4584 can output the through data from the digital receiver inputs (RX1-4) to the TX1/2 pins. The TX3 pin can output transmitter data (SDTI data, A/D converted data and through output from the DIR). The OPS1-0 bits can select the source of the output from the TX1-2 pins and the DIT1-0 bits can select the source of the TX3 pin.

The first 5 bytes of C-bit (Channel Status) can be controlled by CT39-CT0 bits in the control registers. When CT0 bit = "0" (consumer mode), bits20-23 (Audio channel) cannot be controlled directly. When the TCH bit is "1", the AK4584 outputs "1000" as CT20-23 bits for left channel and outputs "0100" at CT20-23 bits for right channel automatically. When TCH bit is "0", the AK4584 outputs "0000".

The U bit (User Data) output has two formats. When the UDIT bit is "0", the U bit is always "L". When UDIT bit is "1", the recovered U bits are passed through the DIT (DIR-DIT loop mode of U bit). This mode is only available when the PLL is locked. When PLL is unlocked, the U bit is set to "L".

OPS1	OPS0	Output Data	
0	0	RX1	Default
0	1	RX2	
1	0	RX3	
1	1	RX4	

Table 9. Output Data Select for TX1/2

DIT1	DIT0	Input Source	
0	0	ADC	Default
0	1	SDTI	
1	0	DIR	
1	1	N/A	

Table 10. Output Data Select for TX3

Note: When the PLL loses lock, the V bit (Validity) data in the block immediately following loss-of-lock may not be accurate. Disregard this data and use the following data blocks.

■ Biphase signal input/output circuit

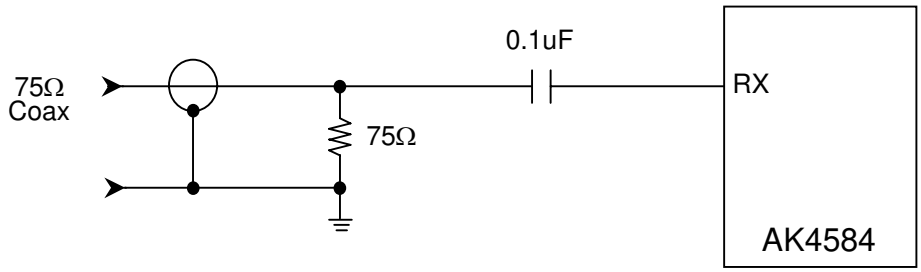


Figure 5. Consumer Input Circuit (Coaxial Input)

Note 1: Coax input only : if a coupling level to this input from the next RX input line pattern exceeds 50mV, an incorrect operation may occur. In this case, it is possible to lower the coupling level by adding this decoupling capacitor.
Note 2: Ground of the RCA connector and terminator should be connected to PVSS of the AK4584 with low impedance on PC board.

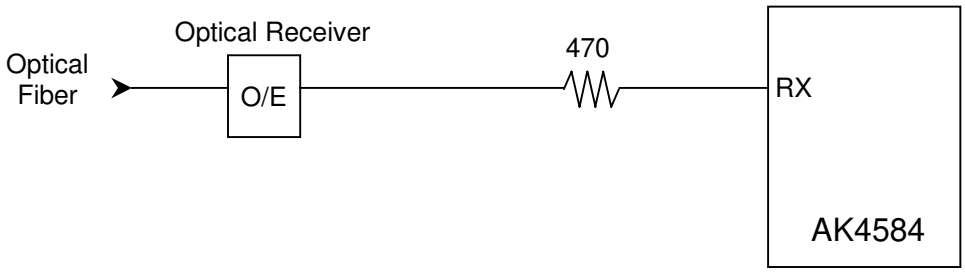


Figure 6. Consumer Input Circuit (Optical Input)

When using coaxial input, the input level of the RX line is small. Care must be taken to reduce, crosstalk among RX input lines by inserting a shield pattern between them.

The AK4584 includes a TX output buffer. The output level is 0.5V, +/−20% using the external resistor network shown below. The T1 in Figure 7 is a 1:1 transformer.

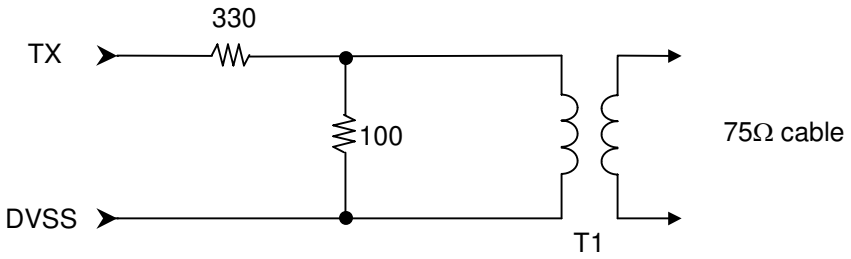


Figure 7. TX External Resistor Network

■ Sampling Frequency and Pre-emphasis Detection

The AK4584 has two methods for detecting the sampling frequency. The sampling frequency is detected by comparing the recovered clock to the X'tal oscillator, and the detected frequency is reported on FS3-0 bits. XTL1-0 bits can select reference X'tal frequency (Table 11). When XTL1-0 bits = "11" and XTALE pin = "L", X'tal oscillator is stopped and the sampling frequency is detected by the channel status sampling frequency information. The detected frequency is reported on FS3-0 bits. The default values of FS3-0 bits are "0000".

XTL1	XTL0	X'tal Frequency	
0	0	11.2896MHz	Default
0	1	12.288MHz	
1	0	24.576MHz	
1	1	Use channel status	

Table 11. Reference X'tal Frequency

Register Output				fs	Except XTL1-0 bits="11"	XTL1-0 bits="11"		
					Clock comparison	Consumer Mode (Note 1)	Pro Mode	
FS3	FS2	FS1	FS0			Byte3 Bit3,2,1,0	Byte0 Bit7,6	Byte4 Bit6,5,4,3
0	0	0	0	44.1kHz	± 3%	0000	01	0000
0	0	0	1	Reserved	-	0001	(others)	0000
0	0	1	0	48kHz	± 3%	0010	10	0000
0	0	1	1	32kHz	± 3%	0011	11	0000
1	0	0	0	88.2kHz	± 3%	(1000)	00	1010
1	0	1	0	96kHz	± 3%	(1010)	00	0010
1	1	0	0	176.4kHz	± 3%	(1100)	00	1011
1	1	1	0	192kHz	± 3%	(1110)	00	0011

Table 12. fs Information

Note 1. In consumer mode, Byte3 Bit3-0 are copied to FS3-0.

The pre-emphasis information is detected and reported on the PEM bit. This information is extracted from channel 1 (default). It can be switched to channel 2 via the CS12 bit in the control register.

PEM bit	Pre-emphasis	Byte0 Bit3,4,5
0	OFF	≠ 0X100
1	ON	0X100

Table 13. PEM in Consumer Mode

PEM bit	Pre-emphasis	Byte0 Bit2,3,4
0	OFF	≠ 100
1	ON	100

Table 14. PEM in Pro Mode