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AK4589
2/8-Channel Audio CODEC with DIR

GENERAL DESCRIPTION

The AK4589 is a single chip CODEC that includes two channels of ADC and eight channels of DAC. The ADC outputs 24bit data and the DAC accepts up to 24bit input data. The ADC has the Enhanced Dual Bit architecture with wide dynamic range. The DAC introduces the new developed Advanced Multi-Bit architecture, and achieves wider dynamic range and lower outband noise. The AK4589 has a dynamic range of 102dB for ADC, 114dB for DAC and is well suited for digital surround for home theater audio. The AK4589 also has the balance volume control corresponding to the Dolby Digital (AC-3) system.

The also has digital audio receiver (DIR) and transmitter (DIT) compatible with 192kHz, 24bits. The DIR has 8-channel input selector and can automatically detect a Non-PCM bit stream. The AK4589 provides a compatibility of hardware and software with the AK4588.

*Dolby Digital (AC-3) is a trademark of Dolby Laboratories.

FEATURES

☐ ADC/DAC part

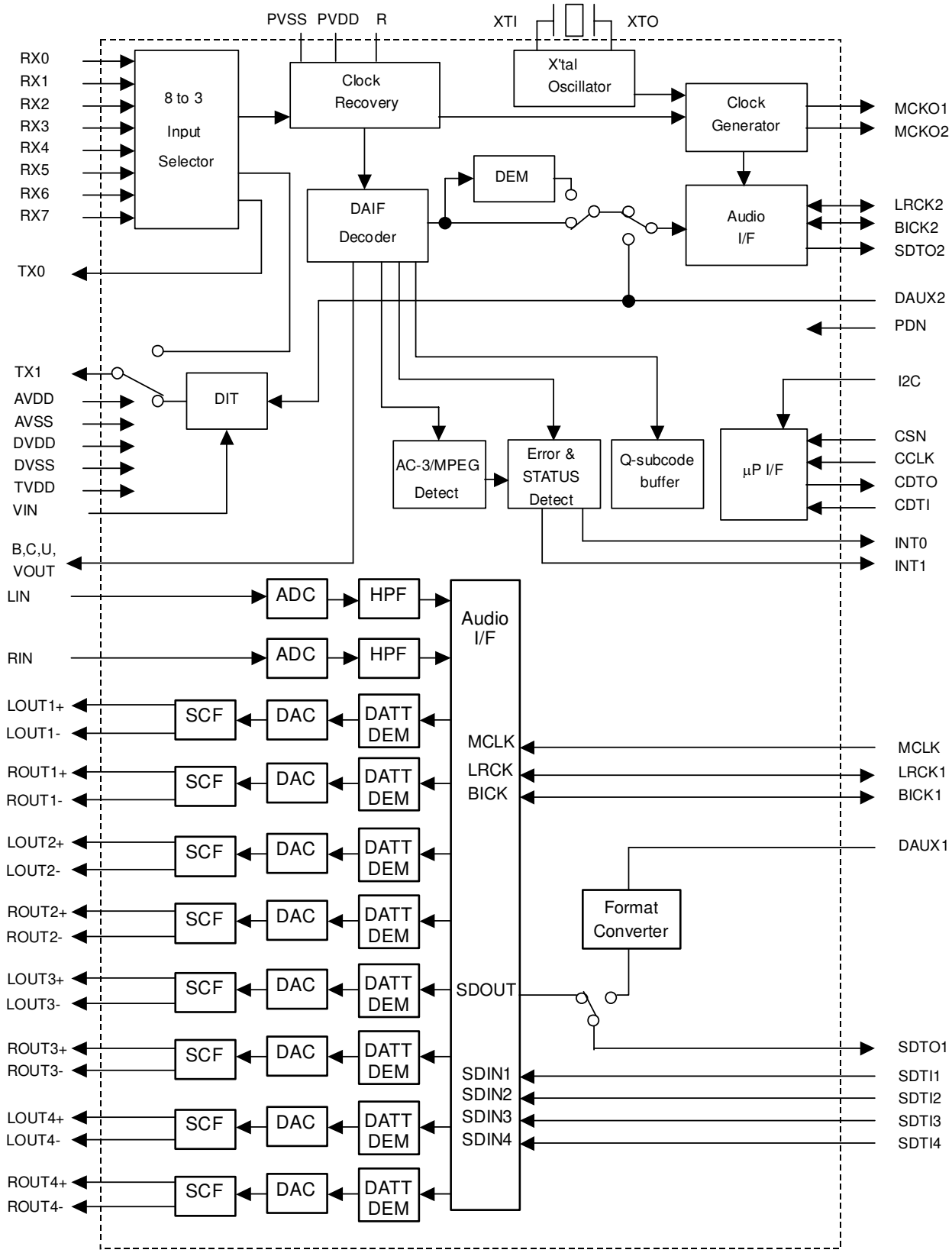
- **2ch 24bit ADC**
  - **64x Oversampling**
  - **Sampling Rate up to 96kHz**
  - **Linear Phase Digital Anti-Alias Filter**
  - **Single-Ended Input**
  - **S/(N+D): 92dB**
  - **Dynamic Range, S/N: 102dB**
  - **Digital HPF for offset cancellation**
  - **Overflow flag**
- **8ch 24bit DAC**
  - **128x Oversampling**
  - **Sampling Rate up to 192kHz**
  - **24bit 8 times Digital Filter**
  - **Differential Outputs**
  - **On-chip Switched-Capacitor Filter**
  - **S/(N+D): 94dB**
  - **Dynamic Range, S/N: 114dB**
  - **Individual channel digital volume with 128 levels and 0.5dB step**
  - **Soft mute**
  - **De-emphasis for 32kHz, 44.1kHz, 48kHz**
  - **Zero Detect Function**
- **High Jitter Tolerance**
- **Extenal Master Clock Input:**
  - **256fs, 384fs, 512fs (fs=32kHz ~ 48kHz)**
  - **128fs, 192fs, 256fs (fs=64kHz ~ 96kHz)**
  - **128fs (fs=120kHz ~ 192kHz)**

☐ DIR/DIT Part

- **AES3, IEC60958, S/PDIF, EIAJ CP1201 Compatible**
- **Low jitter Analog PLL**
- **PLL Lock Range : 32kHz to 192kHz**
- **Clock Source: PLL or X'tal**
- **8-channel Receiver input**
- **2-channel Transmission output (Through output or DIT)**
- **Auxiliary digital input**
- **De-emphasis for 32kHz, 44.1kHz, 48kHz and 96kHz**
- **Detection Functions**
  - **Non-PCM Bit Stream Detection**
  - **DTS-CD Bit Stream Detection**
  - **Sampling Frequency Detection (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, 192kHz)**
  - **Unlock & Parity Error Detection**
  - **Validity Flag Detection**
- **Up to 24bit Audio Data Format**
- **Audio I/F: Master or Slave Mode**
- **40-bit Channel Status Buffer**
- **Burst Preamble bit Pc and Pd Buffer for Non-PCM bit stream**
- **Q-subcode Buffer for CD bit stream**
- **Serial μP I/F**
- **Two Master Clock Outputs: 64fs/128fs/256fs/512fs**

☐ TTL Level Digital I/F
☐ 4-wire Serial and I^2C Bus μP I/F for mode setting
☐ Operating Voltage: 4.75 to 5.25V with 5V tolerance
☐ Power Supply for output buffer: 2.7 to 5.25V
☐ 80pin LQFP Package (0.5mm pitch)
☐ AK4588 compatible w/o analog outputs

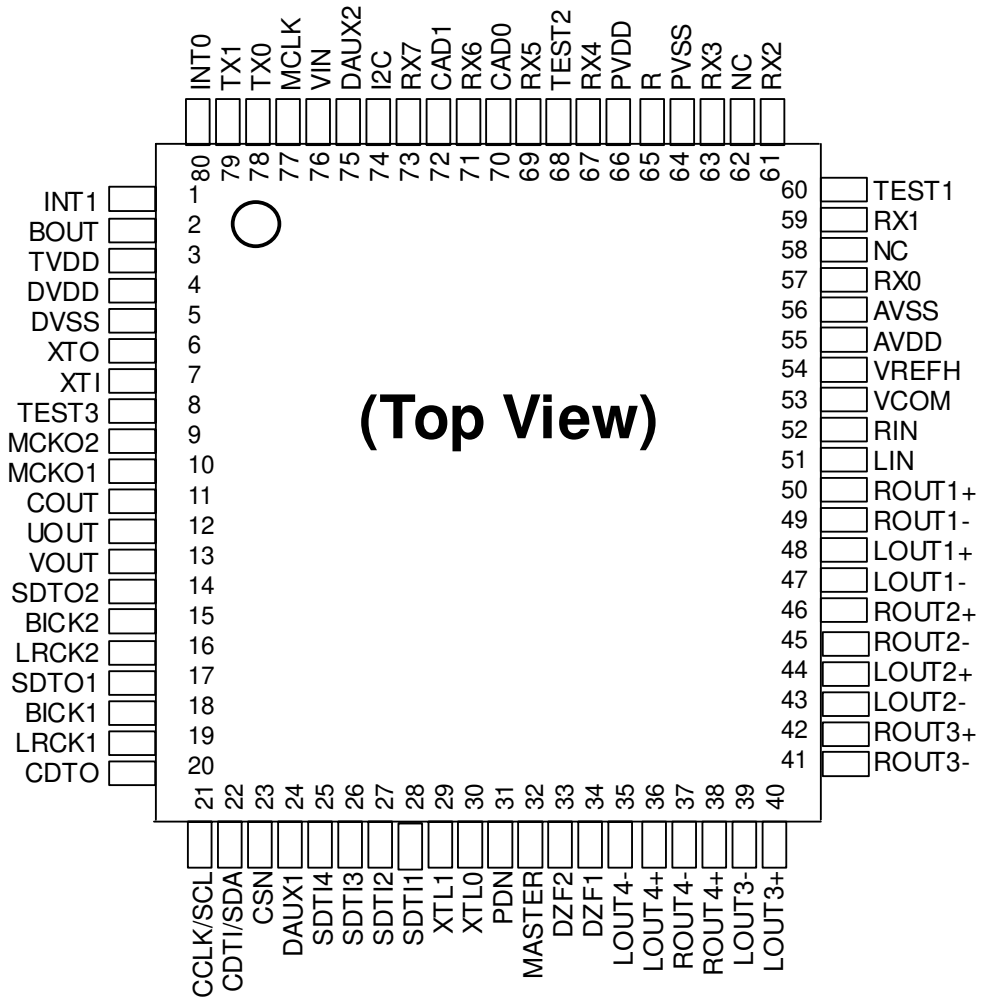
■ Block Diagram



■ Ordering Guide

AK4589VQ	-10 ~ +70°C	80pin LQFP(0.5mm pitch)
AKD4589	Evaluation Board for AK4589	

■ Pin Layout



■ Compatibility with AK4588

Functions	AK4588	AK4589
DAC output	Single end	Differentianl
DAC S/(N+D)	90dB	94dB
DAC S/N	106dB	114dB
DAC Output voltage	Typ 3.0Vpp	Typ ±2.7Vpp
DAC AOUT	AOUT=0.6xVREFH	AOUT=0.54xVREFH
Load Resistance	5k ohm	2k ohm
Frequency Response 80kHz	±1.0	+0/-0.6
Output pin	#35,#37, #39,#41,#43,#45,#47,#49	#35 - #50
Power Supply voltage	Min=4.5V, Max=5.5V	Min=4.75V, Max=5.25V

(*) The AK4589 has two register maps including ADC/DAC part (compatible with the AK4588) and DIR/DIT part (compatible with AK4588). Each register is selected by Chip Address.

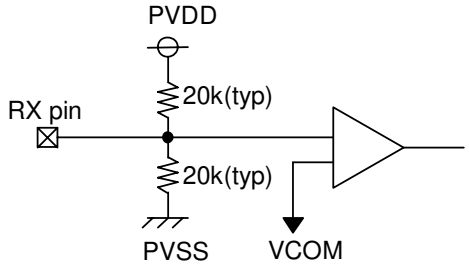
PIN/FUNCTION

No.	Pin Name	I/O	Function
1	INT1	O	Interrupt 1 Pin
2	BOUT	O	Block-Start Output Pin for Receiver Input "H" during first 40 flames.
3	TVDD	-	Output Buffer Power Supply Pin, 2.7V~5.25V
4	DVDD	-	Digital Power Supply Pin, 4.75V~5.25V
5	DVSS	-	Digital Ground Pin
6	XTO	O	X'tal Output Pin
7	XTI	I	X'tal Input Pin
8	TEST3	I	Test 3 Pin This pin should be connected to DVSS.
9	MCKO2	O	Master Clock Output 2 Pin
10	MCKO1	O	Master Clock Output 1 Pin
11	COUT	O	C-bit Output Pin for Receiver Input
12	UOUT	O	U-bit Output Pin for Receiver Input
13	VOUT	O	V-bit Output Pin for Receiver Input
14	SDTO2	O	Audio Serial Data Output Pin (DIR/DIT part)
15	BICK2	I/O	Audio Serial Data Clock Pin (DIR/DIT part)
16	LRCK2	I/O	Channel Clock Pin (DIR/DIT part)
17	SDTO1	O	Audio Serial Data Output Pin (ADC/DAC part)
18	BICK1	I/O	Audio Serial Data Clock Pin (ADC/DAC part)
19	LRCK1	I/O	Input Channel Clock Pin
20	CDTO	O	Control Data Output Pin in Serial Mode, I2C= "L".
21	CCLK	I	Control Data Clock Pin in Serial Mode, I2C= "L"
	SCL	I	Control Data Clock Pin in Serial Mode, I2C= "H"
22	CDTI	I	Control Data Input Pin in Serial Mode, I2C= "L".
	SDA	I/O	Control Data Pin in Serial Mode, I2C= "H".
23	CSN	I	Chip Select Pin in Serial Mode, I2C= "L".
		I	This pin should be connected to DVSS, I2C= "H".
24	DAUX1	I	AUX Audio Serial Data Input Pin (ADC/DAC part)
25	SDTI4	I	DAC4 Audio Serial Data Input Pin
26	SDTI3	I	DAC3 Audio Serial Data Input Pin
27	SDTI2	I	DAC2 Audio Serial Data Input Pin
28	SDTI1	I	DAC1 Audio Serial Data Input Pin
29	XTL1	I	X'tal Frequency Select 0 Pin
30	XTL0	I	X'tal Frequency Select 1 Pin

No.	Pin Name	I/O	Function	
31	PDN	I	Power-Down Mode Pin When "L", the AK4589 is powered-down, all digital output pins go "L", all registers are reset. When CAD1/0 pins are changed, the AK4589 should be reset by PDN pin.	
32	MASTER	I	Master Mode Select Pin "H": Master mode, "L": Slave mode	
33	DZF2	O	Zero Input Detect 2 Pin (Table 13) When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". And when RSTN bit is "0", PWDAN bit is "0", this pin goes to "H". It always is in "L" when P/S pin is "H".	
	OVF	O	Analog Input Overflow Detect Pin This pin goes to "H" if the analog input of Lch or Rch overflows.	
34	DZF1	O	Zero Input Detect 1 Pin (Table 13) When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". And when RSTN bit is "0", PWDAN bit is "0", this pin goes to "H". Output is selected by setting DZFE pin when P/S pin is "H".	
35	LOUT4-	O	DAC4 Lch Negative Analog Output Pin	470pF capacitor should be connected between LOUT4- and LOUT4+.
36	LOUT4+	O	DAC4 Lch Positive Analog Output Pin	
37	ROUT4-	O	DAC4 Rch Negative Analog Output Pin	470pF capacitor should be connected between ROUT4- and ROUT4+.
38	ROUT4+	O	DAC4 Rch Positive Analog Output Pin	
39	LOUT3-	O	DAC3 Lch Negative Analog Output Pin	470pF capacitor should be connected between LOUT3- and LOUT3+.
40	LOUT3+	O	DAC3 Lch Positive Analog Output Pin	
41	ROUT3-	O	DAC3 Rch Negative Analog Output Pin	470pF capacitor should be connected between ROUT3- and ROUT3+.
42	ROUT3+	O	DAC3 Rch Positive Analog Output Pin	
43	LOUT2-	O	DAC2 Lch Negative Analog Output Pin	470pF capacitor should be connected between LOUT2- and LOUT2+.
44	LOUT2+	O	DAC2 Lch Positive Analog Output Pin	
45	ROUT2-	O	DAC2 Rch Negative Analog Output Pin	470pF capacitor should be connected between ROUT2- and ROUT2+.
46	ROUT2+	O	DAC2 Rch Positive Analog Output Pin	
47	LOUT1-	O	DAC1 Lch Negative Analog Output Pin	470pF capacitor should be connected between LOUT1- and LOUT1+.
48	LOUT1+	O	DAC1 Lch Positive Analog Output Pin	
49	ROUT1-	O	DAC1 Rch Negative Analog Output Pin	470pF capacitor should be connected between ROUT1- and ROUT1+.
50	ROUT1+	O	DAC1 Rch Positive Analog Output Pin	
51	LIN	I	Lch Analog Input Pin	
52	RIN	I	Rch Analog Input Pin	
53	VCOM	-	Common Voltage Output Pin 2.2μF capacitor should be connected to AVSS externally.	
54	VREFH	-	Positive Voltage Reference Input Pin, AVDD	

No.	Pin Name	I/O	Function
55	AVDD	-	Analog Power Supply Pin, 4.75V~5.25V
56	AVSS	-	Analog Ground Pin, 0V
57	RX0	I	Receiver Channel 0 Pin (Internal biased pin. Internally biased at PVDD/2)
58	NC	-	No Connect pin No internal bonding. This pin should be connected to PVSS.
59	RX1	I	Receiver Channel 1 Pin (Internal biased pin. Internally biased at PVDD/2)
60	TEST1	I	Test 1 Pin This pin should be connected to PVSS.
61	RX2	I	Receiver Channel 2 Pin (Internal biased pin. Internally biased at PVDD/2)
62	NC	-	No Connect pin No internal bonding. This pin should be connected to PVSS.
63	RX3	I	Receiver Channel 3 Pin (Internal biased pin. Internally biased at PVDD/2)
64	PVSS	-	PLL Ground pin
65	R	-	External Resistor Pin 12kΩ +/-1% resistor should be connected to PVSS externally.
66	PVDD	-	PLL Power supply Pin, 4.75V~5.25V
67	RX4	I	Receiver Channel 4 Pin (Internal biased pin. Internally biased at PVDD/2)
68	TEST2	I	Test 2 Pin This pin should be connected to PVSS.
69	RX5	I	Receiver Channel 5 Pin (Internal biased pin. Internally biased at PVDD/2)
70	CAD0	I	Chip Address 0 Pin (ADC/DAC part)
71	RX6	I	Receiver Channel 6 Pin (Internal biased pin. Internally biased at PVDD/2)
72	CAD1	I	Chip Address 1 Pin (ADC/DAC part)
73	RX7	I	Receiver Channel 7 Pin (Internal biased pin. Internally biased at PVDD/2)
74	I2C	I	Control Mode Select Pin. "L": 4-wire Serial, "H": I^2C Bus
75	DAUX2	I	Auxiliary Audio Data Input Pin (DIR/DIT part)
76	VIN	I	V-bit Input Pin for Transmitter Output
77	MCLK	I	Master Clock Input Pin
78	TX0	O	Transmit Channel (Through Data) Output 0 Pin
79	TX1	O	Transmit Channel Output1 pin When DIT bit = "0", Through Data. When DIT bit = "1", DAUX2 Data.
80	INT0	O	Interrupt 0 Pin

Note: All input pins except internal biased pins and Analog input pins (RX0-7, LIN, RIN) should not be left floating.



Internal biased pin Circuit

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	RX0-7, LOUT1-4, ROUT1-4, LIN, RIN	These pins should be open.
Digital	INT0-1, BOUT, XTO, MCKO1-2, COUT, UOUT, VOUT, SDTO1-2, CDTO, DZF1-2, TX1-0	These pins should be open.
	CSN, DAUX1-2, SDTI1-4, XTL0-1	These pins should be connected to DVSS.
	TEST1-3	These pins should be connected to PVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS, PVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	PLL	PVDD	-0.3	6.0	V
	Output buffer	TVDD	-0.3	6.0	V
	|AVSS-DVSS| (Note 2)	ΔGND1	-	0.3	V
	|AVSS-PVSS| (Note 2)	ΔGND2	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (LIN, RIN pins)		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage					
	Except LRCK1-2, BICK1-2, RX0-7, CAD0-1, TEST1-2 pins	VIND1	-0.3	DVDD+0.3	V
	LRCK1-2, BICK1-2 pins	VIND2	-0.3	TVDD+0.3	V
	RX0-7, CAD0-1, TEST1-2 pins	VIND3	-0.3	PVDD+0.3	V
Ambient Temperature (power applied)		Ta	-10	70	°C
Storage Temperature		Tstg	-65	150	°C

Notes:
1. All voltages with respect to ground.
2. AVSS, DVSS and PVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS, PVSS=0V; Note 3)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 4)	Analog	AVDD	4.75	5.0	5.25	V
	Digital	DVDD	4.75	5.0	AVDD	V
	PLL	PVDD	4.75	5.0	AVDD	V
	Output buffer	TVDD	2.7	5.0	DVDD	V

Notes:
3. All voltages with respect to ground.
4. The power up sequence between AVDD, DVDD, PVDD and TVDD is not critical. To save leak current in power down mode, AVDD, DVDD, PVDD become the same voltage as much as possible.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, PVDD, TVDD=5V; AVSS, DVSS=0V; VREFH=AVDD; fs=48kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at fs=48kHz, 20Hz~40kHz at fs=96kHz; 20Hz~40kHz at fs=192kHz, unless otherwise specified)

Parameter			min	typ	max	Units
ADC Analog Input Characteristics						
Resolution					24	Bits
S/(N+D)	(-0.5dBFS)	fs=48kHz	84	92		dB
		fs=96kHz	-	86		dB
DR	(-60dBFS)	fs=48kHz, A-weighted	94	102		dB
		fs=96kHz	88	96		dB
		fs=96kHz, A-weighted	93	102		dB
S/N	(Note 5)	fs=48kHz, A-weighted	93	102		dB
		fs=96kHz	88	96		dB
		fs=96kHz, A-weighted	93	102		dB
Interchannel Isolation			90	110		dB
DC Accuracy						
Interchannel Gain Mismatch				0.2	0.3	dB
Gain Drift				20	-	ppm/°C
Input Voltage		AIN=0.62xVREFH	2.90	3.10	3.30	Vpp
Input Resistance		fs=48kHz	15	25		kΩ
		fs=96kHz	9	16		kΩ
Power Supply Rejection		(Note 7)		50		dB
DAC Analog Output Characteristics						
Resolution					24	Bits
S/(N+D)		fs=48kHz	86	94		dB
		fs=96kHz	84	92		dB
		fs=192kHz	-	92		dB
DR	(-60dBFS)	fs=48kHz, A-weighted	104	114		dB
		fs=96kHz	98	108		dB
		fs=96kHz, A-weighted	104	114		dB
		fs=192kHz	-	108		dB
		fs=192kHz, A-weighted		114		dB
S/N	(Note 8)	fs=48kHz, A-weighted	104	114		dB
		fs=96kHz	98	108		dB
		fs=96kHz, A-weighted	104	114		dB
		fs=192kHz	-	108		dB
		fs=192kHz, A-weighted	-	114		dB
Interchannel Isolation			90	100		dB
DC Accuracy						
Interchannel Gain Mismatch				0.2	0.5	dB
Gain Drift				20	-	ppm/°C
Output Voltage		AOUT=0.54xVREFH	±2.5	±2.7	±2.9	Vpp
Load Resistance		(AC Load) (Note 6)	2			kΩ
Power Supply Rejection		(Note 7)		50		dB
Power Supplies						
Power Supply Current						
Normal Operation	(PDN = "H")	(Note 9)				
AVDD		fs=48kHz,fs=96kHz		70	98	mA
		fs=192kHz		57	80	mA
PVDD				12	17	mA
DVDD+TVDD		fs=48kHz (Note 10)		44	62	mA
		fs=96kHz		57	80	mA
		fs=192kHz		68	95	mA
Power-down mode (PDN pin = "L")		(Note 11)		0.1	1	mA

Notes:

5. S/N measured by CCIR-ARM is 96dB(@fs=48kHz).
6. For AC-load. 4kΩ for DC-load
7. PSR is applied to AVDD, DVDD, PVDD and TVDD with 1kHz, 50mVpp. VREFH pin is held a constant voltage.
8. S/N measured by CCIR-ARM is 102dB(@fs=48kHz).
9. C_L=20pF, X'tal=24.576MHz, CM1-0="10", CM1-0="10", OCKS1-0="10"@48kHz,"00"@96kHz, "11"@192kHz.
10. TVDD=13mA(typ).
11. In the power-down mode. RX inputs are open and all digital input pins including clock pins (MCLK, BICK, LRCK) are held DVSS.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, PVDD=4.75~5.25V; TVDD=2.7~5.25V; fs=48kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 12)	±0.1dB	PB	0		18.9	kHz
	-0.2dB		-	20.0	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband		SB	28.0			kHz
Passband Ripple		PR			±0.04	dB
Stopband Attenuation		SA	68			dB
Group Delay (Note 13)		GD		16		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 12)	-3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz
DAC Digital Filter:						
Passband (Note 12)	-0.1dB	PB	0		21.8	kHz
	-6.0dB		-	24.0	-	kHz
Stopband		SB	26.2			kHz
Passband Ripple		PR			±0.02	dB
Stopband Attenuation		SA	54			dB
Group Delay (Note 13)		GD		19.2		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 20.0kHz		FR		±0.2		dB
40.0kHz (Note 14)		FR		±0.3		dB
80.0kHz (Note 14)		FR		+0/-0.6		dB

Notes:

12. The passband and stopband frequencies scale with fs.
    For example, 21.8kHz at –0.1dB is 0.454 x fs (DAC). The reference frequency of these responses is 1kHz.
13. The calculating delay time which occurred by digital filtering. This time is from setting the input of analog signal to setting the 24bit data of both channels to the output register for ADC.
    For DAC, this time is from setting the 20/24bit data of both channels on input register to the output of analog signal.
14. 40kHz@fs=96kHz, 80kHz@fs=192kHz

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, PVDD=4.75~5.25V; TVDD=2.7~5.25V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	(Except XTI pin)	VIH	2.2	-	-	V
	(XTI pin)	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	(Except XTI pin)	VIL	-	-	0.8	V
	(XTI pin)	VIL	-	-	30%DVDD	V
Input Voltage at AC Coupling (XTI pin)	(Table 15)	VAC	40%DVDD	-	-	Vpp
High-Level Output Voltage						
(Except TX0-1, DZF pins: Iout=-400μA)		VOH	TVDD-0.4	-	-	V
(TX0-1 pin: Iout=-400μA)		VOH	DVDD-0.4	-	-	V
(DZF pin: Iout=-400μA)		VOH	AVDD-0.4	-	-	V
Low-Level Output Voltage	(Iout=400μA)	VOL	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	μA

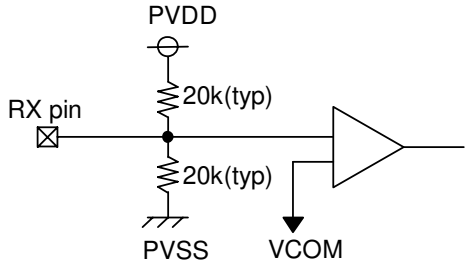
Note:

15. In case of connecting capacitance (0.1μF) to XTI pin.

S/PDIF RECEIVER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, PVDD=4.75~5.25V; TVDD=2.7~5.25V)

Parameter	Symbol	min	typ	max	Units
Input Resistance	Zin		10		kΩ
Input Voltage (internally biased at PVDD/2)	VTH	200			mVpp
Input Hysteresis	VHY	-	50		mV
Input Sample Frequency	fs	32	-	192	kHz



Internal biased pin Circuit

SWITCHING CHARACTERISTICS (ADC/DAC part)

(Ta=25°C; AVDD, DVDD, PVDD=4.75~5.25V; TVDD=2.7~5.25V; C_L=20pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Master Clock						
256fsn, 128fsd:		fCLK	8.192		12.288	MHz
Pulse Width Low		tCLKL	27			ns
Pulse Width High		tCLKH	27			ns
384fsn, 192fsd:		fCLK	12.288		18.432	MHz
Pulse Width Low		tCLKL	20			ns
Pulse Width High		tCLKH	20			ns
512fsn, 256fsd, 128fsq:		fCLK	16.384		24.576	MHz
Pulse Width Low		tCLKL	15			ns
Pulse Width High		tCLKH	15			ns
LRCK1 Timing (Slave Mode)						
Normal mode						
Normal Speed Mode		fsn	32		48	kHz
Double Speed Mode		fsd	64		96	kHz
Quad Speed Mode		fsq	120		192	kHz
Duty Cycle		Duty	45		55	%
TDM 256 mode						
LRCK1 frequency		fsd	32		48	kHz
"H" time		tLRH	1/256fs			ns
"L" time		tLRL	1/256fs			ns
TDM 128 mode						
LRCK1 frequency		fsd	64		96	kHz
"H" time		tLRH	1/128fs			ns
"L" time		tLRL	1/128fs			ns
LRCK1 Timing (Master Mode)						
Normal mode						
Normal Speed Mode		fsn	32		48	kHz
Double Speed Mode		fsd	64		96	kHz
Quad Speed Mode		fsq	120		192	kHz
Duty Cycle		Duty		50		%
TDM 256 mode						
LRCK1 frequency		fsn	32		48	kHz
"H" time	(Note 16)	tLRH		1/8fs		ns
TDM 128 mode						
LRCK1 frequency		fsd	64		96	kHz
"H" time	(Note 16)	tLRH		1/4fs		ns
Power-down & Reset Timing						
PDN Pulse Width	(Note 17)	tPD	150			ns
PDN "↑" to SDTO1 valid	(Note 18)	tPDV		522		1/fs

Notes:

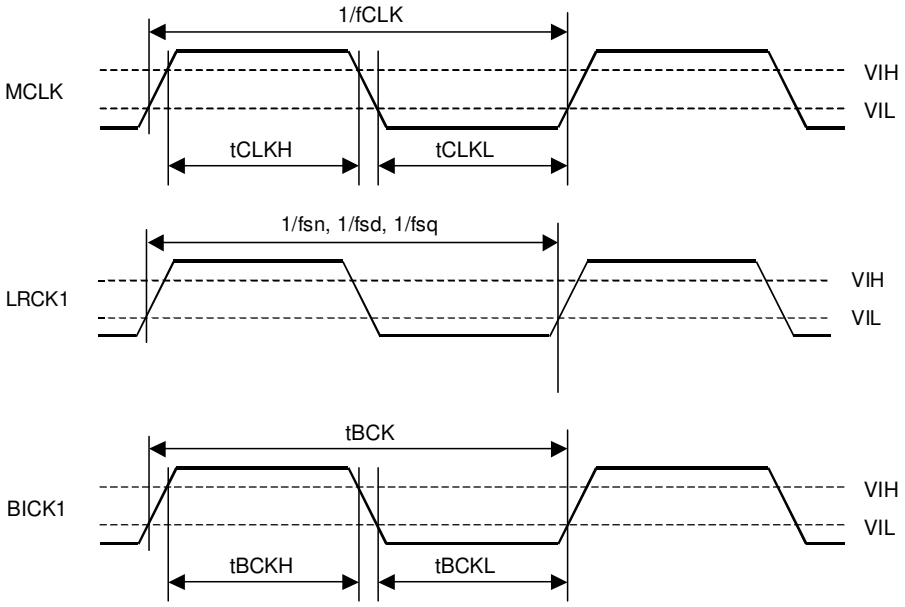
16. "L" time at I^2S format.
17. The AK4589 can be reset by bringing PDN "L" to "H" upon power-up.
18. These cycles are the number of LRCK rising from PDN rising.

Parameter		Symbol	min	typ	max	Units
Audio Interface Timing (Slave Mode)						
Normal mode						
BICK1 Period		tBCK	81			ns
BICK1 Pulse Width Low		tBCKL	32			ns
Pulse Width High		tBCKH	32			ns
LRCK1 Edge to BICK1 "↑"	(Note 19)	tLRB	20			ns
BICK1 "↑" to LRCK1 Edge	(Note 19)	tBLR	20			ns
LRCK1 to SDTO1(MSB)		tLRS			40	ns
BICK1 "↓" to SDTO1		tBSD			40	ns
SDTI1-4,DAUX1 Hold Time		tSDH	20			ns
SDTI1-4,DAUX1 Setup Time		tSDS	20			ns
TDM 256 mode						
BICK1 Period		tBCK	81			ns
BICK1 Pulse Width Low		tBCKL	32			ns
Pulse Width High		tBCKH	32			ns
LRCK1 Edge to BICK1 "↑"	(Note 19)	tLRB	20			ns
BICK1 "↑" to LRCK1 Edge	(Note 19)	tBLR	20			ns
BICK1 "↓" to SDTO1		tBSD			20	ns
SDTI1 Hold Time		tSDH	10			ns
SDTI1 Setup Time		tSDS	10			ns
TDM 128 mode						
BICK1 Period		tBCK	81			ns
BICK1 Pulse Width Low		tBCKL	32			ns
Pulse Width High		tBCKH	32			ns
LRCK1 Edge to BICK1 "↑"	(Note 19)	tLRB	20			ns
BICK1 "↑" to LRCK1 Edge	(Note 19)	tBLR	20			ns
BICK1 "↓" to SDTO1		tBSD			20	ns
SDTI1-2 Hold Time		tSDH	10			ns
SDTI1-2 Setup Time		tSDS	10			ns
Audio Interface Timing (Master Mode)						
Normal mode						
BICK1 Frequency		fBCK		64fs		Hz
BICK1 Duty		dBCK		50		%
BICK1 "↓" to LRCK1 Edge		tMBLR	-20		20	ns
BICK1"↓" to SDTO1		tBSD			40	ns
SDTI1-4,DAUX1 Hold Time		tSDH	20			ns
SDTI1-4,DAUX1 setup Time		tSDS	20			ns
TDM 256 mode						
BICK1 Frequency		fBCK		256fs		Hz
BICK1 Duty	(Note 20)	dBCK		50		%
BICK1 "↓" to LRCK1 Edge		tMBLR	-12		12	ns
BICK1 "↓" to SDTO1		tBSD			20	ns
SDTI1 Hold Time		tSDH	10			ns
SDTI1 Setup Time		tSDS	10			ns
TDM 128 mode						
BICK1 Frequency		fBCK		128fs		Hz
BICK1 Duty	(Note 21)	dBCK		50		%
BICK1 "↓" to LRCK1 Edge		tMBLR	-12		12	ns
BICK1 "↓" to SDTO1		tBSD			20	ns
SDTI1-2 Hold Time		tSDH	10			ns
SDTI1-2 Setup Time		tSDS	10			ns

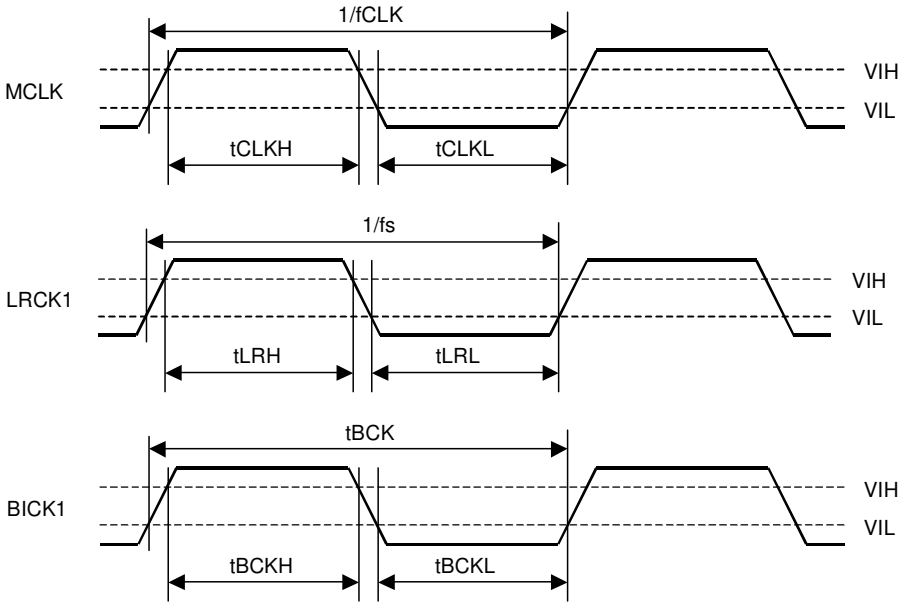
Notes:

19. BICK1 rising edge must not occur at the same time as LRCK1 edge.
20. When MCLK is 512fs, dBCK is guaranteed. When 384fs and 256fs, dBCK can not be guaranteed.
21. When MCLK is 256fs, dBCK is guaranteed. When 128fs, dBCK can not be guaranteed.

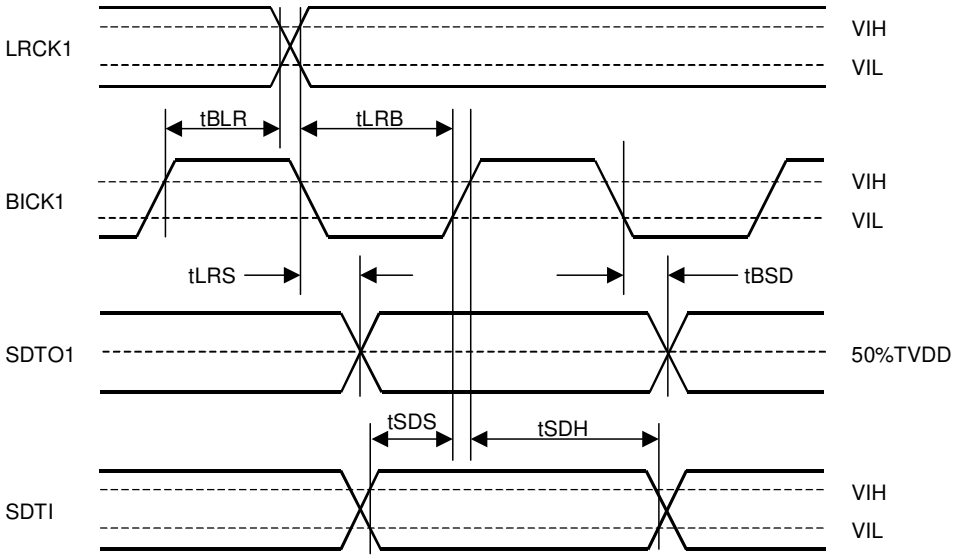
■ **Timing Diagram(ADC/DAC part)**



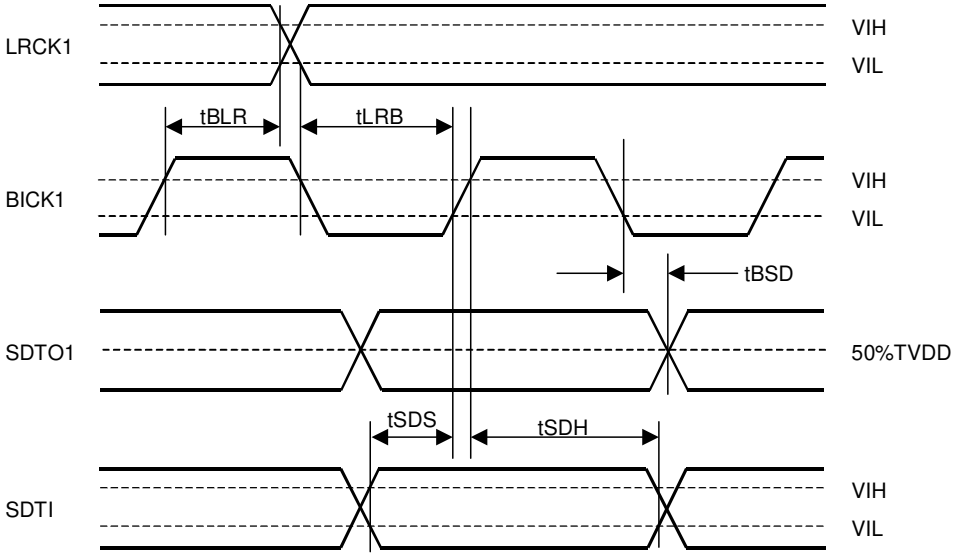
Clock Timing (Normal mode)



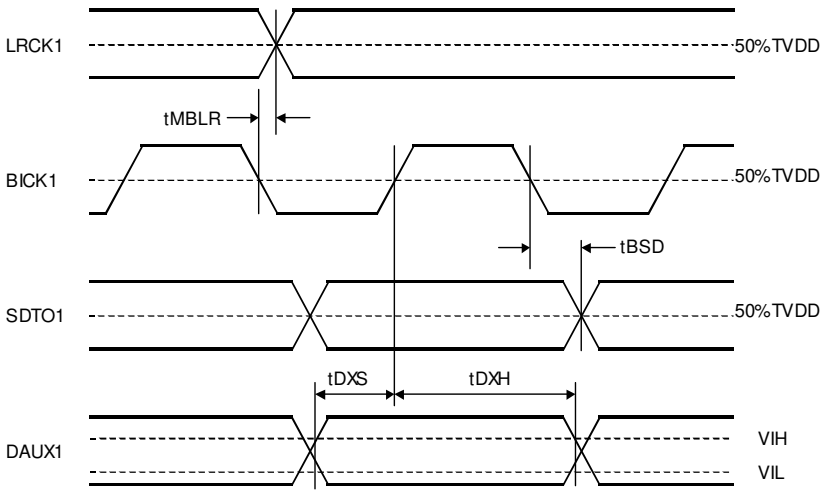
Clock Timing (TDM 256 mode, TDM 128 mode)



Audio Interface Timing (Normal mode)



Audio Interface Timing (TDM 256 mode, TDM 128 mode)



Audio Interface timing (Master Mode)

SWITCHING CHARACTERISTICS (DIR/DIT part)

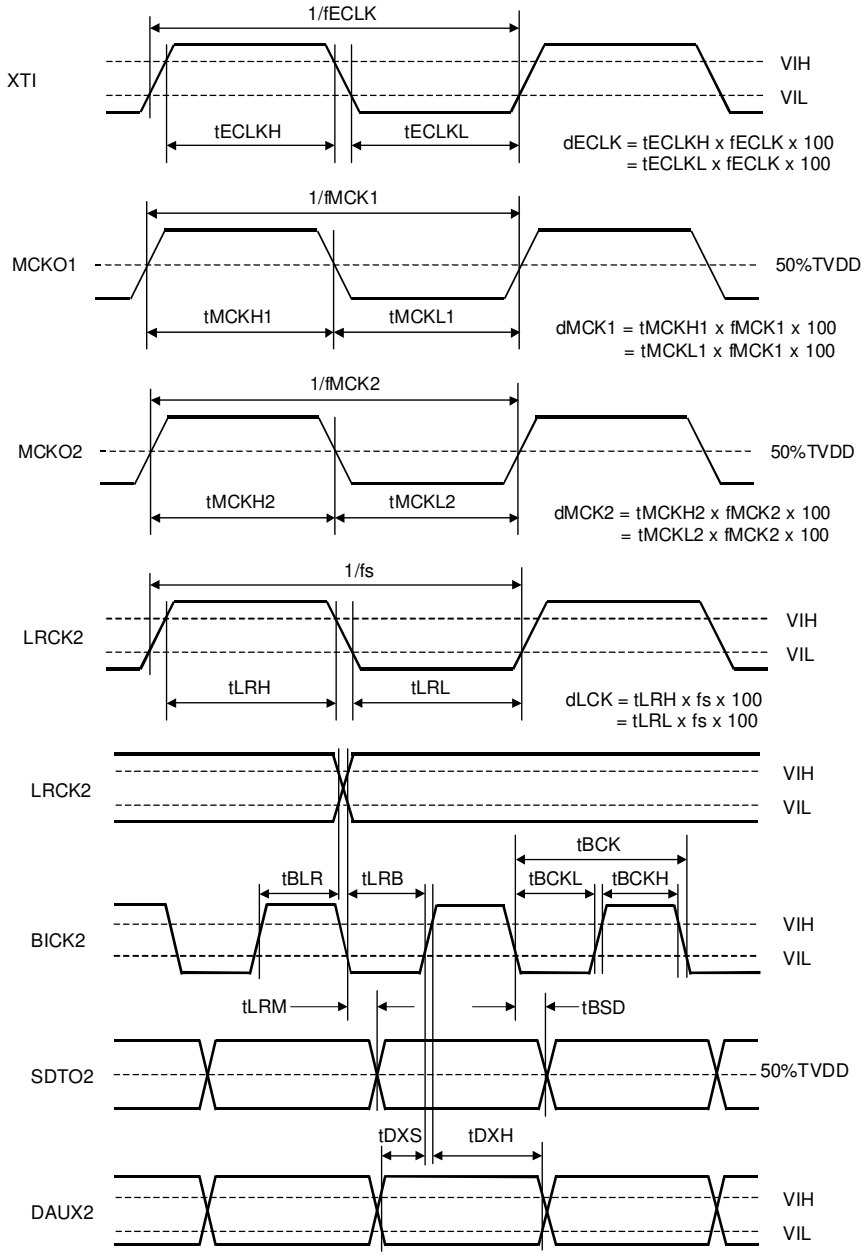
(Ta=25°C; DVDD, AVDD, PVDD4.75~5.25V, TVDD=2.7~5.25V; C_L=20pF)

Parameter			Symbol	min	typ	max	Units
Master Clock Timing							
Crystal Resonator	Frequency		fXTAL	11.2896		24.576	MHz
External Clock	Frequency		fECLK	11.2896		24.576	MHz
	Duty		dECLK	40	50	60	%
MCKO1 Output	Frequency		fMCK1	4.096		24.576	MHz
	Duty		dMCK1	40	50	60	%
MCKO2 Output	Frequency		fMCK2	2.048		24.576	MHz
	Duty		dMCK2	40	50	60	%
PLL Clock Recover Frequency (RX0-7)			fpll	32	-	192	kHz
LRCK2 Frequency			fs	32		192	kHz
Duty Cycle			dLCK	45		55	%
Audio Interface Timing							
Slave Mode							
BICK2 Period			tBCK	80			ns
BICK2 Pulse Width Low			tBCKL	30			ns
Pulse Width High			tBCKH	30			ns
LRCK2 Edge to BICK2 "↑"		(Note 22)	tLRB	20			ns
BICK2 "↑" to LRCK2 Edge		(Note 22)	tBLR	20			ns
LRCK2 to SDTO2 (MSB)			tLRM			30	ns
BICK2 "↓" to SDTO2			tBSD			30	ns
DAUX2 Hold Time			tDXH	20			ns
DAUX2 Setup Time			tDXS	20			ns
Master Mode							
BICK2 Frequency			fBCK		64fs		Hz
BICK2 Duty			dBCK		50		%
BICK2 "↓" to LRCK2			tMBLR	-20		20	ns
BICK2 "↓" to SDTO2			tBSD			15	ns
DAUX2 Hold Time			tDXH	20			ns
DAUX2 Setup Time			tDXS	20			ns

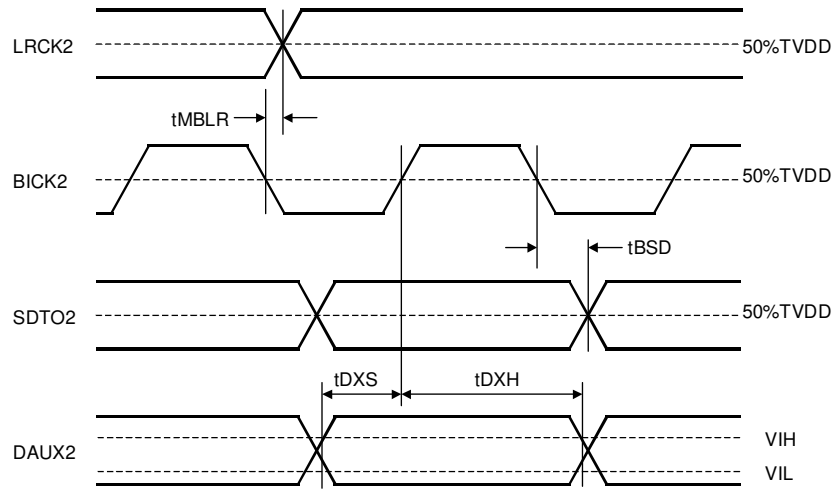
Notes;

22. BICK2 rising edge must not occur at the same time as LRCK2 edge.

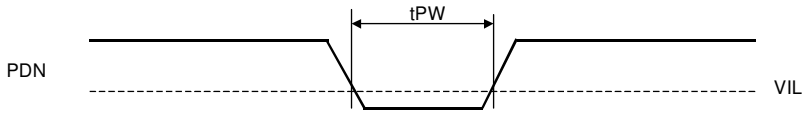
■ Timing Diagram(DIR/DIT part)



Serial Interface Timing (Slave Mode)



Serial Interface Timing (Master Mode)



Power Down & Reset Timing

SWITCHING CHARACTERISTICS (ADC/DAC part and DIR/DIT part)

(Ta=25°C; AVDD, DVDD, PVDD=4.75~5.25V; TVDD=2.7~5.25V; C_L=20pF)

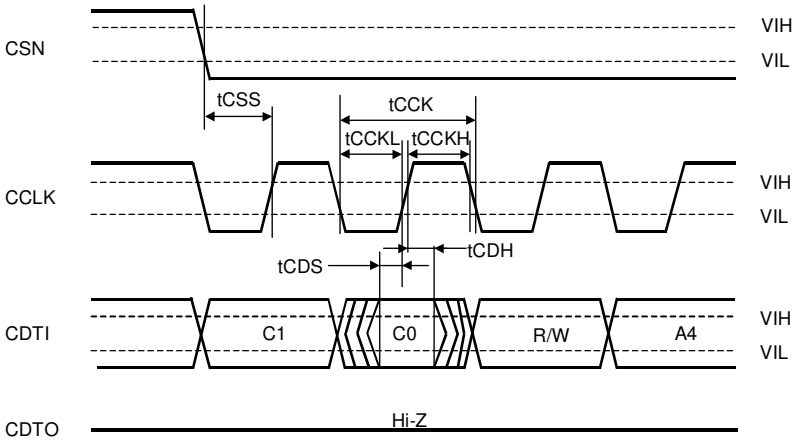
Parameter	Symbol	min	typ	max	Units
Control Interface Timing (4-wire serial mode)					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
CDTO Delay	tDCD			45	ns
CSN "↑" to CDTO Hi-Z	tCCZ			70	ns
Control Interface Timing (I^2C Bus mode)					
SCL Clock Frequency	fSCL	-		100	kHz
Bus Free Time Between Transmissions	tBUF	4.7		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	4.0		-	µs
Clock Low Time	tLOW	4.7		-	µs
Clock High Time	tHIGH	4.0		-	µs
Setup Time for Repeated Start Condition	tSU:STA	4.7		-	µs
SDA Hold Time from SCL Falling (Note 23)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.25		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	4.0		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF

Notes:

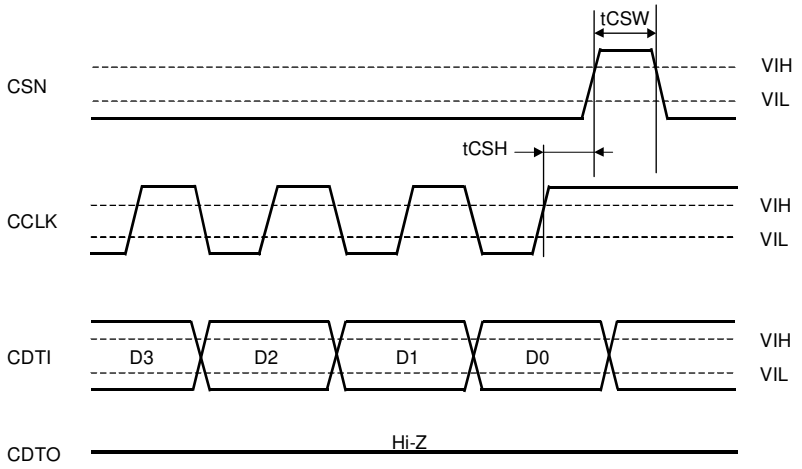
23. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
24. I^2C is a registered trademark of Philips Semiconductors.

Purchase of Asahi Kasei Microsystems Co., Ltd I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conform to the I^2C specifications defined by Philips.

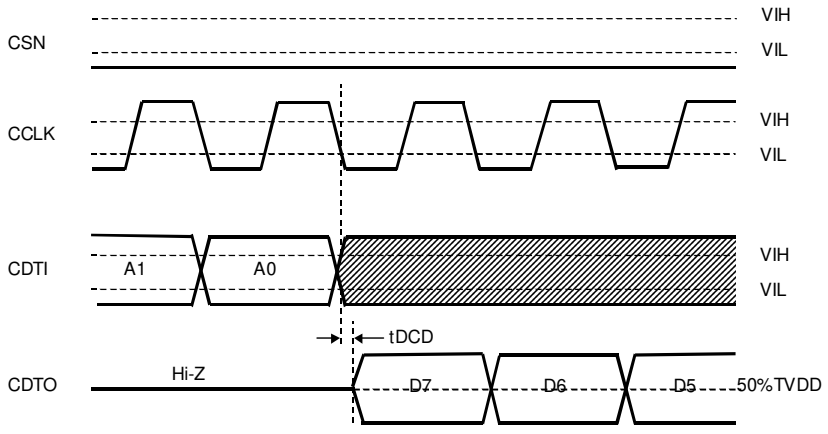
■ **Timing Diagram (ADC/DAC part and DIR/DIT part)**



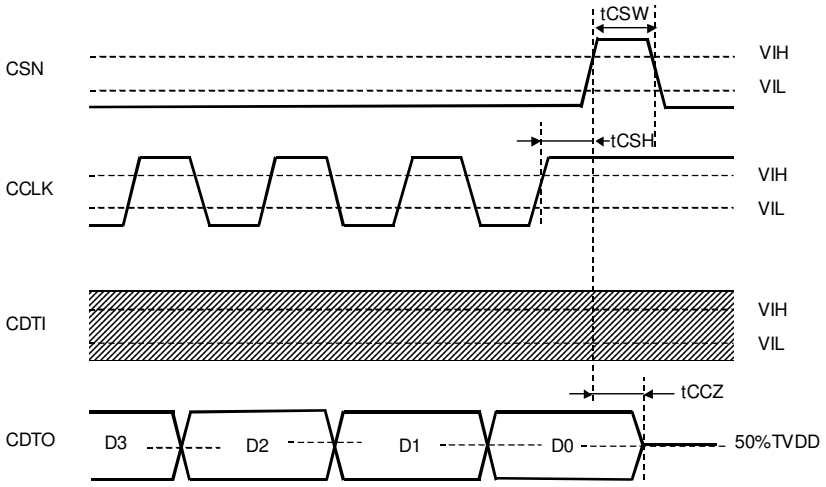
WRITE/READ Command Input Timing in 4-wire serial mode
The ADC/DAC part doesn't support READ command.



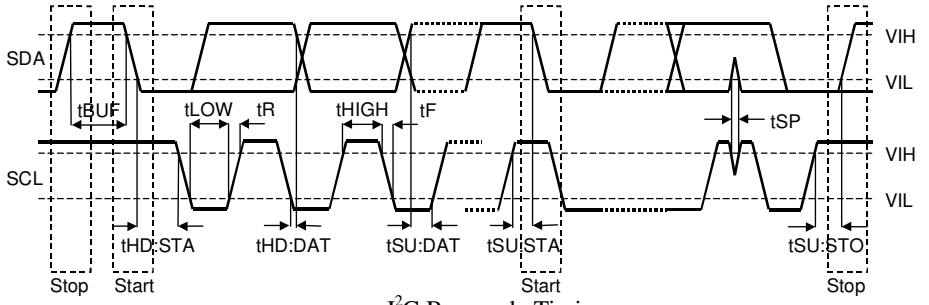
WRITE Data Input Timing in 4-wire serial mode



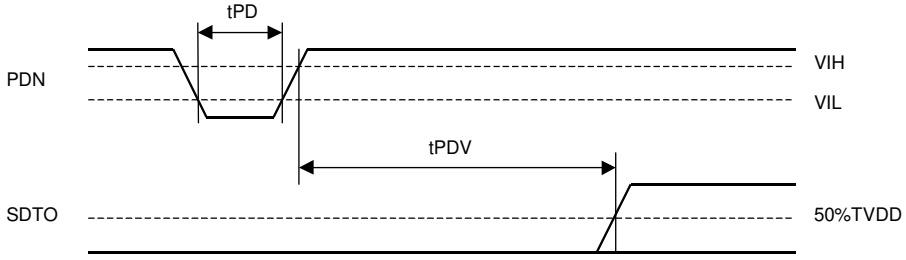
READ Data Output Timing 1 in 4-wire serial mode
The ADC/DAC part doesn't support READ command..



READ Data Input Timing 2 in 4-wire serial mode
The ADC/DAC part doesn't support READ command.



I^2C Bus mode Timing
The ADC/DAC part doesn't support READ command.



Power-down & Reset Timing

OPERATION OVERVIEW (ADC/DAC part)

■System Clock

The external clocks, which are required to operate the AK4589, are MCLK, LRCK1 and BICK1. MCLK should be synchronized with LRCK1 but the phase is not critical. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit = "0": Default), the sampling speed is set by DFS1-0 bit (Table 1). The frequency of MCLK at each sampling speed is set automatically. (Table 3, 4, 5) In Auto Setting Mode (ACKS bit = "1"), as MCLK frequency is detected automatically (Table 6) and the internal master clock becomes the appropriate frequency (Table 7), it is not necessary to set DFS1-0 bits.

Only MCLK is necessary in the master mode. Master Clock Input Frequency should be selected by CKS1-0 bits (Table 2), and Sampling Speed should be selected by DFS1-0 bits (Table 1). The frequencies and the duties of the clocks (LRCK1, BICK1) may not be stabile after setting CKS1-0 bits and DFS1-0 bits up.

In slave mode, external clocks (MCLK, BICK1, LRCK1) should always be present whenever the AK4589 is in normal operation mode (PDN pin = "H"). If these clocks are not provided, the AK4589 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4589 should be in the power-down mode (PDN pin = "L") or in the reset mode (RSTN1 bit = "0"). After exiting reset at power-up etc., the AK4589 is in the power-down mode until MCLK and LRCK are input.

In the Master mode, External clock(MCLK) should always be supplied except in the power-down mode. It is in power-down mode until MCLK will be supplied, when Reset was canceled by Power-ON and so on.

DFS1	DFS0	Sampling Speed (fs)		
0	0	Normal Speed Mode	32kHz~48kHz	Default
0	1	Double Speed Mode	64kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	

Table 1. Sampling Speed (Manual Setting Mode)

CKS1	CKS0	Normal	Double	Quad	
0	0	256fs	128fs	128fs	Default
0	1	384fs	192fs	128fs	
1	0	512fs	256fs	128fs	
1	1	256fs	256fs	128fs	

Table 2.Master clock input select (Master Mode)

LRCK1	MCLK (MHz)			BICK1 (MHz)
Fs	256fs	384fs	512fs	64fs
32.0kHz	8.1920	12.2880	16.3840	2.0480
44.1kHz	11.2896	16.9344	22.5792	2.8224
48.0kHz	12.2880	18.4320	24.5760	3.0720

Table 3. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK1	MCLK (MHz)			BICK1 (MHz)
Fs	128fs	192fs	256fs	64fs
88.2kHz	11.2896	16.9344	22.5792	5.6448
96.0kHz	12.2880	18.4320	24.5760	6.1440

Table 4. System Clock Example (Double Speed Mode @Manual Setting Mode)
(Note: At Double speed mode (DFS1= "0", DFS0 = "1"), 128fs and 192fs are not available for ADC.)